PERFISANS NETWORKS

Product Brief

10/100/1000Mbps Ethernet Network Accelerator ENA1001

Key Features:

- Single 10/100/1000Mbps triple-speed MAC
  - Half/full duplex in 10/100Mbps, full duplex in 1000Mbps
  - MII/GMII/TBI connection to external PHY
  - Built-in management interface to external PHY
- 32/64-bit PCI interface at 33/66MHz
  - PCI version 2.3
  - External EEPROM for customized identification
- Customized hardware acceleration for offloading host CPU
- Internal 32KB receive FIFO and 8KB transmit FIFO
- Support large frames up to 8KB
- Independent transmit and receive processing queues
- Built-in power management capability
- Statistic gathering (SNMP MIB II, Ethernet MIB)
- Full JTAG, MBIST, and scan test provisions
- Low power 0.15um design with 3.3V CMOS I/O – no Heatsink required
- Standard 176-pin QFP package
- Operating temperature range between 0° to 70°

Standard Compliance:

- IP v.4
- IEEE 802.3/u/z 10/100/1000Base-T/TX/SX
- IEEE 802.3x Flow Control – h/w and s/w control
- IEEE 802.1q VLAN tagging
- IEEE 802.1p Priority Processing – up to 8 queues
- IEEE 802.3ad Link Aggregation

Host Offloading Features:

- IP, TCP, and UDP checksum offload capabilities for TX and RX
- TCP segmentation on TX
- Conditional IP de-fragmentation on RX
- Conditional segment reassembly on RX
- VLAN tag insertion and removal
- Advanced configurable packet filtering capabilities
- Proprietary descriptor ring management hardware for TX and RX
- Adaptive interrupts for TX and RX

Manageability Features:

- Support ACPI v2.0, PCI power management, OnNow, WoL
- SNMP and RMON statistic counters with automatic DMA transfer of contents to host memory
- Diagnostic capabilities including internal loop back and packet error reports

Operating Systems:

- Acceleration drivers for Windows 2000 and Windows XP
- Standard and enhanced drivers for Linux (Red Hat), and other derivatives

Summary

The Perfisans 10/100/1000Mbps Ethernet Network Accelerator is a high performance, and low cost system-on-chip (SOC) solution targeting value-added Gigabit Ethernet Connectivity. Microsoft TCP/IP Offload features are supported by fully configurable dedicated hardware protocol engines.

Product Description

TCP/IP offload at Gigabit Ethernet speed is now brought to the popular Windows 2000 and XP customer base. Primary host CPU offload functions include: checksum assistance in TX and RX, TCP segmentation of TX traffic, IP de-fragmentation and TCP reassembly assistance on RX, and VLAN header insertion/removal. The solution is consisted of a triple-speed MAC with internal memory for high performance packet processing. The ENA1001 Ethernet Network Accelerator offers a 32/64-bit PCI 2.2 compliant interface. The accelerator offers a full duplex 2Gbps wire speed throughput. An application programming interface (API) specification is also provided to allow OEMs to customize advanced packet filtering, and manageability features.

Benefits

- Fully ready for Gigabit Ethernet, and backward compatible with existing 10/100Mbps network infrastructure
- Built-in host offloading features along with efficient PCI bus operation reduce host CPU utilization which results higher overall performance
- Configurable acceleration engine provides flexibility and adaptability for various target applications

Applications

- Network interface card (NIC)
- LAN on mother-board (LOM)
- Host bus adapter
- Server and host applications
- Storage area network applications

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Overview

The ENA1001 is a standards-compliant Ethernet MAC controller focused on maximizing network performance. The high-speed, low-power design is implemented in a 0.15um process with 3.3V I/O, and is contained in a low-cost 176-pin QFP package.

PCI Interface

Its PCI bus interface complies with the PCI Bus Specification Rev 2.3, and supports 32 and 64-bit bus widths along with 64-bit addressing, interrupt coalescing and power management. This easily meets the bandwidth requirements to sustain full duplex 1Gbps link speeds. PCI configuration along with product specific data are auto-loaded from an external EEPROM at system reset.

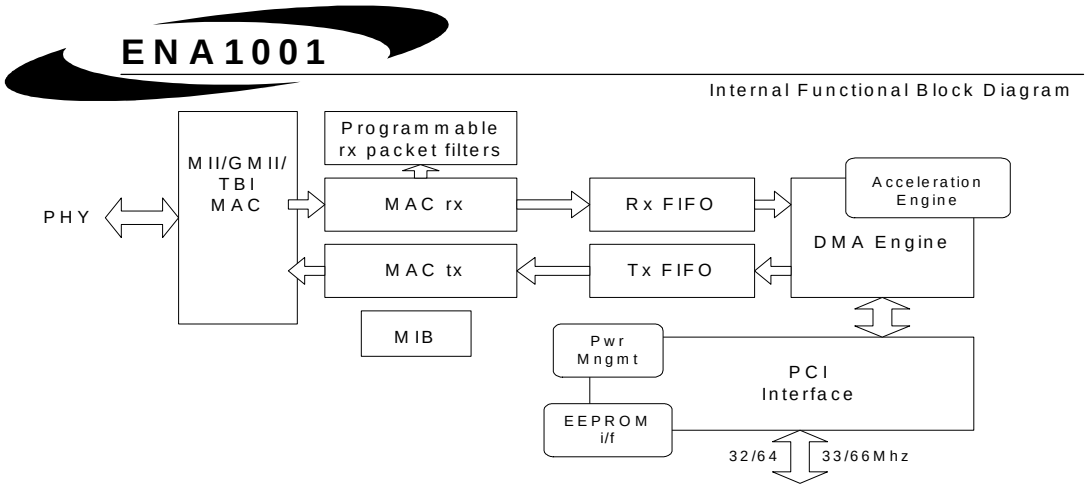
DMA and Acceleration Engine

The DMA engine supports bus-mastering to/from a descriptor-based buffer list organization in host memory. This buffer organization supports up to 8 VLAN queues in both TX and RX directions. A highly programmable weight-assignment facility is used to establish priority among queues. Maximum PCI burst lengths can be tailored to facilitate sharing of the system PCI bus bandwidth. Arbitration between receive and transmit is designed to minimize risk of RX buffer overrun.

A variety of offload capabilities are implemented in the acceleration engine to optimize performance of drivers and upper-level software protocol layers. Among these, TCP/UDP/IP checksum insertion on transmit and checksum validation on receive, VLAN insertion/removal, full TCP segmentation on transmit, and proprietary conditional IP de-fragmentation and TCP/UDP reassembly on receive.

MAC Controller

The triple-speed MAC controller supports full duplex at 10/100/1000Mbps and additionally half-duplex at 10/100Mbps. It is fully compliant with IEEE 802/u/x/z/ab/ac. The design is backed by an on-board 8K-byte transmit buffer and a 32K-byte receive buffer. Both transmit and receive statistics gathering are supported by an internal MIB module. A built-in TX-to-RX loop-through path simplifies self-diagnostic checks. The flexible PHY interface supports MII (10/100 Mbps), GMII and TBI interface configurations.



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