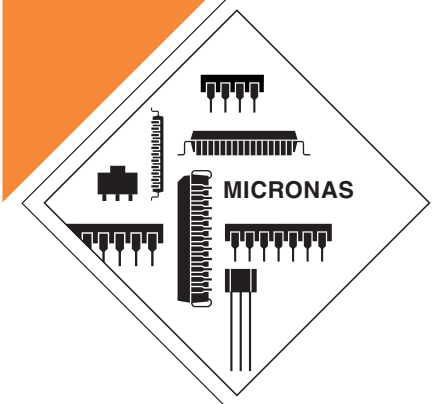

PRELIMINARY DATA SHEET

DAC 3555A
Stereo Audio DAC

Edition Jan. 8, 2002
6251-575-1PD

MICRONAS

Contents

Stereo Audio DAC

1. Introduction

The DAC 3555A is a single-chip, high-precision, stereo digital-to-analog converter designed for audio applications. The employed conversion technique is based on oversampling with noise-shaping. With Micronas' unique multibit sigma-delta technique, less sensitivity to clock jitter, high linearity, and a superior S/N ratio have been achieved. The DAC 3555A is controlled via I^2C bus.

Digital audio input data is received by a versatile I^2S interface. The analog back-end consists of internal analog filters and op amps for cost-effective additional external sound processing. The DAC 3555A provides line-out, headphone/speaker amplifiers, and volume control. Moreover, mixing additional analog audio sources to the D/A-converted signal is supported.

The DAC 3555A is designed for all kinds of applications in the audio and multimedia field, such as: MPEG players, CD players, DVD players, CD-ROM players, mobile phones, etc.

The DAC 3555A ideally complements the MP3 audio decoders MAS 3507D, MAS 35x9F, and PUC 303xA.

No crystal or external clock required for standard applications with sample rates from 32 to 48 kHz and 96 kHz.
It is required for automatic sample rate detection below 32 kHz, MPEG mode (refer to Section 2.10.1.), and use of clock output CLKOUT.

1.1. Main Features

- no master main input clock required
- no external crystal required
- integrated stereo headphone amplifier and mono speaker amplifier
- SNR of 103 dB(A)
- I^2C bus, I^2S bus
- internal clock oscillator
- sample rates from 8 kHz to 96 kHz
- analog deemphasis for 44.1 kHz
- analog volume and balance: +18…–75 dB and mute
- THD better than 0.01%
- two additional analog stereo inputs (AUX) with source selection and mixing
- supply range: 2.7 V…5.5 V
- zero-power mode
- additional line-out
- on-chip op amps for cost-effective external analog sound processing
- pin-compatible to DAC 3550A
- PMQFP44 or PQFN40 package

1.2. Differences between DAC 3555A and DAC 3550A

- new zero-power mode
- operation in I^2C mode only. Stand-alone operation is not supported.
- new quiet wake-up mode: after power-on, the DAC 3555A switches into zero-power mode. Waking-up is done via I^2C command. This feature avoids audible "plops".
- sample rates up to 96 kHz
- not register-compatible to DAC 3550A

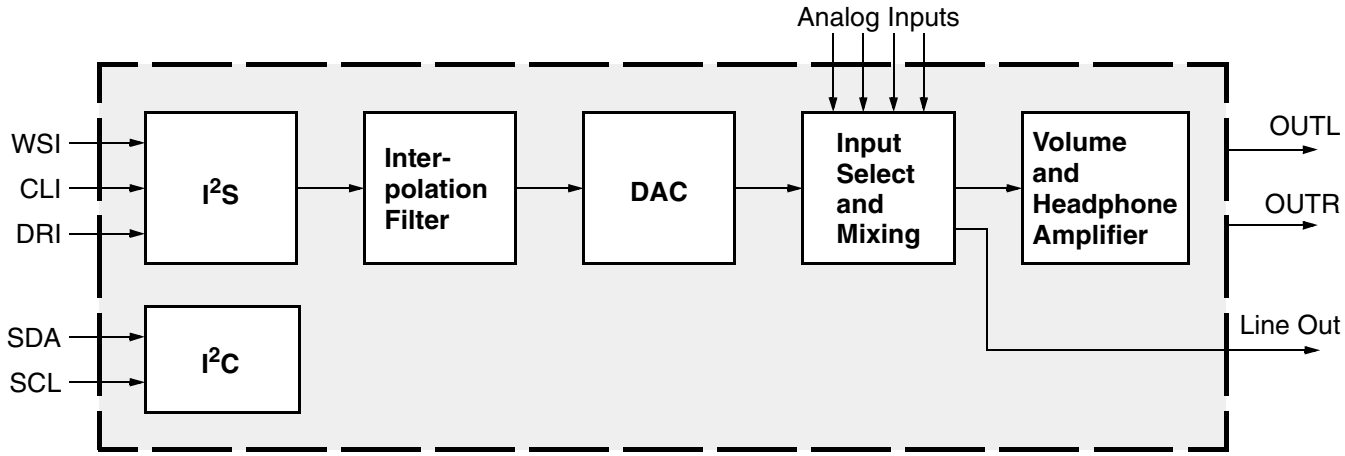

Fig. 1–1: Block diagram of the DAC 3555A

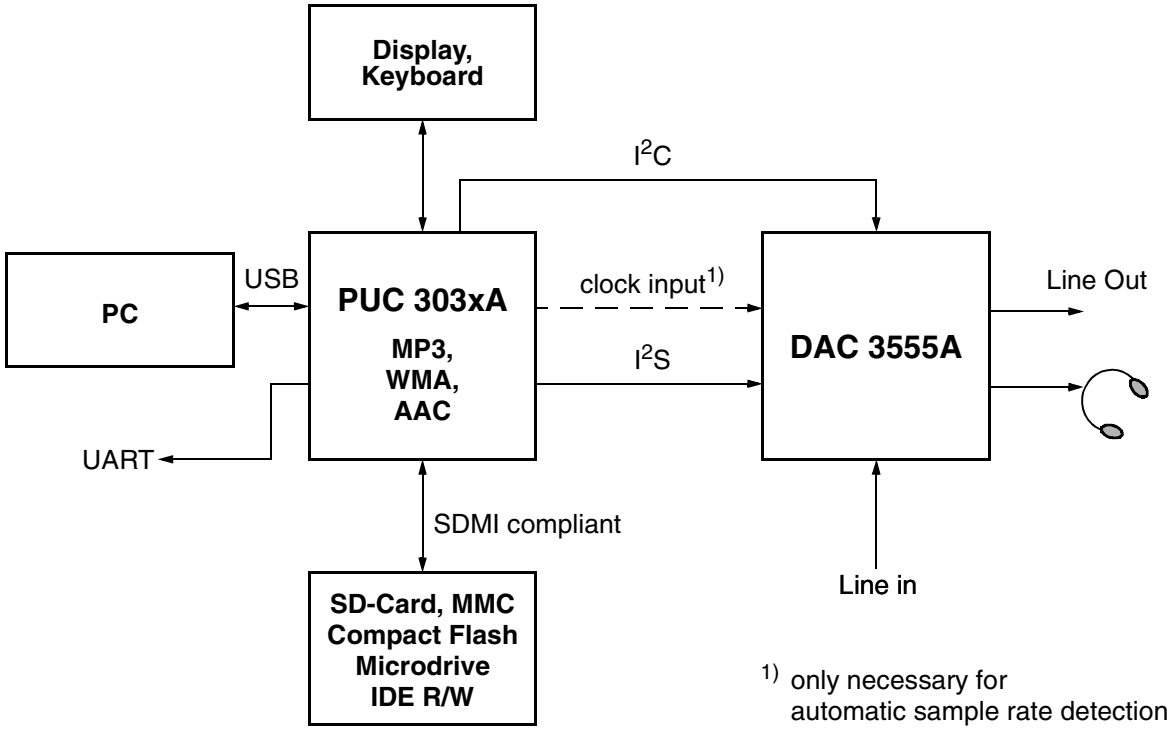

Fig. 1–2: Typical application: Secure Music Player

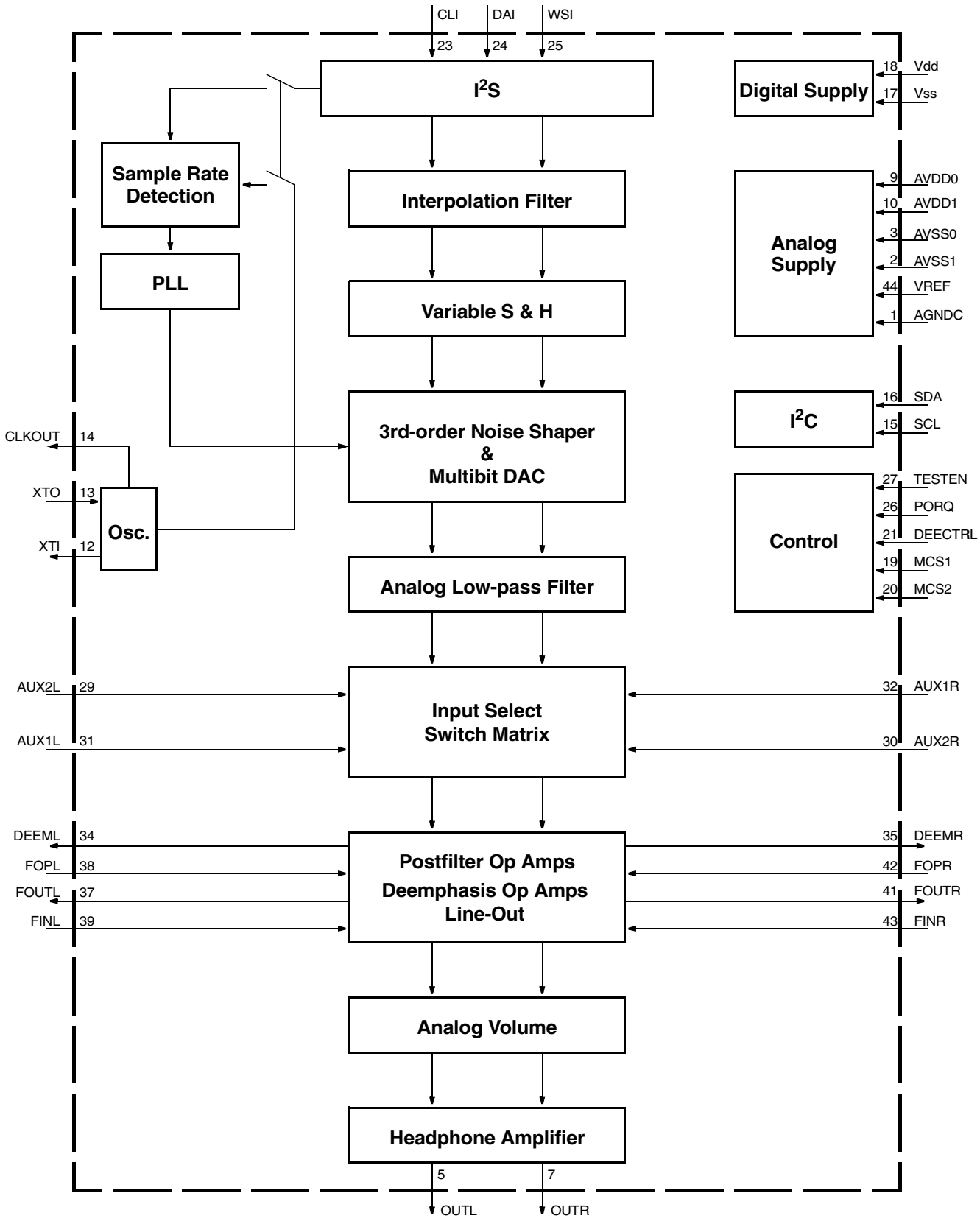

Fig. 1–3: Block diagram of the DAC 3555A

2. Functional Description

2.1. I²S Interface

The I²S interface is the digital audio interface between the DAC 3555A and external digital audio sources such as CD/DAT players, MPEG decoders etc. It covers most of the I²S-compatible formats.

All modes have two common features:

1. The MSB is left justified to an I²S frame identification (WSI) transition.

2. Data is valid on the rising edge of the bit clock CLI.

16-bit mode
In this case, the bit clock is $32 \times fs_{audio}$. Maximum word length is 16 bit.

32-bit mode
In this case, the bit clock is $64 \times fs_{audio}$. Maximum word length is 32 bit.

Automatic Detection
No I²C control is required to switch between 16- and 32-bit mode. It is recommended to switch the DAC 3555A into mute position during changing between 16- and 32-bit mode.

For high-quality audio, it is recommended to use the 32-bit mode of the I²S interface to make use of the full dynamic range (if more than 16 bits are available).

Left-Right Selection
Standard I²S format defines an audio frame always starting with left channel and low-state of WSI. However, I²C control allows changing the polarity of WSI.

Delay Bit
Standard I²S format requires a delay of one clock cycle between transitions of WSI and data MSB. In order to fit other formats, however, this characteristic can be switched off and on by I²C control.

Note: Volume mute should be applied before changing I²S mode in order to avoid audible clicks.

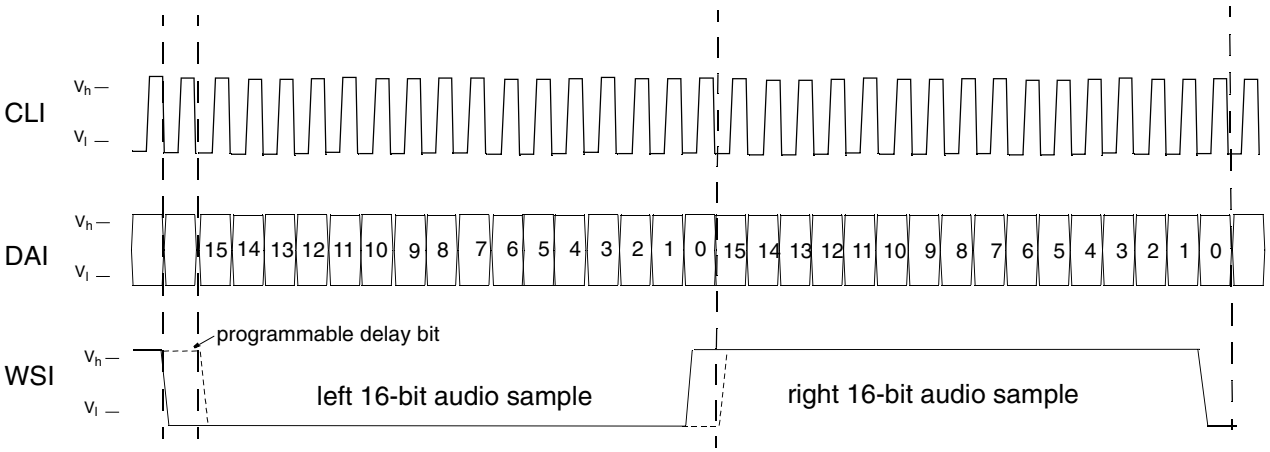

Fig. 2–1: I²S 16-bit mode (LR_SEL = 0)

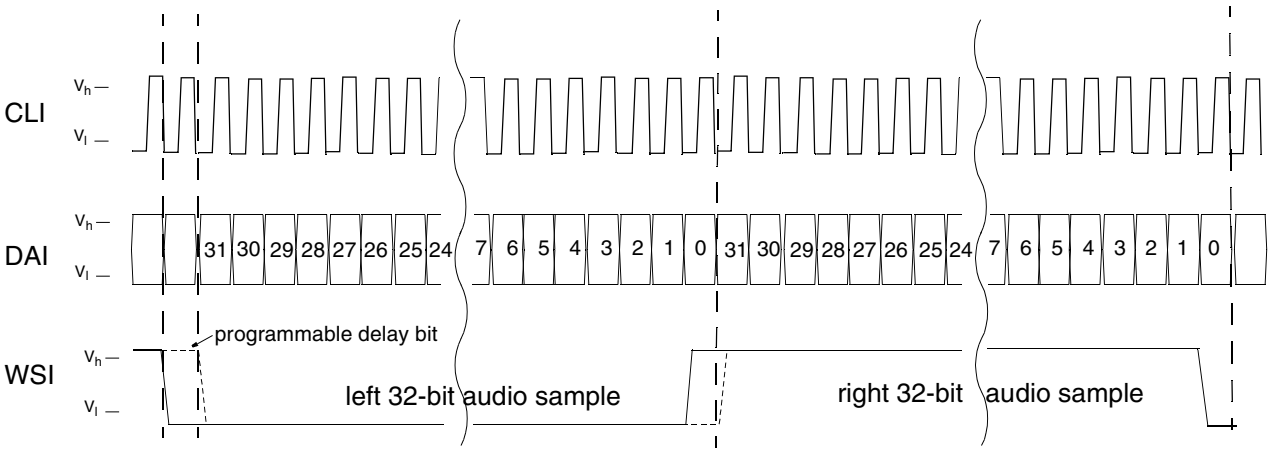

Fig. 2–2: I²S 32-bit mode (LR_SEL = 0)

2.2. Interpolation Filter

The interpolation filter increases the sampling rate by a factor of 8. The characteristic for fs_{audio} = 48 kHz is shown in Fig. 2–1.

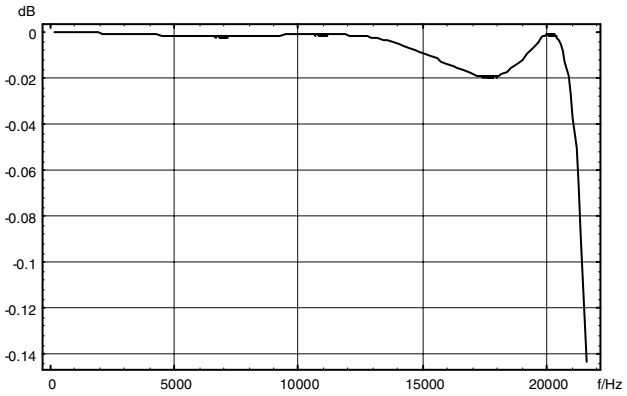

Fig. 2–1: 1→8 Interpolation filter; frequency range: 0...22 kHz

2.3. Variable Sample and Hold

The advantage of this system is that even at low sample frequencies the out-of-band noise is not scaled down to audible frequencies.

2.4. 3rd-order Noise Shaper and Multibit DAC

The 3rd-order noise shaper converts the oversampled audio signal into a 5-bit noise-shaping signal at a high sampling rate. This technique results in extremely low quantization noise in the audio band.

2.5. Analog Low-pass

The analog low-pass is a first order filter with a cut-off frequency of approximately 1.4 MHz which removes the high-frequency components of the noise-shaping signal.

2.6. Input Select and Mixing Matrix

This block is used to switch between or mix the auxiliary inputs and the signals coming from the DAC. A switch matrix allows to select between mono and stereo mode as shown in Fig. 2–1.

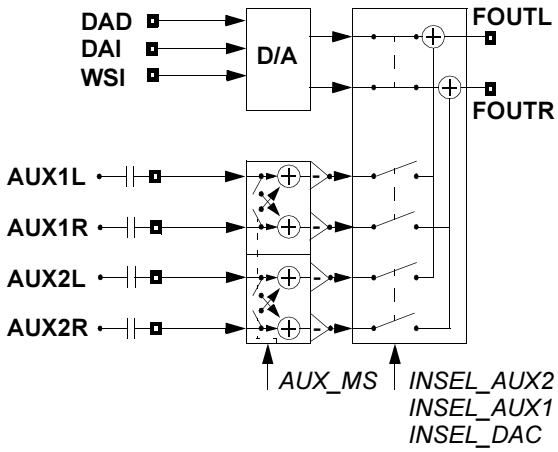

Fig. 2–1: Switch matrix

Mono mode is realized by adding left and right channel.

2.7. Postfilter Op Amps, Deemphasis Op Amps, and Line-Out

This block contains the active components for the analog postfilters and the deemphasis network. The op amps and all I/O-pins for this block are shown in Fig. 2–2.

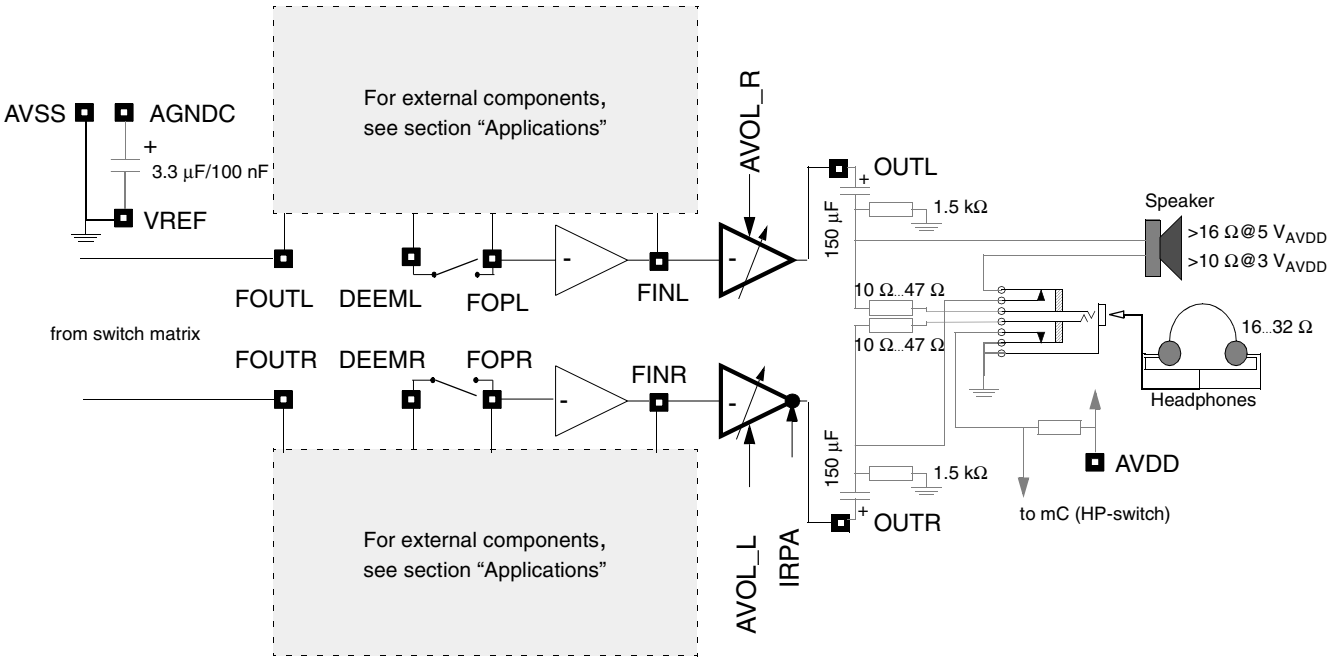

Fig. 2–2: Postfilter op amps, deemphasis op amps, and line-out

2.8. Analog Volume

The analog volume control covers a range from +18 dB to –75 dB. The lowest step is the mute position.

Step size is split into a 3-dB and a 1.5-dB range:

–75 dB...–54 dB: 3 dB step size
–54 dB...+18 dB: 1.5 dB step size

Table 2–1: Volume Control

Volume/dB	AVOL
18.0	111000
16.5	110111
15.0	110110
13.5	110101
–	–
0.0	101100 (default)
–1.5	101011
–	–
–54.0	001000
–57.0	000111
–	–
–75	000001
Mute	000000

2.9. Headphone Amplifier

The headphone amplifier output is provided at the OUTL and OUTR pins connected either to stereo headphones or a mono loudspeaker. The stereo headphones require external 10...47-Ω serial resistors in both channels. If a loudspeaker is connected to these outputs, the power amplifier for the right channel must be switched to inverse polarity. In order to optimize the available power, the source of the two output amplifiers should be identical, i.e. a monaural signal.

Please note, that if a speaker is connected, it should strictly be connected as shown in Fig. 2–2. Never use a separate connector for the speaker, because electrostatic discharge could damage the output transistors.

2.10. Clock System

The advantage of the DAC 3555A clock system is that no external master clock is needed. Most DACs need $256 \times fs_{audio}$, $384 \times fs_{audio}$, or at least an asynchronous clock.

All internal clocks are generated by a PLL circuit, which locks to the I^2S bit clock (CLI). If no I^2S clock is present, the PLL runs free, and it is guaranteed that there is always a clock to keep the IC controllable by I^2C.

The device can be set to two different modes:

– Standard mode

– MPEG mode

In the standard mode, I^2C subaddressing is possible (ADR0, ADR1, ADR2).
MPEG mode always uses ADR3.

To select the modes, the MCS1/MCS2 pins must be set according to Table 2–2.

Table 2–2: Operation Modes

MCS1	MCS2	Mode	Sub-address	Default Sample Rate
0	0	Standard	ADR0	32–48 kHz
0	1	Standard	ADR1	32–48 kHz
1	0	Standard	ADR2	32–48 kHz
1	1	MPEG	ADR3	Automatic

2.10.1. Standard Mode

In standard mode, sample rates from 48 kHz to 32 kHz are handled without I^2C control automatically. The setting for this range is the default setting. Other sample rates require an I^2C control to set the PLL divider. This ensures that even at low sample rates, the DAC 3555A runs at a high clock rate. This avoids audible effects due to the noise-shaping technique of the DAC 3555A. Sample rate range is continuous from 8 to 48 kHz. The I^2C setting of non-standard sample rates must follow Table 2–2.

An additional mode allows automatic sample rate detection. In this case, the clock oscillator is required and must run at frequencies between 13.3 MHz to 17 MHz. This mode, however, does not support continuous sample rates. Only the following sample rates are allowed:

8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz

The sample rate detection allows a tolerance of ±200 ppm at WSI.

2.10.2. MPEG Mode

This mode should be used in conjunction with PUC 30x3A in MPEG player applications. All MPEG sample rates from 8 to 48 kHz can be detected if the PUC 30x3A sends a clock signal between 13.3 MHz and 17 MHz to the DAC 3555A. The internal processing and the DAC itself are automatically adjusted to keep constant performance throughout the entire range. I^2C control for sample rate adjustment is not needed in this case.

The MPEG sample rates:

8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz,
24 kHz, 32 kHz, 44.1 kHz, 48 kHz

As in standard mode, the sample rate detection allows a tolerance of ±200 ppm at WSI.

Subaddressing is not possible in MPEG mode; this means, in multi-DAC systems, only one DAC 3555A can run in MPEG mode.

2.11. I²C Bus Interface

The DAC 3555A is equipped with an I²C bus slave interface. The I²C bus interface uses one level of subaddressing: The I²C bus address is used to address the IC. The subaddress allows chip select in multi DAC applications and selects one of the three internal registers. The registers are write-only. The I²C bus chip address is given below.

Device Address = $4D_{hex}$.

The registers of the DAC 3555A have 8- or 16-bit data size; 16-bit registers are accessed by writing two 8-bit data words.

2.12. Registers

In Section 3.5. “Control Registers” on page 18, a definition of the DAC 3555A control registers is shown. A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in the table.

All registers are write-only.

The register address is coded by 3 bits (RA1, RA0) according to Table 2–3.

Table 2–3: I²C Register Address

RA1	RA0	Mnemonics
0	1	SR_REG
1	0	AVOL
1	1	GCFG

2.13. Chip Select

Chip select allows to connect up to four DAC 3555A to an I²C control bus. The chip subaddresses are defined by the MCS1/MCS2 (Mode and Chip Select) pins. Only in standard mode, chip select is possible. MPEG mode always uses chip subaddress 3.

Register address and chip select are mapped into the subaddress field in Table 2–4.

Table 2–4: I²C Subaddress

7	6	5	4	3	2	1	0
MCS2	MCS1					RA1	RA0

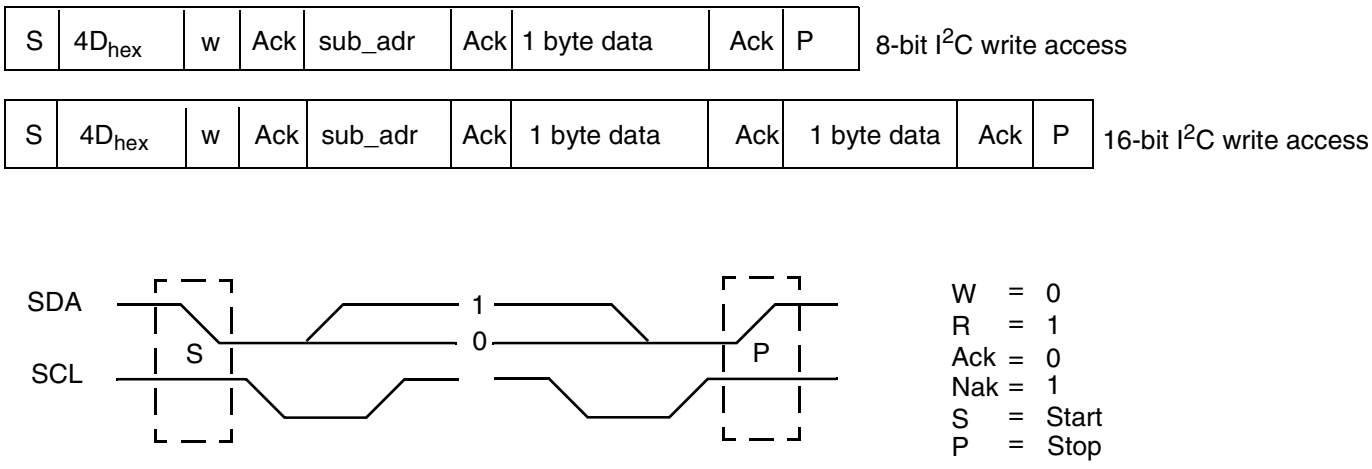

Fig. 2–1: I²C bus protocols for write operations

2.14. Power Modes

The DAC 3555A supports four different power modes, which can be selected by I^2C.

1. Zero Power
This is the default mode after power up. In this mode digital and analog blocks are inactive.
Please note that minimum power consumption is only achieved if all digital input pins connected to peripheral circuits are low or tristate.

2. Analog Stand-by
This mode activates the internal analog reference system and allows a fast and quiet transition to the active modes below.

3. Aux to Line
This active mode is used, if no digital audio signals are present. Only the analog back-end is active.

4. Full Power
All blocks are active in this mode.

Start-up sequence: The recommended sequence for stepping through the power modes is shown in Section 4.5. “Power-up/down Sequence” on page 30.

2.15. Oscillator

The I^2C-controlled oscillator (see Section 3.5. “Control Registers” on page 18) switches on in the following modes, only:

1. DAC ON - Standard Mode - automatic sample rate detection

2. DAC ON - MPEG Mode

In all other modes the oscillator is not required internally and therefore switched off.

For test purpose it is possible to switch on the oscillator in all modes (control register AVOL, bit 15). It is not recommended to use this option in normal applications.

3. Specifications

3.1. Outline Dimensions

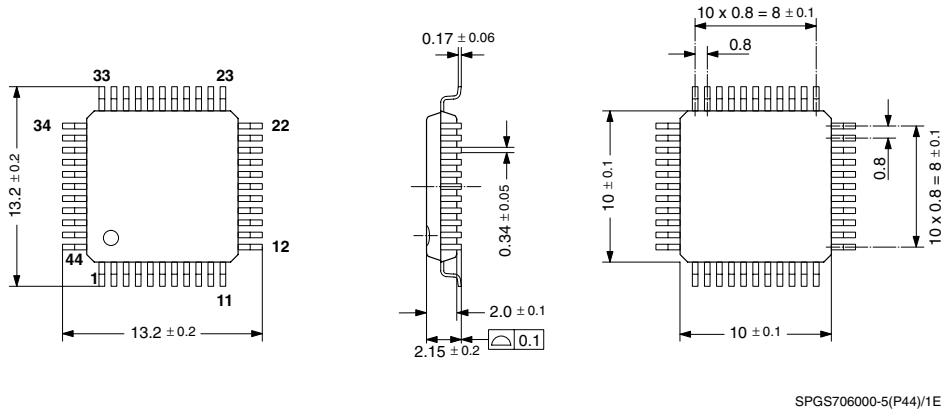

Fig. 3–1:
44-Pin Plastic Metric Quad Flat Package
(PMQFP44)
Weight approximately 0.4 g
Dimensions in mm

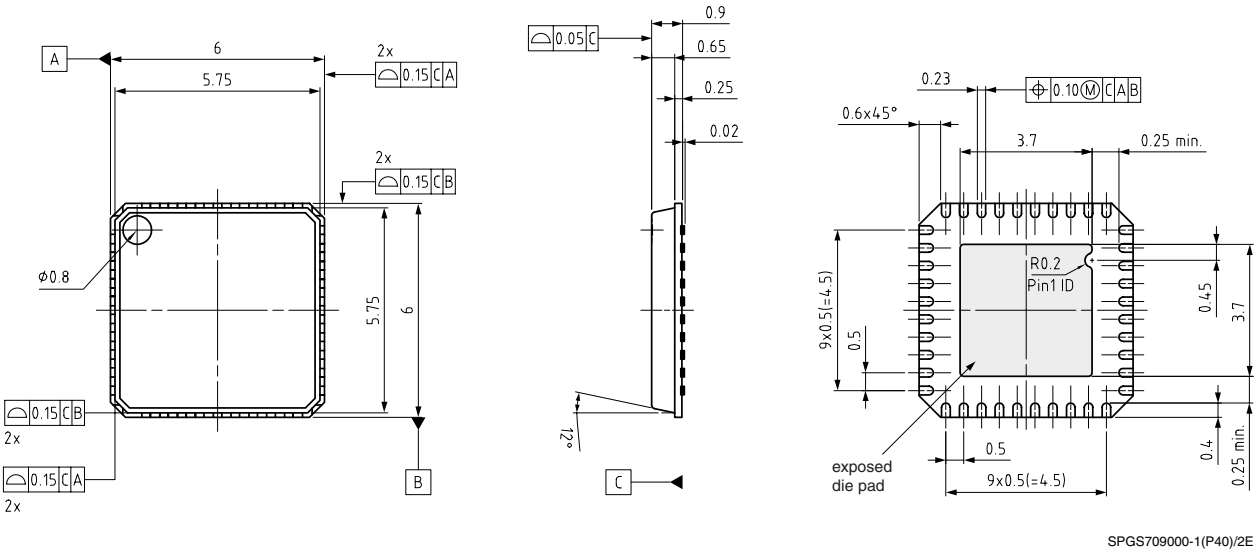

Fig. 3–2:
40-Pin Plastic Quad Flat No leads package
(PQFN40)
Weight approximately 0.096 g
Dimensions in mm

3.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
VSS = if not used, connect to VSS
X = obligatory; connect as described in application diagram
VDD = connect to VDD

Pin No. PMQFP 44-pin	Pin No. PQFN 40-pin	Pin Name	Type	Connection (If not used)	Short Description
1	31	AGNDC	IN/OUT	X	Analog reference Voltage
2	32	AVSS1	IN	X	VSS 1 for audio back-end
3	33	AVSS0	IN	X	VSS 0 for audio output amplifiers
4	16	NC		LV	Not connected
5	34	OUTL	OUT	LV	Audio Output: Headphone left or Speaker +
6	26	NC		LV	Not connected
7	37	OUTR	OUT	LV	Audio Output: Headphone right or Speaker –
8	35	NC		LV	Not connected
9	38	AVDD0	IN	X	VDD 0 for audio output amplifiers
10	40	AVDD1	IN	X	VDD 1 for audio back-end
11	36	NC		LV	Not connected
12	1	XTI	IN	X	Quartz oscillator pin 1
13	2	XTO	IN/OUT	X	Quartz oscillator pin 2
14	3	CLKOUT	OUT	LV	Clock Output
15	4	SCL	IN	LV	I^2C clock
16	5	SDA	IN/OUT	LV	I^2C data
17	6	VSS	IN	X	Digital VSS
18	7	VDD	IN	X	Digital VDD
19	8	MCS1	IN	X	I^2C Chip Select 1
20	9	MCS2	IN	X	I^2C Chip Select 2
21	10	DEECTRL	IN	VSS	Deemphasis on/off Control
22	39	NC	IN	LV	Not connected
23	11	CLI		VSS	I^2S Bit Clock
24	12	DAI	IN	VSS	I^2S Data
25	13	WSI	IN	VSS	I^2S Frame Identification

Pin No. PMQFP 44-pin	Pin No. PQFN 40-pin	Pin Name	Type	Connection (If not used)	Short Description
26	14	PORQ	IN	VDD	Power-On Reset, active-low
27	15	TESTEN	IN	X	Test Enable
28	16	NC		LV	Not connected
29	17	AUX2L	IN	LV	AUX2 left input for external analog signals (e.g. tape)
30	18	AUX2R	IN	LV	AUX2 right input for external analog signals (e.g. tape)
31	19	AUX1L	IN	LV	AUX1 left input for external analog signals (e.g. FM)
32	20	AUX1R	IN	LV	AUX1 right input for external analog signals (e.g. FM)
33	–	NC		LV	Not connected
34	21	DEEML	OUT	LV	Deemphasis Network Left
35	22	DEEMR	OUT	LV	Deemphasis Network Right
36	–	NC		LV	Not connected
37	23	FOUTL	OUT	X	Output to left external filter
38	24	FOPL	IN/OUT	X	Filter op amp inverting input, left
39	25	FINL	IN/OUT	X	Input for FOUTL or filter op amp output (line out)
40	–	NC		LV	Not connected
41	27	FOUTR	OUT	X	Output to right external filter
42	28	FOPR	IN/OUT	X	Right Filter op amp inverting input
43	29	FINR	IN/OUT	X	Input for FOUTR or filter op amp output (line out)
44	30	VREF	IN	X	Analog reference Ground

3.3. Pin Descriptions

3.3.1. Power Supply Pins

The DAC 3555A combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

VDD
VSS
The VDD and VSS power supply pair are connected internally with all digital parts of the DAC 3555A**.**

AVDD0
AVSS0
AVDD0 and AVSS0 are separate power supply pins that are exclusively used for the on-chip headphone/ loudspeaker amplifiers.

AVDD1
AVSS1
The AVDD1 and AVSS1 pins supply the analog audio processing parts, except for the headphone/loudspeaker amplifiers.

3.3.2. Analog Audio Pins

AGNDC
Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against VREF with a 3.3 µF capacitor.

Note: The pin has a typical DC-level of 1.5/2.25 V. It can be used as reference input for external op amps when no current load is applied.

VREF
Reference ground for the internal band-gap and biasing circuits. This pin should be connected to a clean ground potential. Any external distortions on this pin will affect the analog performance of the DAC 3555A.

AUX1L
AUX1R
AUX2L
AUX2R
The AUX pins provide two analog stereo inputs. Auxiliary input signals, e.g. the output of a conventional receiver circuit or the output of a tape recorder can be connected with these inputs. The input signals have to be connected by capacitive coupling.

FOUTL
FOPL
FINL
FOUTR
FOPR
FINR
Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R-pins are directly connected with the inverting inputs of the filter op amps. The FINL/R pins are connected with the outputs of the op amps. The driving capability of the FOUTL/R pins is not sufficient for standard line output signals. Only the FINL/R pins are suitable for line output.

OUTL
OUTR
The OUTL/R pins are connected to the internal output amplifiers. They can be used for either stereo headphones or a mono loudspeaker. The signal of the right channel amplifier can be inverted for mono loudspeaker operation.

Caution: A short circuit at these pins for more than a momentary period may result in destruction of the internal circuits.

3.3.3. Oscillator and Clock Pins

XTI
XTO
The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Both pins should be directly connected to the crystal and two ground-connected capacitors (see application diagram).

CLKOUT
The CLKOUT pin provides a buffered output of the crystal oscillator.

Caution: Power dissipation limit may be exceeded in case of short to VSS or VDD.

CLI
DAI
WSI
These three pins are inputs for the digital audio data DAI, frame indication signal WSI, and bit clock CLI. The digital audio data is transmitted in an I^2S-compatible format. Audio word lengths of 16 and 32 bits are supported, as well as SONY and Philips I^2S protocol.

SCL
SDA
SCL (serial clock) and SDA (serial data) provide the connection to the serial control interface (I^2C).

3.3.4. Other Pins

TESTEN
Test enable. This pin is for test purposes only and must always be connected to VSS.

PORQ
This pin may be used to reset the chip. If not used, this pin must be connected to VDD.

DEEML
DEEMR
These pins connect an external analog deemphasis network to the signal path in the analog back-end. This connection can be switched on and off by an internal switch which is controlled either by I^2C or the DEECTRL-pin.

DEECTRL
Deemphasis can be switched on and off with this pin.

MCS1
MCS2
Mode select pins to select MPEG, Standard Mode, and I^2C subaddress.

3.3.5. Pin Configuration

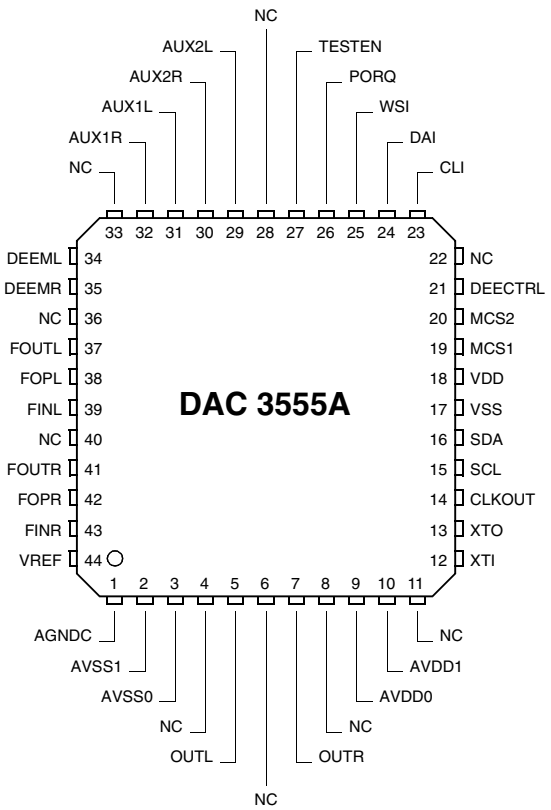

Fig. 3–1: PMQFP44 package

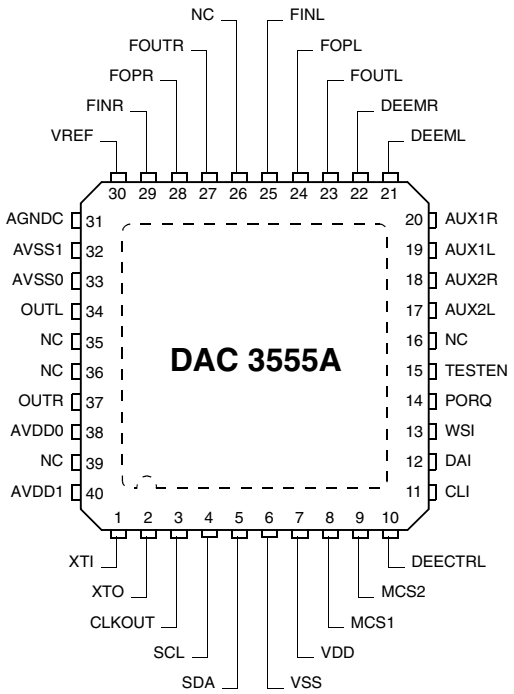

Fig. 3–2: PQFN40 package

3.4. Pin Circuits

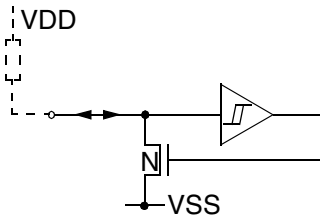

Fig. 3–3: Input/Output Pins SDA, SCL

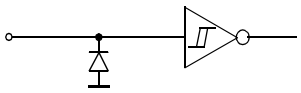

Fig. 3–4: Input Pins PORQ, DAI

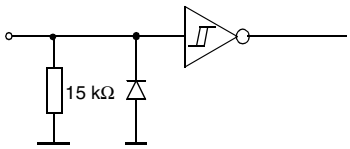

Fig. 3–5: Input Pins WSI, CLI

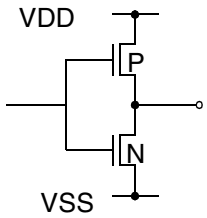

Fig. 3–6: Output Pin CLKOUT

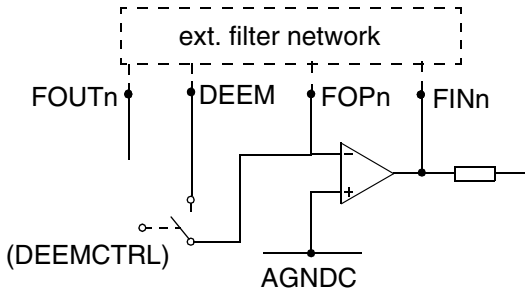

Fig. 3–7: Pins FINR, FOPR, FINL, FOPL, DEEML, DEEMR

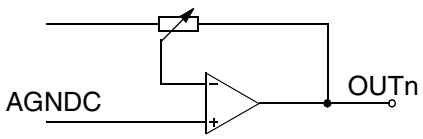

Fig. 3–8: Output Pins OUTL, OUTR

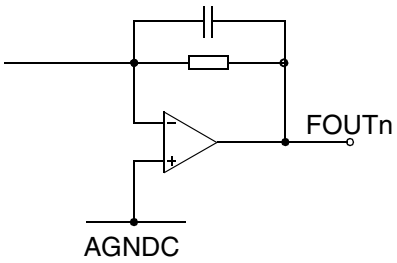

Fig. 3–9: Output Pins FOUTL, FOUTR

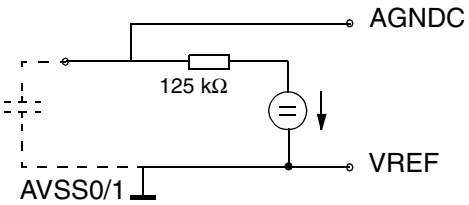

Fig. 3–10: Pins AGNDC, VREF

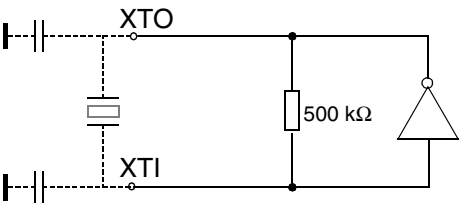

Fig. 3–11: Input/Output Pins XTI, XTO

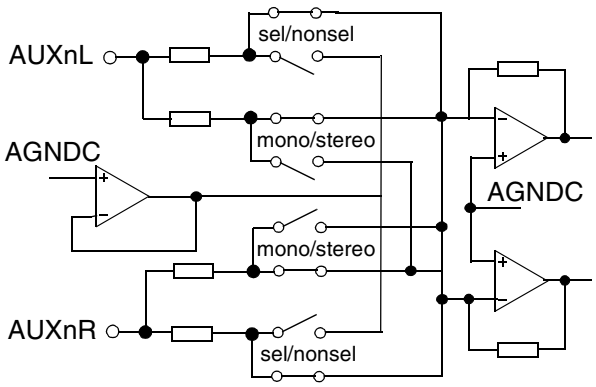

Fig. 3–12: Input Pins AUX1R, AUX1L, AUX2R, AUX2L, AGNDC

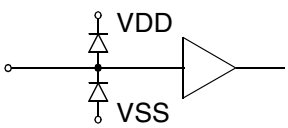

Fig. 3–13: Input Pins MCS1, MCS2, DEECTRL

3.5. Control Registers

I²C Sub-address (hex)	Number of Bits	Mode	Function	Default Values (hex)	Name
SAMPLE RATE CONTROL **SR_REG**					
01	8	w	sample rate control	0_{hex}	
			bit[7:5] not used, set to 0		
			bit[4] L/R-bit 0 (WSI = 0 → left channel)[1)] 1 (WSI = 0 → right channel)[1)]		LR_SEL
			bit[3] Delay-Bit 0 No Delay 1 1 bit Delay		SP_SEL
			bit[2:0] sample rate control 000 32–48 kHz 001 26–32 kHz 010 20–26 kHz 011 14–20 kHz 100 10–14 kHz 101 8–10 kHz 110 96 kHz[2)] 111 automatic detection[3)]		SRC_48 SRC_32 SRC_24 SRC_16 SRC_12 SRC_8 SRC_96 SRC_A
ANALOG VOLUME **AVOL**					
02	16	w	audio volume control	0_{hex}	
			bit[15] Oscillator on/off (for test purpose only) 0 Oscillator on if internally required 1 Oscillator always on		OSC
			bit[14] deemphasis on/off 0 deemphasis off 1 deemphasis on		DEEM
			bit[13:8] analog audio volume level left: 000000 mute 000001 –75 dB 101100 +0 dB (default) 111000 +18 dB		AVOL_L
			bit[7:6] not used, set to 0		
			bit[5:0] analog audio volume level right 000000 mute 000001 –75 dB 101100 +0 dB (default) 111000 +18 dB		AVOL_R

[1)] see Fig. 2–1 and Fig. 2–2 on page 6
[2)] 96 kHz allowed for V_{DD}=5 V only
[3)] 96 kHz is not supported by automatic detection

I²C Sub-address (hex)	Number of Bits	Mode	Function	Default Values (hex)	Name
Global Configuration **GCFG**					
03	8	w	global configuration bit[7] select 3 V – 5 V mode 0 3 V 1 5 V bit[6:4] DAC and Power-Mode bit[6] bit[5] bit[4] 0 0 0 DAC off - Zero Power 0 1 0 DAC off - Analog Standby 1 0 0 DAC off - Aux to Line 1 1 0 DAC off - Full Power 0 x[1)] 1 DAC on - Aux to Line 1 x[1)] 1 DAC on - Full Power bit[3] AUX2 select 0 AUX2 off 1 AUX2 on bit[2] AUX1 select 0 AUX1 off 1 AUX1 on bit[1] aux-mono/stereo 0 stereo 1 mono bit[0] invert right power amplifier 0 not inverted 1 inverted	0_{hex}	SEL_53V PWMD INSEL_AUX2 INSEL_AUX1 AUX_MS IRPA
[1)] don't care					

3.6. Electrical Characteristics

3.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Temperature Range		–40	85	°C
T_S	Storage Temperature		–40	125	°C
P_{max}	Power Dissipation			500	mW
V_{SUPA}	Analog Supply Voltage[1)]	AVDD0/1	–0.3	6	V
V_{SUPD}	Digital Supply Voltage	VDD	–0.3	6	V
V_{Idig1}	Input Voltage, digital inputs	MCS1, MCS2, DEECTRL	–0.3	V_{SUPD} + 0.3	V
V_{Idig2}	Input Voltage, digital inputs	WSI, CLI, DAI, PORQ, SCL, SCI	–0.3	6	V
I_{Idig}	Input Current, all digital inputs		–5	+5	mA
V_{Iana}	Input Voltage, all analog inputs		–0.3	V_{SUPA} + 0.3	V
I_{Iana}	Input Current, all analog inputs		–5	+5	mA
I_{Oaudio}	Output Current, audio output[2)]	OUTL/R	–0.2	0.2	A
I_{Odig}	Output Current, all digital outputs[3)]		–10	10	mA

1) Both pins have to be connected together!
2) These pins are NOT short-circuit proof!
3) Total chip power dissipation must not exceed absolute maximum rating

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Supply Voltages						
T_A	Ambient Temperature Range[1)]		0		70	°C
T_{AE}	Extended Ambient Temperature Range[1)]		–40		85	°C
V_{SUPA1}	Analog Audio Supply Voltage	AVDD0/1	3.0[2)]	3.3	5.5	V
V_{SUPD}	Digital Supply Voltage	VDD	2.7	3.3	5.5	V
V_{SUPD96}	Digital Supply Voltage (if sample rate is 96 kHz)	VDD	4.75	5.0	5.5	V
Relative Supply Voltages						
V_{SUPA}	Analog Audio Supply Voltage in relation to the Digital Supply Voltage	AVDD0/1	V_{SUPD} –0.25 V		5.5	V
Analog Reference						
C_{AGNDC1}	Analog Reference Capacitor	AGNDC	1.0	3.3		µF
C_{AGNDC2}	Analog Reference Capacitor	AGNDC		10		nF
Analog Audio Inputs						
V_{AI}	Analog Input Voltage AC, SEL_53V = 0	AUXnL/R[3)]		0.35	0.7	V_{rms}
V_{AI}	Analog Input Voltage AC, SEL_53V = 1	AUXnL/R[3)]		0.525	1.05	V_{rms}
Analog Filter Input and Output						
Z_{AFLO}	Analog Filter Load Output[4)]	FOUTL/R	7.5		6	kΩ pF
Z_{AFLI}	Analog Filter Load Input[4)]	FINL/R	5.0		7.5	kΩ pF

1) The functionality of the IC in the extended temperature range has been verified by electrical characterization based on sample tests. All data sheet parameters are valid for normal operating temperature range, only.
2) typically operable down to 2.7 V, without loss of performance
3) n = 1 or 2
4) Please refer to Section 4.2. “Recommended Low-Pass Filters for Analog Outputs” on page 28.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Audio Output						
Z_{LO}	Audio Line Output[1)] (680 Ω Series Resistor required)	FINL/R	10		1.0	kΩ nF
Z_{AOL_HP}	Analog Output Load HP (47 Ω Series Resistor required)	OUTL/R		32 400		Ω pF
Z_{AOL_SP}	Analog Output Load SP (bridged)	OUTL/R		32 50		Ω pF
	Analog Output Load SP (Stereo)			16 100		Ω pF
I^2C Input						
f_{I2C}	I^2C Clock Frequency	SCL		400		kHz
Digital Inputs						
V_{IH}	Input High Voltage	CLI, WSI, DAI, PORQ, SCL, SDA	0.5× VDD			V
V_{IL}	Input Low Voltage				0.2× VDD	V
External Clock Input						
V_{IHx}[2)]	Ext. Clock High Voltage	XTI		0.25× VDD_{max}		V
V_{IL}	Input Low Ext. Clock	XTI		0.75× VDD_{min}		V
$I^2S_{Dut1\_96}$	Duty Cycle of I^2S input clock (sample rate=96 kHz)	CLI	45		55	%
$I^2S_{Dut1\_48}$	Duty Cycle of I^2S input clock (sample rate <=48 kHz)	CLI	40		60	%
Crystal Characteristics						
F_P	Load Resonance Frequency at C_l = 20 pF		13.3	14.725	17	MHz
R_{EQ}	Equivalent Series Resistance			12	30	Ω
C_0	Shunt (parallel) Capacitance			3	5	pF
Load at CLKOUT Output						
C_{load}	Capacitance	CLKOUT	0		50	pF

1) Please refer to Section 4.1. “Line Output Details” on page 28.
2) extended clock should be AC-coupled via 10 nF

3.6.3. Characteristics

At T_A = 0 to 70 °C, V_{SUPD} = 2.7 to 5.5 V, V_{SUPA} = 3.0 to 5.5 V; typical values at T_J = 27 °C, V_{SUPD} = V_{SUPA} = 3.3 V, positive current flows into the IC

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply							
I_{VDD}	Current Consumption	VDD		3.7 5.0		mA µA	DAC ON[1] DAC OFF[2] V_{SUPD} = 3.3 V (see I²C register GCFG)
				7.0 5.0		mA µA	DAC ON[1] DAC OFF[2] V_{SUPD} = 5 V
Digital Input Pin – Leakage							
I_I	Input Leakage Current	DAI, TESTEN, PORQ, DEECTRL, MCS1/2			±1	µA	$V_{GND} \leq V_I \leq V_{SUP}$
Digital Output Pin – Clock Out							
V_{OH}	Output High Voltage	CLKOUT	V_{SUPD} −0.3			V	no load at output
V_{OL}	Output Low Voltage				0.3	V	
I²C Bus							
R_{on}	Output Impedance	SCL, SDA			60	Ω	I_{load} = 5 mA, V_{SUPD} = 2.7 V
Analog Supply							
I_{AVDD}	Current Consumption Analog Audio	AVDD0/1		1.0 630 3.6 8.2		µA µA mA mA	Zero Power Analog Standby Aux to Line Full Power SEL_53 = 0 A_{VDD} = 3.3 V[3]
				1.0 750 6.0 12.9		µA µA mA mA	Zero Power Analog Standby Aux to Line Full Power SEL_53 = 1 A_{VDD} = 5 V[3] (see I²C register GCFG)

[1] I²S active, 32-bit mode, fs = 48 kHz
[2] No I²C traffic
[3] DAC on, I²S active, 32-bit mode, fs = 48 kHz, 1 kHz @ 0 dB_{FS} volume = 0 dB

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Output	AVDD0/1, OUTL/R		50		dB	1 kHz sine at 100 mV_{rms}
				20		dB	≤ 100 kHz sine at 100 mV_{rms}
$PSRR_{LO}$	Power Supply Rejection Ratio for Line Output	AVDD0/1, FINL/R		50		dB	1 kHz sine at 100 mV_{rms}
				40		dB	≤ 100 kHz sine at 100 mV_{rms}
Reference Frequency Generation							
V_{DCXTI}	DC Voltage at Oscillator Pins	XTI/O		0.5× V_{SUPA}		V	
C_{LI}	Input Capacitance at Oscillator Pin	XTI/O		3		pF	
Vxtalout	Voltage Swing at Oscillator Pins, pp	XTI/O	60		100	% VSUPA	
	Oscillator Start-Up Time				50	ms	AV_{DD}/V_{DD} ≥ 2.5 V
Analog Audio							
V_{AO}	Analog Output Voltage AC	OUTL/R, FOUTL/R, FINL/R	0.65	0.7	0.75	V_{rms}	SEL_53V = 0, R_L > 5 kΩ, Analog Gain = 0 dB Input = 0 dB_{FS} digital
			1.0	1.05	1.1	V_{rms}	SEL_53V = 1
G_{AUX}	Gain from Auxiliary Inputs to Line Outputs	AUXnL/R, FINL/R	−0.5	0	0.5	dB	f = 1 kHz, sine wave, R_L > 5 kΩ 0.5 V_{rms} to AUXnL/R
P_{HP}	Output Power (Headphone)	OUTL/R		5		mW	SEL_53V = 0, R_L = 32 Ω, Analog Gain = +3 dB, distortion < 1%, external 47 Ω series resistor required
				12		mW	SEL_53V = 1
P_{SP}	Output Power (Speaker)	OUTL/R		120		mW	R_L = 32 Ω (bridged), Analog Gain = +3 dB, distortion < 10%, SEL_53V = 0, IRPA = 1
				280		mW	SEL_53V = 1
G_{AO}	Analog Output Gain Setting Range	OUTL/R	−75		18	dB	
dG_{AO1}	Analog Output Gain Step Size	OUTL/R		3.0		dB	Analog Gain: −75 dB...−54 dB
dG_{AO2}	Analog Output Gain Step Size	OUTL/R		1.5		dB	Analog Gain: −54 dB...+18 dB
E_{GA1}	Analog Output Gain Error	OUTL/R	−2		2	dB	−46.5 dB≥Analog Gain ≥−54 dB

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
E_{GA2}	Analog Output Gain Error	OUTL/R	−1		1	dB	−40.5 dB≥Analog Gain ≥−45 dB
E_{GA3}	Analog Output Gain Error	OUTL/R	−0.5		0.5	dB	+18 dB≥Analog Gain ≥−39 dB
E_{dGA}	Analog Output Gain Step Size Error	OUTL/R	−0.5		0.5	dB	+18 dB≥Analog Gain ≥−48 dB
SNR_{AUX}	Signal-to-Noise Ratio from Analog Input to Line Output	AUXn, FINL/R		98		dB	SEL_53V = 0: input −40 dB below 0.7 V_{rms} Analog Gain = 0 dB, BW =20 Hz...20 kHz unweighted
	Signal-to-Noise Ratio from Analog Input to Headphone Output	AUXn, OUTn		93		dB	
SNR_1	Signal-to-Noise Ratio	OUTL/R	89	91		dB	$R_L \geq 32\ \Omega$ (external 47 Ω series resistor required) BW =20 Hz...0.5 fs[1] unweighted, Analog Gain = 0 dB, Input = −20 dB_{FS}
		FINL/R	90	92		dB	$R_L \geq 5\ k\Omega$, $R_{dec} \geq 612\ \Omega$ BW etc. as above 16 bit I^2S, SEL_53V = 0
				94		dB	32 bit I^2S, SEL_53V = 0
				96		dB	16 bit I^2S, SEL_53V = 1
				98		dB	32 bit I^2S, SEL_53V = 1
				103		dB(A)	32 bit I^2S, SEL_53V = 1
SNR_2	Signal-to-Noise Ratio	OUTL/R		62		dB	$R_L \geq 32\ \Omega$ (external 47 Ω series resistor required) BW = 20 Hz..0.5 fs[1] unweighted Analog Gain = −40.5 dB, Input = −3 dB_{FS}
Lev_{Mute}	Mute Level	OUTL/R		−110		dBV	BW = 20 Hz...22 kHz unweighted, no digital input signal, Analog Gain = Mute
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R, FOUTL/R		−0.1		dB	0...0.446 fs (no external filters used)
$A_{D/A}$	D/A Stop Band Attenuation			40		dB	0.55...7.533 fs (no external filters used)
BW_{AUX}	Bandwidth for Auxiliary Inputs	AUXnL/R, FINL/R		760		kHz	(no external filters used)

[1] BW = 20 Hz...22 kHz if fs = 96 kHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
THD_{ALO}	Total Harmonic Distortion from Auxiliary Inputs to Line Outputs	AUXnL/R, FINL/R			0.01	%	BW = 20 Hz...22 kHz, unweighted, R_L > 5 kΩ Input 1 kHz at 0.5 V_{rms} $R_{dec} \geq 612\ \Omega$
THD_{DLO}	Total Harmonic Distortion (D/A converter to Line Output)	FINL/R			0.01	%	BW = 20 Hz...0.5 fs[1], unweighted, R_L > 5 kΩ Input 1 kHz at −3 dB_{FS} $R_{dec} \geq 612\ \Omega$
THD_{HP}	Total Harmonic Distortion (Headphone)	OUTL/R			0.05	%	BW = 20 Hz...0.5 fs[1], unweighted, $R_L \geq 32\ \Omega$ (47 Ω series resistor required), Analog Gain = 0 dB, Input 1 kHz at −3 dB_{FS}
THD_{SP}	Total Harmonic Distortion (Speaker)	OUTL/R			0.5	%	BW = 20 Hz...0.5 fs[1], unweighted, $R_L \geq 32\ \Omega$ (speaker bridged), Analog Gain = 0 dB, Input 1 kHz at −3 dB_{FS}
$XTALK_{LO}$	Cross-Talk Left/Right Channel (Line Output)	AUXnL/R, FOUTL/R, FINL/R	−70	−80		dB	f = 1 kHz, sine wave, R_L > 7.5 kΩ Analog Gain = 0 dB, Input = −3 dB_{FS} or 0.5 V_{rms} to AUXnL/R
$XTALK_{HP}$	Crosstalk Left/Right Channel (Headphone)	OUTL/R	−70	−80		dB	f = 1 kHz, sine wave, OUTL/R: $R_L \geq 32\ \Omega$ (47 Ω series resistor required) Analog Gain = 0 dB, Input = −3 dB_{FS} or 0.5 V_{rms} to AUXnL/R
$XTALK_2$	Crosstalk between Input Signal Pairs	AUXnL/R	−70	−80		dB	f = 1 kHz, sine wave, FOUTL/R: R_L > 7.5 kΩ OUTL/R: $R_L \geq 32\ \Omega$ (47 Ω series resistor required) Analog Gain = 0 dB, Input = −3 dB_{FS} and 0.5 V_{rms} to AUXnL/R
V_{AGNDC}	Analog Reference Voltage	AGNDC		1.5		V	SEL_53V = 0 R_L >> 10 MΩ, referred to VREF
				2.25		V	SEL_53V = 1 R_L >> 10 MΩ, referred to VREF

[1] BW = 20 Hz...22 kHz if fs = 96 kHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{IAUX}	Input Resistance at Input Pins	AUXnL/R	12.1 11.6	15	17.9 19.0	kΩ kΩ	$T_J = 27$ °C $T_A = 0$ to 70 °C[1)] Input selected, Aux to Line i = ± 10 µA, referred to VREF
			24.2 23.3	30	35.8 37.9	kΩ kΩ	$T_J = 27$ °C $T_A = 0$ to 70 °C[1)] Input not selected i = ± 10 µA, referred to VREF
R_{OOUT}	Output Resistance at Output Pins	OUTL/R		700		Ω	$T_J = 27$ °C Analog Standby i = ± 200 µA, referred to VREF
R_{OFILT}	Output Resistance of Filter Pins	FINL		15		kΩ	full power, Mute i = ± 10 µA, referred to VREF
		FINR		11.25		kΩ	
V_{OffI}	Offset Voltage at Input Pins	AUXnL/R	–20		20	mV	referred to AGNDC
V_{OffO}	Offset Voltage at Output Pins	OUTL/R	–10		10	mV	Mute referred to AGNDC
V_{OffFO}	Offset Voltage at Filter Output Pins	FOUTL/R	–20		20	mV	analog standby, referred to AGNDC
V_{OffFI}	Offset Voltage at Filter Input Pins	FINL/R	–20		20	mV	analog standby, referred to AGNDC
dV_{DCPD}	Difference of DC Voltage at Output Pins	OUTL/R	–10		10	mV	Analog Gain = Mute, switched from analog standby to full power

[1)] BW = 20 Hz...22 kHz if fs = 96 kHz

4. Applications

4.1. Line Output Details

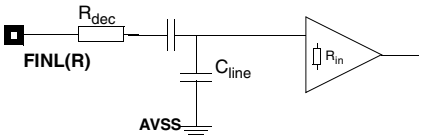

Fig. 4–1: Use of FINL/R as Line Outputs

Table 4–1: Load at FINL/R when used as Line Output for external amplifier

Filter Order	R_{dec}	R_{in}
1st, 2nd, 3rd	680 Ω	> 10 kΩ
R_{dec}: Resistor used for decoupling C_{line} from FINL(R) to achieve stability		
C_{line}: Capacitive load according to e.g. cable, amplifier		
R_{in}: Input resistance of amplifier		

4.2. Recommended Low-Pass Filters for Analog Outputs[1)]

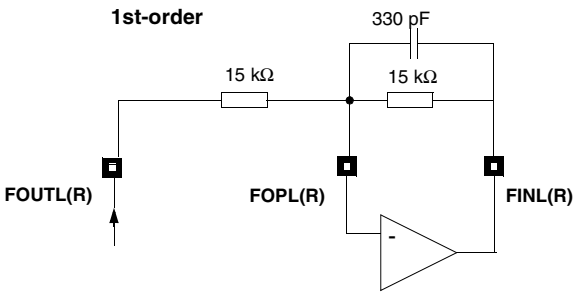

Fig. 4–1: 1st-order low-pass filter

Table 4–2: Attenuation of 1st-order low-pass filter

Frequency	Gain
24 kHz	–2.2 dB
30 kHz	–3.0 dB

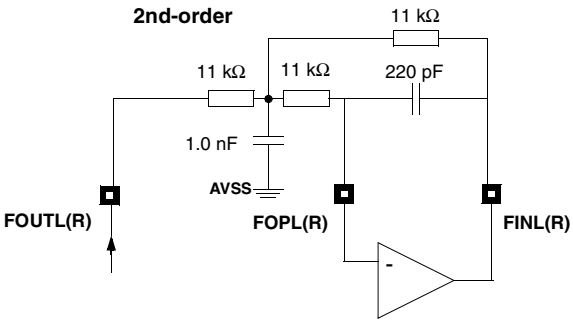

Fig. 4–2: 2nd-order low-pass filter

Table 4–3: Attenuation of 2nd-order low-pass filter

Frequency	Gain
24 kHz	–1.5 dB
30 kHz	–3.0 dB

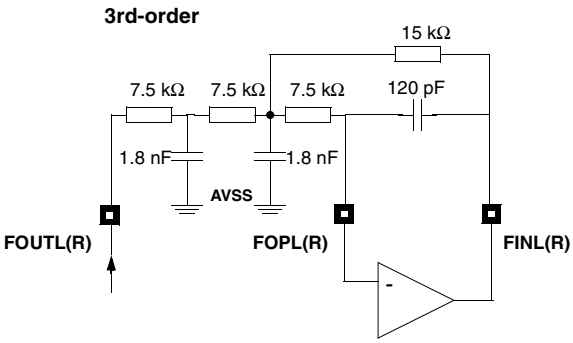

Fig. 4–3: 3rd-order low-pass filter

Table 4–4: Attenuation of 3rd-order low-pass filter

Frequency	Gain
18 kHz	0.17 dB
24 kHz	–0.23 dB
30 kHz	–3.00 dB

[1)] without deemphasis circuit

4.3. Recommendations for Filters and Deemphasis

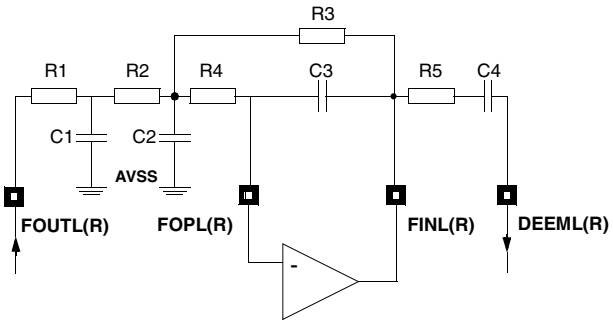

Fig. 4–4: General circuit schematic

Table 4–5: Resistor and Capacitor values

	1st order	2nd order	3rd order
R1 (kΩ)	0		7.5
C1 (pF)	open		560
R2 (kΩ)	18	11	7.5
C2 (pF)	open	1000	270
R3 (kΩ)	18	11	15
C3 (pF)	180	180	82
R4 (kΩ)	0	11	7.5
R5 (kΩ)	18	22	22
C4 (nF)	1.8	1.0	1.0

4.4. Recommendations for MegaBass Filter without Deemphasis

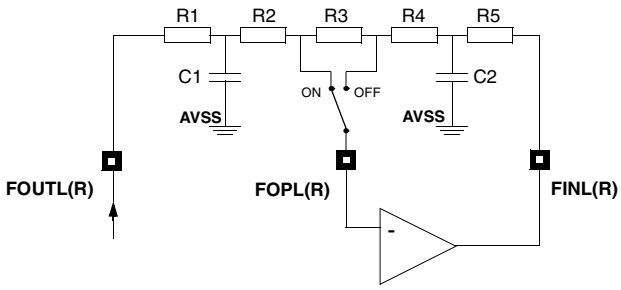

Fig. 4–1: General circuit schematic

Table 4–6: Resistor and Capacitor values

	DC-Gain = 10 dB fc1 = 100 Hz fc2 = 330 Hz
R1 (kΩ)	13
C1 (nF)	47
R2 (kΩ)	0
R3 (kΩ)	15
R4 (kΩ)	15
R5 (kΩ)	13
C2 (nF)	47

4.5. Power-up/down Sequence

In order to get a click-free power-up/down characteristic, it is recommended to use the following sequences:

4.5.1. Power-up Sequence

1. Start V_{DD} from 0 to +3.3 V and start $AV_{DD0/1}$ from 0 to +3.3 V/+5 V. See Fig. 4–2.
2. Release PORQ from 0 to V_{DD}. See Fig. 4–2.
3. Follow the logical power-up sequence in Fig. 4–3.

4.5.2. Power-down Sequence

Follow the logical power-down sequence in Fig. 4–3.

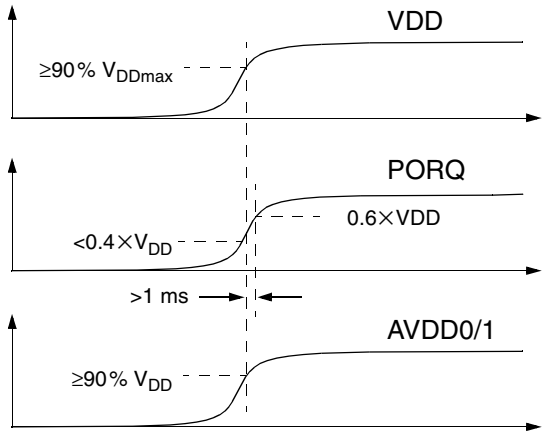

Fig. 4–2: Electrical power-up sequence

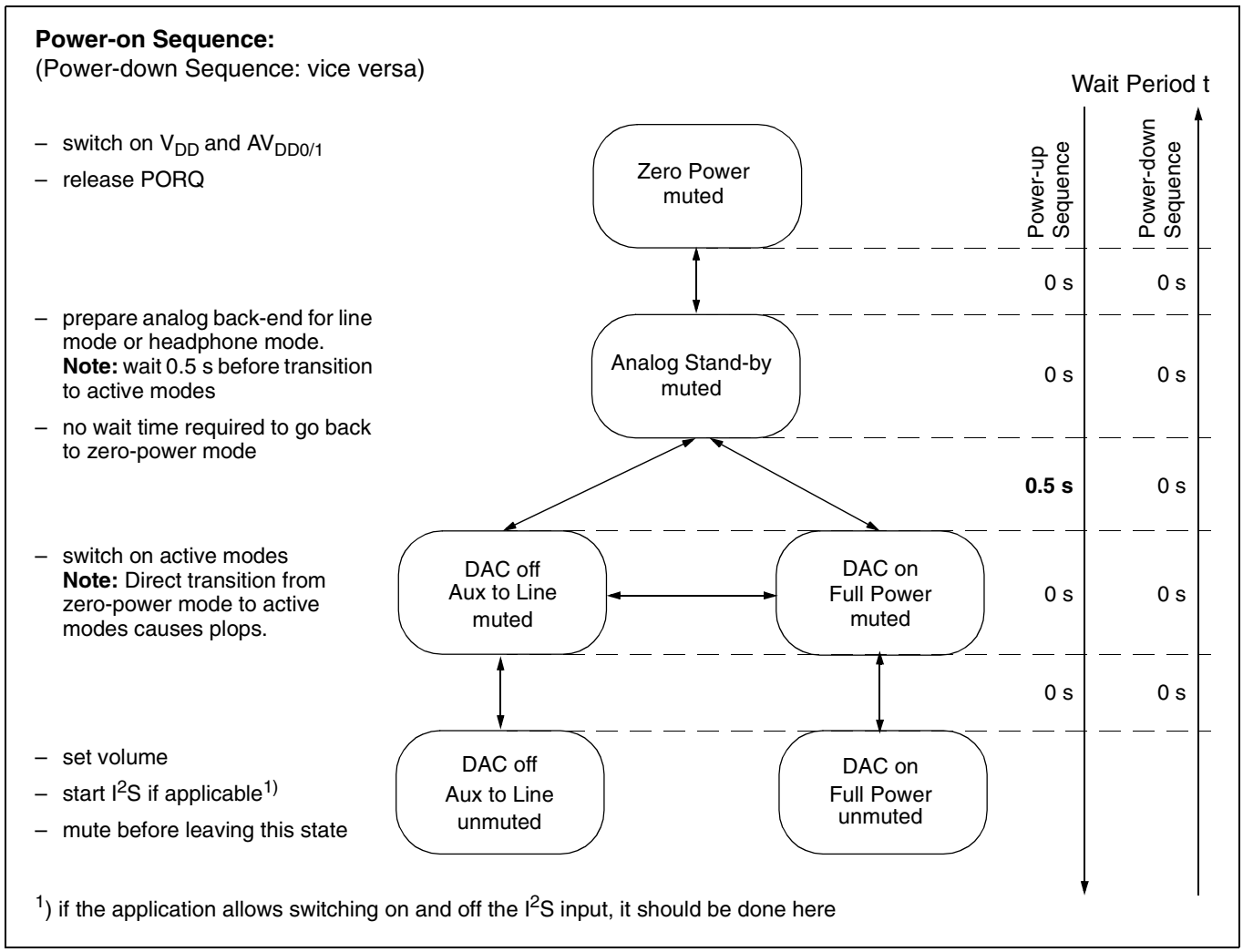

Fig. 4–3: Logical power-up/down sequence

4.6. Typical Applications

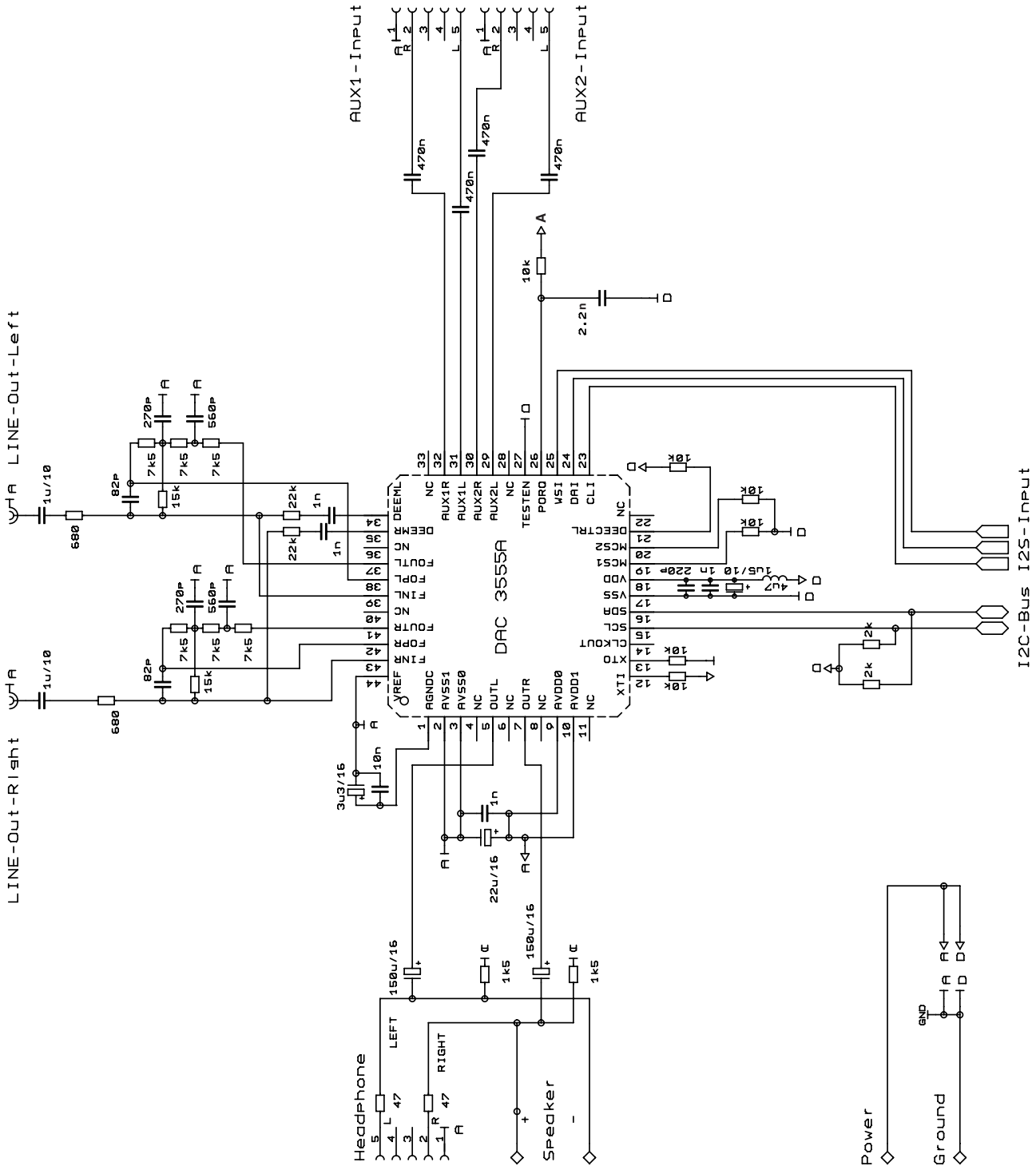

Fig. 4–4: Application circuit schematic 1: Standard application with analog deemphasis. Oscillator not needed.
Package: PMQFP44

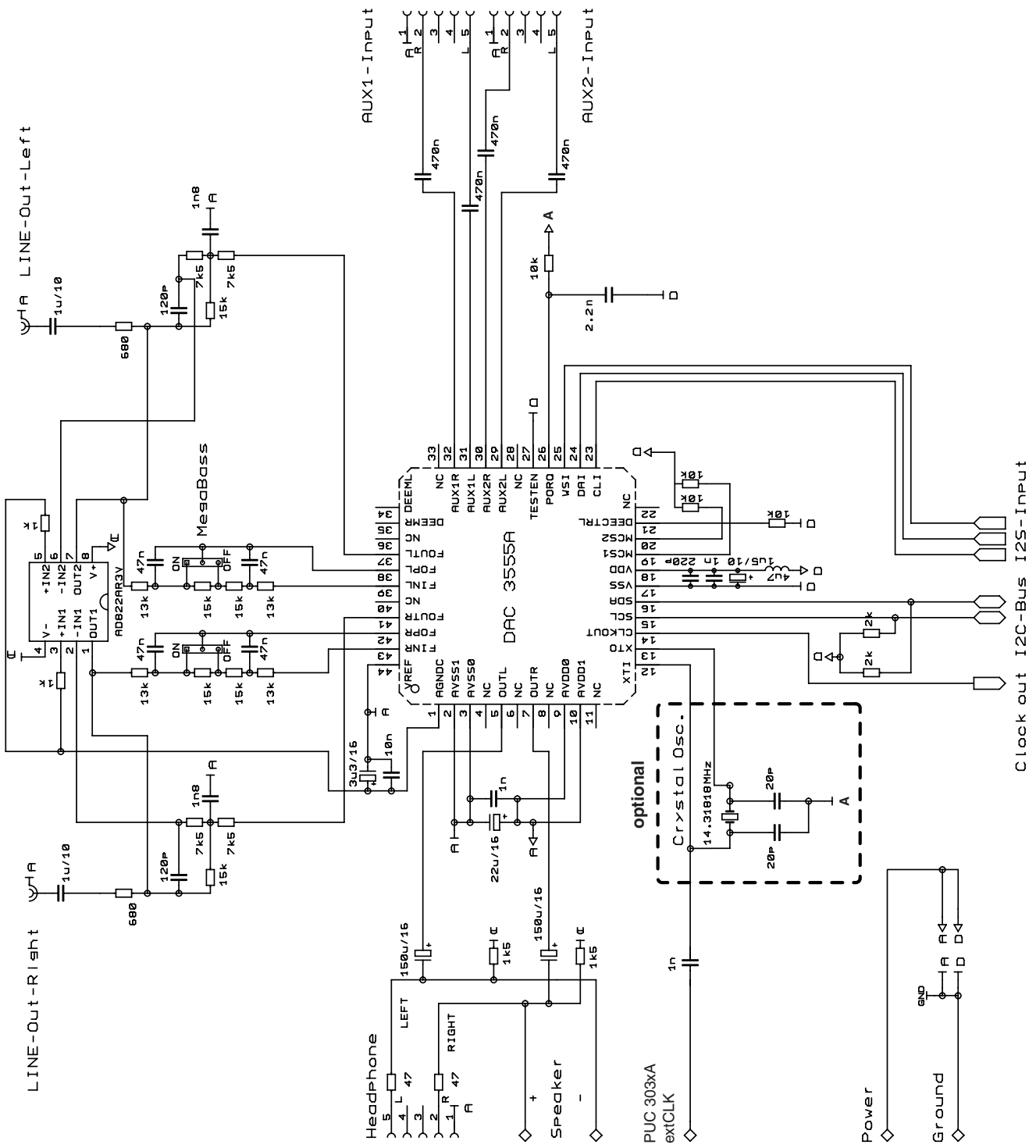

Fig. 4–5: Application circuit schematic 2: MPEG application with analog Megabass and 14.31818 MHz clock input. Package: PMQFP44

5. Data Sheet History

1. Preliminary data sheet: “DAC 3555A Stereo Audio DAC”, Jan. 8, 2002, 6251-575-1PD. First release of the preliminary data sheet.

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Printed in Germany
Order No. 6251-575-1PD