

## 512K x 8 PDIP Static RAM

### Features

- 4.5V–5.5V operation
- CMOS SRAM for optimum speed and power
- Low active power (165 mW max.)
- Low standby power (L Version)—(110  $\mu$ W max)
- 2V data retention (L Version)
- JEDEC-compatible pinout
- 32-pin, 0.6-inch-wide DIP package
- TTL-compatible inputs and outputs

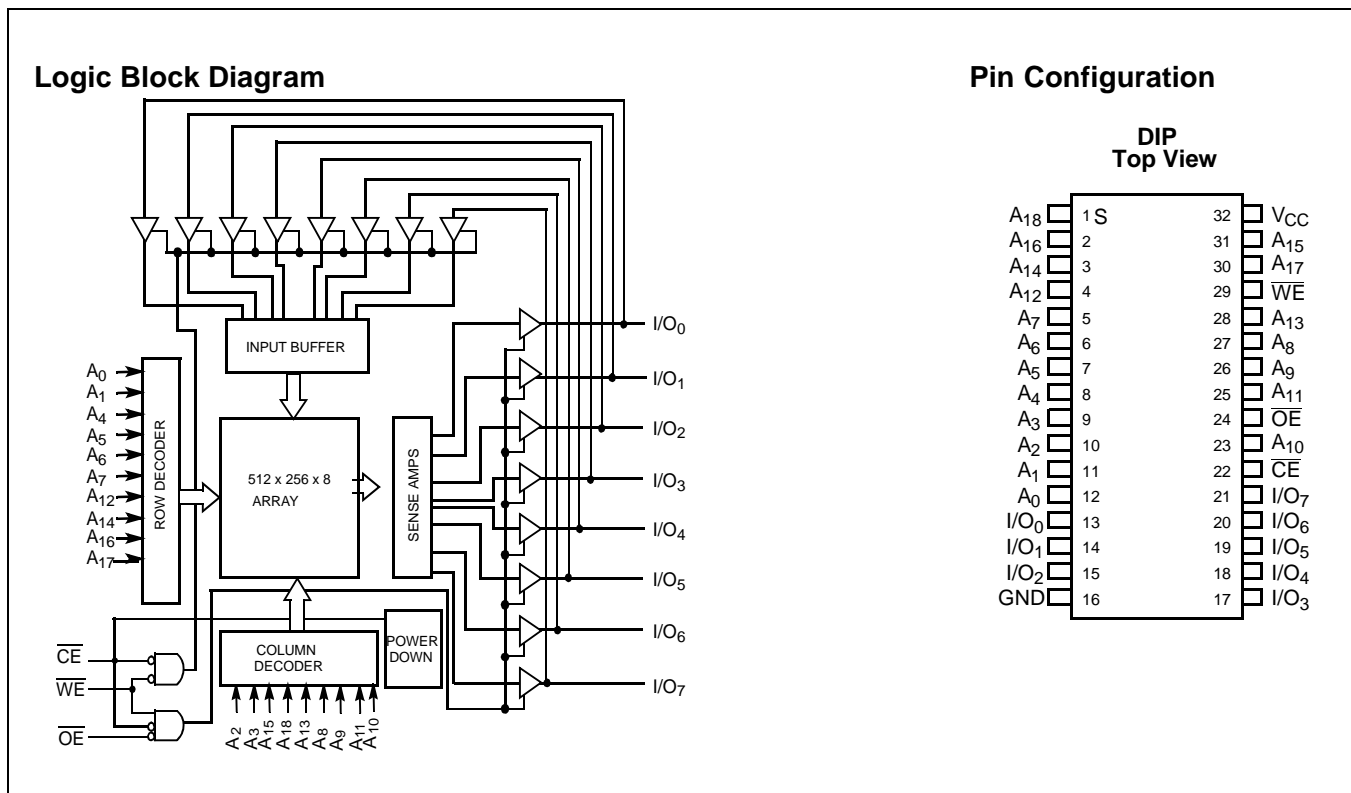
### Functional Description

The CYM1465A is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. This device has

an automatic power-down feature that reduces power consumption by more than 99% when deselected.

Writing to the SRAM is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the eight input/output pins ( $I/O_0$  through  $I/O_7$ ) of the device is then written into the memory location specified on the address pins ( $A_0$  through  $A_{18}$ ). Reading from the device is accomplished by taking chip select ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LOW while write enable ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins ( $A_0$  through  $A_{18}$ ) will appear on the eight appropriate data input/output pins ( $I/O_0$  through  $I/O_7$ ). The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CYM1465A is available in a 32-pin 600-mil wide body PDIP package.



### Selection Guide

	CYM1465A-70	CYM1465A-85
Maximum Access Time (ns)	70	85
Maximum Operating Current (mA)	20	20
Maximum Standby Current ( $\mu$ A)	20	20

### Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... -55°C to +150°C  
 Ambient Temperature with  
 Power Applied..... -10°C to +85°C  
 Supply Voltage to Ground Potential..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

### Operating Range

Range	Ambient Temperature	CYM1465A	
		V <sub>CC</sub>	Unit
Commercial	0°C to +70°C	5V ± 10%	
Industrial	-40°C to +85°C	5V ± 10%	

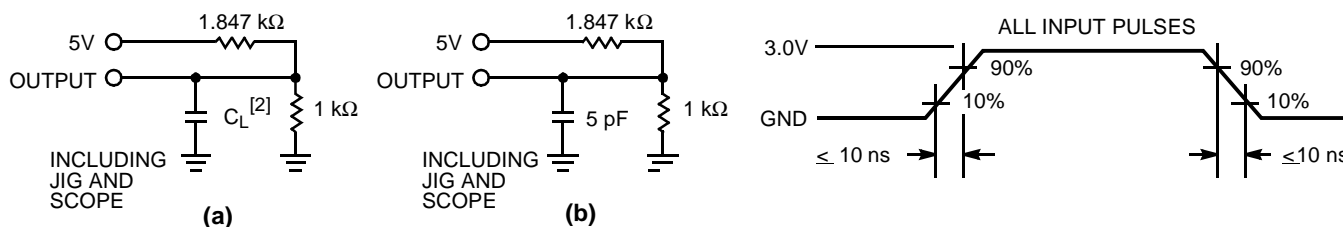
### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1465A		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, $\overline{CS} \leq V_{IL}$		20	mA
I <sub>SB1</sub>	Automatic $\overline{CS}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , Min. Duty Cycle = 100%		1.5	mA
I <sub>SB2</sub>	Automatic $\overline{CS}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} > V_{CC} - 0.3V$ , V <sub>IN</sub> > V <sub>CC</sub> - 0.3V or V <sub>IN</sub> < 0.3V		20	μA

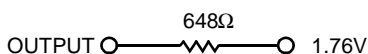
### Capacitance<sup>[1]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



#### Notes:

1. Tested on a sample basis.
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100-pF load capacitance for 85-, 100-, 120-, and 150-ns speeds. C<sub>L</sub> = 30 pF for 70-ns speed.

**Switching Characteristics** Over the Operating Range<sup>[2]</sup>

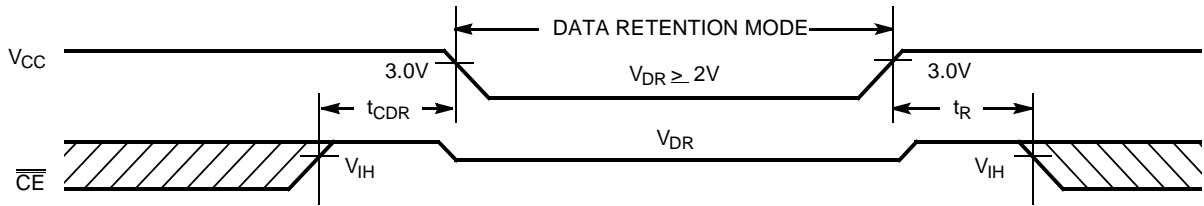
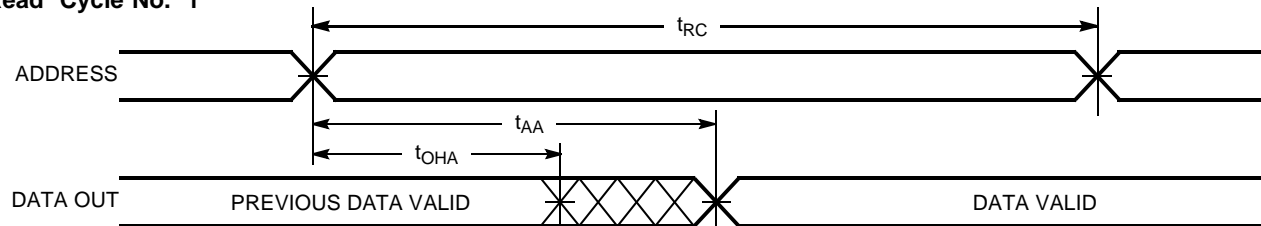
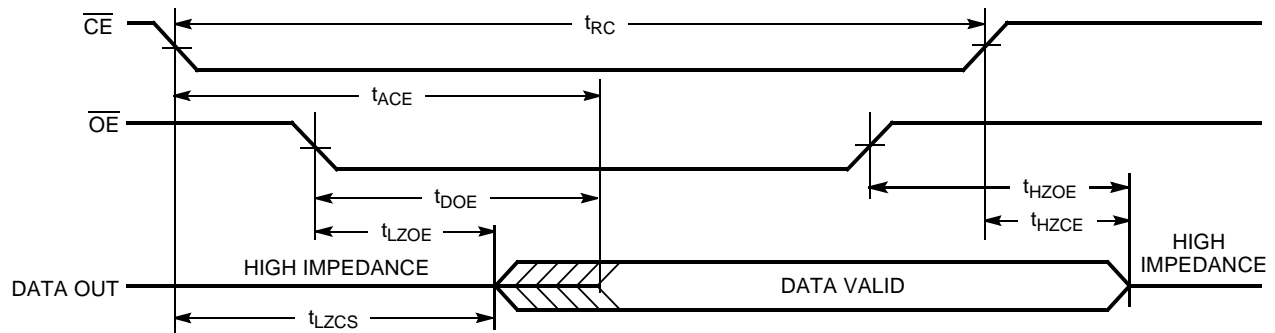
Parameter	Description	CYM1465A-70		CYM1465A-85		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	70		85		ns
$t_{AA}$	Address to Data Valid		70		85	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		70		85	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		35		45	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[3]</sup>		25		30	ns
$t_{LZCS}$	$\overline{CE}$ LOW to Low Z	10		10		ns
$t_{HZCS}$	$\overline{CE}$ HIGH to High Z <sup>[3]</sup>		25		30	ns
$t_{PU}$	$\overline{CE}$ LOW to Power Down	0		0		
$t_{PD}$	$\overline{CE}$ HIGH to Power Down		70		85	
<b>WRITE CYCLE<sup>[4]</sup></b>						
$t_{WC}$	Write Cycle Time	70		85		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	60		75		ns
$t_{AW}$	Address Set-Up to Write End	60		75		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	55		65		ns
$t_{SD}$	Data Set-Up to Write End	30		35		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[3]</sup>		25		30	ns

**Data Retention Characteristics** Over the Operating Range (L Version Only)

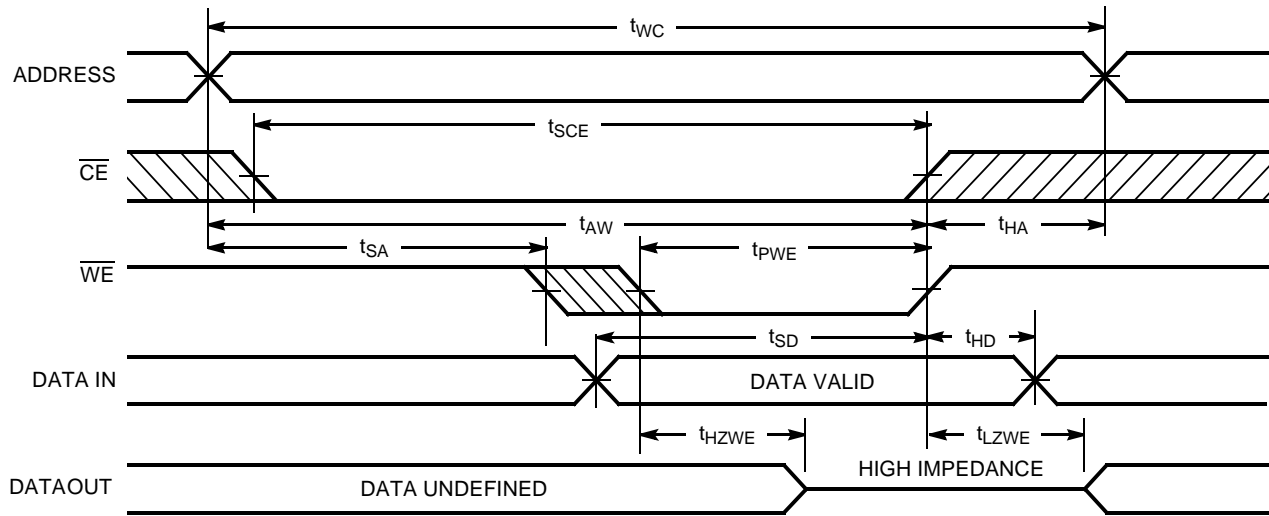
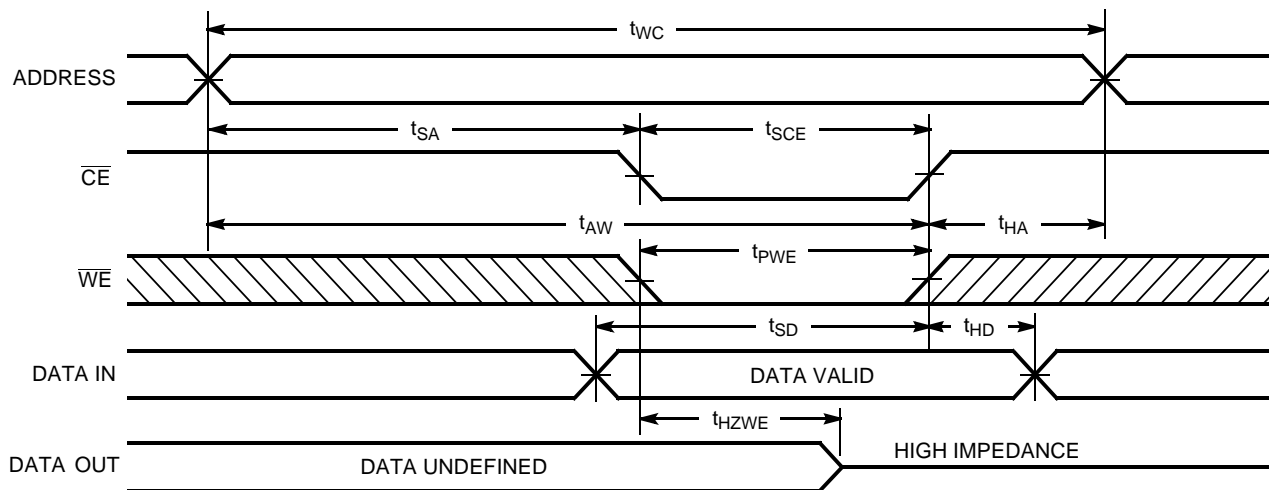
Parameter	Description	Test Conditions	Commercial		Industrial		Unit
			Min.	Max.	Min.	Max.	
$V_{DR}$	$V_{CC}$ for Retention Data		2		2		V
$I_{CCDR3}$	Data Retention Current	No Input may exceed $V_{CC}+0.3V$		20		20	$\mu A$
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time	$V_{DR} = 3.0V,$	0		0		ns
$t_R^{[5]}$	Operation Recovery Time	$\overline{CE} > V_{CC} - 0.3V,$ $V_{IN} > V_{CC} - 0.3V$ or $V_{IN} < 0.3V$	$t_{RC}$		$t_{RC}$		ns

**Notes:**

- $C_L = 5$  pF as in part (b) of AC Test Loads and Waveforms. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- Guaranteed, not tested.

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1** <sup>[6,7]</sup>

**Read Cycle No. 2** <sup>[6,8]</sup>

**Notes:**

6.  $\overline{WE}$  is HIGH for read cycle.
7. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
8. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[4]</sup>**

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[4,9]</sup>**

**Note:**

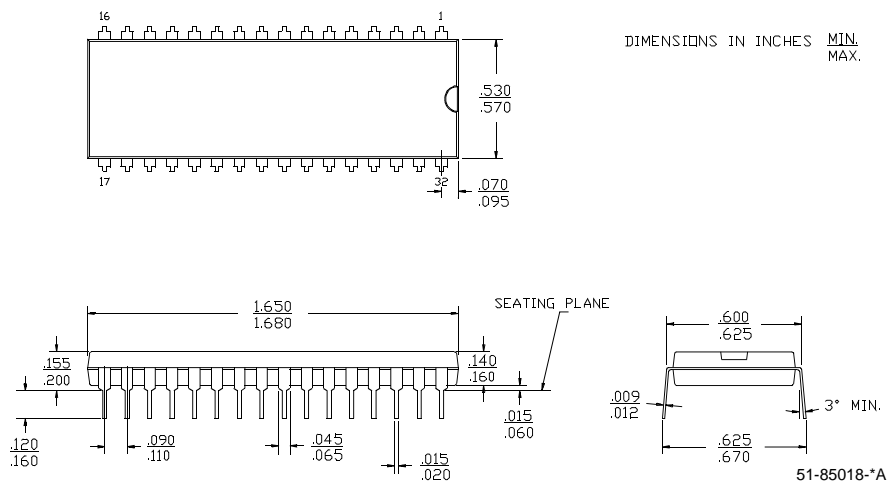
9. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Truth Table**

Inputs			Output	Mode
CE	WE	OE		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM1465ALPD-70C	P19	32-Pin DIP Module	Commercial
70	CYM1465ALPD-70I	P19	32-Pin DIP Module	Industrial
85	CYM1465ALPD-85C	P19	32-Pin DIP Module	Commercial
85	CYM1465ALPD-85I	P19	32-Pin DIP Module	Industrial

**Package Diagram**
**32-Lead (600-Mil) Molded DIP P19**


**Revision History**

<b>Document Title: CYM1465A 512K x 8 PDIP Static RAM</b> <b>Document Number: 38-05269</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>ISSUE DATE</b>	<b>ORIG. OF CHANGE</b>	<b>DESCRIPTION OF CHANGE</b>
**	114171	3/19/02	DSG	Change from Spec number: 38-M-00036 to 38-05269