Advance Product Information

VSC7128

Hex Port Bypass Circuit / Dual Repeater for 1.0625 Gb/s FC-AL Disk Arrays

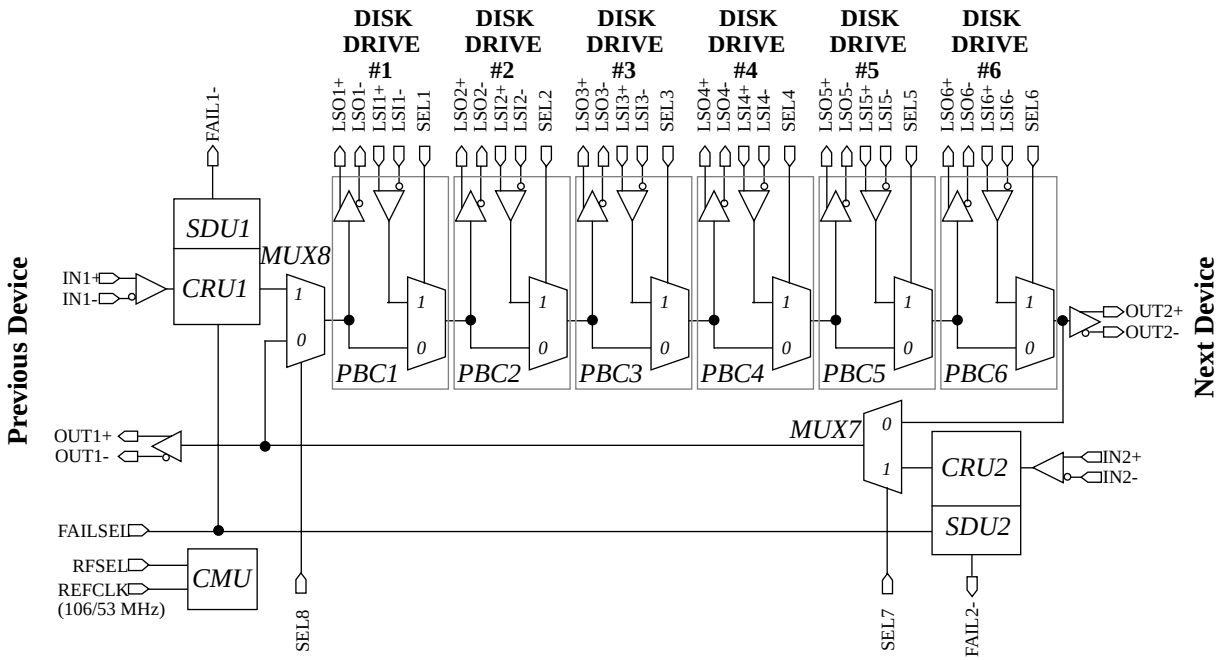
Features

- Supports ANSI X3T11 1.0625Gb/s FC-AL Disk Attach for Resiliency
- Dual Repeaters (CRUs) Improve Signal Quality
- Six Port Bypass Circuits (PBCs) for Resiliency
- Dual Digital Signal Detect Units (SDUs)
- Fully Differential for Minimum Jitter
- Selectable REFCLK: 53.125 / 106.25MHz
- TTL Bypass Select
- 3.3V Supply, 1.3W
- 64-Pin, 14 mm Thermally Enhanced PQFP

General Description

The VSC7128 contains six Port Bypass Circuits (PBCs), dual embedded Clock Recovery Unit repeaters (CRU) and dual Signal Detect Units (SDU). These functions are integrated into a single part to minimize circuit size, part count, cost, high frequency routing and jitter accumulation. Together, they allow for optimized designs of FC-AL JBOD systems that provide resiliency and hot insertion/removal of disk drives. The PBCs configure the FC-AL loop to either include or exclude each drive. Repeaters retime the incoming signal thereby attenuating jitter so that downstream devices see high amplitude, low jitter signals. The SDUs determine whether the output of the CRU is a valid Fibre Channel signal. Disk drives are connected directly to the LSO/LSI/SEL pins while the IN/OUT pins can be connected to any FC-AL devices.

VSC7128 Block Diagram



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Functional Description

A Port Bypass Circuit contains a differential 2:1 mux operating at 1.0625 Gb/s. The input to the PBC is always passed to the LSOx output of the PBC to let the disk drive monitor loop activity. The mux selects either the disk drive's input, LSIx, or the input from the previous PBC as determined by the SELx input which is normally connected directly to the disk drives EN_BYP output. When SELx is HIGH, the mux selects the disk drive input, LSIx. When SELx is LOW, the mux bypasses the disk drive input and passes the output of the previous PBC to the output of the PBC. Two extra muxes help route serial signals. MUX7 passes either the output of PBC6 (bypass mode) or the output of CRU2 (normal mode) to MUX8/OUT1 depending whether SEL7 is LOW or HIGH. MUX8 passes either the output of CRU1 or the output of MUX7 to PBC1 depending on whether SEL8 is HIGH or LOW.

A TTL reference clock, REFCLK, is used by the internal Clock Multiplier Unit (CMU) to generate a baud rate clock at 1.0625 Gb/s. If RFSEL is HIGH, the CMU multiplies REFCLK (nominally 106.25MHz) by a factor of 10. If RFSEL is LOW, the CMU multiplies REFCLK (nominally 53.125MHz) by a factor of 20. The user must ensure that RFSEL is properly set in order to match the frequency of REFCLK.

Two fully integrated Clock Recovery Units (CRUs) are provided to improve signal quality and determine whether the input to the repeater is a valid Fibre Channel signal. Each repeater consists of a Clock Recovery Unit (CRU) and a digital Signal Detect Unit (SDU). The CRU locks onto the incoming signal, generates a recovered clock (at 1.0625 GHz) and uses this clock to resynchronize the incoming signal. The recovered data has improved signal quality due to amplification and jitter attenuation. Recovered data is retimed to the recovered clock, not to REFCLK. The design of the CRU eliminates the need for any Lock-to-Reference signal since, in the absence of data, the CRU locks onto REFCLK automatically thereby eliminating the need for any external control circuitry.

The Signal Detect Units (SDUs) tests the output of the CRUs for valid Fibre Channel data by detecting run length errors (more than 5 consecutive 1's or 0's) and the absence of a seven bit pattern found in the K28.5 character of either disparity ('0000101' or '1111010'). This K28.5 pattern should occur multiple times between frames. The maximum length of a Fibre Channel frame is 2148 bytes (or 21,480 encoded bits) and the SDU divides time into ~31 microsecond time intervals (2^15 bit times). At the end of each interval, any run length or K28.5 errors which occurred during the interval are stored internally for use by the state machine which drives the SDU output, FAILx-.

The FAILSEL input controls both SDUs and the FAILx- outputs provide the status of each SDU. FAILSEL selects two different modes generated by the SDU; Single Frame (LOW) or Multiple Frame (HIGH) Error Mode. In Single Frame Error Mode, any error condition that occurs within an interval causes FAILx- to be asserted LOW immediately after that interval. FAILx- remains asserted until immediately after an error-free interval occurs. In Multiple Frame Error Mode, FAILx- is asserted after four consecutive intervals containing errors and remains asserted until four consecutive error-free intervals occur. The intent of the Multiple Frame Error Mode is to allow FAIL1- or FAIL2- to be directly connected to the mux controls, SEL8 or SEL7, in order to configure the part to isolate IN1 or IN2 whenever valid data is not present. Single Frame Error Mode allows the user to develop their own algorithm for monitoring data and controlling MUX8 or MUX7.

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AC Characteristics

Figure 1: AC Timing Diagrams

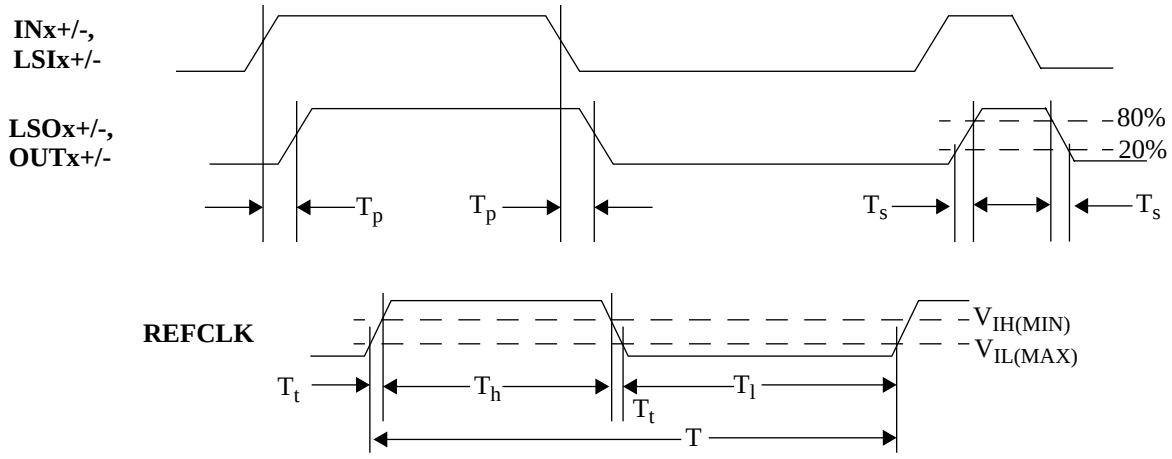

Table 1: AC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
	Differential Inputs/Outputs				
T_p	Latency from IN, LSI to LSO, OUT	0.25	7.0	ns	75 Ohm Load
T_s	Differential Output Rise/Fall time	—	300	ps	Between 20% and 80% Tested on a sample basis
	Reference Clock Requirements				
T_t	REFCLK input rise/fall times	—	2.0	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
F	REFCLK Frequency	105 52.5	108 54	MHz	106.25 MHz Nominal if RFSEL is HIGH 53.125 MHz Nominal if RFSEL is LOW
T	REFCLK Period	9.2 18.5	9.53 19.0	ns	RFSEL = HIGH RFSEL = LOW
F_o	Frequency Offset	-200	+200	ppm	Maximum frequency offset between 10 or 20 times REFCLK and the data rate of the serial input to the CRU.
DC	REFCLK Duty Cycle	35	65	%	Measured at 1.5V
T_h, T_l	REFCLK Input HIGH/LOW time	2.5	—	ns.	From $V_{IL(min)}$ to $V_{IH(min)}$ or $V_{IH(max)}$ to $V_{IL(max)}$

DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	Output LOW Voltage (TTL)	—	—	0.5	V	I_{OL}= +1.0mA
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.3V ± 5%
P_D	Power Dissipation	—	1.3	2.1	W	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply current	—	390	620	mA	Outputs open, V_{DD} = V_{DD} max
$\Delta V_{IN(DF)}$	PECL input swing	300	—	2600	mVp-p	AC Coupled. Internally biased at $V_{DD}/2$
ΔV_{OUT75}	PECL output swing: LSO, OUT	1200	—	2200	mVp-p	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	PECL output swing: LSO, OUT	1200	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{DD}) ..... -0.5V to +4V
PECL DC Input Voltage ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage ..... -0.5V to 5.5V
DC Voltage Applied to TTL Outputs ..... -0.5V to V_{DD} + 0.5V
TTL Output Current ..... +/-50mA
PECL Output Current ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65° to + 150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage ..... 3.3V +/- 5%
Ambient Operating Temperature Range ..... 0°C Ambient to +90°C Case

Notes:

1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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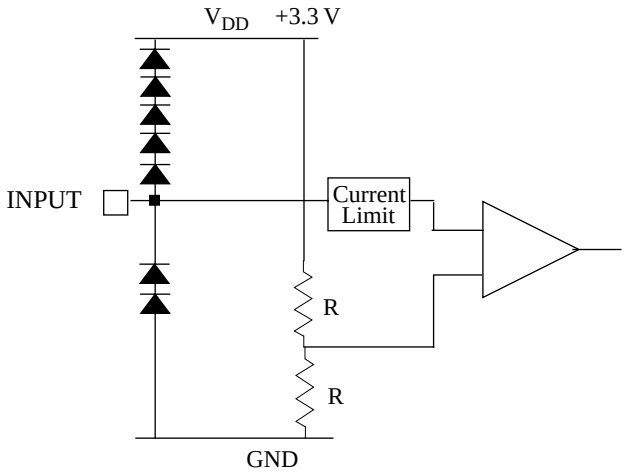
Input Structures

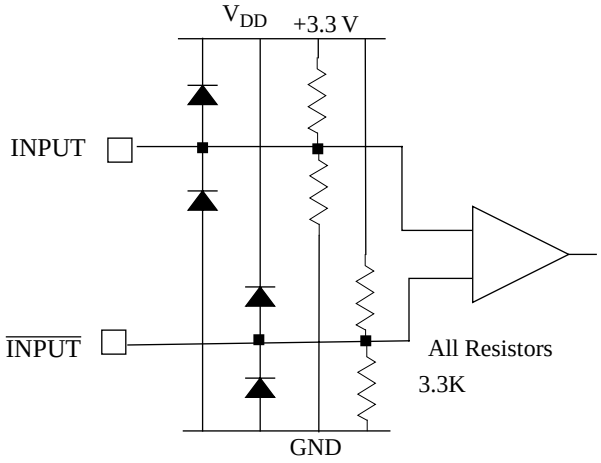
Two input structures exists in this part; TTL and High Speed, Differential Inputs. The TTL Inputs will interface with any TTL or 3.3V or 5V CMOS outputs. The High Speed, Differential Inputs are intended to be AC Coupled per the FC-PH specification. Being AC Coupled, the High Speed, Differential Input buffers are biased at $V_{DD}/2$. Refer to Figure 2 for High Speed, Differential Input structure.

Figure 2: Input Structures



REFCLK and TTL Inputs

A

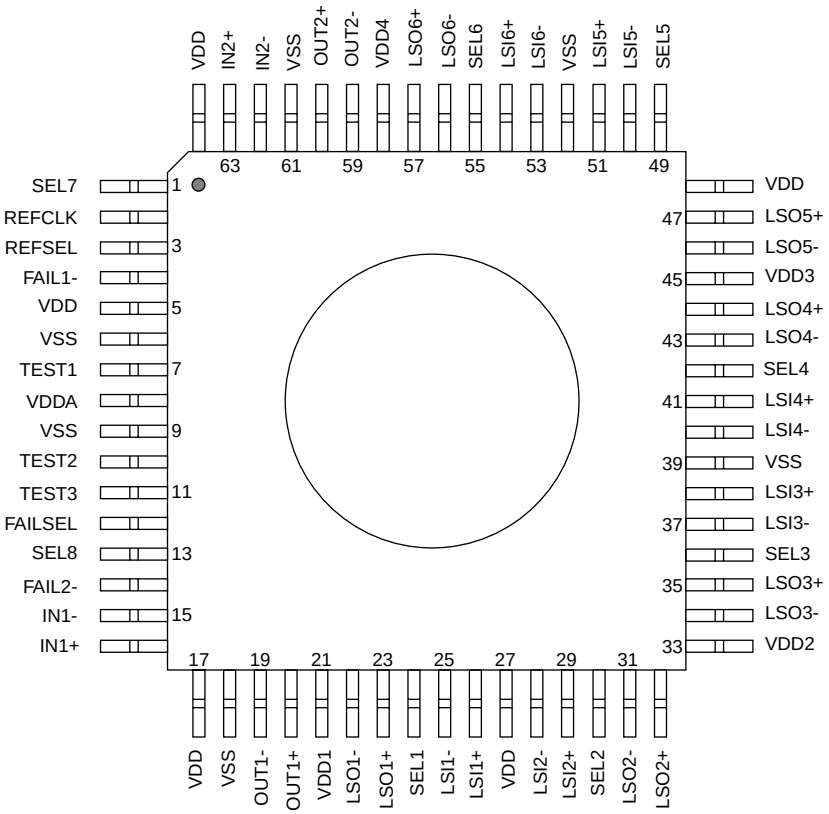


High Speed Differential Input (RX+/RX-)

B

Package Pin Descriptions

Figure 3: Pin Diagram



(Top View)

NOTE: Heatsink is not internally connected electrically.
It should not be connected electrically by the user.

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Table 2: Pin Description

Pin #	*Name*	*Description*
16, 15 63, 62	IN1+, IN1- IN2+, IN2-	INPUT - Differential. Serial input to CRU1/CRU2 (AC Coupling recommended) (Biased internally at $V_{DD}/2$).
20, 19 60, 59	OUT1+, OUT1- OUT2+, OUT2-	OUTPUT - Differential. Serial output from MUX7/PBC6 (AC Coupling recommended).
26, 25 29, 28 38, 37 41, 40 51, 50 54, 53	LSI1+, LSI1- LSI2+, LSI2- LSI3+, LSI3- LSI4+, LSI4- LSI5+, LSI5- LSI6+, LSI6-	INPUT - Differential. Serial input from disk drive 'x' to PBCx (AC Coupling recommended) (Biased internally at $V_{DD}/2$).
23, 22 32, 31 35, 34 44, 43 47, 46 57, 56	LSO1+, LSO1- LSO2+, LSO2- LSO3+, LSO3- LSO4+, LSO4- LSO5+, LSO5- LSO6+, LSO6-	OUTPUT - Differential. Serial output from PBCx to disk drive 'x' (AC Coupling recommended).
24, 30 36, 42 49, 55 1, 13	SEL1, SEL2 SEL3, SEL4 SEL5, SEL6 SEL7, SEL8	INPUT - TTL. A LOW bypasses the disk drive input and passes the output from the previous PBC to the output of PBCx. A HIGH selects the disk drive input (LSIx) as the output of the PBC. SEL7 configures MUX7. SEL8 configures MUX8.
2	REFCLK	INPUT - TTL.. REFerence CLocK at 1/10th or 1/20th the baud rate (Nominally 53.125 or 106.25 MHz) as determined by RFSEL. Used for internal clock multiplier unit.
3	RFSEL	INPUT - TTL. ReFclk SELect. When HIGH, REFCLK is 1/10th the baud rate and would normally be 106.25 MHz. When LOW, REFCLK is 1/20th the baud rate (53.125 MHz)
4, 14	FAIL1- FAIL2-	OUTPUT - TTL. When LOW, indicates that the output of CRU1/2 does not contain valid Fibre Channel data.
12	FAILSEL	INPUT - TTL. Selects the algorithm to drive the FAIL1-/FAIL2- outputs. When HIGH, the "Multiple Frame Error Mode" is used. When LOW, the "Single Frame Error Mode" is selected.
7, 10, 11	TEST1 TEST2 TEST3	INPUT - TTL. LOW for factory test, HIGH for normal operation.
5, 17, 27, 48, 64	VDD	Power Supply. 3.3V Supply.
21, 33, 45, 58	VDD1, VDD2, VDD3, VDD4	High-Speed Output Power Supply. 3.3V Supply for PECL drivers. VDD1 powers OUT1 and LSO1, VDD2 powers LSO2 and LSO3, VDD3 powers LSO4 and LSO5, VDD4 powers LSO6 and OUT2. If the pair of outputs are not used, VDDx may be grounded to conserve power.
8	VDDA	Analog Power Supply. 3.3V for Clock Multiplier PLL.
6, 9, 18, 39, 52, 61	VSS	Ground.

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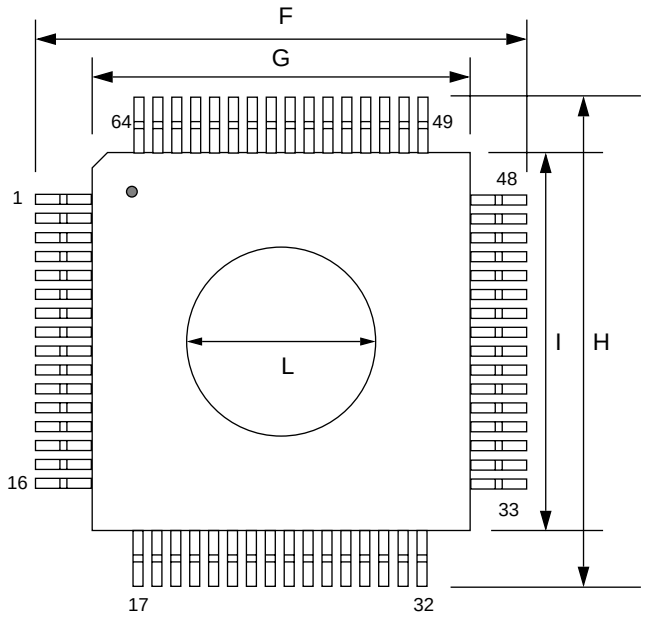
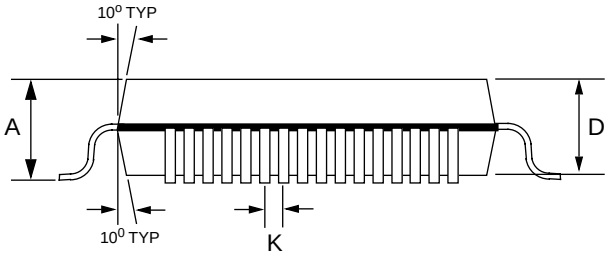
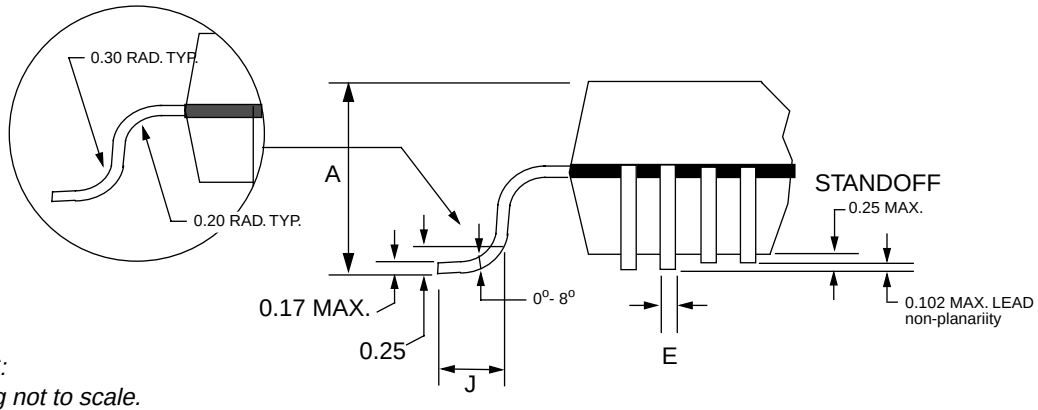
Package Information

64 Pin PQFP Package Drawings



Item	14 mm	Tol.
A	2.45	MAX
D	2.00	+0.10
E	0.35	±0.05
F	17.20	±0.25
G	14.00	±0.10
H	17.20	±0.25
I	14.00	±0.10
J	0.80	±0.15
K	0.80	BASIC
L	N/A	±0.50 DIA.





NOTES:
Drawing not to scale.
All units in mm unless otherwise noted.
Heat spreader is not electrically connected.

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Package Thermal Characteristics

The VSC7128 is packaged into a thermally enhanced plastic quad flatpack with an exposed heat spreader. This package adheres to industry standard EIAJ footprints for a 14x14mm body, 64 lead PQFP. The package construction and thermal properties are shown below.

The user must ensure that the maximum case temperature specification (90° C) is not violated. Given the thermal resistance of the package in still air, the user may operate the VSC7128 in still air if the ambient temperature does not exceed 32° C (90° C - 1.7W ° C * 35 °C/W = 32° C). If operation above this ambient temperature is required, an appropriate heatsink must be used with the part or adequate airflow must be provided. The thermal resistances given above are for a PCB which is not thermally saturated since significant amounts of heat can transfer through the leadframe and into the PCB.

Figure 4: Package Cross Reference

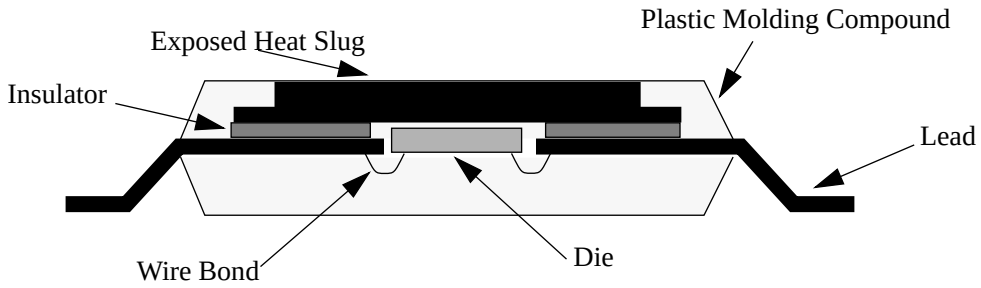


Table 3: Thermal Resistance

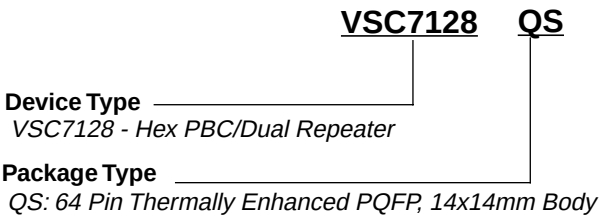
Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	2.5	°C/W
θ_{ca-0}	Thermal resistance from case to ambient, still air	35	°C/W
θ_{ca-100}	Thermal resistance from case to ambient, 100 LFPM air	29	°C/W
θ_{ca-200}	Thermal resistance from case to ambient, 200 LFPM air	26	°C/W
θ_{ca-400}	Thermal resistance from case to ambient, 400 LFPM air	22	°C/W
θ_{ca-600}	Thermal resistance from case to ambient, 600 LFPM air	19	°C/W

Moisture Sensitivity Level

This device is rated with a moisture sensitivity level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

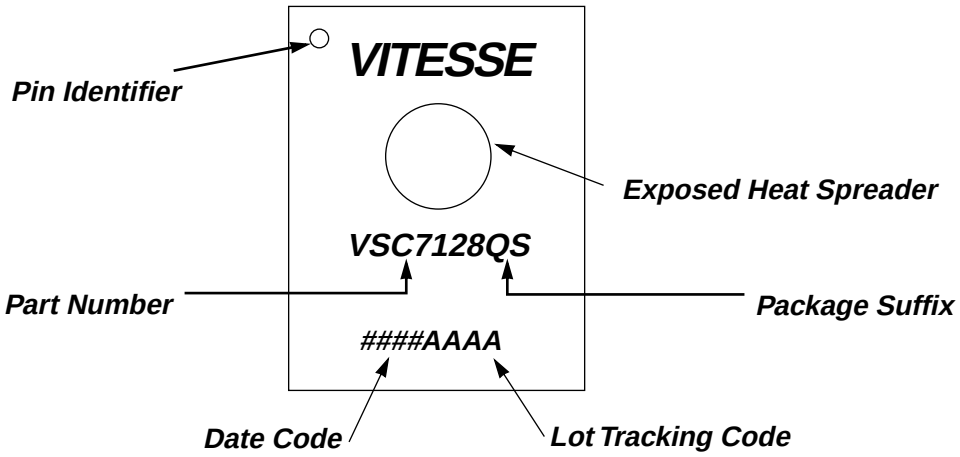
Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Marking Information

The package is marked with three lines of text as shown below (QS Package):



Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

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