NEC

MOS INTEGRATED CIRCUIT

μPD161623

528 OUTPUT TFT-LCD SOURCE DRIVER WITH RAM

DESCRIPTION

The μPD161623 is a TFT-LCD source driver that includes display RAM.

This driver has 528 outputs, a display RAM capacity of 760,320 bits (176 pixels x 18 bits x 240 lines) and, can provide a 262,144-color display.

FEATURES

- TFT-LCD driver with on-chip display RAM
- I/O circuit power supply voltage: 1.7 to 3.6 V
- Logic power supply voltage: 2.5 to 3.6 V
- Driver power supply voltage: 4.3 to 5.5 V
- Display RAM: 176 x 18 x 240 bits
- Driver outputs: 528 output
- CPU interface: Serial, 18-bit/16-bit parallel interface selectable
- Colors: 262,144 colors/pixel
- On-chip VCOM generator
- On-chip timing generator
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD161623P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum on product quality, so please contact one of our sales representatives.

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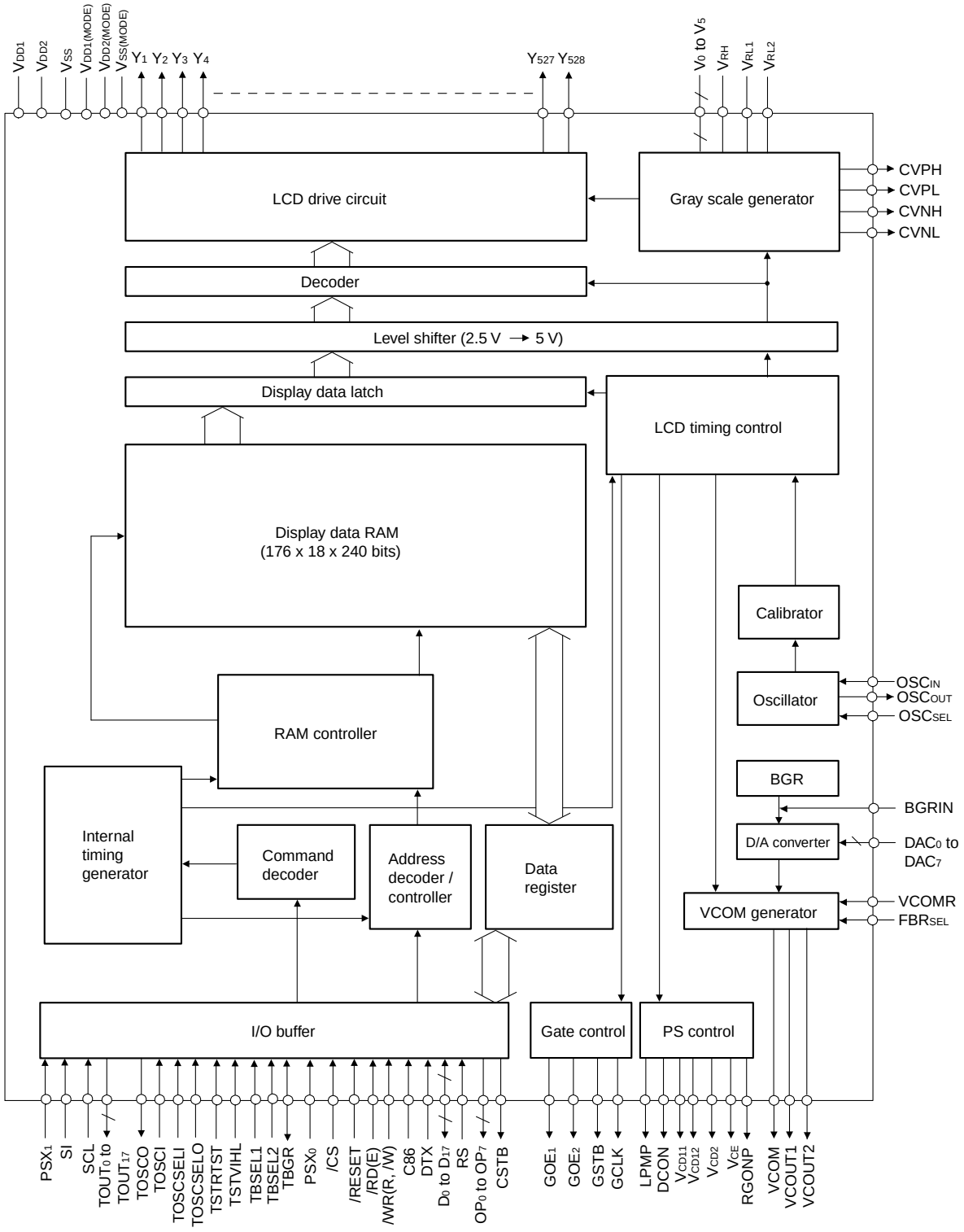
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (PAD LAYOUT)

Chip size: 3.75 x 23.00 mm^2 TYP.

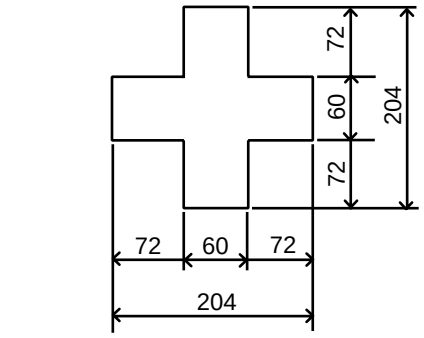
Bump size (output): 35 x 94 μm^2 TYP.

Bump size (input & dummy): 80 x 86 μm^2 TYP.

Alignment mark (Mark center, unit: μm)

	X	Y
M1	−1690	11315
M2	−1690	−11315

Alignment mark reference (unit: μm)



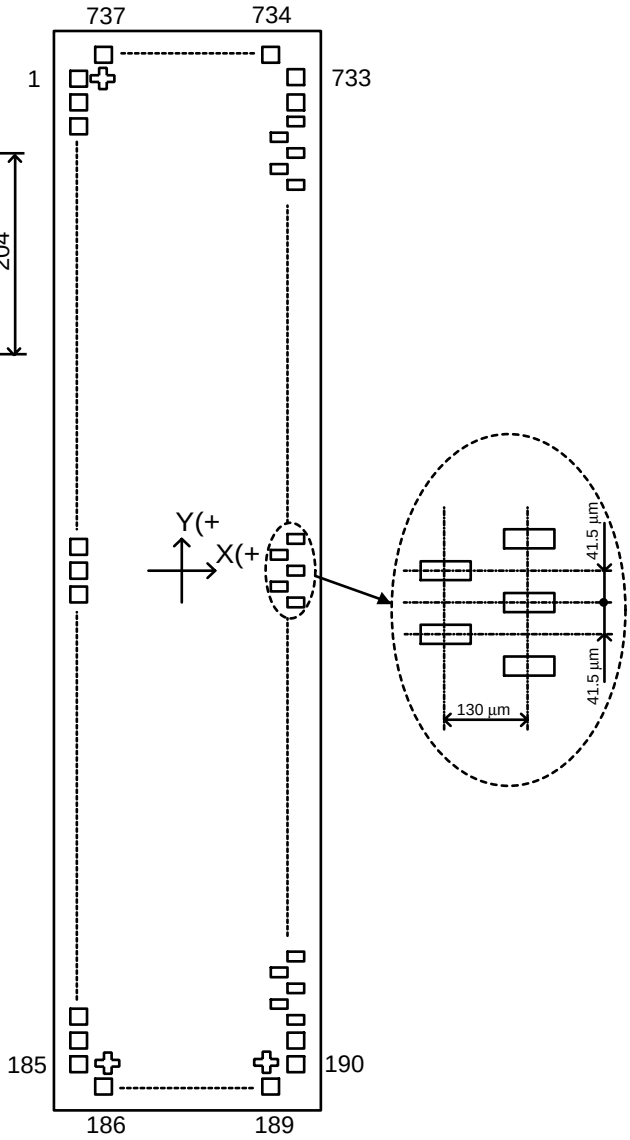


Table 2–1. Pad Layout (1/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Pad Layout [μm] Y
1	DUMMY	B	-1749.00	11000.00
2	DUMMY	B	-1749.00	10880.00
3	DUMMY	B	-1749.00	10760.00
4	DUMMY	B	-1749.00	10640.00
5	DUMMY	B	-1749.00	10520.00
6	DUMMY	B	-1749.00	10400.00
7	DUMMY	B	-1749.00	10280.00
8	DUMMY	B	-1749.00	10160.00
9	DUMMY	B	-1749.00	10040.00
10	DUMMY	B	-1749.00	9920.00
11	DUMMY	B	-1749.00	9800.00
12	DUMMY	B	-1749.00	9680.00
13	DUMMY	B	-1749.00	9560.00
14	DUMMY	B	-1749.00	9440.00
15	DUMMY	B	-1749.00	9320.00
16	DUMMY	B	-1749.00	9200.00
17	TOUT17	B	-1749.00	9080.00
18	TOUT16	B	-1749.00	8960.00
19	TOUT15	B	-1749.00	8840.00
20	TOUT14	B	-1749.00	8720.00
21	TOUT13	B	-1749.00	8600.00
22	TOUT12	B	-1749.00	8480.00
23	TOUT11	B	-1749.00	8360.00
24	TOUT10	B	-1749.00	8240.00
25	TOUT9	B	-1749.00	8120.00
26	TOUT8	B	-1749.00	8000.00
27	TOUT7	B	-1749.00	7880.00
28	TOUT6	B	-1749.00	7760.00
29	TOUT5	B	-1749.00	7640.00
30	TOUT4	B	-1749.00	7520.00
31	TOUT3	B	-1749.00	7400.00
32	TOUT2	B	-1749.00	7280.00
33	TOUT1	B	-1749.00	7160.00
34	TOUT0	B	-1749.00	7040.00
35	VSS(MODE)	B	-1749.00	6920.00
36	TSTVIHL	B	-1749.00	6800.00
37	TSTRTST	B	-1749.00	6680.00
38	TOSCSELO	B	-1749.00	6560.00
39	TOSCSELI	B	-1749.00	6440.00
40	TOSCI	B	-1749.00	6320.00
41	TOSCO	B	-1749.00	6200.00
42	VDD2(MODE)	B	-1749.00	6080.00
43	OSCSEL	B	-1749.00	5960.00
44	VSS(MODE)	B	-1749.00	5840.00
45	OSCOUT	B	-1749.00	5720.00
46	VSS(MODE)	B	-1749.00	5600.00
47	OSCIN	B	-1749.00	5480.00
48	VSS(MODE)	B	-1749.00	5360.00
49	CSTB	B	-1749.00	5240.00
50	D17	B	-1749.00	5120.00
51	D16	B	-1749.00	5000.00
52	D15	B	-1749.00	4880.00
53	D14	B	-1749.00	4760.00
54	D13	B	-1749.00	4640.00
55	D12	B	-1749.00	4520.00
56	D11	B	-1749.00	4400.00
57	D10	B	-1749.00	4280.00
58	D9	B	-1749.00	4160.00
59	D8	B	-1749.00	4040.00
60	D7	B	-1749.00	3920.00
61	D6	B	-1749.00	3800.00
62	D5	B	-1749.00	3680.00
63	D4	B	-1749.00	3560.00
64	D3	B	-1749.00	3440.00
65	D2	B	-1749.00	3320.00
66	D1	B	-1749.00	3200.00
67	D0	B	-1749.00	3080.00
68	VSS(MODE)	B	-1749.00	2960.00
69	/CS	B	-1749.00	2840.00
70	/RESET	B	-1749.00	2720.00
71	RS	B	-1749.00	2600.00
72	/WR (R, /W)	B	-1749.00	2480.00
73	/RD (E)	B	-1749.00	2360.00
74	VSS(MODE)	B	-1749.00	2240.00
75	SI	B	-1749.00	2120.00
76	SCL	B	-1749.00	2000.00
77	VDD1	B	-1749.00	1880.00
78	PSX1	B	-1749.00	1760.00
79	VSS(MODE)	B	-1749.00	1640.00
80	PSX0	B	-1749.00	1520.00
81	VDD1(MODE)	B	-1749.00	1400.00
82	C86	B	-1749.00	1280.00
83	VSS(MODE)	B	-1749.00	1160.00
84	DTX	B	-1749.00	1040.00
85	VDD1(MODE)	B	-1749.00	920.00
86	VCE	B	-1749.00	800.00
87	VCD2	B	-1749.00	680.00
88	VCD12	B	-1749.00	560.00
89	VCD11	B	-1749.00	440.00
90	LPMP	B	-1749.00	320.00
91	RGONP	B	-1749.00	200.00
92	DCON	B	-1749.00	80.00
93	VCOUT2	B	-1749.00	-40.00
94	VSS	B	-1749.00	-160.00
95	VDD1	B	-1749.00	-280.00
96	VDD2	B	-1749.00	-400.00
97	VSS	B	-1749.00	-520.00
98	VSS	B	-1749.00	-640.00
99	CVNL	B	-1749.00	-760.00
100	CVNH	B	-1749.00	-880.00
101	CVPL	B	-1749.00	-1000.00
102	CVPH	B	-1749.00	-1120.00
103	VS	B	-1749.00	-1240.00
104	VS	B	-1749.00	-1360.00
105	VSS	B	-1749.00	-1480.00
106	VCOUT1	B	-1749.00	-1600.00
107	VCOUT1	B	-1749.00	-1720.00
108	VDD2	B	-1749.00	-1840.00
109	VDD2	B	-1749.00	-1960.00
110	VCOM	B	-1749.00	-2080.00
111	DUMMY	B	-1749.00	-2200.00
112	DUMMY	B	-1749.00	-2320.00
113	VSS(MODE)	B	-1749.00	-2440.00
114	VCOMR	B	-1749.00	-2560.00
115	BGRIN	B	-1749.00	-2680.00
116	VDD2(MODE)	B	-1749.00	-2800.00
117	FBRSEL	B	-1749.00	-2920.00
118	VSS(MODE)	B	-1749.00	-3040.00
119	VRH	B	-1749.00	-3160.00
120	V0	B	-1749.00	-3280.00
121	V1	B	-1749.00	-3400.00
122	V2	B	-1749.00	-3520.00
123	V3	B	-1749.00	-3640.00
124	V4	B	-1749.00	-3760.00
125	V5	B	-1749.00	-3880.00
126	VRL1	B	-1749.00	-4000.00
127	VRL2	B	-1749.00	-4120.00
128	VSS(MODE)	B	-1749.00	-4240.00
129	TBSEL1	B	-1749.00	-4360.00
130	TBSEL2	B	-1749.00	-4480.00
131	TBGR	B	-1749.00	-4600.00
132	DAC7	B	-1749.00	-4720.00
133	DAC6	B	-1749.00	-4840.00
134	DAC5	B	-1749.00	-4960.00
135	DAC4	B	-1749.00	-5080.00
136	DAC3	B	-1749.00	-5200.00
137	DAC2	B	-1749.00	-5320.00
138	DAC1	B	-1749.00	-5440.00
139	DAC0	B	-1749.00	-5560.00
140	VSS(MODE)	B	-1749.00	-5680.00
141	OP0	B	-1749.00	-5800.00
142	OP1	B	-1749.00	-5920.00
143	OP2	B	-1749.00	-6040.00
144	OP3	B	-1749.00	-6160.00
145	OP4	B	-1749.00	-6280.00
146	OP5	B	-1749.00	-6400.00
147	OP6	B	-1749.00	-6520.00
148	OP7	B	-1749.00	-6640.00
149	GSTB	B	-1749.00	-6760.00
150	GCLK	B	-1749.00	-6880.00
151	GOE1	B	-1749.00	-7000.00
152	GOE2	B	-1749.00	-7120.00
153	DUMMY	B	-1749.00	-7240.00
154	DUMMY	B	-1749.00	-7360.00
155	DUMMY	B	-1749.00	-7480.00
156	DUMMY	B	-1749.00	-7600.00
157	DUMMY	B	-1749.00	-7720.00
158	DUMMY	B	-1749.00	-7840.00
159	DUMMY	B	-1749.00	-7960.00
160	DUMMY	B	-1749.00	-8080.00
161	DUMMY	B	-1749.00	-8200.00
162	DUMMY	B	-1749.00	-8320.00
163	DUMMY	B	-1749.00	-8440.00
164	DUMMY	B	-1749.00	-8560.00
165	DUMMY	B	-1749.00	-8680.00
166	DUMMY	B	-1749.00	-8800.00
167	DUMMY	B	-1749.00	-8920.00
168	DUMMY	B	-1749.00	-9040.00
169	DUMMY	B	-1749.00	-9160.00
170	DUMMY	B	-1749.00	-9280.00
171	DUMMY	B	-1749.00	-9400.00
172	DUMMY	B	-1749.00	-9520.00
173	DUMMY	B	-1749.00	-9640.00
174	DUMMY	B	-1749.00	-9760.00
175	DUMMY	B	-1749.00	-9880.00
176	DUMMY	B	-1749.00	-10000.00
177	DUMMY	B	-1749.00	-10120.00
178	DUMMY	B	-1749.00	-10240.00
179	DUMMY	B	-1749.00	-10360.00
180	DUMMY	B	-1749.00	-10480.00
181	DUMMY	B	-1749.00	-10600.00
182	DUMMY	B	-1749.00	-10720.00
183	DUMMY	B	-1749.00	-10840.00
184	DUMMY	B	-1749.00	-10960.00
185	DUMMY	B	-1749.00	-11080.00
186	DUMMY	B	-1350.00	-11374.00
187	DUMMY	B	-450.00	-11374.00
188	DUMMY	B	450.00	-11374.00
189	DUMMY	B	1350.00	-11374.00
190	DUMMY	A	1745.00	-11302.50
191	DUMMY	A	1745.00	-11252.50
192	DUMMY	A	1745.00	-11201.50
193	Y528	A	1745.00	-11140.50
194	Y527	A	1615.00	-11099.00
195	Y526	A	1745.00	-11057.50
196	Y525	A	1615.00	-11016.00
197	Y524	A	1745.00	-10974.50
198	Y523	A	1615.00	-10933.00
199	Y522	A	1745.00	-10891.50
200	Y521	A	1615.00	-10850.00
201	Y520	A	1745.00	-10808.50
202	Y519	A	1615.00	-10767.00
203	Y518	A	1745.00	-10725.50
204	Y517	A	1615.00	-10684.00
205	Y516	A	1745.00	-10642.50
206	Y515	A	1615.00	-10601.00
207	Y514	A	1745.00	-10559.50
208	Y513	A	1615.00	-10518.00
209	Y512	A	1745.00	-10476.50
210	Y511	A	1615.00	-10435.00

Table 2–1. Pad Layout (2/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Y
211	Y510	A	1745.00	-10393.50
212	Y509	A	1615.00	-10352.00
213	Y508	A	1745.00	-10310.50
214	Y507	A	1615.00	-10269.00
215	Y506	A	1745.00	-10227.50
216	Y505	A	1615.00	-10186.00
217	Y504	A	1745.00	-10144.50
218	Y503	A	1615.00	-10103.00
219	Y502	A	1745.00	-10061.50
220	Y501	A	1615.00	-10020.00
221	Y500	A	1745.00	-9978.50
222	Y499	A	1615.00	-9937.00
223	Y498	A	1745.00	-9895.50
224	Y497	A	1615.00	-9854.00
225	Y496	A	1745.00	-9812.50
226	Y495	A	1615.00	-9771.00
227	Y494	A	1745.00	-9729.50
228	Y493	A	1615.00	-9688.00
229	Y492	A	1745.00	-9646.50
230	Y491	A	1615.00	-9605.00
231	Y490	A	1745.00	-9563.50
232	Y489	A	1615.00	-9522.00
233	Y488	A	1745.00	-9480.50
234	Y487	A	1615.00	-9439.00
235	Y486	A	1745.00	-9397.50
236	Y485	A	1615.00	-9356.00
237	Y484	A	1745.00	-9314.50
238	Y483	A	1615.00	-9273.00
239	Y482	A	1745.00	-9231.50
240	Y481	A	1615.00	-9190.00
241	Y480	A	1745.00	-9148.50
242	Y479	A	1615.00	-9107.00
243	Y478	A	1745.00	-9065.50
244	Y477	A	1615.00	-9024.00
245	Y476	A	1745.00	-8982.50
246	Y475	A	1615.00	-8941.00
247	Y474	A	1745.00	-8899.50
248	Y473	A	1615.00	-8858.00
249	Y472	A	1745.00	-8816.50
250	Y471	A	1615.00	-8775.00
251	Y470	A	1745.00	-8733.50
252	Y469	A	1615.00	-8692.00
253	Y468	A	1745.00	-8650.50
254	Y467	A	1615.00	-8609.00
255	Y466	A	1745.00	-8567.50
256	Y465	A	1615.00	-8526.00
257	Y464	A	1745.00	-8484.50
258	Y463	A	1615.00	-8443.00
259	Y462	A	1745.00	-8401.50
260	Y461	A	1615.00	-8360.00
261	Y460	A	1745.00	-8318.50
262	Y459	A	1615.00	-8277.00
263	Y458	A	1745.00	-8235.50
264	Y457	A	1615.00	-8194.00
265	Y456	A	1745.00	-8152.50
266	Y455	A	1615.00	-8111.00
267	Y454	A	1745.00	-8069.50
268	Y453	A	1615.00	-8028.00
269	Y452	A	1745.00	-7986.50
270	Y451	A	1615.00	-7945.00
271	Y450	A	1745.00	-7903.50
272	Y449	A	1615.00	-7862.00
273	Y448	A	1745.00	-7820.50
274	Y447	A	1615.00	-7779.00
275	Y446	A	1745.00	-7737.50
276	Y445	A	1615.00	-7696.00
277	Y444	A	1745.00	-7654.50
278	Y443	A	1615.00	-7613.00
279	Y442	A	1745.00	-7571.50
280	Y441	A	1615.00	-7530.00
281	Y440	A	1745.00	-7488.50
282	Y439	A	1615.00	-7447.00
283	Y438	A	1745.00	-7405.50
284	Y437	A	1615.00	-7364.00
285	Y436	A	1745.00	-7322.50
286	Y435	A	1615.00	-7281.00
287	Y434	A	1745.00	-7239.50
288	Y433	A	1615.00	-7198.00
289	Y432	A	1745.00	-7156.50
290	Y431	A	1615.00	-7115.00
291	Y430	A	1745.00	-7073.50
292	Y429	A	1615.00	-7032.00
293	Y428	A	1745.00	-6990.50
294	Y427	A	1615.00	-6949.00
295	Y426	A	1745.00	-6907.50
296	Y425	A	1615.00	-6866.00
297	Y424	A	1745.00	-6824.50
298	Y423	A	1615.00	-6783.00
299	Y422	A	1745.00	-6741.50
300	Y421	A	1615.00	-6700.00
301	Y420	A	1745.00	-6658.50
302	Y419	A	1615.00	-6617.00
303	Y418	A	1745.00	-6575.50
304	Y417	A	1615.00	-6534.00
305	Y416	A	1745.00	-6492.50
306	Y415	A	1615.00	-6451.00
307	Y414	A	1745.00	-6409.50
308	Y413	A	1615.00	-6368.00
309	Y412	A	1745.00	-6326.50
310	Y411	A	1615.00	-6285.00
311	Y410	A	1745.00	-6243.50
312	Y409	A	1615.00	-6202.00
313	Y408	A	1745.00	-6160.50
314	Y407	A	1615.00	-6119.00
315	Y406	A	1745.00	-6077.50
316	Y405	A	1615.00	-6036.00
317	Y404	A	1745.00	-5994.50
318	Y403	A	1615.00	-5953.00
319	Y402	A	1745.00	-5911.50
320	Y401	A	1615.00	-5870.00
321	Y400	A	1745.00	-5828.50
322	Y399	A	1615.00	-5787.00
323	Y398	A	1745.00	-5745.50
324	Y397	A	1615.00	-5704.00
325	Y396	A	1745.00	-5662.50
326	Y395	A	1615.00	-5621.00
327	Y394	A	1745.00	-5579.50
328	Y393	A	1615.00	-5538.00
329	Y392	A	1745.00	-5496.50
330	Y391	A	1615.00	-5455.00
331	Y390	A	1745.00	-5413.50
332	Y389	A	1615.00	-5372.00
333	Y388	A	1745.00	-5330.50
334	Y387	A	1615.00	-5289.00
335	Y386	A	1745.00	-5247.50
336	Y385	A	1615.00	-5206.00
337	Y384	A	1745.00	-5164.50
338	Y383	A	1615.00	-5123.00
339	Y382	A	1745.00	-5081.50
340	Y381	A	1615.00	-5040.00
341	Y380	A	1745.00	-4998.50
342	Y379	A	1615.00	-4957.00
343	Y378	A	1745.00	-4915.50
344	Y377	A	1615.00	-4874.00
345	Y376	A	1745.00	-4832.50
346	Y375	A	1615.00	-4791.00
347	Y374	A	1745.00	-4749.50
348	Y373	A	1615.00	-4708.00
349	Y372	A	1745.00	-4666.50
350	Y371	A	1615.00	-4625.00
351	Y370	A	1745.00	-4583.50
352	Y369	A	1615.00	-4542.00
353	Y368	A	1745.00	-4500.50
354	Y367	A	1615.00	-4459.00
355	Y366	A	1745.00	-4417.50
356	Y365	A	1615.00	-4376.00
357	Y364	A	1745.00	-4334.50
358	Y363	A	1615.00	-4293.00
359	Y362	A	1745.00	-4251.50
360	Y361	A	1615.00	-4210.00
361	Y360	A	1745.00	-4168.50
362	Y359	A	1615.00	-4127.00
363	Y358	A	1745.00	-4085.50
364	Y357	A	1615.00	-4044.00
365	Y356	A	1745.00	-4002.50
366	Y355	A	1615.00	-3961.00
367	Y354	A	1745.00	-3919.50
368	Y353	A	1615.00	-3878.00
369	Y352	A	1745.00	-3836.50
370	Y351	A	1615.00	-3795.00
371	Y350	A	1745.00	-3753.50
372	Y349	A	1615.00	-3712.00
373	Y348	A	1745.00	-3670.50
374	Y347	A	1615.00	-3629.00
375	Y346	A	1745.00	-3587.50
376	Y345	A	1615.00	-3546.00
377	Y344	A	1745.00	-3504.50
378	Y343	A	1615.00	-3463.00
379	Y342	A	1745.00	-3421.50
380	Y341	A	1615.00	-3380.00
381	Y340	A	1745.00	-3338.50
382	Y339	A	1615.00	-3297.00
383	Y338	A	1745.00	-3255.50
384	Y337	A	1615.00	-3214.00
385	Y336	A	1745.00	-3172.50
386	Y335	A	1615.00	-3131.00
387	Y334	A	1745.00	-3089.50
388	Y333	A	1615.00	-3048.00
389	Y332	A	1745.00	-3006.50
390	Y331	A	1615.00	-2965.00
391	Y330	A	1745.00	-2923.50
392	Y329	A	1615.00	-2882.00
393	Y328	A	1745.00	-2840.50
394	Y327	A	1615.00	-2799.00
395	Y326	A	1745.00	-2757.50
396	Y325	A	1615.00	-2716.00
397	Y324	A	1745.00	-2674.50
398	Y323	A	1615.00	-2633.00
399	Y322	A	1745.00	-2591.50
400	Y321	A	1615.00	-2550.00
401	Y320	A	1745.00	-2508.50
402	Y319	A	1615.00	-2467.00
403	Y318	A	1745.00	-2425.50
404	Y317	A	1615.00	-2384.00
405	Y316	A	1745.00	-2342.50
406	Y315	A	1615.00	-2301.00
407	Y314	A	1745.00	-2259.50
408	Y313	A	1615.00	-2218.00
409	Y312	A	1745.00	-2176.50
410	Y311	A	1615.00	-2135.00
411	Y310	A	1745.00	-2093.50
412	Y309	A	1615.00	-2052.00
413	Y308	A	1745.00	-2010.50
414	Y307	A	1615.00	-1969.00
415	Y306	A	1745.00	-1927.50
416	Y305	A	1615.00	-1886.00
417	Y304	A	1745.00	-1844.50
418	Y303	A	1615.00	-1803.00
419	Y302	A	1745.00	-1761.50
420	Y301	A	1615.00	-1720.00

Table 2–1. Pad Layout (3/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Pad Layout [μm] Y
421	Y300	A	1745.00	-1678.50
422	Y299	A	1615.00	-1637.00
423	Y298	A	1745.00	-1595.50
424	Y297	A	1615.00	-1554.00
425	Y296	A	1745.00	-1512.50
426	Y295	A	1615.00	-1471.00
427	Y294	A	1745.00	-1429.50
428	Y293	A	1615.00	-1388.00
429	Y292	A	1745.00	-1346.50
430	Y291	A	1615.00	-1305.00
431	Y290	A	1745.00	-1263.50
432	Y289	A	1615.00	-1222.00
433	Y288	A	1745.00	-1180.50
434	Y287	A	1615.00	-1139.00
435	Y286	A	1745.00	-1097.50
436	Y285	A	1615.00	-1056.00
437	Y284	A	1745.00	-1014.50
438	Y283	A	1615.00	-973.00
439	Y282	A	1745.00	-931.50
440	Y281	A	1615.00	-890.00
441	Y280	A	1745.00	-848.50
442	Y279	A	1615.00	-807.00
443	Y278	A	1745.00	-765.50
444	Y277	A	1615.00	-724.00
445	Y276	A	1745.00	-682.50
446	Y275	A	1615.00	-641.00
447	Y274	A	1745.00	-599.50
448	Y273	A	1615.00	-558.00
449	Y272	A	1745.00	-516.50
450	Y271	A	1615.00	-475.00
451	Y270	A	1745.00	-433.50
452	Y269	A	1615.00	-392.00
453	Y268	A	1745.00	-350.50
454	Y267	A	1615.00	-309.00
455	Y266	A	1745.00	-267.50
456	Y265	A	1615.00	-226.00
457	Y264	A	1745.00	-184.50
458	DUMMY	A	1615.00	-143.00
459	DUMMY	A	1745.00	-101.50
460	DUMMY	A	1615.00	-60.00
461	DUMMY	A	1745.00	-18.50
462	DUMMY	A	1615.00	23.00
463	DUMMY	A	1745.00	64.50
464	DUMMY	A	1615.00	106.00
465	DUMMY	A	1745.00	147.50
466	DUMMY	A	1615.00	189.00
467	DUMMY	A	1745.00	230.50
468	Y263	A	1615.00	272.00
469	Y262	A	1745.00	313.50
470	Y261	A	1615.00	355.00
471	Y260	A	1745.00	396.50
472	Y259	A	1615.00	438.00
473	Y258	A	1745.00	479.50
474	Y257	A	1615.00	521.00
475	Y256	A	1745.00	562.50
476	Y255	A	1615.00	604.00
477	Y254	A	1745.00	645.50
478	Y253	A	1615.00	687.00
479	Y252	A	1745.00	728.50
480	Y251	A	1615.00	770.00
481	Y250	A	1745.00	811.50
482	Y249	A	1615.00	853.00
483	Y248	A	1745.00	894.50
484	Y247	A	1615.00	936.00
485	Y246	A	1745.00	977.50
486	Y245	A	1615.00	1019.00
487	Y244	A	1745.00	1060.50
488	Y243	A	1615.00	1102.00
489	Y242	A	1745.00	1143.50
490	Y241	A	1615.00	1185.00
491	Y240	A	1745.00	1226.50
492	Y239	A	1615.00	1268.00
493	Y238	A	1745.00	1309.50
494	Y237	A	1615.00	1351.00
495	Y236	A	1745.00	1392.50
496	Y235	A	1615.00	1434.00
497	Y234	A	1745.00	1475.50
498	Y233	A	1615.00	1517.00
499	Y232	A	1745.00	1558.50
500	Y231	A	1615.00	1600.00
501	Y230	A	1745.00	1641.50
502	Y229	A	1615.00	1683.00
503	Y228	A	1745.00	1724.50
504	Y227	A	1615.00	1766.00
505	Y226	A	1745.00	1807.50
506	Y225	A	1615.00	1849.00
507	Y224	A	1745.00	1890.50
508	Y223	A	1615.00	1932.00
509	Y222	A	1745.00	1973.50
510	Y221	A	1615.00	2015.00
511	Y220	A	1745.00	2056.50
512	Y219	A	1615.00	2098.00
513	Y218	A	1745.00	2139.50
514	Y217	A	1615.00	2181.00
515	Y216	A	1745.00	2222.50
516	Y215	A	1615.00	2264.00
517	Y214	A	1745.00	2305.50
518	Y213	A	1615.00	2347.00
519	Y212	A	1745.00	2388.50
520	Y211	A	1615.00	2430.00
521	Y210	A	1745.00	2471.50
522	Y209	A	1615.00	2513.00
523	Y208	A	1745.00	2554.50
524	Y207	A	1615.00	2596.00
525	Y206	A	1745.00	2637.50
526	Y205	A	1615.00	2679.00
527	Y204	A	1745.00	2720.50
528	Y203	A	1615.00	2762.00
529	Y202	A	1745.00	2803.50
530	Y201	A	1615.00	2845.00
531	Y200	A	1745.00	2886.50
532	Y199	A	1615.00	2928.00
533	Y198	A	1745.00	2969.50
534	Y197	A	1615.00	3011.00
535	Y196	A	1745.00	3052.50
536	Y195	A	1615.00	3094.00
537	Y194	A	1745.00	3135.50
538	Y193	A	1615.00	3177.00
539	Y192	A	1745.00	3218.50
540	Y191	A	1615.00	3260.00
541	Y190	A	1745.00	3301.50
542	Y189	A	1615.00	3343.00
543	Y188	A	1745.00	3384.50
544	Y187	A	1615.00	3426.00
545	Y186	A	1745.00	3467.50
546	Y185	A	1615.00	3509.00
547	Y184	A	1745.00	3550.50
548	Y183	A	1615.00	3592.00
549	Y182	A	1745.00	3633.50
550	Y181	A	1615.00	3675.00
551	Y180	A	1745.00	3716.50
552	Y179	A	1615.00	3758.00
553	Y178	A	1745.00	3799.50
554	Y177	A	1615.00	3841.00
555	Y176	A	1745.00	3882.50
556	Y175	A	1615.00	3924.00
557	Y174	A	1745.00	3965.50
558	Y173	A	1615.00	4007.00
559	Y172	A	1745.00	4048.50
560	Y171	A	1615.00	4090.00
561	Y170	A	1745.00	4131.50
562	Y169	A	1615.00	4173.00
563	Y168	A	1745.00	4214.50
564	Y167	A	1615.00	4256.00
565	Y166	A	1745.00	4297.50
566	Y165	A	1615.00	4339.00
567	Y164	A	1745.00	4380.50
568	Y163	A	1615.00	4422.00
569	Y162	A	1745.00	4463.50
570	Y161	A	1615.00	4505.00
571	Y160	A	1745.00	4546.50
572	Y159	A	1615.00	4588.00
573	Y158	A	1745.00	4629.50
574	Y157	A	1615.00	4671.00
575	Y156	A	1745.00	4712.50
576	Y155	A	1615.00	4754.00
577	Y154	A	1745.00	4795.50
578	Y153	A	1615.00	4837.00
579	Y152	A	1745.00	4878.50
580	Y151	A	1615.00	4920.00
581	Y150	A	1745.00	4961.50
582	Y149	A	1615.00	5003.00
583	Y148	A	1745.00	5044.50
584	Y147	A	1615.00	5086.00
585	Y146	A	1745.00	5127.50
586	Y145	A	1615.00	5169.00
587	Y144	A	1745.00	5210.50
588	Y143	A	1615.00	5252.00
589	Y142	A	1745.00	5293.50
590	Y141	A	1615.00	5335.00
591	Y140	A	1745.00	5376.50
592	Y139	A	1615.00	5418.00
593	Y138	A	1745.00	5459.50
594	Y137	A	1615.00	5501.00
595	Y136	A	1745.00	5542.50
596	Y135	A	1615.00	5584.00
597	Y134	A	1745.00	5625.50
598	Y133	A	1615.00	5667.00
599	Y132	A	1745.00	5708.50
600	Y131	A	1615.00	5750.00
601	Y130	A	1745.00	5791.50
602	Y129	A	1615.00	5833.00
603	Y128	A	1745.00	5874.50
604	Y127	A	1615.00	5916.00
605	Y126	A	1745.00	5957.50
606	Y125	A	1615.00	5999.00
607	Y124	A	1745.00	6040.50
608	Y123	A	1615.00	6082.00
609	Y122	A	1745.00	6123.50
610	Y121	A	1615.00	6165.00
611	Y120	A	1745.00	6206.50
612	Y119	A	1615.00	6248.00
613	Y118	A	1745.00	6289.50
614	Y117	A	1615.00	6331.00
615	Y116	A	1745.00	6372.50
616	Y115	A	1615.00	6414.00
617	Y114	A	1745.00	6455.50
618	Y113	A	1615.00	6497.00
619	Y112	A	1745.00	6538.50
620	Y111	A	1615.00	6580.00
621	Y110	A	1745.00	6621.50
622	Y109	A	1615.00	6663.00
623	Y108	A	1745.00	6704.50
624	Y107	A	1615.00	6746.00
625	Y106	A	1745.00	6787.50
626	Y105	A	1615.00	6829.00
627	Y104	A	1745.00	6870.50
628	Y103	A	1615.00	6912.00
629	Y102	A	1745.00	6953.50
630	Y101	A	1615.00	6995.00

Table 2–1. Pad Layout (4/4)

Pad No.	Pad Name	Pad Type	Pad Layout [μm] X	Pad Layout [μm] Y
631	Y100	A	1745.00	7036.50
632	Y99	A	1615.00	7078.00
633	Y98	A	1745.00	7119.50
634	Y97	A	1615.00	7161.00
635	Y96	A	1745.00	7202.50
636	Y95	A	1615.00	7244.00
637	Y94	A	1745.00	7285.50
638	Y93	A	1615.00	7327.00
639	Y92	A	1745.00	7368.50
640	Y91	A	1615.00	7410.00
641	Y90	A	1745.00	7451.50
642	Y89	A	1615.00	7493.00
643	Y88	A	1745.00	7534.50
644	Y87	A	1615.00	7576.00
645	Y86	A	1745.00	7617.50
646	Y85	A	1615.00	7659.00
647	Y84	A	1745.00	7700.50
648	Y83	A	1615.00	7742.00
649	Y82	A	1745.00	7783.50
650	Y81	A	1615.00	7825.00
651	Y80	A	1745.00	7866.50
652	Y79	A	1615.00	7908.00
653	Y78	A	1745.00	7949.50
654	Y77	A	1615.00	7991.00
655	Y76	A	1745.00	8032.50
656	Y75	A	1615.00	8074.00
657	Y74	A	1745.00	8115.50
658	Y73	A	1615.00	8157.00
659	Y72	A	1745.00	8198.50
660	Y71	A	1615.00	8240.00
661	Y70	A	1745.00	8281.50
662	Y69	A	1615.00	8323.00
663	Y68	A	1745.00	8364.50
664	Y67	A	1615.00	8406.00
665	Y66	A	1745.00	8447.50
666	Y65	A	1615.00	8489.00
667	Y64	A	1745.00	8530.50
668	Y63	A	1615.00	8572.00
669	Y62	A	1745.00	8613.50
670	Y61	A	1615.00	8655.00
671	Y60	A	1745.00	8696.50
672	Y59	A	1615.00	8738.00
673	Y58	A	1745.00	8779.50
674	Y57	A	1615.00	8821.00
675	Y56	A	1745.00	8862.50
676	Y55	A	1615.00	8904.00
677	Y54	A	1745.00	8945.50
678	Y53	A	1615.00	8987.00
679	Y52	A	1745.00	9028.50
680	Y51	A	1615.00	9070.00
681	Y50	A	1745.00	9111.50
682	Y49	A	1615.00	9153.00
683	Y48	A	1745.00	9194.50
684	Y47	A	1615.00	9236.00
685	Y46	A	1745.00	9277.50
686	Y45	A	1615.00	9319.00
687	Y44	A	1745.00	9360.50
688	Y43	A	1615.00	9402.00
689	Y42	A	1745.00	9443.50
690	Y41	A	1615.00	9485.00
691	Y40	A	1745.00	9526.50
692	Y39	A	1615.00	9568.00
693	Y38	A	1745.00	9609.50
694	Y37	A	1615.00	9651.00
695	Y36	A	1745.00	9692.50
696	Y35	A	1615.00	9734.00
697	Y34	A	1745.00	9775.50
698	Y33	A	1615.00	9817.00
699	Y32	A	1745.00	9858.50
700	Y31	A	1615.00	9900.00
701	Y30	A	1745.00	9941.50
702	Y29	A	1615.00	9983.00
703	Y28	A	1745.00	10024.50
704	Y27	A	1615.00	10066.00
705	Y26	A	1745.00	10107.50
706	Y25	A	1615.00	10149.00
707	Y24	A	1745.00	10190.50
708	Y23	A	1615.00	10232.00
709	Y22	A	1745.00	10273.50
710	Y21	A	1615.00	10315.00
711	Y20	A	1745.00	10356.50
712	Y19	A	1615.00	10398.00
713	Y18	A	1745.00	10439.50
714	Y17	A	1615.00	10481.00
715	Y16	A	1745.00	10522.50
716	Y15	A	1615.00	10564.00
717	Y14	A	1745.00	10605.50
718	Y13	A	1615.00	10647.00
719	Y12	A	1745.00	10688.50
720	Y11	A	1615.00	10730.00
721	Y10	A	1745.00	10771.50
722	Y9	A	1615.00	10813.00
723	Y8	A	1745.00	10854.50
724	Y7	A	1615.00	10896.00
725	Y6	A	1745.00	10937.50
726	Y5	A	1615.00	10979.00
727	Y4	A	1745.00	11020.50
728	Y3	A	1615.00	11062.00
729	Y2	A	1745.00	11103.50
730	Y1	A	1615.00	11145.00
731	DUMMY	A	1745.00	11206.50
732	DUMMY	A	1745.00	11257.50
733	DUMMY	A	1745.00	11307.50
734	DUMMY	B	1340.00	11374.00
735	DUMMY	B	440.00	11374.00
736	DUMMY	B	-460.00	11374.00
737	DUMMY	B	-1360.00	11374.00

3. PIN FUNCTIONS

3.1 Power Supply System Pins

Symbol	Pin Name	Pad No.	I/O	Function
V_{DD1}	Logic power supply	77, 95	–	Power supply pin for logic circuit
V_{DD2}	I/O power supply	96, 108, 109	–	Power supply pin for I/O buffer
V_S	Driver power supply	103, 104	–	Power supply pin for driver circuit
V_{SS}	Ground	94, 97, 98, 105	–	Ground pin for logic and driver circuits
V_0 to V_5 V_{RH} V_{RL1}, V_{RL2}	Power supply for γ-curve correction	120 to 125, 119, 126, 127	–	The μPD161623 includes power supplies and registers for the γ-curve, so if the characteristics of the γ-curve and LCD panel in the μPD161623 match, leave V_0 to V_5, V_{RH}, V_{RL1}, V_{RL2} open. If some kind of correction is required, adjust the γ-curve by connecting registers between the V_0 to V_5, V_{RH}, V_{RL1}, V_{RL2} pins (see **5.9 γ-Curve Correction Power Supply Circuit**).
$V_{DD1 (MODE)}$	Mode setting pull-up power supply	81, 85	–	Pull-up power supply pin for mode setting
$V_{DD2 (MODE)}$	Mode setting pull-down power supply	42, 116	–	Pull-down power supply pin for mode setting
$V_{SS (MODE)}$	Mode setting ground	35, 44, 46, 48, 68, 74, 79, 83, 113, 118, 128, 140	–	Ground pin for mode setting

3.2 Logic System Pins (1/2)

Symbol	Pin Name	Pad No.	I/O	Function
PSX_0	CPU interface selection	80	Input	This pin is used to select the CPU interface mode. PSX_0 = H: 18-bit parallel interface PSX_0 = L: 16-bit parallel interface
/CS	Chip select	69	Input	This pin is used for chip select signals. When /CS = L, the chip is active and can perform data input/output operations including command and data I/O.
/RESET	Reset	70	Input	When /RESET is L, an internal reset is performed. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.
/RD (E)	Read (Enable)	73	Input	When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low. When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations.
/WR (R, /W)	Write (Read/write)	72	Input	When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations. Data is written at the rising edge of this signal. When M68 series parallel data transfer (R, /W) and serial data has been selected, this pin is used to determine the direction of data transfer. L: Write H: Read
C86	Select interface	82	Input	This pin is used to switch between interface modes (i80 series CPU or M68 series CPU). L: Selects i80 series CPU mode H: Selects M68 series CPU mode

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
D_0 to D_{17}	Data bus	67 to 50	I/O	These pins comprise 18-bit bi-directional data. When the chip is not selected, D_0 to D_{17} are in high impedance mode.
RS	Data/command selection	71	Input	When parallel data transfer has been selected, this pin is usually connected to the least significant bit of the standard CPU address bus and is used to distinguish between data from display data and commands. RS = H: Indicates that data from D_0 to D_{17} is display data. RS = L: Indicates that data from D_0 to D_{17} is commands.
DTX	Data major select	84	Input	When parallel data transfer has been selected, this pin is selected data major selection that inputs display data through serial interface. DTX = H: 1-pixel/18-bit mode DTX = L: 1-pixel/16-bit mode
OSC_{SEL}	Oscillation signal selection	43	Input	This pin is for oscillation signal selection. When is used external resistance connected oscillation circuit, this pin sets H. When in used CR internal oscillation circuit, this pin sets L. OSC_{SEL} = H: External resistance connected oscillation circuit select OSC_{SEL} = L: CR internal oscillation circuit select
OSC_{IN}	Oscillation signal	47	Input	This pin is for oscillation signal input. OSC_{SEL} = H: Connect 42 kΩ resistance between OSC_{IN} and OSC_{OUT}. (240 line, in case of NGO = 0) OSC_{SEL} = L: Leave it open.
OSC_{OUT}	Oscillation signal	45	Output	This pin is for oscillation signal input. OSC_{SEL} = H: Connect 42 kΩ resistance between OSC_{IN} and OSC_{OUT}. (240 line, in case of NGO = 0) OSC_{SEL} = L: Leave it open.
CSTB	GSTB logic signal	49	Output	This pin outputs STB signal for gate driver leveled by interface power supply voltage (V_{DD1}). This output signal is reverse signal of GSTB.
OP_0 to OP_7	Output port	141 to 148	Output	This is a general-purpose output port. The status of these pins (H or L) can be write via a command. Leave open when in unused.

3.3 Gate Driver IC Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
GOE_1	OE_1 output for gate driver	151	Output	This pin is an output pin for the low power mode (for the OE_1). Connect to the OE_1 pin of the gate driver. Timing signal for output, refer to **5.4 Display Timing Generator.**
GOE_2	OE_2 output for gate driver	152	Output	This pin is the OE_2 output for the gate driver. Connect to the OE_2 pin of the gate driver. Timing signal for output, refer to **5.4 Display Timing Generator.**
GSTB	STB output for gate driver	149	Output	This pin is the STB output for the gate driver. Connect to the STVR or STVL pin of the gate driver. Timing signal for output, refer to **5.4 Display Timing Generator.**
GCLK	CLK output for gate driver	150	Output	This pin is the CLK output for the gate driver. Connect to the CLK pin of the gate driver.

3.4 Power Supply Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
LPMP	Low power mode signal	90	Output	Low power mode control signal output pin (for power supply IC). This pin connects to LPM pin of power supply IC.
DCON	DC/DC converter control	92	Output	DC/DC converter ON/OFF signal pin for power supply IC. This pin connects DCON pin of power supply IC.
RGONP	Regulator control	91	Output	Regulator ON/OFF control signal pin for power supply IC. This pin connects to RGONP pin of power supply IC.
V_{CD11}, V_{CD12}	V_{DD1} booster selection	89, 88	Output	Control signal to select x4/x5/x6/x7 booster of power supply IC for V_{DD1}. Connect to the V_{CD11} and V_{CD12} pins of the power supply IC.
V_{CD2}	V_{DD2} booster selection	87	Output	Control signal to select x2/x3 booster of power supply IC for V_{DD2}. Connect to the V_{CD2} pin of the power supply IC.
V_{CE}	V_O level selection	86	Output	Signal for selecting the level of the power supply IC booster voltage, to be used for the maximum voltage of V_O. Selects that the booster voltage level is either the same level as V_{DD1} or a multiple of minus 1. Connect to the V_{CE} pin of the power supply IC.

3.5 Driver-Related Pins (1/2)

Symbol	Pin Name	Pad No.	I/O	Function
Y_1 to Y_{528}	Source output	730 to 468, 457 to 193	Output	These pins are source output pins.
VCOM	COM adjustment	110	Output	This pin is the common adjustment output pin.
VCOUT1	Center rectangle signal output	106, 107	Output	This pin is the center rectangle signal output (V_{p-p}) for common modulation between 0 V and V_S.
VCOUT2	Center rectangle signal output	93	Output	This pin is the center rectangle signal output (V_{p-p}) for common modulation between 0 V and V_{DD2}.
BGRIN	External-power supply connect	115	Input	This is an external-power supply input pin for VCOM. This pin is valid when BGRS (power supply control register 1: R25) = 1. In this case, the reference voltage of the amplifier for setting the common waveform center value is input from outside the μPD161623. When BGRS = 0, the μPD161623 internal voltage is set as the reference voltage of the amplifier for setting the common waveform center value. In this case, leave it open.
VCOMR	VCOM setting register connection	114	Input	This pin connects an external feedback resistor for setting VCOM. This pin is valid when FBR_{SEL} = L. In this case, connect a feedback resistor between the VCOM pin and GND. When FBR_{SEL} = H, the amplifier for setting the common waveform center value operates as a voltage follower. In this case, leave it open.

(2/2)

Symbol	Pin Name	Pad No.	I/O	Function
FBR_{SEL}	VCOM setting external circuit select	117	Input	This pin is used to select the method of adjusting the amplifier for setting the common waveform center value used to set the COMMON drive waveform center level. FBR_{SEL} = H: Voltage follower circuit used (VCOMR connected to VCOM internally) FBR_{SEL} = L: External feedback resistor used
★ CVPH, CVPL, CVNH, CVNL	Basis power supply pin for γ-corrected power supplies	102, 101, 100, 99	Output	This is operational amplifier output pin for the g-corrected power supplies. Normally, this pin connects capacitor of 1.0 μF.
DAC_0 to DAC_7	D/A converter value setting	139 to 132	Input	These pins set the reference voltage of the amplifier for setting the VCOM value used to set the COMMON drive waveform center level. These pins are valid when the VCOM output center value setting register (R29) = 00H and BGRS (R25: D_6) = 0. For more details, refer to **5.5 Common Adjustment Circuit.**

Remark T.B.D. (To be determined.)

3.6 Test or Other Pins

Symbol	Pin Name	Pad No.	I/O	Function
$TOUT_0$ to $TOUT_{17}$, TOSCO	Source output	34 to 17, 41	Output	This is output pin when μPD161623 is in test mode. Normally, leave it open.
TSTRTST, TSTVIHL, TOSCI, TOSCSELI, TOSCSELO, TBSEL1, TBSEL2, PSX_1	COM adjustment	37, 36, 40, 39, 38, 129, 130, 78	Output	These pins are to set up test mode of μPD161623. Normally, fixed it to V_{SS}.
SI, SCL	Test input	75, 76	Input	These pins are to set up test mode of μPD161623. Normally, fixed it to either V_{DD1} or V_{SS}.
TBGR	Test input/output	131	I/O	This is output pin when μPD161623 is in test mode. Normally, leave it open.
DUMMY	Dummy	1 to 16, 111, 112, 153 to 192, 458 to 467, 731 to 737	–	Dummy pin

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

	Pin Name	Input Type	I/O	Power Supply	Recommended Connection of Unused Pins	Note
	PSX_0	Schmitt trigger	Input	V_{DD1}	Mode setting pin	1
	/RESET	Schmitt trigger	Input	V_{DD1}	Always reset on power application	–
★	/RD(E)	Schmitt trigger	Input	V_{DD1}	Connect to V_{DD1} (when i80 series interface)	–
★	C86	Schmitt trigger	Input	V_{DD1}	Mode setting pin	1
★	D_0 to D_{17}	Schmitt trigger	I/O	V_{DD1}	–	–
	RS	Schmitt trigger	Input	V_{DD1}	Register setting pin	2
	OP_0 to OP_7	–	Output	V_{DD2}	Leave open	–
	OSC_{IN}	CMOS	Input	V_{DD2}	Input external clock (in OSC_{SEL} = H mode)	–
	OSC_{OUT}	CMOS	Input	V_{DD2}	Leave open (in OSC_{SEL} = H mode)	–
	CSTB	–	Output	V_{DD1}	Leave open	–
	OSC_{SEL}	Schmitt trigger	Input	V_{DD2}	Mode setting pin	3
	GOE_1	–	Output	V_{DD2}	Always connect to the gate driver	–
	GOE_2	–	Output	V_{DD2}	Always connect to the gate driver	–
	GSTB	–	Output	V_{DD2}	Always connect to the gate driver	–
	GCLK	–	Output	V_{DD2}	Always connect to the gate driver	–
	LPMP	–	Output	V_{DD2}	Leave open	–
	DCON	–	Output	V_{DD2}	Always connect to the power IC	–
	RGONP	–	Output	V_{DD2}	Always connect to the power IC	–
	V_{CD11}, V_{CD12}	–	Output	V_{DD2}	Always connect to the power IC	–
	V_{CD2}	–	Output	V_{DD2}	Always connect to the power IC	–
	V_{CE}	–	Output	V_{DD2}	Always connect to the power IC	–
	V_{COM}	–	Output	V_S	Leave open (FRB_{SEL} = H)	–
	VCOUT1	–	Output	V_S	Leave open	–
	VCOUT2	–	Output	V_{DD2}	Leave open	–
★	BGRIN	–	Input	V_S	Leave open (BGRS = 0 [R25])	–
★	VCOMR	–	Input	V_S	Leave open (FRB_{SEL} = H)	–
	$TOUT_0$ to $TOUT_{17}$	–	Output	V_{DD2}	Leave open	–
	TOSCO	–	Output	V_{DD2}	Leave open	–
	TSTRTST	–	Input	V_{DD2}	Connect to V_{SS}	–
	TSTVIHL	–	Input	V_{DD2}	Connect to V_{SS}	–
	TOSCI	–	Input	V_{DD2}	Connect to V_{SS}	–
	TOSCSELI	–	Input	V_{DD2}	Connect to V_{SS}	–
	TOSCSELO	–	Input	V_{DD2}	Connect to V_{SS}	–
	TBSEL1	–	Input	V_{DD2}	Connect to V_{SS}	–
	TBSEL2	–	Input	V_{DD2}	Connect to V_{SS}	–
	TBGR	–	Input	V_{DD2}	Connect to V_{SS}	–
	PSX_1	–	Input	V_{DD1}	Connect to V_{SS}	–
	SCL	–	Input	V_{DD1}	Connect to V_{DD1} or V_{SS}	–
	SI	–	Input	V_{DD1}	Connect to V_{DD1} or V_{SS}	–
	DTX	Schmitt trigger	Input	V_{DD1}	Connect to V_{DD1} or V_{SS}	1
	FBR_{SEL}	CMOS	Input	V_{DD2}	Connect to V_{DD2} or V_{SS}	3

Notes 1. Connect to V_{DD1} or V_{SS}, depending on the mode selected.

2. Input either H or L by CPU, depending on the register selected.

3. Connect to V_{DD2} or V_{SS}, depending on the mode selected.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μPD161623 chip transfers data using a 18-bit bi-directional data bus (D_{17} to D_0), 16-bit bi-directional data bus (D_{15} to D_0). Setting the polarity of the PSX_0 pin as either H or L enables the selections shown in Table 5–1 below.

Table 5–1.

PSX_0	Mode	/CS	RS	/RD (E)	/WR (R, /W)	C86	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
H	18-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
L	16-bit parallel	/CS	RS	/RD (E)	/WR (R, /W)	C86	Hi-Z Note	D_{15} to D_8	D_7 to D_0

Note Hi-Z: High impedance

5.1.2 Selection of data transfer mode

In the μPD161623, when the 16-bit parallel interface is selected, there are two types of modes to transfer data to display RAM. The mode can be selected as follows with the DTX command.

When using the 16-bit parallel interface and the 1-pixel/18-bit mode (DTX = H) is selected, one pixel of display data must be transferred every two words, as shown in Figure 5–4. At this time, the data of DB_{15} to DB_9 is treated as invalid data.

When the 1-pixle/16-bit mode (DTX = L) is selected, one pixel of display data is transferred every word. However, because one pixel data is 16 bits long, the display color range is restricted to 65,536.

When the 18-bit parallel interface is used, the data transfer method is fixed to 1-pixel/18-bit mode, regardless of the setting of the DTX pin.

Because the display RAM in the μPD161623 has a 1-pixel/18-bit configuration, when using the 1-pixel/16-bit mode (DTX = L), it will be necessary to add supplementary data for the two-bit data deficiency that occurs when (16-bit) data is transferred from the CPU.

For the relationship between the display data and the supplementary data set by the data supplement register, refer to Figure 5–3.

Table 5–2.

PSX_0	Interface Mode	DTX	Mode
H	18-bit parallel	X Note	1-pixel/18-bit
L	16-bit parallel	H	1-pixel/18-bit
		L	1-pixel/16-bit

Note X: Don't care (H or L)

Table 5–3. Data Supplement Register

	Supplemented Display Data
CD12	When 1-pixel/16-bit mode is used, the value set by this flag is stored in the display RAM as D_{12} data.
CD0	When 1-pixel/16-bit mode is used, the value set by this flag is stored in the display RAM as D_0 data.

Figure 5–1. Relationship between Data Bus and Display RAM Data (18-bit parallel interface)

Data bus side

18-bit data																	
DB_{17}	DB_{16}	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1						Dot 2						Dot 3					
1st pixel																	

Display RAM side

Figure 5–2. Relationship between Data Bus and Display RAM Data (1-pixel/18-bit mode [DTX = H], 16-bit parallel interface)

Data bus side

9-bit data (1st word)									9-bit data (2nd word)								
DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1						Dot 2						Dot 3					
1st pixel																	

Display RAM side

Note When in used 16-bit parallel interface, DB_{15} to DB_9 is treated as invalid data.

Figure 5–3. Relationship between Data Bus and Display RAM Data (1-pixel/16-bit mode [DTX = L], 16-bit parallel interface)

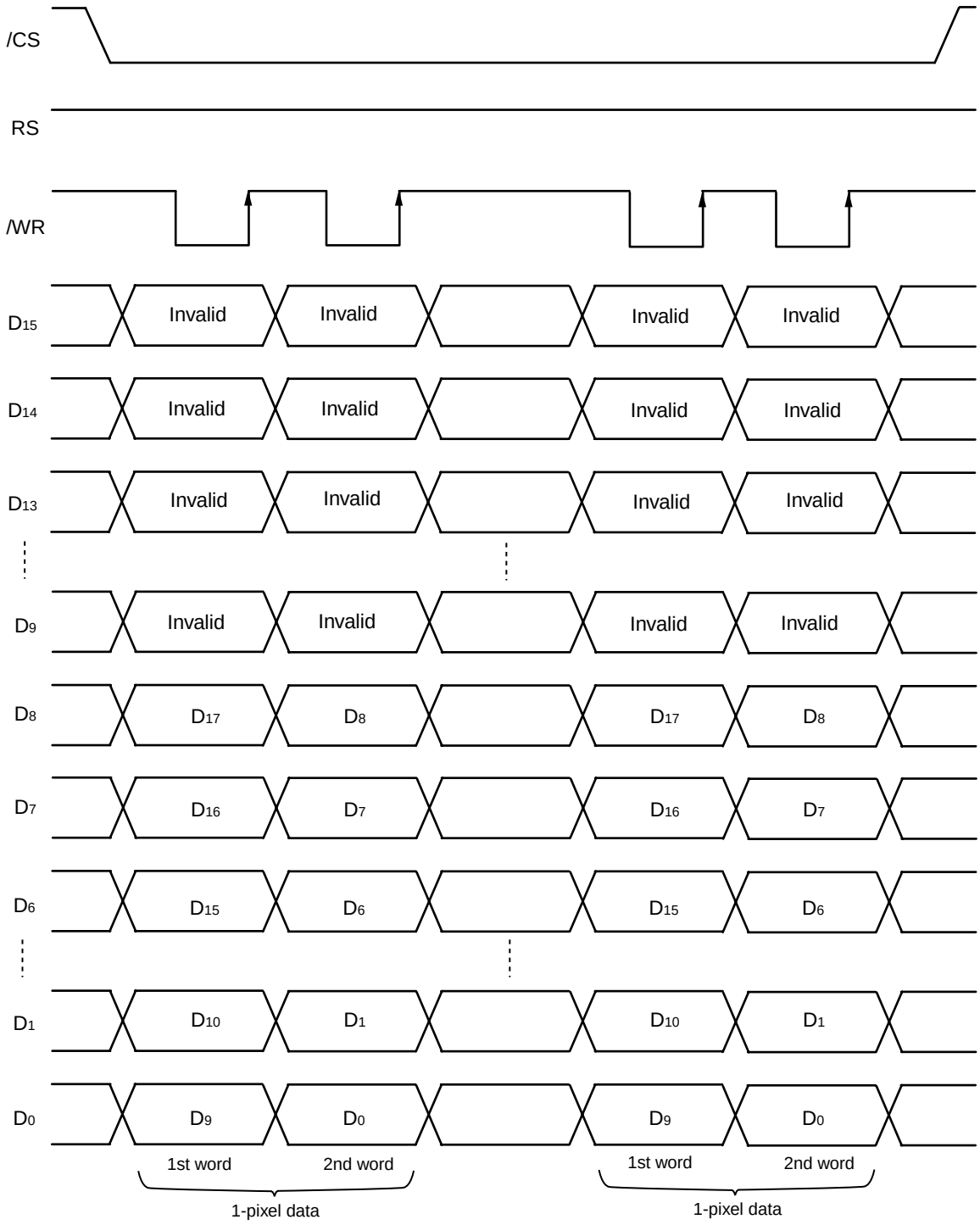
Data bus side

16-bit data																	
DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	---	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	---
Data supplement function																	
					CD_{12}												CD_0
					Note												**Note**
D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1						Dot 2						Dot 3					
1st pixel																	

Display RAM side

Note When In used 16-bit parallel interface, display RAM data D_{12} and D_0 are added to the 16-bit data by the data supplement register (R4), and written to the display RAM as 18-bit data.

Figure 5–4. 16-bit Parallel Interface Date Transfer (1-pixel/18-bit mode [DTX = H])



5.1.3 Parallel interface

When the parallel interface has been selected, setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see Table 5–4 below).

Table 5–4.

C86	Mode	/RD (E)	/WR (R, /W)	PSX_0	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
H	M68 series CPU	E	R, /W	H	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
				L	Hi-Z **Note**	D_{15} to D_8	D_7 to D_0
L	i80 series CPU	/RD	/WR	H	D_{17}, D_{16}	D_{15} to D_8	D_7 to D_0
				L	Hi-Z **Note**	D_{15} to D_8	D_7 to D_0

Note Hi-Z: High impedance. Leave it open.

The data bus signal is identified according to the combination of the RS, /RD (E), and /WR (R, /W) signals, as shown in the following Table 5–5.

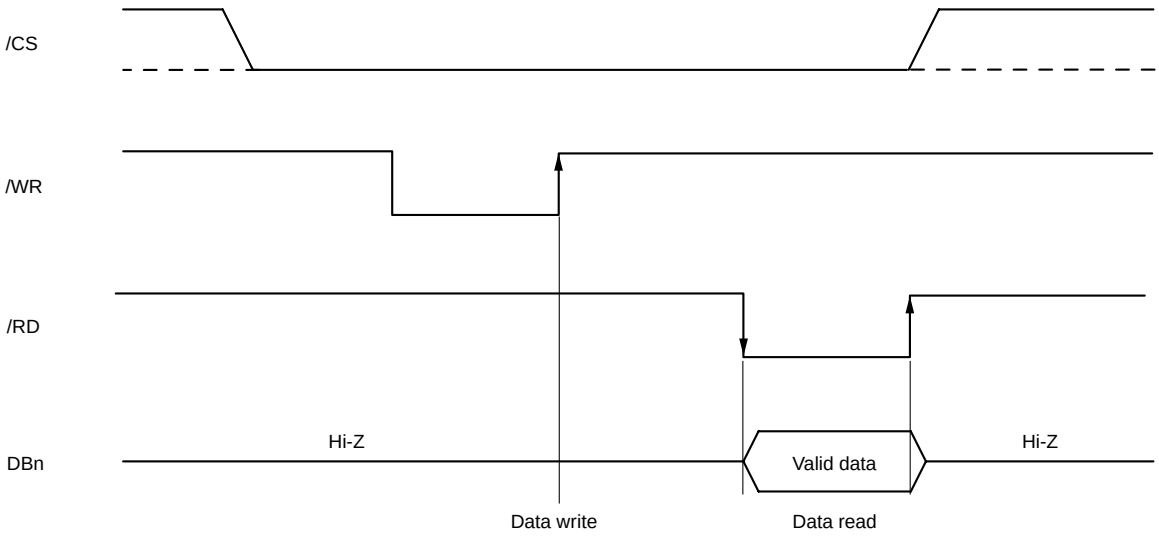
★ **Table 5–5.**

Common	M68 series CPU	i80 series CPU		Function
RS	R, /W	/RD	/WR	
H	H	L	H	Read display data
H	L	H	L	Write display data
L	H	L	H	Prohibited
L	L	H	L	Write to control index register

(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μPD161623 at L period of the /WR signal. The data is output to the data bus when the /RD signal is L.

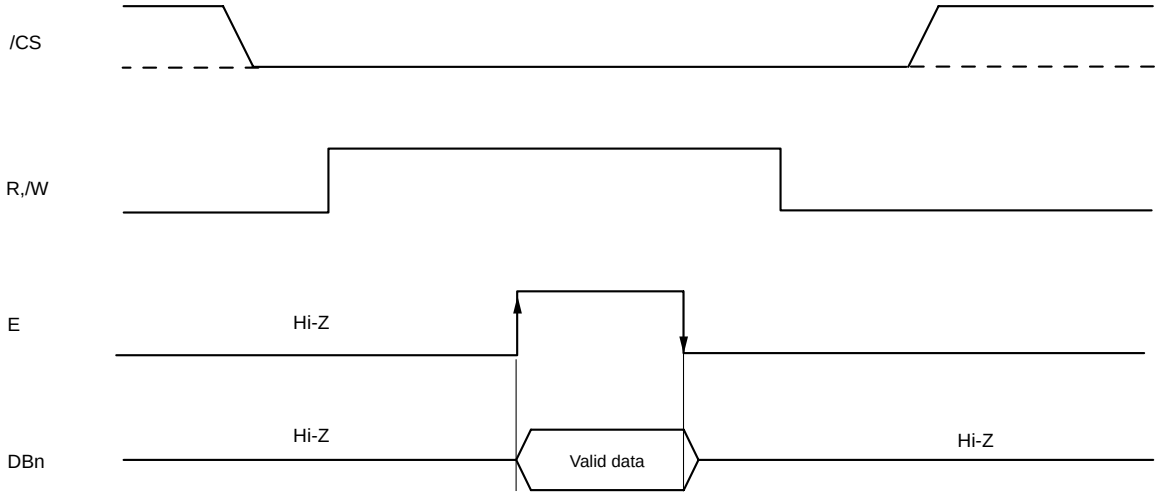
Figure 5–5. i80 Series Interface Data Bus Status



(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the H period of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

Figure 5–6. M68 Series Interface Data Bus Status (When data read)



5.1.4 Chip select

The μPD161623 has two chip select pins (/CS). The CPU parallel interface can be used only when /CS = L. When the chip select pin is inactive, D_0 to D_{17} are set to high impedance (invalid) and input of RS, /RD, or /WR is not active.

5.1.5 Access to display data RAM and internal registers

When the CPU accessed the μPD161623, the CPU only has to satisfy the requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take wait time into consideration.

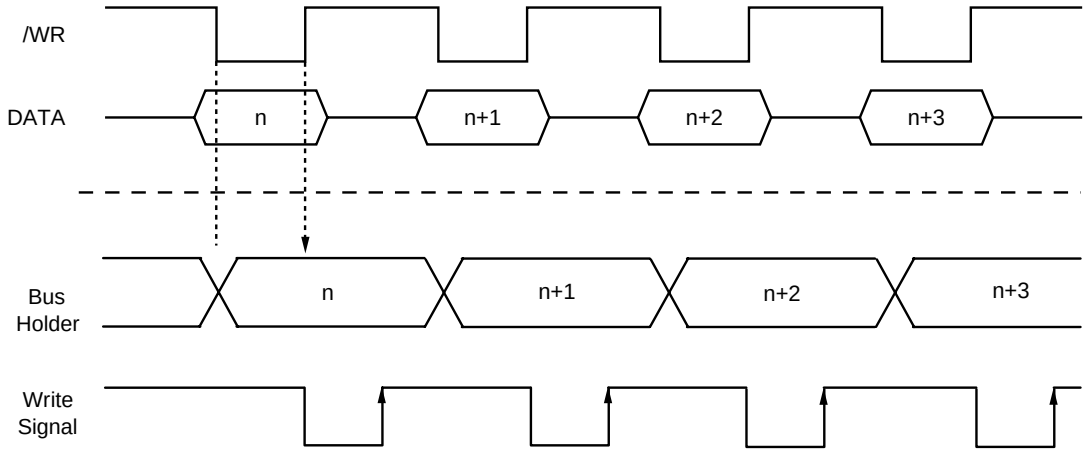
A high-speed RAM write function, as well as the ordinary RAM write function, is provided for writing data to the display data RAM. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported. For details, refer to **5.2.5 High-speed RAM write mode**

Dummy data is not required when writing data. In the μPD161623, only for reading display data, needs dummy data. This relationship is shown in Figure 5–7.

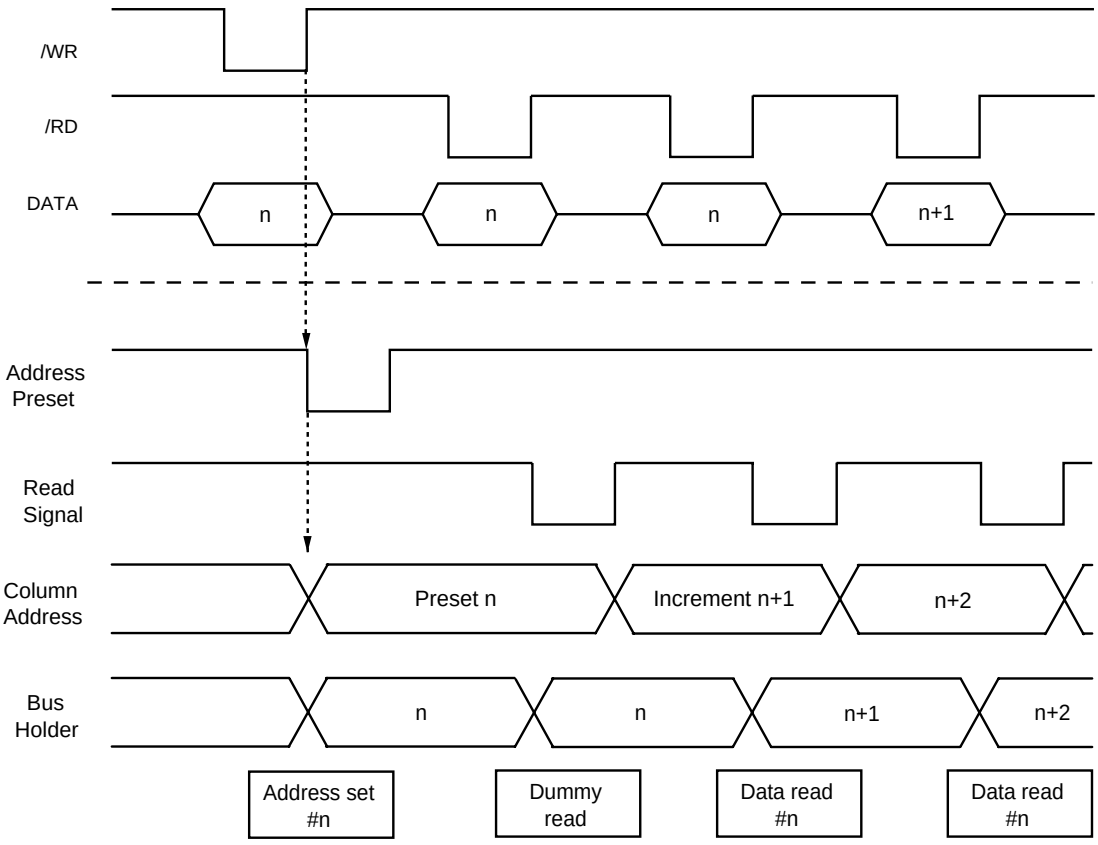
Note that when in write mode of data at high speed for data read mode of read cycle time, this mode equals to normal mode.

Figure 5–7. Image of internal access to display RAM

Writing



Reading



5.2 Display Data RAM

This RAM stores dot data for display and consists of 3,168 bits (176 x 18) x 240 bits. Any address of this RAM can be accessed by specifying an X address and an Y address.

Display data D_0 to D_{17} transmitted from the CPU corresponds to the pixels on the LCD (refer to Table 5–8).

Figure 5–8. Display Data RAM

D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1						Dot 2						Dot 3					
Pixel 1 (= 1 X address)																	

LCD panel									
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8	
	00H	01H	02H	03H	04H	05H	06H	07H	

5.2.1 X address circuit

An X address of the display data RAM is specified by using the X address register (R6) as shown in Figure 5–9.

The specified X address is incremented by one each time display data is written or read.

In the increment mode, the X address is incremented up to AFH. If more display data is written or read, the Y address is incremented, and the X address returns to 00H.

5.2.2 Y address circuit

A Y address of the display data RAM is specified by using the Y address register (R7) as shown in Figure 5–9.

The Y address is incremented each by one when one each time display is written or read and X address is incremented to last address.

When the Y address has been incremented up to EFH and the X address up to the final address, if further display data is read or written, the X and Y addresses return to 00H.

5.2.3 Column address circuit

When the contents of the display data RAM are displayed, column addresses are output to the source output pins as shown in Figure 5–9.

The correspondence relationship between the column addresses of the display RAM and source outputs can be reversed by the ADC flag (source driver direction select flag) of control register 1 (R0) as shown in Table 5–6. This reduces the restrictions on chip layout when the LCD module is assembled.

Table 5–6. Relationship between Column Address of Display RAM and Source Output

Source Output		Y_1	Y_2	→		→	Y_{527}	Y_{528}
ADC	0	000H	001H	→	Column address	→	20EH	20FH
	1	20FH	20EH	←	Column address	←	001H	000H

Figure 5–9. μPD161623 RAM Addressing

Source output														
	ADC=0	Y1	Y2	Y3	Y4	Y5	Y6	---	---	Y523	Y524	Y525	Y526	Y527
	ADC=1	Y528	Y527	Y526	Y525	Y524	Y523	---	---	Y6	Y5	Y4	Y3	Y2
	X-address	000H			001H			---	---	AEH			AFH	
	Column addr	000H	001H	002H	003H	004H	005H	---	---	20AH	20BH	20CH	20DH	20EH
		D17--D12	D11--D6	D5---D0	D17--D12	D11--D6	D5---D0			D17--D12	D11--D6	D5---D0	D17--D12	D11--D6
		1st pixel			2nd pixel					1st pixel			2nd pixel	

Gate output		Y-address	
R,/L=H	R,/L=L	ADR=0	ADR=1
O1	O240	00H	EFH
O2	O239	01H	EEH
|	|	|	|
O87	O90	56H	59H
O88	O89	57H	58H
O89	O88	58H	57H
O90	O87	59H	56H
|	|	|	|
O239	O2	EEH	01H
O240	O1	EFH	00H

Scan direction

Display area

5.2.4 Arbitrary address area access (window access mode (WAS))

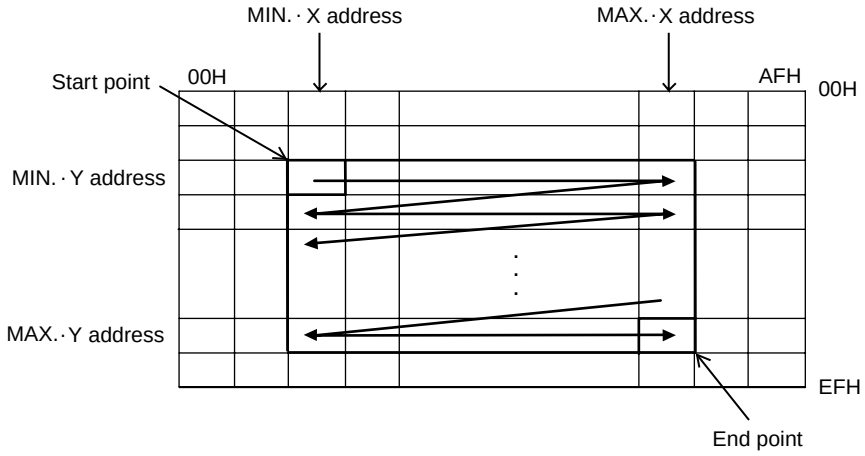
With the μPD161623, any area of the display RAM selected by the MIN.·X/Y address registers (R8 and R10) and MAX.· X/Y address registers (R9 and R11) can be accessed.

★ When WAS of data access control register (R5) is set to 1, the window access mode is then selected and accessed by setting only address area of the MIN.·X/Y address registers and MAX.·X/Y address registers.

. The address scanning setting is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register (R6) and Y address register (R7).

Note that the display RAM must be accessed after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.· X/Y address register or MAX.· X/Y address register.

Figure 5–10. Example of Incrementing Address when in Window Access Mode



Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

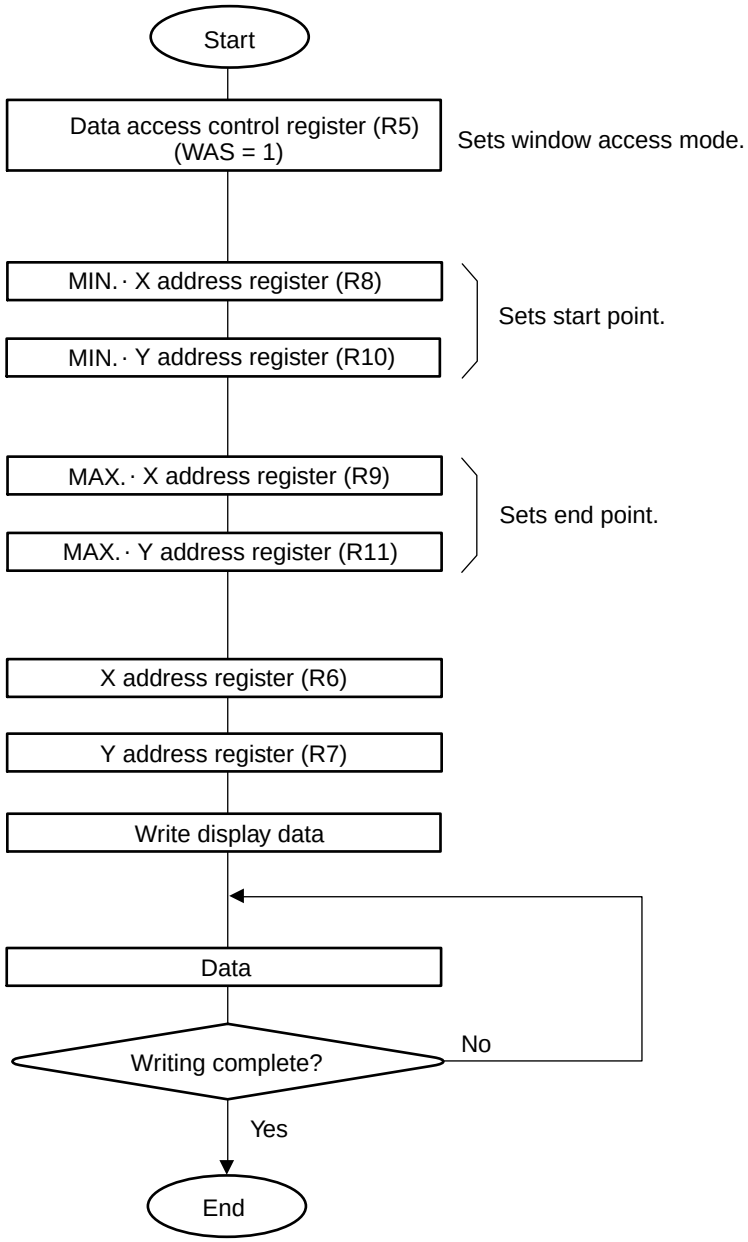
Item	Address Relationship
X address	00H ≤ MIN.·X address ≤ X address (R6) ≤ MAX.·X address ≤ AFH
Y address	00H ≤ MIN.·Y address ≤ Y address (R7) ≤ MAX.·Y address ≤ EFH

2. If invalid address data is set as the MIN./MAX.· address, operation is not guaranteed.

★ **3. Do not specify any value other than the address value 2n–2 (n = 1 to 88) for the X address in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.**

4. Access the display RAM after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.· X/Y address register or MAX.· X/Y address register.

Figure 5–11. Example of Sequence in Window Access Mode



5.2.5 High-speed RAM write mode

With the μPD161623, two types of access modes can be selected for accessing the display RAM.

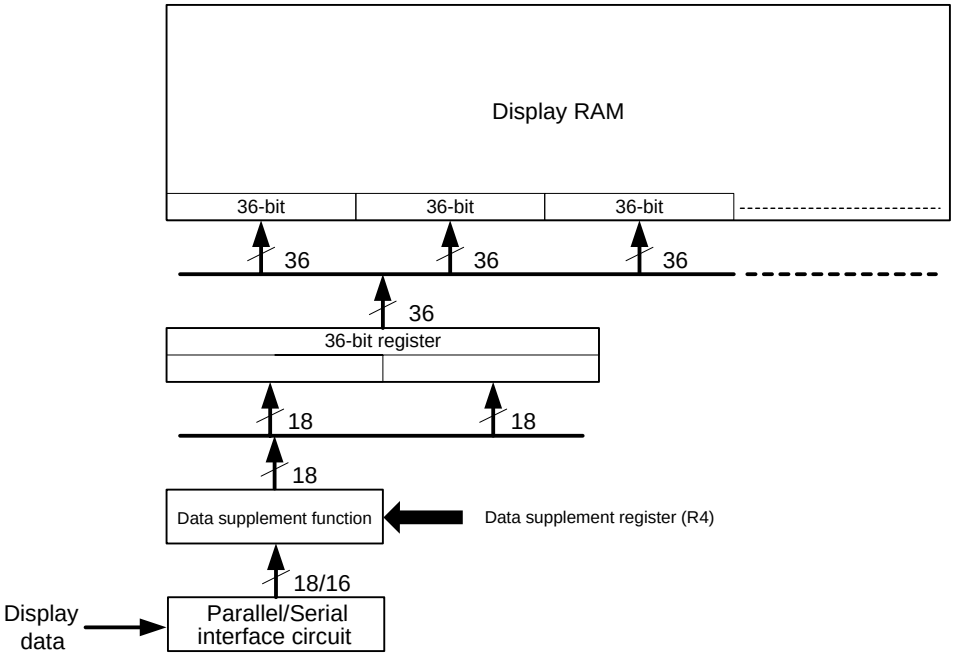
The μPD161623 has a high-speed RAM write function, as well as an ordinary RAM write function. By using the high-speed write function, data can be written to the display RAM at an access speed two times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported.

When the high-speed RAM write mode is selected by using BSTR of the data access control register (R5), data is temporarily stored in an internal register of the μPD161623. When data of 36 bits (18 bits x 2) has been stored in the register, it is written to the display RAM. It is also possible to write the next data to the internal register while the first data is being written to the RAM.

In the high-speed RAM write mode, however, the CPU must transmit data in units of 2 pixel data (1-pixel/18-bit mode: 36-bit, 1-pixel/16-bit mode: 32-bit) have been written to the internal register. If data of less than 2-pixel data is transmitted in the high-speed RAM write mode, this data is not written to the display RAM. Therefore, CPU data is not reflected on the LCD display even if it is transmitted. In this case, the data that is not reflected remains stored in the register. When the next data is transmitted, it is written to the register from where the preceding data is stored. However, if the chip select signal is disserted inactive (/CS = H) in the middle of data transfer, and then asserted active again and when the display data write is set, the register is initialized. Consequently, the data stored in the register is lost.

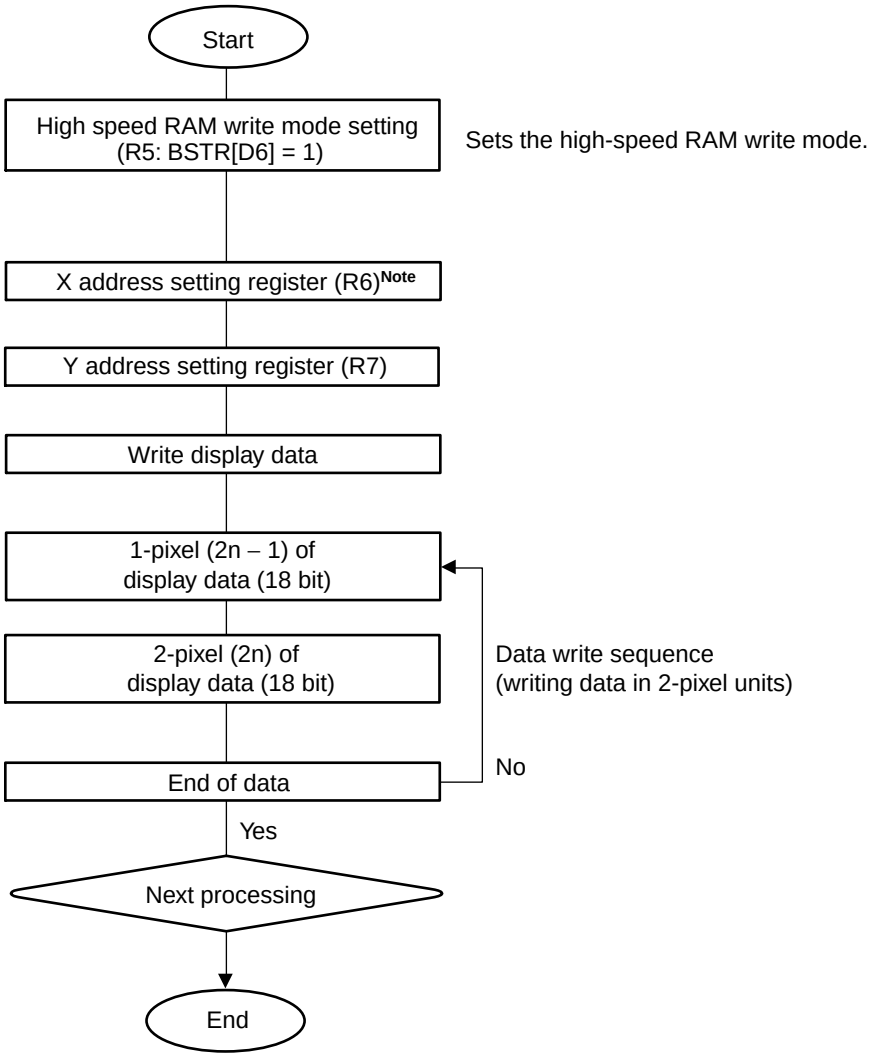
It is therefore recommended to transmit display data in 2-pixel units when using the high-speed RAM write mode.

Figure 5–12. Image of Operation in High-speed Write Mode



Caution Do not specify any value other than the address value 2n – 2 (n = 1 to 88) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

Figure 5–13. Example of Sequence in High-Speed RAM Write Mode (with 18-Bit Parallel Interface)



n: n ≥ 1

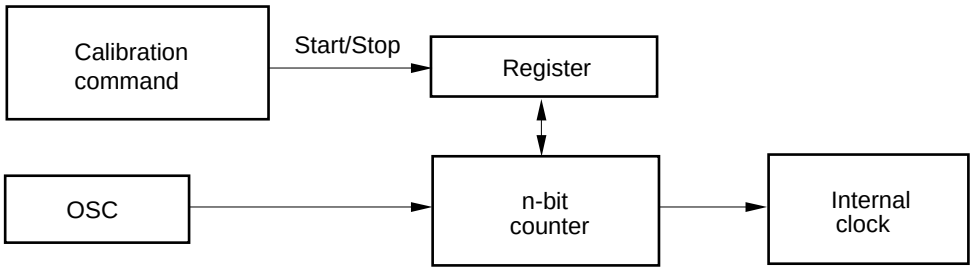
Note Do not specify any value other than the address value 2n – 2 (n = 1 to 88) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

5.3 Oscillator

The μPD161623 has a CR oscillator (with external R resistance), which generate the display clock. When OSC_{SEL} is L, an internal CR oscillator is selected. On the other hand, leave both OSC_{IN} and OCS_{OUT} pin open. When OSC_{SEL} is H, an external connection oscillator is selected. Connect 42 kΩ resistance between OSC_{IN} an OSC_{OUT} pin (when in used 240 lines).

This oscillator also has a calibration function, which is available by itself to set the number of frame frequency of display driving. Frame frequency calibration is set by calibration register (R45). The time to select one line is set by the calibration start and stop commands.

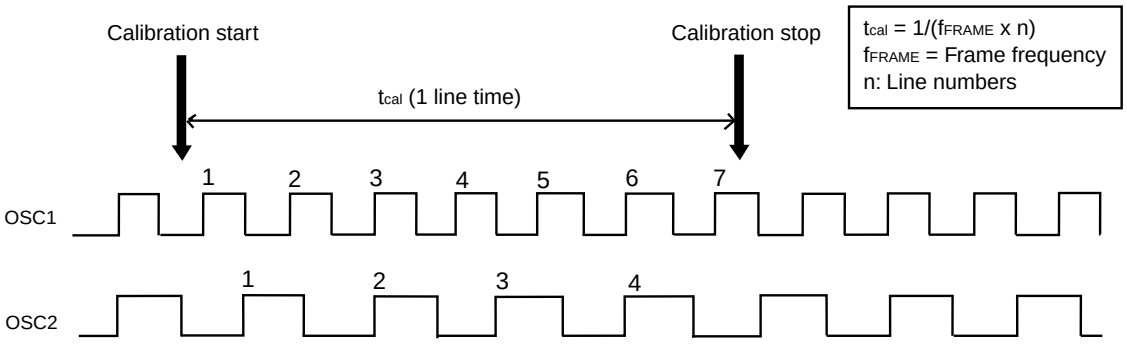
Figure 5–14. Frame Frequency Calibration



The calibration function involves counting the number of oscillation clocks generated between the start and stop signals and storing that number in a register. The number of oscillation clocks is then continually compared with this register value in subsequent operations, and the time of the clock number stored in the register is set as 1 line selection time, and used as the internal reference clock.

Using the time to set calibration (t_{cal}) can be selected either t_{cal} or t_{cal} x 2 through control register 2 (R1): LTS.

Figure 5–15. Calibration Function Timing (LTS [R1] = 0)



5.4 Display Timing Generator

5.4.1 Display timing

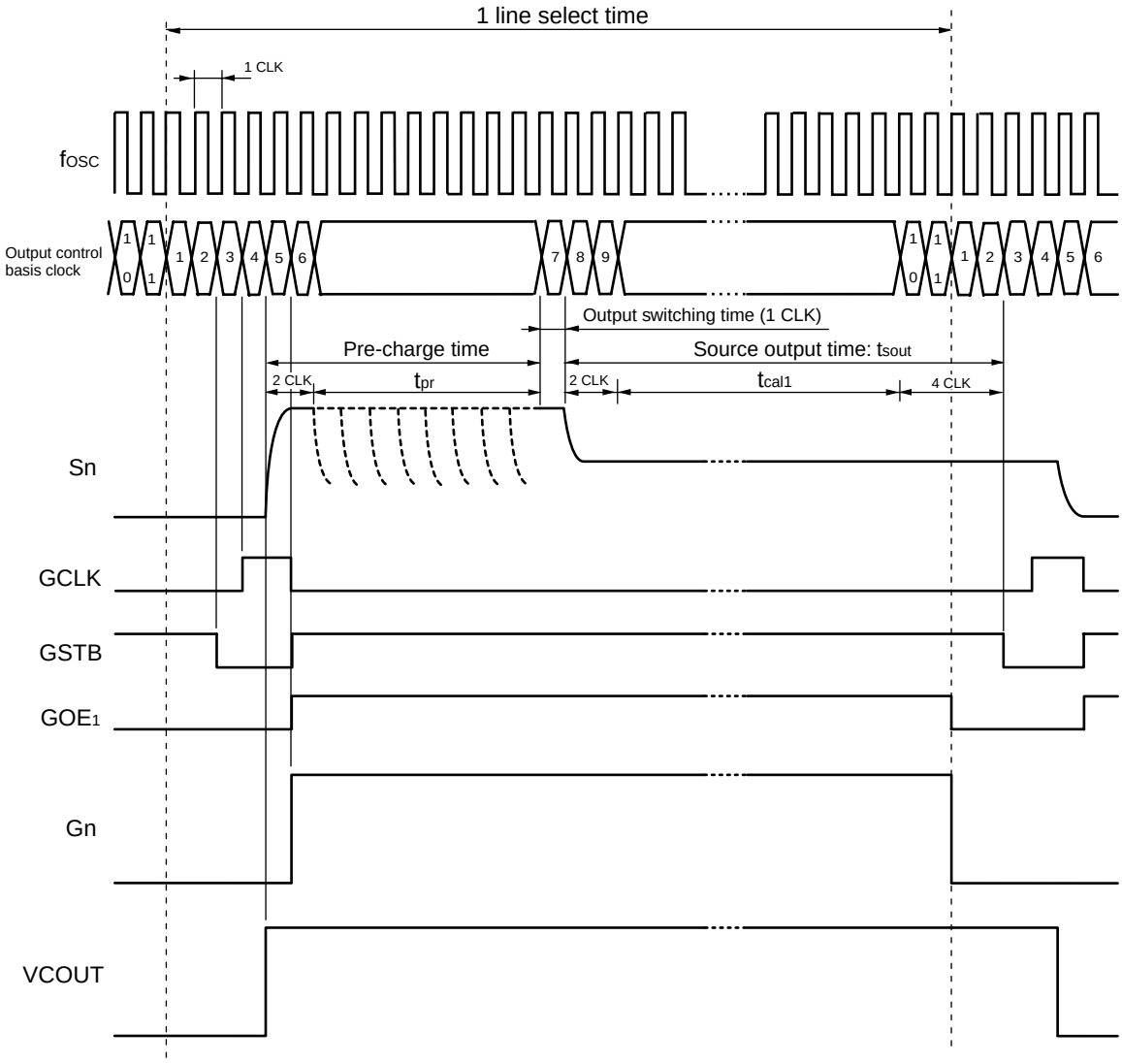
The μPD161623 generates the TFT-:CD drive timing inside the μPD161623. The TFT-LCD panel is driven at the timing of one line selection period generated based on the calibration time (t_{cal}) set by the calibration function, as shown in the figure below. One line selection period is made up of a pre-charge period, a source output period, and the μPD161623 output control clock. The pre-charge and source output periods are set by the pre-charge period setting register (R46) and calibration register (R45), respectively, based on the following expressions.

1 line selection period = t_{cal}
Pre-charge period = t_{pr}
Source output period = t_{sout}

t_{cal}: Calibration setting time [R45]
$t_{pr} = (1/f_{OSC}) \times (CLK_{pr} + 2\ CLK)$
$t_{sout} = t_{cal} - (t_{pr} + 3\ CLK)$

CLK_{cal}: Calibration setting time (t_{cal}) clock number = $t_{cal} \div (1/f_{OSC})$
CLKpr: Pre-charge peiod setting register clock number [R46: PLIMn] n
1 CLK = $1/f_{OSC}$
f_{OSC}: Oscillator frequency

Figure 5–16. 1-line Select Time



The display timing generator generates the timing signals for the internal timing of the source driver and for the gate driver. The output timings for normal operation, for normal operation → stand-by mode, and for stand-by mode → normal operation, are shown below.

Figure 5–17. During Normal Operation (during line inversion)

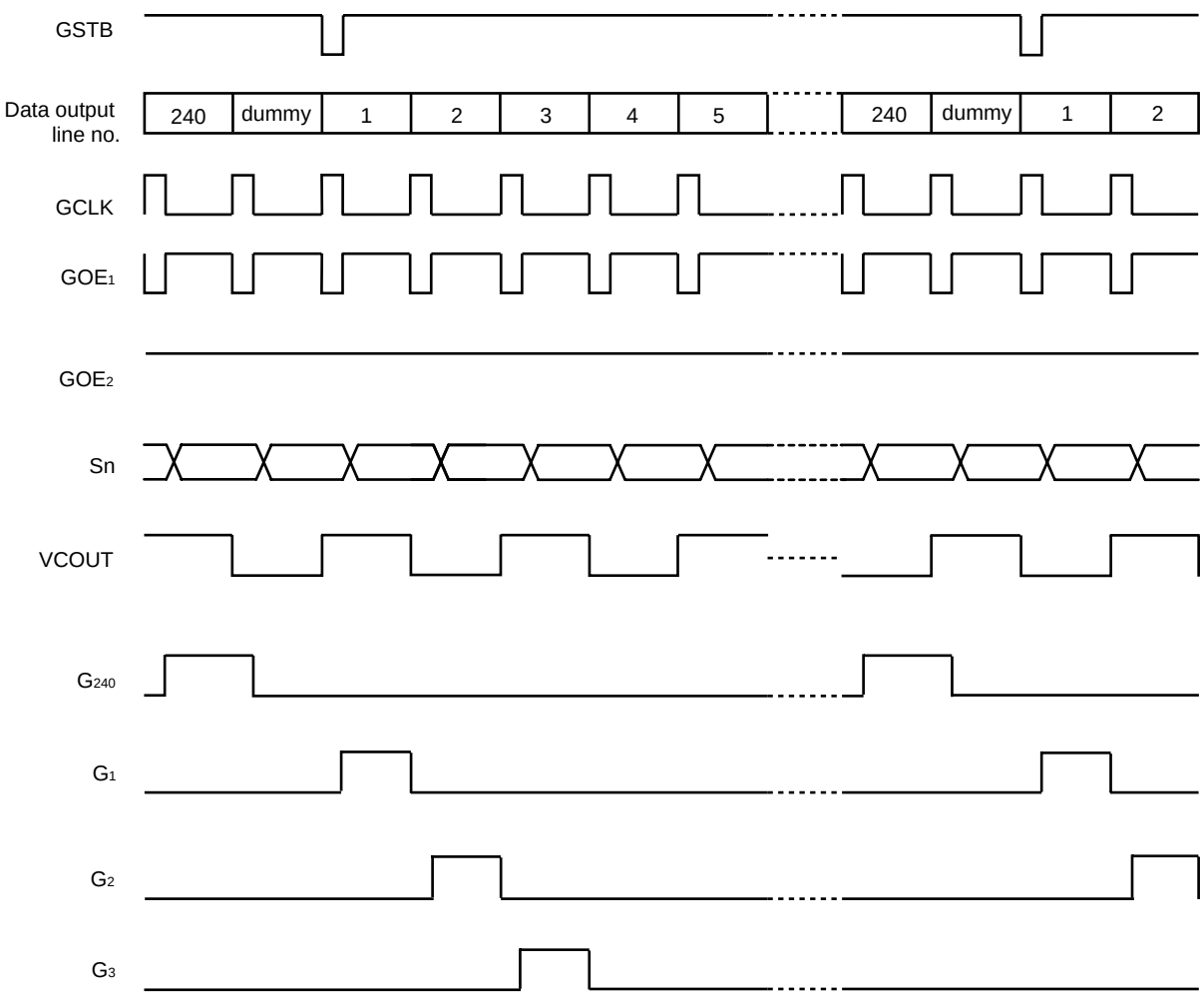


Figure 5–18. Normal Operation → Stand-by Input (during line inversion)

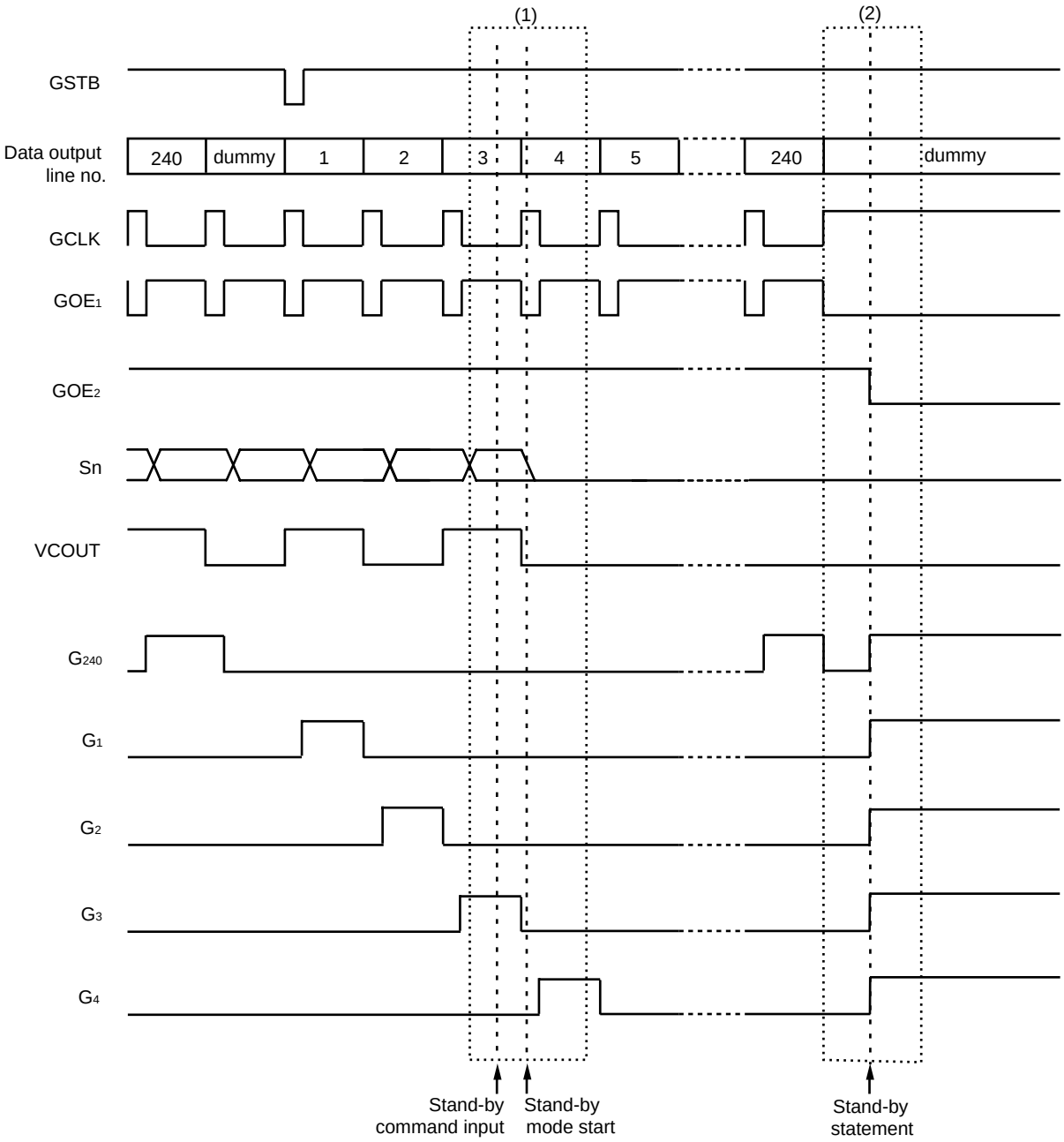


Figure 5–19. Normal Operation → Stand-by Input (during line inversion) (1) Reference

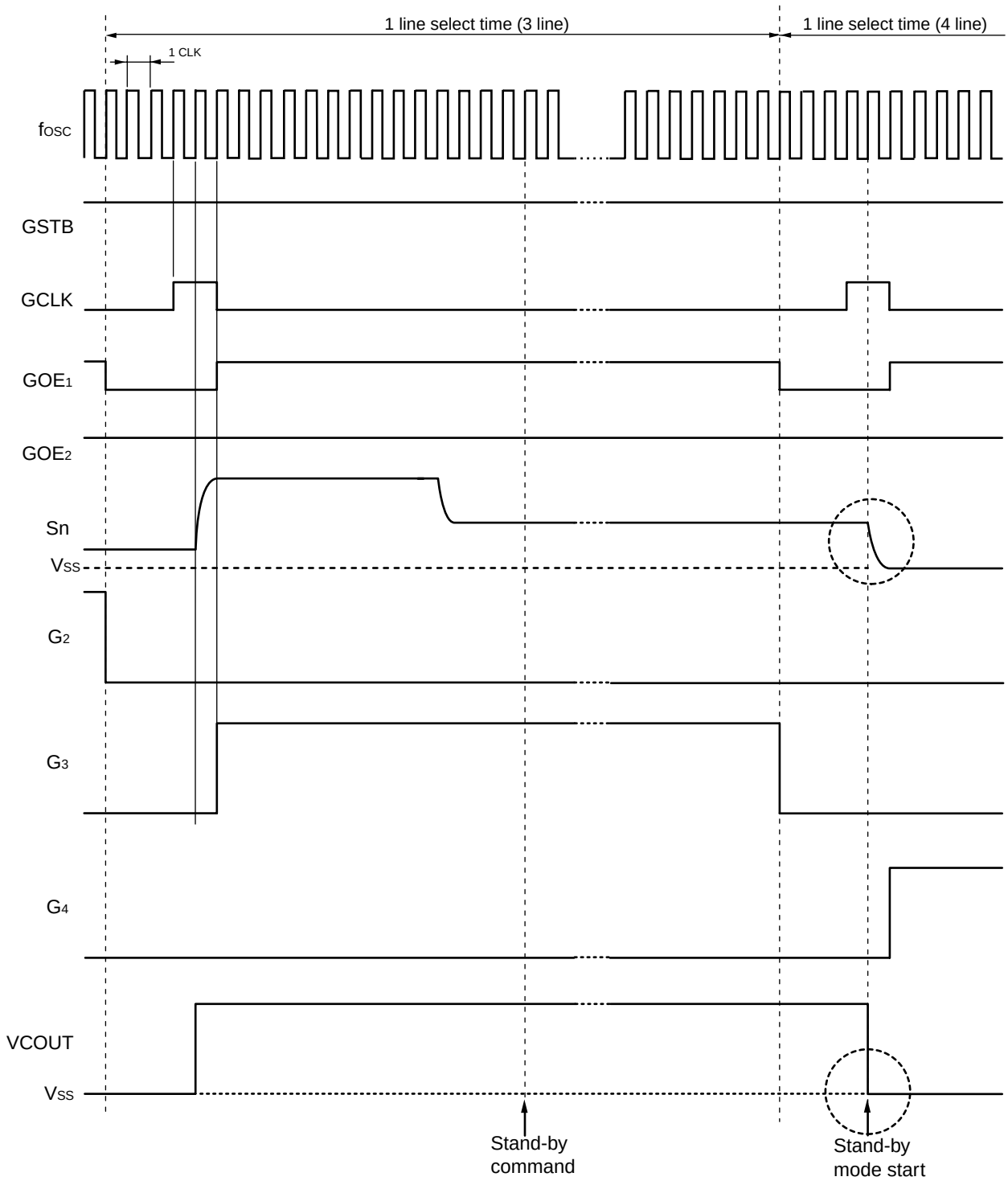


Figure 5–20. Normal Operation → Stand-by Input (during line inversion) (2) Reference

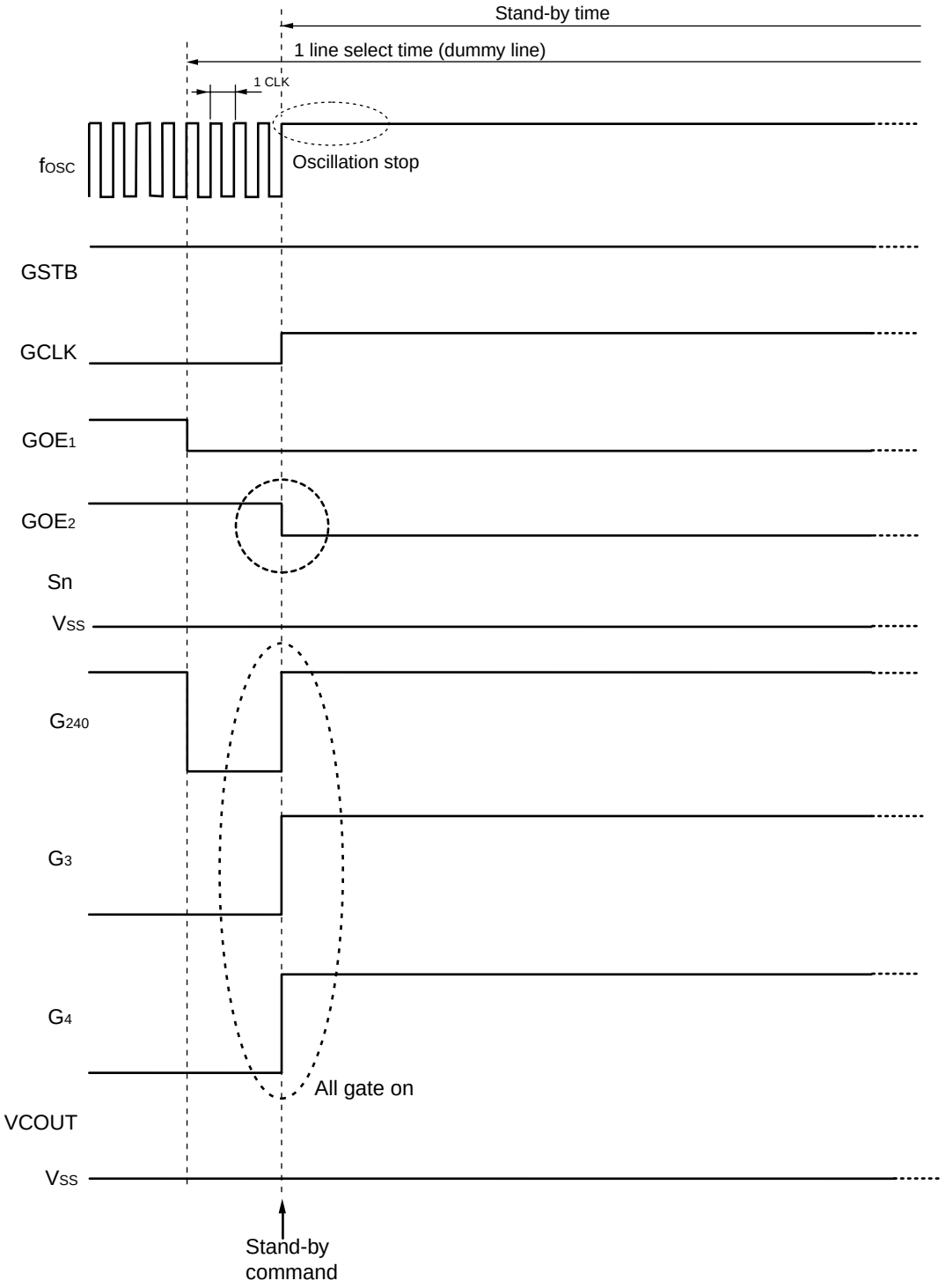
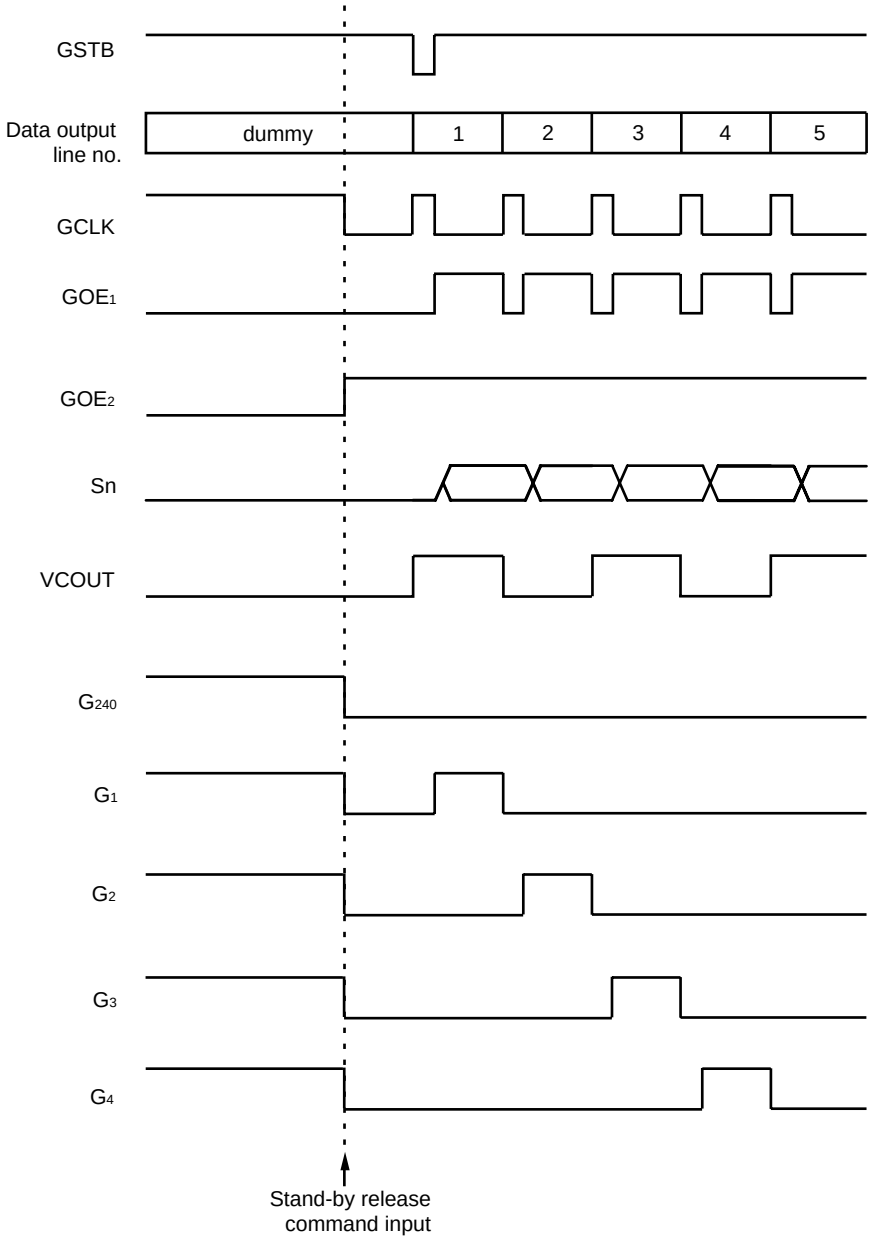


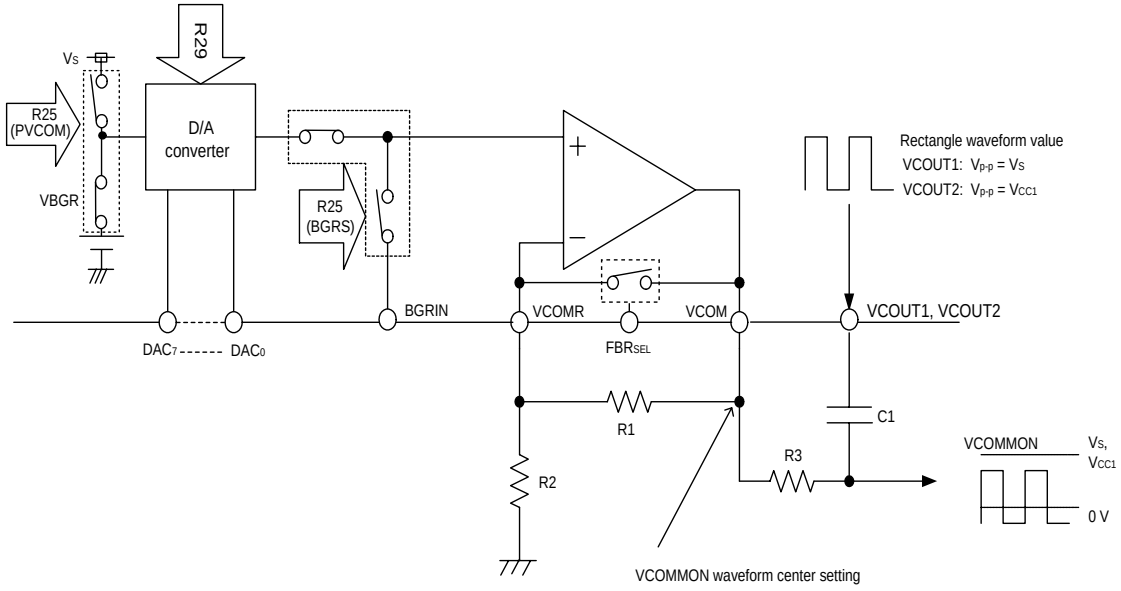
Figure 5–21. Stand-by → Return to Normal Operation (during line inversion)



5.5 Common Adjustment Circuit

To generate common output, the center voltage of the common waveform is output from the VCOM pin along with output of a 0 to V_S (V) square waveform from the VCOUT1 pin and 0 to V_{DD1} (V) from VCOUT2. The level of the VCOM output can be adjusted using as external resistor.

★ **Figure 5–22. Common Adjustment Circuit**



The VCOM voltage formulas are shown below.

★ <When internal power supply is used 1 (D_6 of R25: BGRS = 0, D_3 of PVCOM = 0) >

COM voltage = (1+R1/R2) x VBGR x (α ÷ 256)

VBGR = 3.0 V TYP.

α: Setting of VCOM electric volume register (R29)

★ < When internal power supply is used 2 (D_6 of R25: BGRS = 0, D_3 of PVCOM = 1) >

COM voltage = (1+R1/R2) x V_S x (α ÷ 256)

α: Setting of VCOM electric volume register (R29)

★ <When external power supply is used (D_6 of R25: BGRS = 1)>

COM voltage = (1+R1/R2) x VBGRIN

VBGRIN = External supply voltage (voltage input from BGRIN)

★ <Recommended values for R1 to R3, and C1>

Use the values listed below as a guideline. The user is responsible for ultimately determining the resistance values and recommended values based on careful evaluation on actual panels.

R1: 200 kΩ

R2: 51 to 100 kΩ

R3: 51 to 100 kΩ

C1: 10 μF

5.6 Rectangular Signal Generator

This circuit generates a common rectangular signal. A rectangular wave of 0 to V_S (V) is output from the VCOUT1 pin, and a wave of 0 to V_{DD2} (V) is output from the VCOUT2 pin. The common output wave necessary for driving an LCD can be generated by connecting an external circuit as shown in Figure 5–22.

5.7 Reference Voltage Generator (VBGR)

The μPD161623 has a reference voltage generator for the voltage regulator. This reference voltage generator generates a constant voltage from V_{DD2}. The constant voltage generated by this circuit is connected to the input of the operational amplifier that adjusts the center level of the COMMON drive output, via a D/A converter.

By using this voltage, therefore, the center level of the COMMON drive output can be kept constant, without being affected by fluctuations in the supply voltage.

The common waveform output necessary for driving an LCD can be generated by connecting the external circuit show in Figure 5–16.

When the internal reference voltage generator is not used (R25: BGRS = 1), directly input the reference voltage to the operational amplifier that adjusts the center level of the COMMON drive output.

5.8 D/A Converter Circuit

The μPD161623 is provided with an internal D/A converter to adjust the voltage of the reference voltage generator for the voltage regulator. This D/A converter divides the constant voltage generated by the reference voltage generator (VBFR) by 256, and a level of voltage between VBGR and V_{SS} can be selected by setting the VCOM electronic volume register (R29).

In addition, this D/A converter also has a function to select a level by using an external pin. If the set value of the VCOM electronic volume register (R29) is 00H, the set statuses of the DAC_7 to DAC_0 pins are valid.

Table 5–7. α Setting of VCOM Electronic Volume Register (R25: BGRS = 0)

	EV_7	EV_6	EV_5	EV_4	EV_3	EV_2	EV_1	EV_0	α	Remark
	DAC_7	DAC_6	DAC_5	DAC_4	DAC_3	DAC_2	DAC_1	DAC_0		
00H	0	0	0	0	0	0	0	0	DAC_n set value	R29
									0	DAC_n
01H	0	0	0	0	0	0	0	1	2	
02H	0	0	0	0	0	0	1	0	3	
03H	0	0	0	0	0	0	1	1	4	
⋮				⋮					⋮	
FEH	1	1	1	1	1	1	1	0	255	
FFH	1	1	1	1	1	1	1	1	256	

5.9 γ-Curve Correction Power Supply Circuit

The μPD161623 includes a γ-curve correction power supply circuit. If the internal γ-curve correction matches the LCD characteristics, no external components are necessary. This power circuit has white level and black level reference voltage generators on the positive and negative polarity sides, and also supports unbalanced driving. The reference voltage generators consist of a D/A converter and an operational amplifier and divide V_S to V_{SS} by 256. One level of voltage can be selected by using the γ-contrast value setting register1 to 4 (R36 to R39)

Figure 5–23. γ-Curve Correction Circuit

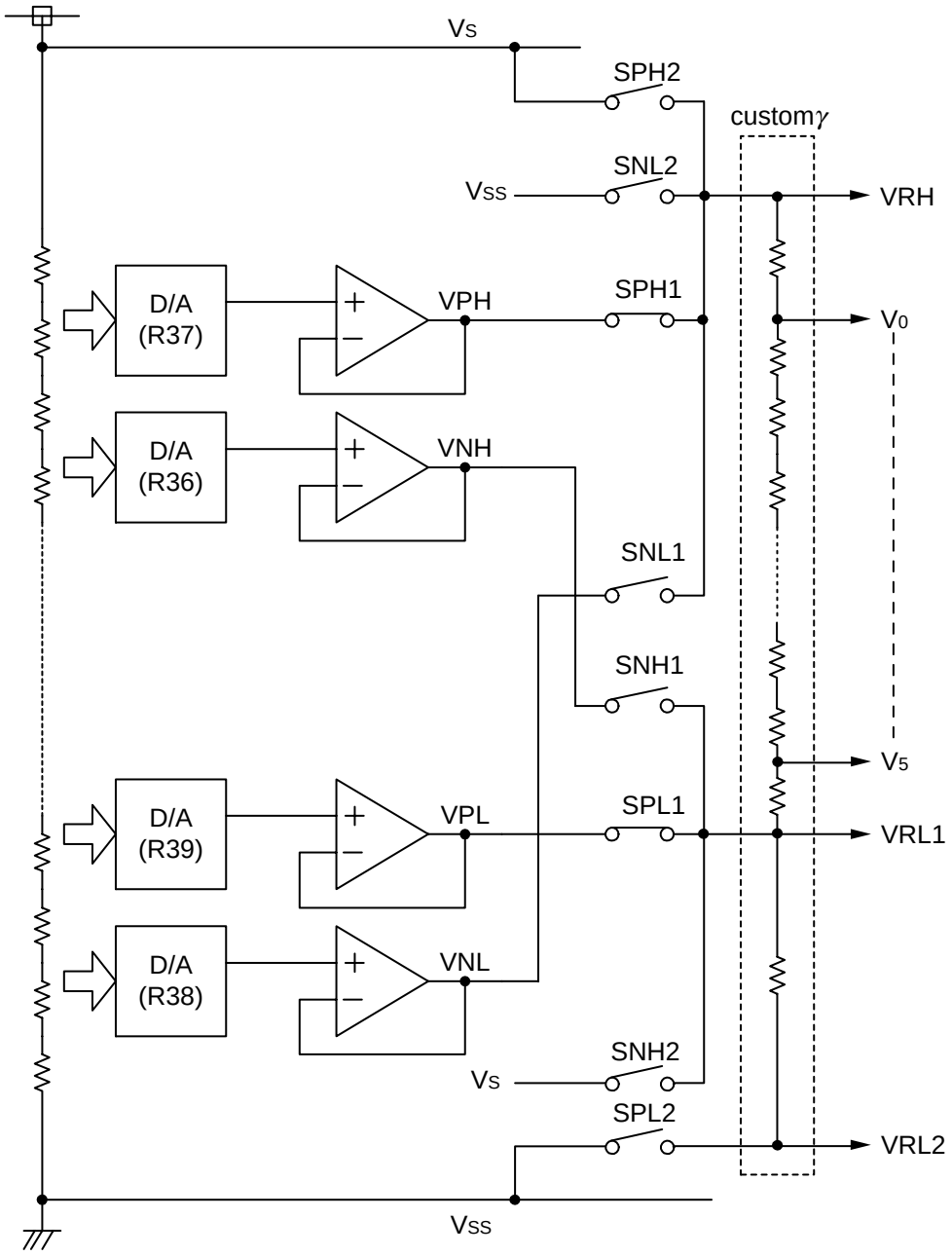
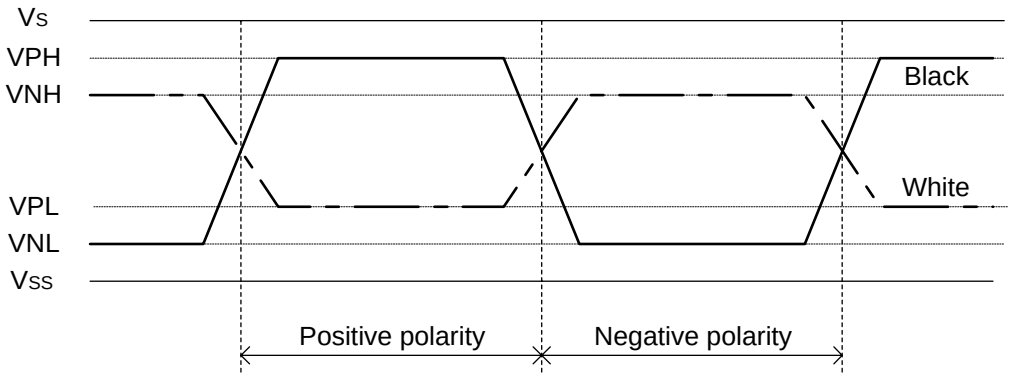


Figure 5–24. Relationship of TFT Drive Voltage (Normally White)



	Drive Level	Setting Register	
VPH	Positive polarity, black	Contrast value setting register 1	R36
VNH	Negative polarity, white	Contrast value setting register 2	R37
VPL	Positive polarity, black	Contrast value setting register 3	R38
VNL	Negative polarity, white	Contrast value setting register 4	R39

The value of each amplifier output can be expressed as follows and the value of β can be set as shown in Table 5–8 and 5–9 by using the contrast value registers (R36, R37, R38, and R39)

VNL, VPL, VNH, VPH = (β ÷ 256) x Vs

Caution The usable range in which each output level of VPH, VNH, VPL, and VNL can be set depends on the γ-curve.

Table 5–8. γ-Contrast Value Setting and Electronic Volume Register β Setting 1 (VPH, VNL)

R36	GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0	β value Setting or
R37	GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0	Status Setting
00H	0	0	0	0	0	0	0	0	Fixed to Vs (Amplifier OFF)
01H	0	0	0	0	0	0	0	1	255
02H	0	0	0	0	0	0	1	0	254
03H	0	0	0	0	0	0	1	1	253
⋮				⋮					⋮
FEH	1	1	1	1	1	1	1	0	2
FFH	1	1	1	1	1	1	1	1	1

Table 5–9. γ-Contrast Value Setting and Electronic Volume Register β Setting 2 (VPL, VNL)

R36	GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0	β value Setting or
R37	GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0	Statement Setting
00H	0	0	0	0	0	0	0	0	Fixed to V_S (Amplifier OFF)
01H	0	0	0	0	0	0	0	1	1
02H	0	0	0	0	0	0	1	0	2
03H	0	0	0	0	0	0	1	1	3
⋮				⋮					⋮
FEH	1	1	1	1	1	1	1	0	254
FFH	1	1	1	1	1	1	1	1	255

The relationship between the setting of the contrast value setting register and the driven waveform is explained next, taking the γ-curve in Figure 5–23 as an example.

Table 5–10. Switch Status when γ-Curve Correction Power Supply Circuit is not used (R36, R37, R38, R39 = 00H)

Polarity	Switch Status							
	SPH1	SNL1	SNH1	SPL1	SPH2	SNL2	SNH2	SPL2
Positive	X	X	X	X	ON	OFF	OFF	ON
Negative	X	X	X	X	OFF	ON	ON	OFF

Remark X: Switch is normally OFF with the amplifier OFF.

Relationship of drive voltage (normally white)

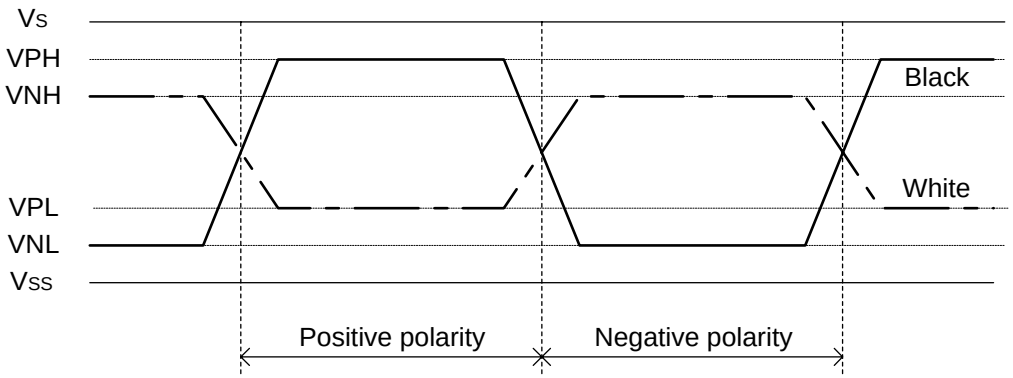


Table 5–11. Switch Status when γ-Curve Correction Power Circuit is used (R36, R37, R38, R39 = other than 00H)

Polarity	Switch Status							
	SPH1	SNL1	SNH1	SPL1	SPH2	SNL2	SNH2	SPL2
Positive	ON	OFF	OFF	ON	x	x	x	x
Negative	OFF	ON	ON	OFF	x	x	x	x

Remark x: Switch is normally OFF

Relationship of drive voltage (normally white)

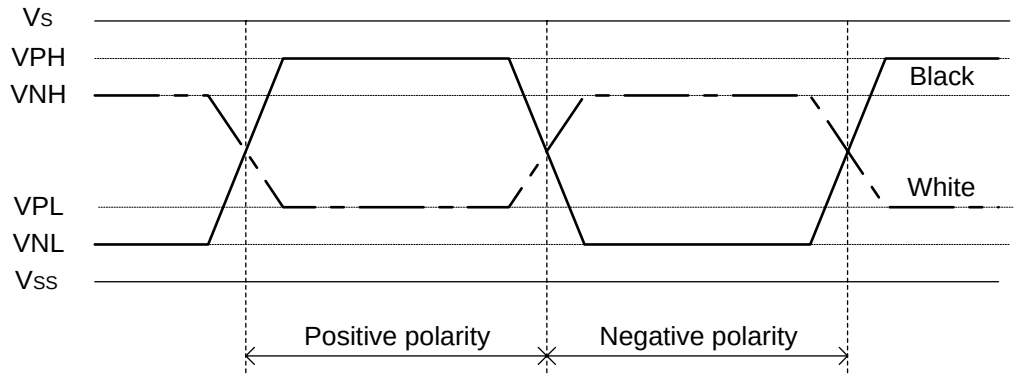


Figure 5–25. TFT Drive Voltage Level

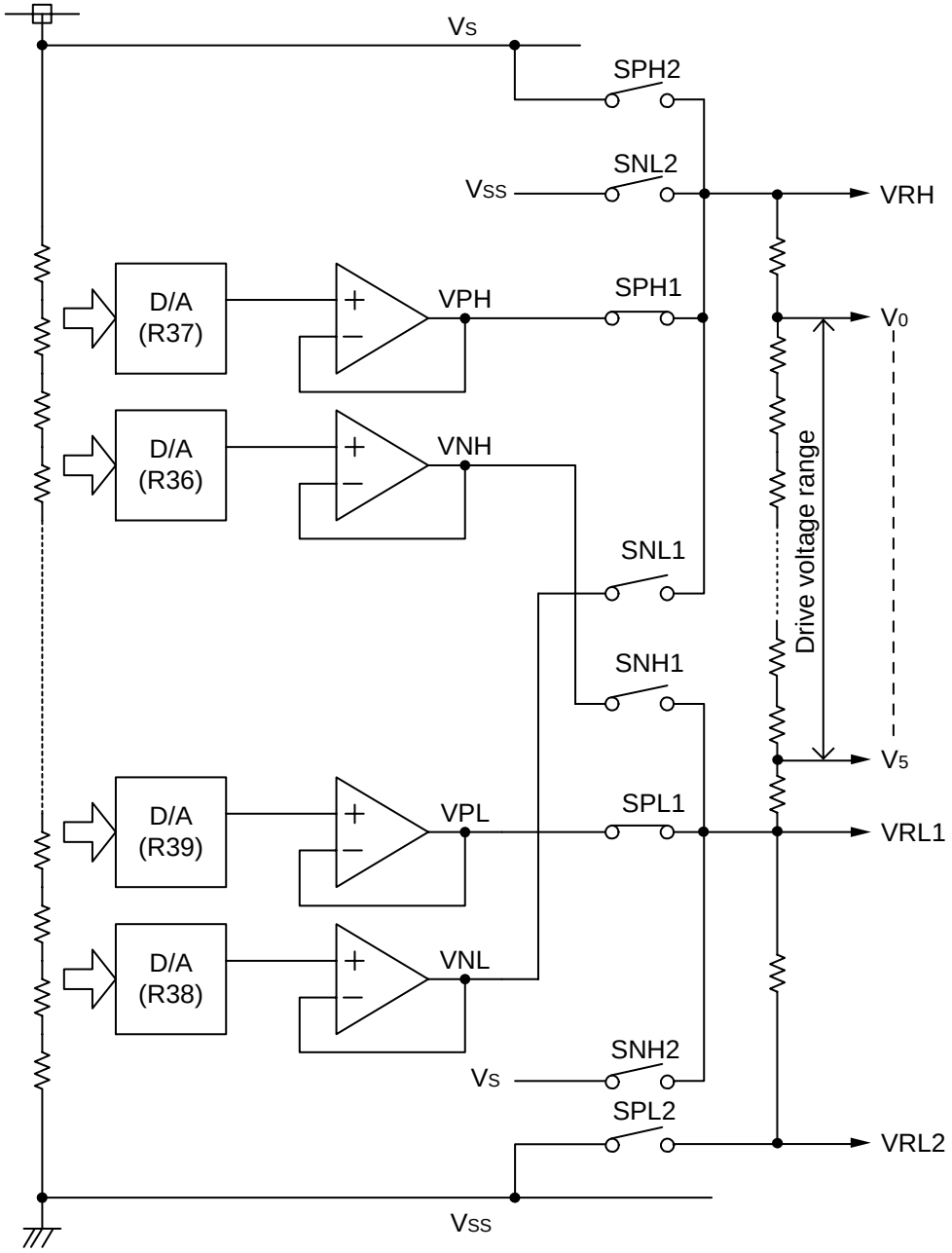


Table 5–12. γ-Curve Correction Circuit (γ-Correction Resistance)

Display Data							Resistance (kΩ)		Output Voltage (V)	
Glay Scale	Dn+5	Dn+4	Dn+3	Dn+2	Dn+1	Dn	r 1	1.587	Positive Voltage	Negative Voltage
0	0	0	0	0	0	0	r 2	1.226	4.901	0.107
1	0	0	0	0	0	1	r 3	2.453	4.824	0.190
2	0	0	0	0	1	0	r 4	3.390	4.671	0.356
3	0	0	0	0	1	1	r 5	4.112	4.459	0.586
4	0	0	0	1	0	0	r 6	4.905	4.202	0.864
5	0	0	0	1	0	1	r 7	1.731	3.895	1.196
6	0	0	0	1	1	0	r 8	1.443	3.787	1.313
7	0	0	0	1	1	1	r 9	1.587	3.697	1.411
8	0	0	1	0	0	0	r 10	1.515	3.598	1.519
9	0	0	1	0	0	1	r 11	1.082	3.503	1.621
10	0	0	1	0	1	0	r 12	1.082	3.436	1.694
11	0	0	1	0	1	1	r 13	1.154	3.368	1.768
12	0	0	1	1	0	0	r 14	1.226	3.296	1.846
13	0	0	1	1	0	1	r 15	1.298	3.219	1.929
14	0	0	1	1	1	0	r 16	1.082	3.138	2.017
15	0	0	1	1	1	1	r 17	0.649	3.070	2.090
16	0	1	0	0	0	0	r 18	0.721	3.030	2.134
17	0	1	0	0	0	1	r 19	0.794	2.985	2.183
18	0	1	0	0	1	0	r 20	0.721	2.935	2.236
19	0	1	0	0	1	1	r 21	0.794	2.890	2.285
20	0	1	0	1	0	0	r 22	0.505	2.840	2.339
21	0	1	0	1	0	1	r 23	0.577	2.809	2.373
22	0	1	0	1	1	0	r 24	0.577	2.773	2.412
23	0	1	0	1	1	1	r 25	0.577	2.737	2.451
24	0	1	1	0	0	0	r 26	0.505	2.701	2.490
25	0	1	1	0	0	1	r 27	0.433	2.669	2.524
26	0	1	1	0	1	0	r 28	0.433	2.642	2.554
27	0	1	1	0	1	1	r 29	0.433	2.615	2.583
28	0	1	1	1	0	0	r 30	0.433	2.588	2.612
29	0	1	1	1	0	1	r 31	0.505	2.561	2.642
30	0	1	1	1	1	0	r 32	0.361	2.529	2.676
31	0	1	1	1	1	1	r 33	0.433	2.507	2.700
32	1	0	0	0	0	0	r 34	0.433	2.480	2.729
33	1	0	0	0	0	1	r 35	0.433	2.453	2.759
34	1	0	0	0	1	0	r 36	0.433	2.426	2.788
35	1	0	0	0	1	1	r 37	0.433	2.399	2.817
36	1	0	0	1	0	0	r 38	0.433	2.372	2.847
37	1	0	0	1	0	1	r 39	0.505	2.344	2.876
38	1	0	0	1	1	0	r 40	0.433	2.313	2.910
39	1	0	0	1	1	1	r 41	0.433	2.286	2.939
40	1	0	1	0	0	0	r 42	0.433	2.259	2.969
41	1	0	1	0	0	1	r 43	0.505	2.232	2.998
42	1	0	1	0	1	0	r 44	0.361	2.200	3.032
43	1	0	1	0	1	1	r 45	0.433	2.178	3.057
44	1	0	1	1	0	0	r 46	0.433	2.151	3.086
45	1	0	1	1	0	1	r 47	0.361	2.124	3.115
46	1	0	1	1	1	0	r 48	0.361	2.101	3.140
47	1	0	1	1	1	1	r 49	0.361	2.078	3.164
48	1	1	0	0	0	0	r 50	0.361	2.056	3.188
49	1	1	0	0	0	1	r 51	0.433	2.033	3.213
50	1	1	0	0	1	0	r 52	0.433	2.006	3.242
51	1	1	0	0	1	1	r 53	0.433	1.979	3.271
52	1	1	0	1	0	0	r 54	0.505	1.952	3.301
53	1	1	0	1	0	1	r 55	0.505	1.921	3.335
54	1	1	0	1	1	0	r 56	0.505	1.889	3.369
55	1	1	0	1	1	1	r 57	0.721	1.858	3.403
56	1	1	1	0	0	0	r 58	0.721	1.812	3.452
57	1	1	1	0	0	1	r 59	0.866	1.767	3.501
58	1	1	1	0	1	0	r 60	0.866	1.713	3.560
59	1	1	1	0	1	1	r 61	1.587	1.659	3.618
60	1	1	1	1	0	0	r 62	2.597	1.560	3.726
61	1	1	1	1	0	1	r 63	2.597	1.398	3.901
62	1	1	1	1	1	0	r 64	12.047	1.235	4.077
63	1	1	1	1	1	1	r 65	7.719	0.482	4.893
					Total			80.000		

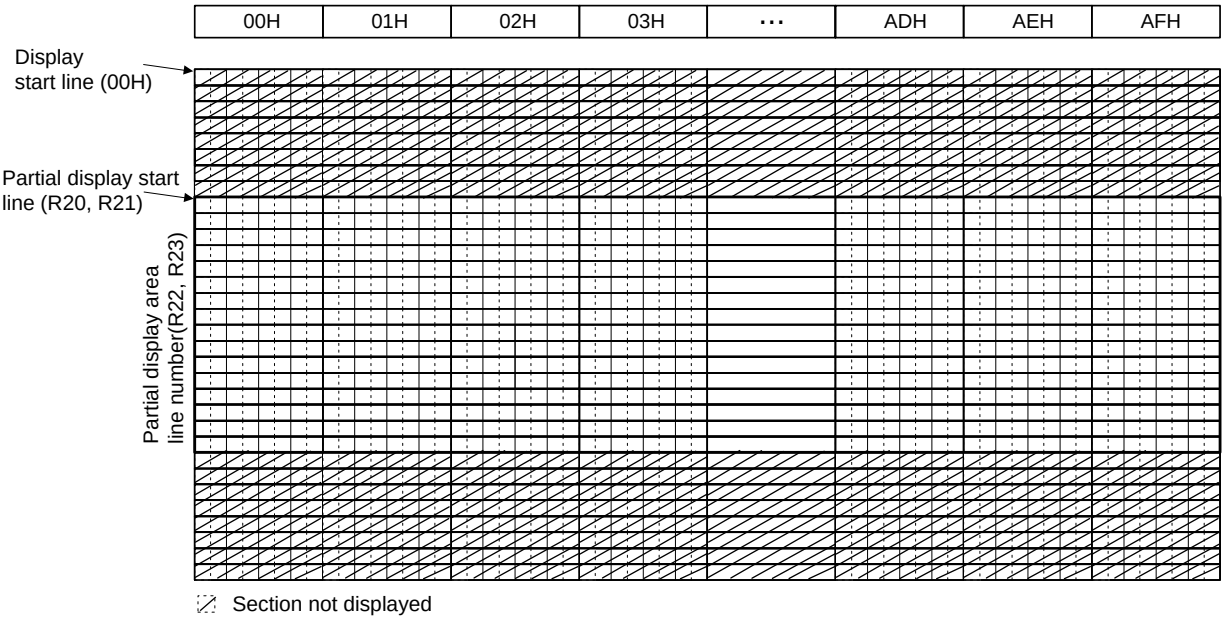
5.10 Partial Display Mode

The μPD161623 is provided with a function that allows sections within the screen to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register (R20, R21), the number of lines in the area to be displayed is set using the partial display area line count register (R22, R23), and the color of the area not to be displayed is set using the partial off area color register (R19). If "1" is set in the partial display area line count registers (R22, R23), the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by R20 and R22 is called Partial 1, and the non-display area indicates by R21 and R23 is called Partial 2. The Partial 2 setting is enabled only when the Partial 1 setting has been performed (when R22 ≠ 0). Therefore, to set only one area as a non-display area, perform only the setting for Partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-color mode.

Figure 5–26. Partial Display Mode



Cautions 1. The "scroll step count register (R17)" command is ignored in the partial display mode.

2. The specified partial areas must not directly overlap, and the Partial 1 area and Partial 2 area must be separated by at least one line. If the areas overlap, only the Partial 1 settings are valid, and partial display is not performed for the Partial 2 area.

3. When setting the partial display areas, be sure to observe the following relationship.

"00H" ≤ R20 (R21)

R22 (R23) ≤ "AFH"

The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode

DISP1 = 1	R0	D_7	<1> Display off
↓			
PGDn setting	R19	D_2 ⋮ D_0	<2> Partial off area color register setting Note1
↓			
Display data overwrite (for partial display)			<3> Display data overwrite Note1
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ⋮ D_0	<4> Partial display area start line setting Note1
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ⋮ D_0	<5> Partial display area line count setting Note1
↓			
DTY = 1, COLOR = 1	R0	D_4, D_2	<6> Partial display mode, 8-color mode Note2
↓			
DISP1 = 0	R0	D_7	<7> Display on

Notes 1. <2> to <5> can be executed in any order.

2. <6> must be executed after <4> and <5> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode

DISP1 = 1	R0	D_7	<1> Display off
↓			
Display data overwrite (for normal display)			<2> Display data overwrite [Note]
↓			
DTY = 0, COLOR = 0	R0	D_4, D_2	<3> Partial display mode, 260,000-color mode [Note]
↓			
DISP1 = 0	R0	D_7	<4> Display on

Note <2> to <3> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)

DISP1 = 1	R0	D_7	<1> Display off
↓			
(Display data overwrite)			<2> Display data overwrite Notes [Note1, 2]
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ⋮ D_0	<3> Partial display area start line setting [Note1]
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ⋮ D_0	<4> Partial display area line count setting [Note1]
↓			
DTY = 1	R0	D_4	<5> Partial display mode [Note3]
↓			
DISP1 = 0	R0	D_7	<6> Display on

Notes 1. <2> to <4> can be executed in any order.

2. Execute <2> only when necessary.

3. <5> must be executed after <3> and <4> have been set.

(4) Partial display setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	00H	Sets Y address 00H
Partial display area line count register (R22, R23)	78H	Sets an area of 120 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	78H	Sets Y address 78H
Partial display area line count register (R22, R23)	78H	Sets an area of 120 lines

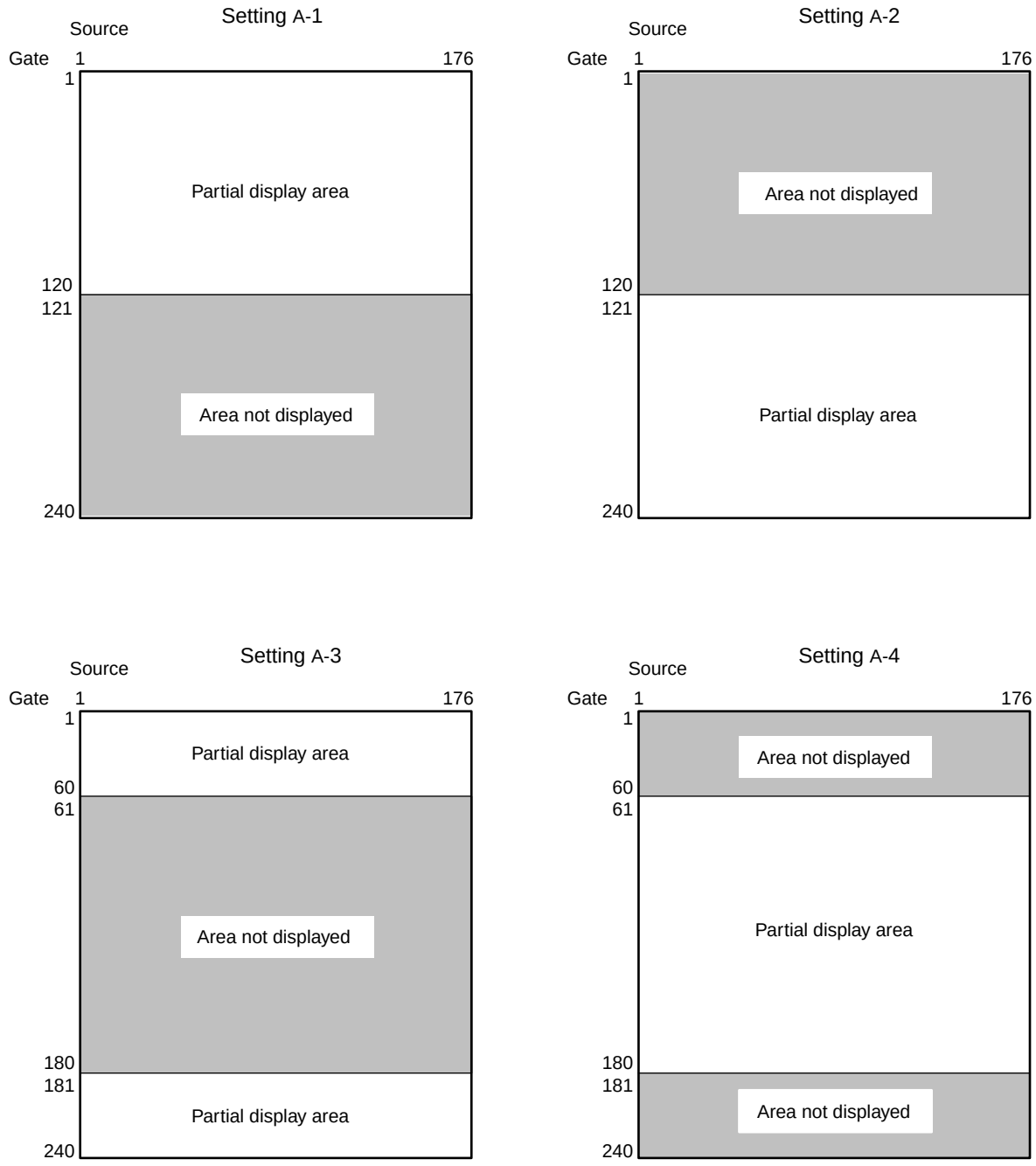
Setting A-3

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	B4H	Sets Y address B4H
Partial display area line count register (R22, R23)	78H	Sets an area of 120 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	3CH	Sets Y address 3CH
Partial display area line count register (R22, R23)	78H	Sets an area of 120 lines

Figure 5–27. Partial Display Setting Examples



5.11 Screen Scroll

The μPD161623 has a screen scroll function. Any area of the screen can be scrolled by using the scroll area start line register (R15), scroll area line count register (R16), and scroll step count register (R17) to set the Y address of the top line of the area to be scrolled, the count of lines of the area to be scrolled, and the scroll step number, respectively.

Note that in partial mode, the screen scroll function is disabled.

Table 5–13. Scroll Area Start Line Register (R15)

SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	Start Line Y Address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
0	0	0	0	0	0	1	1	03H
				⋮				⋮
1	0	1	0	1	1	0	1	EDH
1	0	1	0	1	1	1	0	EEH
1	0	1	0	1	1	1	1	EFH

Table 5–14. Scroll Area Line Count Register (R16)

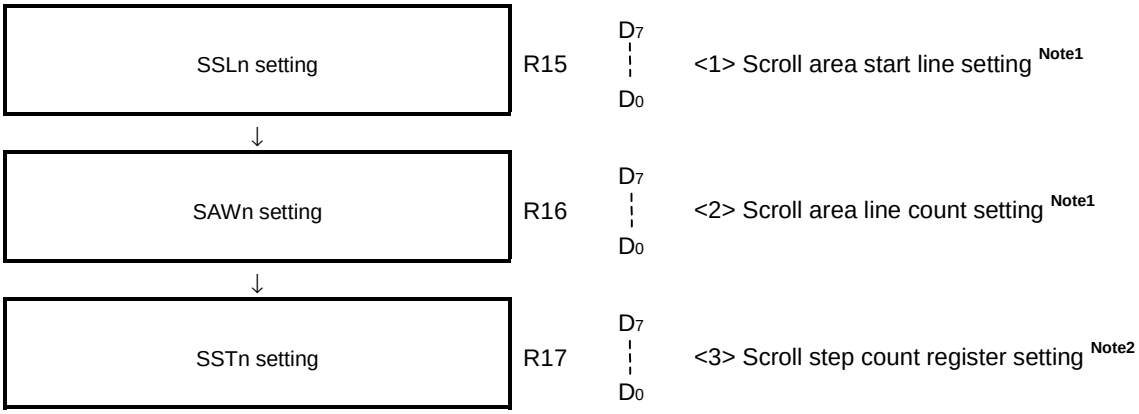
SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	Scroll Area Line Number
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
				⋮				⋮
1	0	1	0	1	1	0	1	238
1	0	1	0	1	1	1	0	239
1	0	1	0	1	1	1	1	240

Table 5–15. Scroll Step Count Register (R17)

SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Step Number
0	0	0	0	0	0	0	0	0 (No scroll)
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
				⋮				⋮
1	0	1	0	1	1	0	1	237
1	0	1	0	1	1	1	0	238
1	0	1	0	1	1	1	1	239

Scrolling must be set using the following sequence.

(1) Recommended scroll sequence



Notes 1. <1> to <2> can be executed in any order.

2. <3> must be executed after <1> and <2> have been set.

Remark Set SSTn to 00H to disable the scroll operation. No particular sequence is required for this.

Cautions 1. If the sum of the values of SSLn and SAWn is 240 (EFH) or over, it is invalid (no scroll operation).

2. Set the step number SSTn so that it does not exceed the line number SAWn. If a value exceeding SAWn is set, it will be invalid (no scroll operation).

(2) Scroll setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	00H	Sets Y address 00H
Scroll area line count register (R16)	EFH	Sets an area of 240 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	00H	Sets Y address 00H
Scroll area line count register (R16)	77H	Sets an area of 120 lines

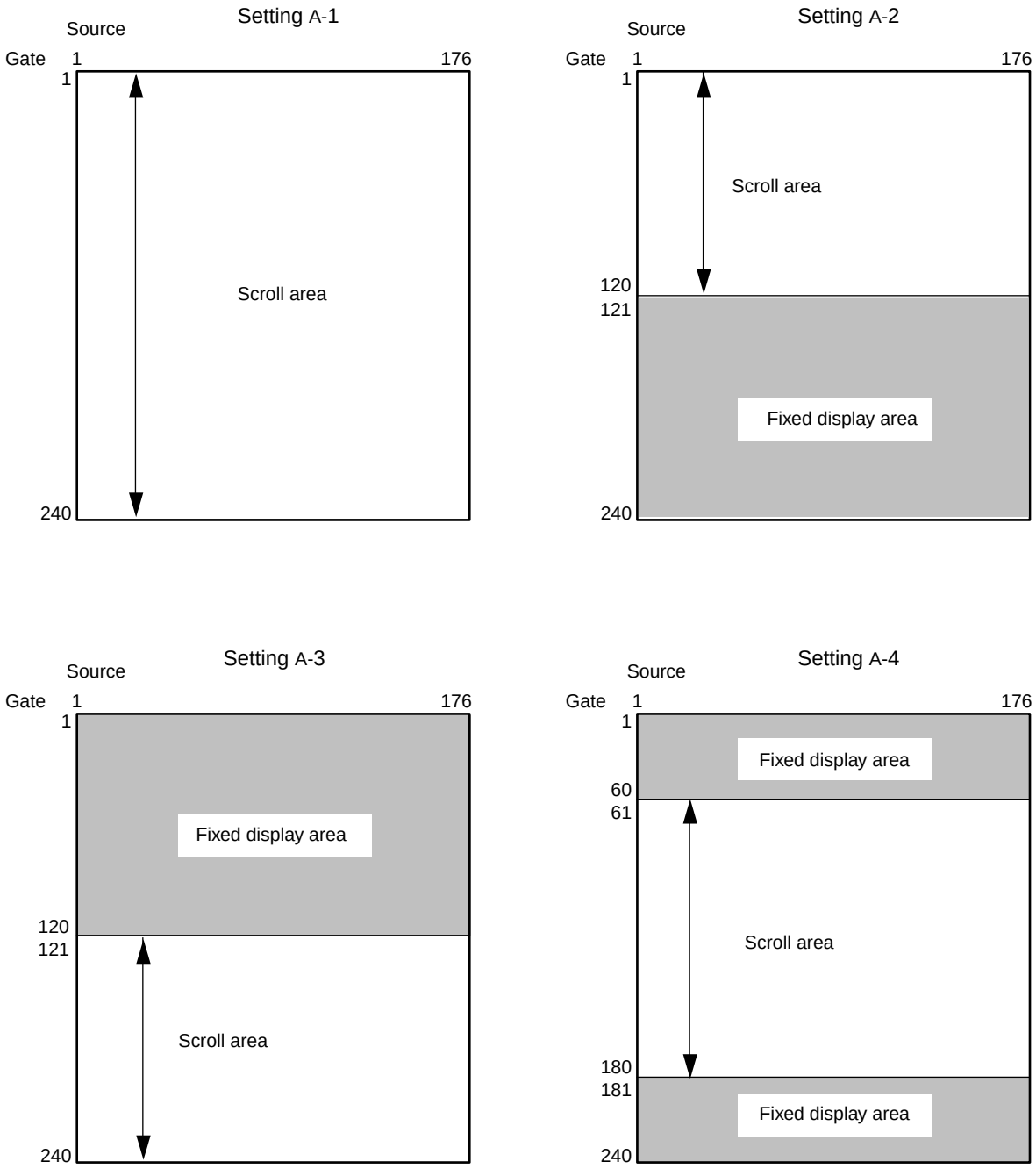
Setting A-3

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	78H	Sets Y address 78H
Scroll area line count register (R16)	77H	Sets an area of 120 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	B4H	Sets Y address B4H
Scroll area line count register (R16)	77H	Sets an area of 120 lines

Figure 5–28. Display Scroll Setting Examples



(3) Scroll setting flowchart example

Start

↓

Scroll area start line register setting (R15)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	1	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 **to** D_0 **are the data for Scroll area start line.**

↓

Scroll area line count register setting (R16)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	1	0	0	0	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 **to** D_0 **are the data for Scroll area line count register.**

↓

Scroll step count register setting (1 step) (R17)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	1	0	0	0	1
	0	0	0	0	0	0	0	1

↓

X address register setting (R6)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	0	1	1	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 **to** D_0 **depend on application condition.**

↓

Y address register setting (R7)

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	0	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 **to** D_0 **depend on application condition.**

↓

Display data Re-write scrolling area 1 (Start)

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} **to** D_0 **are display memory data.**

↓

Display data Re-write scrolling area 2

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} **to** D_0 **are display memory data.**

↓
↓
↓

Display data Re-write scrolling area n (End)

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} **to** D_0 **are display memory data.**

↓

↓

Scroll step count register setting (2 steps) — R17

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	1	0	0	1	0
	0	0	0	0	0	0	0	1

↓

X address register setting — R6

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	0	1	1	0
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

↓

Y address register setting — R7

RS	D_{15} / D_7							D_8 / D_0
L	X	0	0	0	0	1	1	1
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

↓

Display data Re-write scrolling area 1 (Start)

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data Re-write scrolling area 2

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓
↓
↓

Display data Re-write scrolling area n (End)

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

(Repeat)

↓
↓
↓

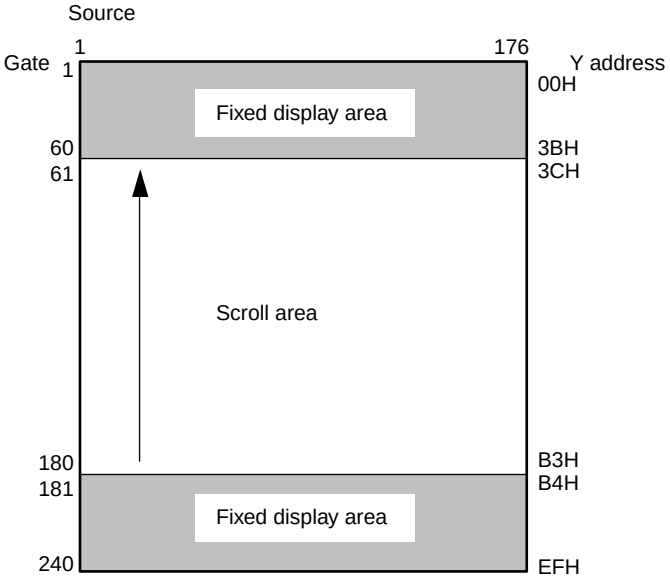
Next transaction

(4) Scroll function example

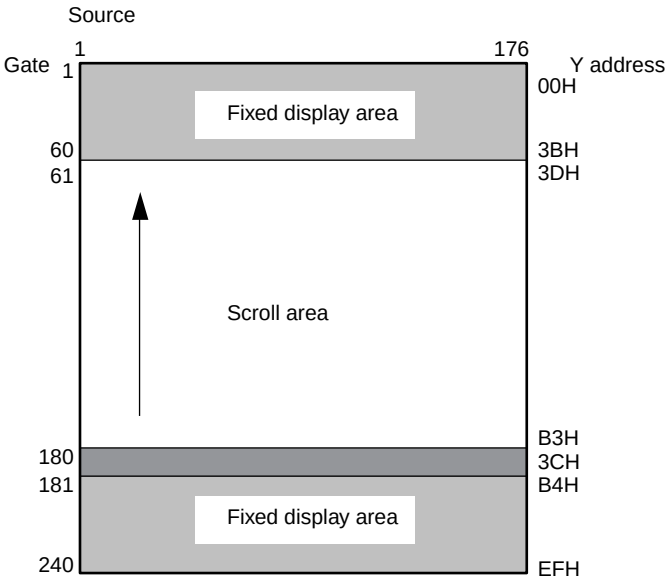
Scroll area start line register (R15): 3CH

Scroll area line count register (R16): 77H

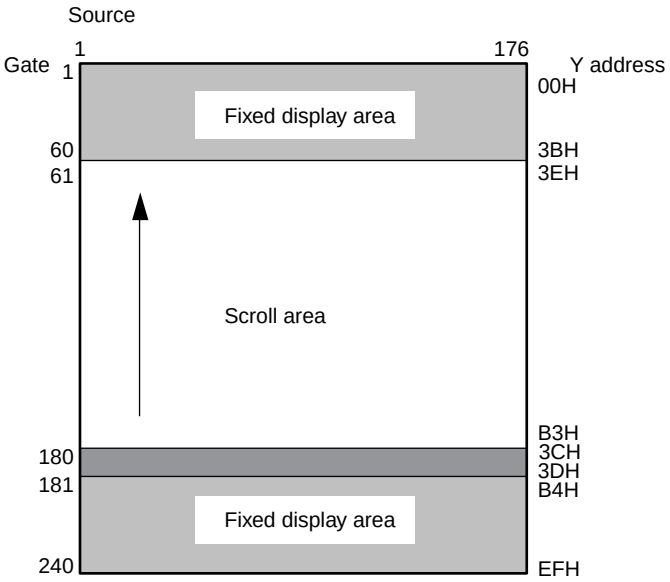
(a) Scroll step count register setting (R17): 00H



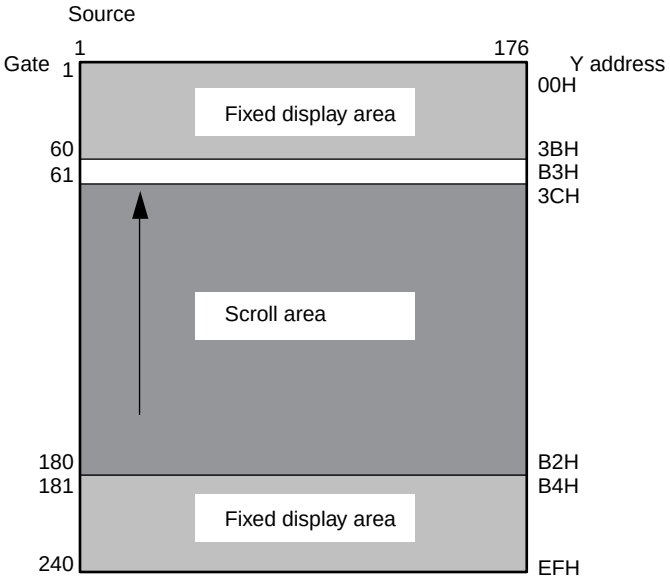
(b) Scroll step count register setting (R17): 01H



(c) Scroll step count register setting (R17): 02H



(d) Scroll step count register setting (R17): 57H



5.12 Stand-by

The μPD161623 has a stand-by function. Input of a stand-by command is acknowledged when the STBY bit of the control register 1 (R0) is set to 1.

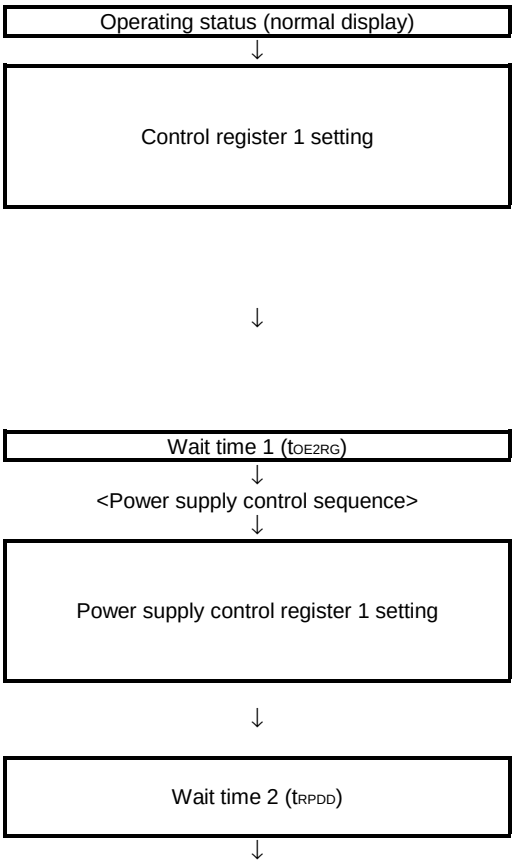
When the stand-by command has been input, the μPD161623 is forcibly placed in the V_{SS} display status, and scans the frame being display to the end. When scanning is complete, all gate outputs are turned on, the charge of the pixel on the TFT panel is decreased to 0, and the output stage amplifier and internal oscillator are stopped.

The stand-by function is valid for only the source driver IC; the gate IC (μPD161641) and power IC (μPD161660) connected to the μPD161623 are not controlled by this function.

After executing the stand-by command, therefore, execute commands that turn off the regulator for the gate IC and power IC an turn off the DC/DC converter.

When the stand-by status is released, turn on the DC/DC converter and the regulator of the gate IC and power IC, and then issue an ordinary operation command (STBY = 0), in the reverse order to which the stand-by command was input.

(1) Stand-by sequence



R0 D_{15} to D_0 Control register 1

RS	D_{15}							D_8
	D_7							D_0
L	0	0	0	0	0	0	0	0
	X	X	D_5	0	**1**	0	0	0

D_7: Don't care
D_6: Don't care
D_4: Normal display mode (not partial display mode)
D_3: Stand-by ON
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.
The source output is automatically fixed to the V_{SS} level by stand-by, so D_7 and D_6 can be set to any value.

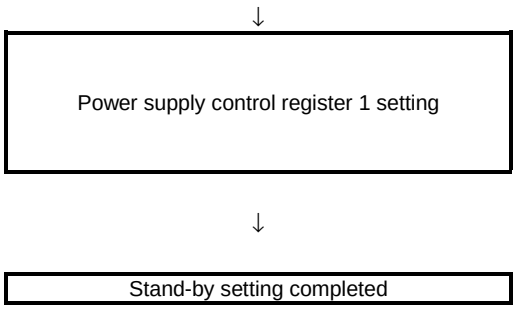
At least one frame period

R25 D_{15} to D_0 Power supply control register 1

RS	D_{15}							D_8
	D_7							D_0
L	0	0	0	1	1	0	0	1
	X	D_6	D_5	D_4	D_3	X	**0**	1

D_6 to D_3 are set in accordance with the usage conditions.
D_1: Power supply IC regulator OFF
D_0: DC/DC converter ON

Although a setting of 0 ns has no negative effect in terms of the device, be sure to finalize the timing after sufficient evaluation with the LCD module.

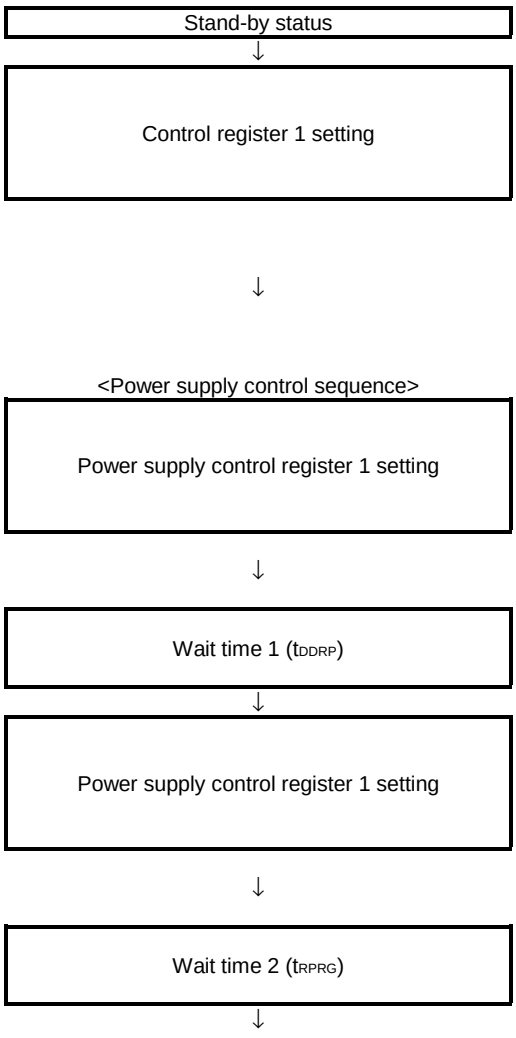


R25 D_{15} to D_0 Power supply control register 1

RS	D_{15}							D_8
	D_7							D_0
L	0	0	0	1	1	0	0	1
	X	D_6	D_5	D_4	D_3	X	0	**0**

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator OFF
D_1: Power supply IC regulator OFF
D_0: DC/DC converter OFF

(2) Stand-by release sequence



R0 D_7 to D_0 Control register 1

RS	D_{15}							D_8
	D_7							D_0
L	X	X	X	X	X	X	X	X
	1	0	D_5	0	**0**	0	0	0

D_7: All data “1” output (normally white: white output)
D_6: Normal display
D_4: Normal display mode (not partial display mode)
D_3: Normal mode (stand-by release)
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.

R25 D_{15} to D_0 Power supply control register 1

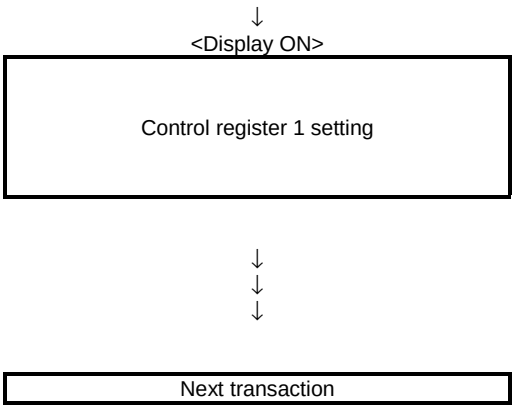
RS	D_{15}							D_8
	D_7							D_0
L	0	0	0	1	1	0	0	1
	X	D_6	D_5	D_4	D_3	X	0	**1**

D_6 to D_3 is set in accordance with the usage conditions.
D_1: Power supply IC regulator OFF
D_0: DC/DC converter ON
t_{DDRP} is the output stable period of the DC/DC converter.
Although a setting of about 50 ms is the target, be sure to finalize the timing after sufficient evaluation with the LCD module.

R25 D_7 to D_0 Power supply control register 1

RS	D_{15}							D_8
	D_7							D_0
L	0	0	0	1	1	0	0	1
	X	D_6	D_5	D_4	D_3	0	**1**	1

D_6 to D_3 is set in accordance with the usage conditions.
D_1: Power supply IC regulator ON
D_0: DC/DC converter ON
t_{RPRG} is the output stable period of the DC/DC converter.
Although a setting of about 20 ms is the target, be sure to finalize the timing after sufficient evaluation with the LCD module.



R0

D_7 to D_0 Control register 1

RS	D_{15} to D_8							
	D_7							D_0
L	0	0	0	0	0	0	0	0
	0	0	D_5	0	**0**	0	0	0

D_7: Normal display (All data "1" output → display ON)
D_6: Normal display
D_4: Normal display mode (not partial display mode)
D_3: Normal mode (stand-by release)
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.

6 RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

Register	Rn	/RESET Pin Note1	Reset Command	Default Value
Control register 1	R0	X	O	A0H
Control register 2	R1	X	O	00H
Data supplement register	R4	X	O	00H
Data access control register	R5	X	O	00H
X address register	R6	X	O	00H
Y address register	R7	X	O	00H
MIN. ·X address register	R8	X	O	00H
MAX. ·X address register	R9	X	O	00H
MIN. ·Y address register	R10	X	O	00H
MIN. ·Y address register	R11	X	O	00H
Display size setting register	R13	X	O	00H
Scroll area start line register	R15	X	O	00H
Scroll area line count register	R16	X	O	00H
Scroll step count register	R17	X	O	00H
Partial off area color register	R19	X	O	00H
Partial 1 display area start line register	R20	X	O	00H
Partial 2 display area start line register	R21	X	O	00H
Partial 1 display area line count register	R22	X	O	00H
Partial 2 display area line count register	R23	X	O	00H
Power supply control register 1	R25	X	O	00H
Power supply control register 2	R26	X	O	00H
VCOM output center value setting register	R29	X	O	00H
Output stage capacity setting register	R30	X	O	00H
γ-reference-voltage generator capacity setting register	R31	X	O	00H
γ-contrast value setting register 1	R36	X	O	00H
γ-contrast value setting register 2	R37	X	O	00H
γ-contrast value setting register 3	R38	X	O	00H
γ-contrast value setting register 4	R39	X	O	00H
★ Pre-charge direction setting data register	R40	X	O	00H
γ-correction input disconnect register	R42	X	O	00H
Calibration register Note2	R45	X	O	01H
★ Pre-charge period supplement pulse setting register	R46	X	O	06H
Output port register	R49	X	O	00H
Interface operating voltage setting register	R114	X	O	00H
Internal logic operating voltage setting register	R115	X	O	00H
Test mode		X	O	00H

Remark O: Default value set, X: Default value not set

Notes 1. The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

2. The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.

$t_{cal} = 1/f_{OSC} \times 37$

7. COMMAND

7.1 Command List

Display data access

RAM access	RS	R/W	Data Bit								
			DB_{17}	DB_{16}	DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9
			DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
18-bit parallel interface											
Display data read 1	1	1	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data write 1	1	0	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9
			D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
16-bit parallel interface (1-pixel/16-bit mode [DTX=L])											
Display data read 2	1	1	**Hi-Z**	**Hi-Z**	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{11}	D_{10}
			D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
Display data write 2	1	0	–	–	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{11}	D_{10}
			D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
16-bit parallel interface (1-pixel / 18-bit mode [DTX=H])											
Display data read 3	1	1	**Hi-Z**	**Hi-Z**	**“0”**	**“0”**	**“0”**	**“0”**	**“0”**	**“0”**	**“0”**
			D_{17} (D_8)	D_{16} (D_7)	D_{15} (D_6)	D_{14} (D_5)	D_{13} (D_4)	D_{12} (D_3)	D_{11} (D_2)	D_{10} (D_1)	D_9 (D_0)
Display data write 3	1	0	**Hi-Z**	**Hi-Z**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
			D_{17} (D_8)	D_{16} (D_7)	D_{15} (D_6)	D_{14} (D_5)	D_{13} (D_4)	D_{12} (D_3)	D_{11} (D_2)	D_{10} (D_1)	D_9 (D_0)
Common											
Status Read	0	1									

Remark Hi-Z: High impedance, X: Invalid data

Caution When the 16-bity parallel interface is used in 1-pixel/18-bit mode (DTX = H), data access of two words per pixel is required.

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 **(1/3)**

Rn	Register	RS	R/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R0	Control register 1	0	0	0	0	0	0	0	0	0	0
				DISP1	DISP0	ADC	DTY	STBY	COLOR	LPM	GSM
R1	Control register 2	0	0	0	0	0	0	0	0	0	1
						VSEL	GSEL	0	0	LTS	INV
R2	–	0	0	0	0	0	0	0	0	1	0
R3	Reset register	0	0	0	0	0	0	0	0	1	1
											RES
R4	Data supplement register	0	0	0	0	0	0	0	1	0	0
										CD12	CD0
R5	Data access control register	0	0	0	0	0	0	0	1	0	1
					BSTR		WAS		**0**	**0**	**0**
R6	X address register	0	0	0	0	0	0	0	1	1	0
				XA_7	XA_6	XA_5	XA_4	XA_3	XA_2	XA_1	XA_0
R7	Y address register	0	0	0	0	0	0	0	1	1	1
				YA_7	YA_6	YA_5	YA_4	YA_3	YA_2	YA_1	YA_0
R8	MIN. ·X address register	0	0	0	0	0	0	1	0	0	0
				XMIN7	XMIN6	XMIN5	XMIN4	XMIN3	XMIN2	XMIN1	XMIN0
R9	MAX. ·X address register	0	0	0	0	0	0	1	0	0	1
				XMAX7	XMAX6	XMAX5	XMAX4	XMAX3	XMAX2	XMAX1	XMAX0
R10	MIN. ·Y address register	0	0	0	0	0	0	1	0	1	0
				YMIN7	YMIN6	YMIN5	YMIN4	YMIN3	YMIN2	YMIN1	YMIN0
R11	MAX. ·Y address register	0	0	0	0	0	0	1	0	1	1
				YMAX7	YMAX6	YMAX5	YMAX4	YMAX3	YMAX2	YMAX1	YMAX0
R12	–	0	0	0	0	0	0	1	1	0	0
R13	Display size setting register	0	0	0	0	0	0	1	1	0	1
											NGO0
R14	–	0	0	0	0	0	0	1	1	1	0
R15	Scroll area start line register	0	0	0	0	0	0	1	1	1	1
				SSL_7	SSL_6	SSL_5	SSL4	SSL3	SSL2	SSL1	SSL0
R16	Scroll area line count register	0	0	0	0	0	1	0	0	0	0
				SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0
R17	Scroll step count register	0	0	0	0	0	1	0	0	0	1
				SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
R18	–	0	0	0	0	0	1	0	0	1	0
R19	Partial off area color register	0	0	0	0	0	1	0	0	1	1
									PGR	PGG	PGB
R20	Partial 1 display area start line register	0	0	0	0	0	1	0	1	0	0
				P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0
R21	Partial 2 display area start line register	0	0	0	0	0	1	0	1	0	1
				P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 **(2/3)**

Rn	Register	RS	R/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R22	Partial 1 display area line count register	0	0	0	0	0	1	0	1	1	0
				P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0
R23	Partial 2 display area line count register	0	0	0	0	0	1	0	1	1	1
				P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0
R24	–	0	0	0	0	0	1	1	0	0	0
R25	Power supply control register 1	0	0	0	0	0	1	1	0	0	1
					BGRS	VCE	VCD2	PVCOM		RGONP	DCON
R26	Power supply control register 2	0	0	0	0	0	1	1	0	1	0
										VCD12	VCD11
R27	–	0	0	0	0	0	1	1	0	1	1
R28	–	0	0	0	0	0	1	1	1	0	0
R29	VCOM output center value setting register	0	0	0	0	0	1	1	1	0	1
				EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0
R30	Output stage capacity setting register	0	0	0	0	0	1	1	1	1	0
				BPL	CI2	CI1	CI0	VCOMC	SF2	SF1	SF0
R31	γ-reference-voltage generator capacity setting register	0	0	0	0	0	1	1	1	1	1
				WHP	WI2	WI1	WI0	BHP	BI2	BI1	BI0
R32	–	0	0	0	0	1	0	0	0	0	0
R33	–	0	0	0	0	1	0	0	0	0	1
R34	–	0	0	0	0	1	0	0	0	1	0
R35	–	0	0	0	0	1	0	0	0	1	1
R36	γ-contrast value setting register 1	0	0	0	0	1	0	0	1	0	0
				GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0
R37	γ-contrast value setting register 2	0	0	0	0	1	0	0	1	0	1
				GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0
R38	γ-contrast value setting register 3	0	0	0	0	1	0	0	1	1	0
				GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0
R39	γ-contrast value setting register 4	0	0	0	0	1	0	0	1	1	1
				GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0
R40	Pre-charge direction setting data register	0	0	0	0	1	0	1	0	0	0
				RDTP3	RDTP2	RDTP1	RDTP0	RDTN3	RDTN2	RDTN1	RDTN0
R41	–	0	0	0	0	1	0	1	0	0	1
R42	γ-correction input disconnect register	0	0	0	0	1	0	1	0	1	0
											GHSW
R43	–	0	0	0	0	1	0	1	0	1	1

18-bit parallel interface mode, DB_{17}, DB_{16} = 0 **(3/3)**

Rn	Register	RS	R/W	Data Bit							
				DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8
				DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
R44	–	0	0	0	0	1	0	1	1	0	0
R45	Calibration register	0	0	0	0	1	0	1	1	0	1
											OC
R46	Pre-charge period supplement pulse setting register	0	0	0	0	1	0	1	1	1	0
					PLIM6	PLIM5	PLIM4	PLIM3	PLIM2	PLIM1	PLIM0
R47	–	0	0	0	0	1	0	1	1	1	1
R48	–	0	0	0	0	1	1	0	0	0	0
R49	Output port register	0	0	0	0	1	1	0	0	0	1
				OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
R50	–	0	0	0	0	1	1	0	0	1	0
R51	–	0	0	0	0	1	1	0	0	1	1
R52	–	0	0	0	0	1	1	0	1	0	0
R53	–	0	0	0	0	1	1	0	1	0	1
R54	–	0	0	0	0	1	1	0	1	1	0
R55	–	0	0	0	0	1	1	0	1	1	1
R56	–	0	0	0	0	1	1	1	0	0	0
R57	–	0	0	0	0	1	1	1	0	0	1
R58	–	0	0	0	0	1	1	1	0	1	0
R59	–	0	0	0	0	1	1	1	0	1	1
R60	–	0	0	0	0	1	1	1	1	0	0
R61	–	0	0	0	0	1	1	1	1	0	1
R62	–	0	0	0	0	1	1	1	1	1	0
R63	–	0	0	0	0	1	1	1	1	1	1
R114	Interface operating voltage setting register	0	0	0	1	1	1	0	0	1	0
										RTSC1	RTSC0
R115	Internal logic operating voltage setting register	0	0	0	1	1	1	0	0	1	1
										RTSL1	RTSL0

7.2 Command Explanation

(1/8)

Register	Bit	Symbol	Function
R0	D_7	DISP1	This command performs the same output as when all data is 1, independently of the internal RAM data (white display in the case of normally white). This command is executed, after it has been transferred, when the next line isoutput. 0: Normal operation 1: Ignores data of RAM and outputs all data as 1. DISP1 takes precedence over DISP0. When DISP1 = H, DISP0 = H is ignored.
	D_6	DISP0	This command performs the same output as when all data is 0, independently of the internal RAM data (black display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 0.
	D_5	ADC	Column address direction This command can be used to select the direction of source driver output. For more detail, refer to **5.2.3 Column address circuit**.
	D_4	DTY	This pin selects the partial function. When the partial function s selected in the 260,000-color mode, set the partial-OFF area-color selection register (R27) to 00H. In the 8-color mode, the partial OFF area color can be set to any value from 00H to 07 H. The power consumption cannot be reduced with the partial function. To reduce the power consumption, select the 8-color mode. This command is executed following transfer from the time the next line data is output. 0: Normal display mode 1: Partial display mode
★	D_3	STBY	This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed and the amplifiers at each output stage and the operation of internal oscillation circuit are stopped. However, stand-by control cannot be performed for the power supply ICs (μPD161660 and others) connected to μPD161623. Therefore, after executing the stand-by function using this bit, set both the regulator for the power supply IC to off and set the DC/DC converter to OFF. For the sequence, refer to the data sheets of the power supply IC. Note that when releasing stand-by, perform the opposite operation, i.e., after setting the DC/DC converter to ON and setting the regulators of the power supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (Display read off from RAM, stop both OSC and VCOM, display off = entire data is output as 1)
	D_2	COLOR	This pin switches the 260,000-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output stage. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the time the next line data is output. 0: 260,000-color mode (18-bits/pixels) 1: 8-color mode (3-bits/pixels)

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Register	Bit	Symbol	Function
R0	D_1	LPM	This bit is used when setting the power supply IC (μPD161660) to the low-power mode. When the low-power mode is selected, the LPMP pin signal change from low to high (output changes immediately following command execution.). The LPMP pin must be connected to the LPM pin of the power supply IC. 0: Normal 1: Low power mode
	D_0	GSM	Sets output of the gate scanning signal during partial display. When 1 is selected, gate scanning of the line set in the partial non-display area is stopped. 0: Normal mode 1: Stops gate scanning in partial non-display area
R1	D_5	VSEL	Sets the potential of the pre-charge output of the LCD driver. The maximum/minimum output potential of the pre-charge output is: 0: Maximum output level of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL) 1: Partial voltage (outputs V_S and V_{SS}) IF VSEL = 0, V_S or V_{SS} is automatically output as the pre-charge output.
	D_4	GSEL	Sets the maximum/minimum output voltage of the γ–correction register. If the internal γ-output adjustment circuit is selected, the maximum/minimum output potential of the γ-correction register is: 0: Supply voltage (outputs V_S and V_{SS}). 1: Voltage of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL) 8-color mode (3 bits/pixels)
	D_1	LTS	Selects set time of calibration. The calibration function adjusts the frame frequency by setting time of one line. This command can select the set time of a line from the following: 0: 1 line time = t_{cal} 1: 1 line time = t_{cal} x 2 (t_{cal}: Calibration set time1 = 1 ÷ Frame frequency ÷ Number of displayed lines)
	D_0	INV	This bit selects between the line inversion function and the frame inversion function. The mode selected by this command is executed from the start of the next scan after the gate scan in progress when this command was executed has completed 176 lines. 0: Line inversion 1: Frame inversion
R3	D_0	RES	Command reset function. Be sure to execute this bit after power ON. Command reset automatically clears this bit following execution (RES = 1). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting. 0: Normal operation 1: Command reset
R4	D_1	CD12	When using the 1-pixel/16-bit mode (DTX = L) and the 18-bit parallel interface, when the data from the CPU is stored in the display RAM, this register supplements data (display RAM data: D_{12}, D_0) for the two bits of deficient data using the set data and writes 18-bit data to the display RAM. For details, refer to **5.1.2 Selection of data transfer mode**. CD12: Display RAM data D_{12} is supplemented CD0: Display RAM data D_0 is supplemented
	D_0	CD0	

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R5</td><td>D_6</td><td>BSTR</td><td>Sets the write mode for writing data to the display RAM.
If the high-speed RAM write mode is selected, data is written to the display RAM in 2-pixel units inside the μPD161623. When selecting the high-speed RAM write mode, be sure to write data to the display RAM in 2-pixel units.
0: Normal write mode (18-bit access: 4 MHz MAX.)
1: High-speed RAM write mode (36-bit access: 8 MHz MAX.)</td></tr>
<tr><td></td><td>D_4</td><td>WAS</td><td>Window access mode setting
When the window access mode is set, the address is incremented/decremented only in the range set by the MIN. ·X address setting register (R8), MAX. ·X address setting register (R9), MIN. ·Y address setting register (R10), and MAX. ·Y address setting register (R11).
0: Normal operation
1: Window access mode</td></tr>
<tr><td>R6</td><td>D_7 to D_0</td><td>XAn</td><td>This register sets the X address of the display RAM.
Set a value between 00H and AFH.</td></tr>
<tr><td>R7</td><td>D_7 to D_0</td><td>YAn</td><td>This register sets the Y address of the display RAM.
Set a value between 00H and EFH.</td></tr>
<tr><td>R8</td><td>D_7 to D_0</td><td>XMINn</td><td>Sets the minimum value of the X address in the window access mode.
The X address is incremented up to the maximum value set by the MAX. ·X address register (R9), and then initialized to the address value set by this command.
Set this register to 00H to AEH.</td></tr>
<tr><td>R9</td><td>D_7 to D_0</td><td>XMAXn</td><td>Sets the maximum value of the X address in the window access mode.
The X address is incremented up to the maximum value set by the MIN. ·X address register (R8), and then initialized to the address value set by this command.
Set this register to 01H to AFH.</td></tr>
<tr><td>R10</td><td>D_7 to D_0</td><td>YMINn</td><td>Sets the minimum value of the T address in the window access mode.
The Y address is incremented up to the maximum value set by the MAX. ·Y address register (R11), and then initialized to the address value set by this command.
Set 00H to EEH.</td></tr>
<tr><td>R11</td><td>D_7 to D_0</td><td>YMAXn</td><td>Sets the maximum value of the Y address in the window access mode.
The Y address is incremented up to the address value set by this command, and then initialized to the minimum address value set by the MIN. ·Y address register (R10).
Set 01H to EFH.</td></tr>
<tr><td>R13</td><td>D_0</td><td>NGO0</td><td>Selects output number (gate scan) of gate driver.
<table><tr><th>NGO0</th><th>Gate Output Number</th></tr><tr><td>0</td><td>240-gate outputs</td></tr><tr><td>1</td><td>220-gate outputs</td></tr></table></td></tr>
<tr><td>R15</td><td>D_7 to D_0</td><td>SSLn</td><td>Scroll area start line register (00H to EFH)
When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R16) is scrolled up by the number of steps set by the scroll step count register (R17), starting from the line set by this command.</td></tr>
<tr><td>R16</td><td>D_7 to D_0</td><td>SAWn</td><td>Scroll area line count register (00H to EFH)
When the screen is scrolled, the screen of the number of lines set by this command is scrolled up by the number of steps set by the scroll step count register (R17), starting from the line set by the scroll area start line register (R15).</td></tr>
</table>

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Register	Bit	Symbol	Function
R17	D_7 to D_0	SSTn	Scroll step count register (00H to EFH) When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R16) and the scroll step count register (R17) is scrolled up by the number of steps set by this command. Note that because this command is invalid in the partial display mode, the scroll function cannot be used.
R19	D_2	PGR	Partial off area color register Sets the color of the screen other than the partial display area during partial display (R0: DTY = 1). One of eight colors can be selected (RGB: 1 bit each) as the off color. The relationship between each color data and the bits of this register is as follows. This relationship is not dependent upon the value of ADC. PGR: R OFF= 0, ON = 1 PGG: G OFF= 0, ON = 1 PGB: B OFF= 0, ON = 1
	D_1	PGG	
	D_0	PGB	
R20	D_7 to D_0	P1SLn	Partial1 display area start line register (00H to EFH) During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 1 display area line count register (R22) is the partial 1 display area.
R21	D_7 to D_0	P2SLn	Partial2 display area start line register (00H to EFH) During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 2 display area line count register (R23) is the partial 2 display area.
R22	D_7 to D_0	P1AWn	Partial1 display area line count register (00H to EFH) An area starting from the line set by the partial 1 display area start register (R20) and ending as set by this command is the partial 1 display area. If this register is 0, the values of the partial 2 display area start line register (R29) and the partial 2 display area line count register (R31) are not valid.
R23	D_7 to D_0	$P2AW_n$	Partial 2 display area line count register (00H to EFH) An area starting from the line set by the partial 2 display area start register (R21) and ending as set by this command is the partial 2 display area. If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R21) and partial 2 display area line count register (R23) are not valid.
R25	D_6	BGRS	This pin selects whether to use the internal power supply or an external power supply (input from the BRGIN pin) for generation the common center voltage output from the VCOM pin. 0: The internal power supply is selected as the VCOM power supply 1: Input from the external power supply BGRIN is selected as the BCOM power supply
	D_5	VCE	Selects the V_O output level of the power supply IC (μPD161660). The V_{CE} pin of the μPD161623 and the V_{CE} pin of the power supply IC must be connected. 0: The Vo high-level booster voltage level is V_{DD2} minus 1 level 1: The Vo high-level booster voltage level is the same level as V_{DD2}
	D_4	VCD2	Selects the V_{DD2} output level of the power supply IC (μPD161660). The V_{CD2} pin of the μPD161623 and the V_{CD2} pin of the power supply IC must be connected. 0: $V_{DD2} = V_{CD} \times 2$ 1: $V_{DD2} = V_{CD} \times 3$
	D_3	PVCOM	Selects the voltage supplied to the VCOM output circuit. 0: VCOM output circuit power supply, V_{DD2} 1: VCOM output circuit power supply, V_S

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="2">R25</td><td>D_1</td><td>RGONP</td><td>Switches the internal DC/DC converter of the power supply IC (μPD161660) ON/OFF.
When OFF is selected, a low level is output from the RGONP pin, and when ON is selected, a high level is output from the RGONP pin.
The RGONP pin of this IC and the RGONP pin of the power supply IC must be connected.
0: Regulators of power supply IC (V_T, V_S) are OFF
1: Regulators of power supply IC (V_T, V_S) are ON</td></tr>
<tr><td>D_0</td><td>DCON</td><td>Switches the internal DC/DC converter of the power supply IC (μPD161660) ON/OFF.
When OFF is selected, a low level is output from the DCON pin, and when ON is selected, a high level is output from the DCON pin.
The DCON pin of the μPD161623 and the DCONP pin of the power supply IC must be connected.
0: DC/DC converter is OFF
1: DC/DC converter is ON</td></tr>
<tr><td rowspan="2">R26</td><td>D_1</td><td>VCD12</td><td rowspan="2">Performs booster control for the DC/DC converter in the power supply IC (μPD161660)
The data set with this bit is output from the VCD11 pin and the VCD12 pin.
The VCD11 pin and VCD12 pin of the μPD161623 must be connected to the VCD11 pin and the VCD12 pin of the power supply IC.
VCD12, VCD11 = 0, 0: $V_{DD2} = V_{DC} \times 4$
= 0, 1: $V_{DD2} = V_{DC} \times 5$
= 1, 0: $V_{DD2} = V_{DC} \times 6$
= 1, 1: $V_{DD2} = V_{DC} \times 7$</td></tr>
<tr><td>D_0</td><td>VCD11</td></tr>
<tr><td>R29</td><td>D_7 to D_0</td><td>EVn</td><td>Sets the D/A converter circuit used to adjust the voltage of the reference voltage generator circuit (VBGR) input to the voltage regulator that sets the center value of the panel common drive output. The D/A converter divides the constant voltage generated by the reference voltage generator (VBGR) by 256, and one level can be selected between VBGR and V_{SS} by setting this command.
For more detail, refer to 5.5 Common Adjustment Circuit and 5.8 D/A Converter Circuit.</td></tr>
<tr><td rowspan="2">R30</td><td>D_7</td><td>BPL</td><td>Switched the capacity of the γ-correction circuit reference voltage generation amplifiers on the side not being used (VPH, VPL, VNH, VNL) to the minimum value based on the polarity inversion timing in order to reduce the current consumption.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal
1: Reference voltage generation amplifier capacity switch drive</td></tr>
<tr><td>D_6 to D_4</td><td>CIn</td><td>Sets the bias current of the amplifier for setting the panel's COMMON drive waveform center value (VCOM), as shown in the table below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>CI2</th><th>CI1</th><th>CI0</th><th>VCOM Center Value Setting Amplifier Bias Current Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R30</td><td>D_3</td><td>VCOMC</td><td>Selects whether to use the amplifier for setting the panel's COMMON drive waveform center value (VCOM) or not.
This amplifier can be used under conditions such as when an external COMMON drive circuit is being used.
0: VCOM amplifier operating
1: VCOM amplifier stopped</td></tr>
<tr><td></td><td>D_2 to D_0</td><td>SFn</td><td>Sets the capacity of the source output (Y_1 to Y_{528}), as shown in the table below.
Determine the output capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>SF2</th><th>SF1</th><th>SF0</th><th>Source Output Bias Current Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.15 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.25 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.10 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0.30 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0.40 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
</table></td></tr>
<tr><td>R31</td><td>D_7</td><td>WHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output stage capacity: twice that of normal mode)</td></tr>
<tr><td></td><td>D_6 to D_4</td><td>WIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
<table>
<tr><th>WI2</th><th>WI1</th><th>WI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr>
</table></td></tr>
<tr><td></td><td>D_3</td><td>BHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output stage capacity: twice that of normal mode)</td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R31</td><td>D_2 to D_0</td><td>BIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>BI2</th><th>BI1</th><th>BI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr>
</table></td></tr>
<tr><td>R36</td><td>D_7 to D_0</td><td>GPHn</td><td>Sets the voltage value of the black level of positive polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R37</td><td>D_7 to D_0</td><td>GNHn</td><td>Sets the voltage value of the white level of negative polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R38</td><td>D_7 to D_0</td><td>GPLn</td><td>Sets the voltage value of the white level of positive polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R39</td><td>D_7 to D_0</td><td>GNLn</td><td>Sets the voltage value of the white level of positive polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td rowspan="2">R40</td><td>D_7 to D_4</td><td>RDTPn</td><td>Sets the data value at which the pre-charge direction is switched during positive-polarity drive.
The value set to RDTPn corresponds to the higher 4bits of display RAM data DB_n (6 bits for each of RFB), as shown below.
<table>
<tr><th></th><th>RDTP3</th><th>RDTP2</th><th>RDTP1</th><th>RDTP0</th></tr>
<tr><td>Dot 1 (R)</td><td>D_{17}</td><td>D_{16}</td><td>D_{15}</td><td>D_{14}</td></tr>
<tr><td>Dot 2 (G)</td><td>D_{11}</td><td>D_{10}</td><td>D_9</td><td>D_8</td></tr>
<tr><td>Dot 3 (B)</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td></tr>
</table></td></tr>
<tr><td>D_3 to D_0</td><td>RDTNn</td><td>Sets the data value at which the pre-charge direction is switched during negative-polarity drive.
The value set to RDTNn corresponds to the higher 4 bits of display RAM data DB_n (6 bits for each of RGB), as shown below.
<table>
<tr><th></th><th>RDTN3</th><th>RDTN2</th><th>RDTN1</th><th>RDTN0</th></tr>
<tr><td>Dot 1 (R)</td><td>D_{17}</td><td>D_{16}</td><td>D_{15}</td><td>D_{14}</td></tr>
<tr><td>Dot 2 (G)</td><td>D_{11}</td><td>D_{10}</td><td>D_9</td><td>D_8</td></tr>
<tr><td>Dot 3 (B)</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td></tr>
</table></td></tr>
<tr><td>R42</td><td>D_0</td><td>GHSW</td><td>Controls the γ-correction voltage input pins (V_0 to V_5) and the switch for connecting the μPD161623 internal γ-correction resistor.
0: Switch OFF (disconnected)
1: Switch ON (connected)</td></tr>
<tr><td>R45</td><td>D_0</td><td>OC</td><td>This bit is used for calibration.
The time from calibration start command execution until calibration stop command execution becomes the time for 1 line.
0: Calibration stop
1: Calibration start</td></tr>
</table>

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	Register	Bit	Symbol	Function
	R46	D_6 to D_0	PLIMn	Sets the clock count for the pre-charge period. The value written to this register is set as the clock count (1/f_{OCS}) of the pre-charge period. For details, refer to **5.4.1 Dispaly timing**
	R49	D_7 to D_0	OPn	Output port (OP_7 to OP_0) write When after the output port register is specified in the index register, writing to the output port register is performed, the values written to the OP_7 to OP_0 pins are output.
★	R114	D_1, D_0	RTSCn	Selects the optimum internal circuit operation based on the operating voltage of the interface circuits. To set by this register, we recommend as follow setting. RTSC1: 0, RTSC0: 1 **Caution Always set this register and internal logic operating voltage setting register (R115) to the same value.**
★	R115	D_1, D_0	RTSLn	Selects the optimum internal circuit operation based on the operating voltage of the internal logic circuits. To set by this register, we recommend as follow setting. RTSC1: 0, RTSC0: 1 **Caution Always set this register and interface operating voltage setting register (R114) to the same value.**

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_S	–0.5 to +6.5	V
Power supply voltage	V_{DD1}	–0.5 to V_{DD2} + 0.5	V
Power supply voltage	V_{DD2}	–0.5 to +4.0	V
Power supply voltage for γ-curve correction	V_0 to V_5	–0.5 to V_S + 0.5	V
Input voltage	V_I	–0.5 to V_{DD2} + 0.5	V
Input current	I_I	±10	mA
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_S	4.3	5.0	5.5	V
	V_{DD1}	1.7	1.8	V_{DD2}	V
	V_{DD2}	2.5	2.7	3.6	V
Input voltage	V_{I1} **Note1**	0		V_{DD2}	V
	V_{I2} **Note2**	0		V_{DD1}	V

Notes 1. Pins of V_{DD1} power supply system: PSX, C86, T_{OUT0} to T_{OUT17}, OP_0 to OP_7, LPMP, GOE_1, GOE_2, GSTB, GCLK, DCON, RGONP, V_{CD11}, V_{CD12}, V_{CD2}, V_{CE}, OSC_{SEL}, $TEST_{IN}$, TSTRTST, TSTVIHL, TOSCI

2. Pins of V_{DD2} power supply system: /CS, /RD (E), /WR (R,/W), D_0 to D_{17}, RS, /RESET, OSC_{IN}

Electrical Specifications (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = 1.7 V to V_{DD2}, V_{DD2} = 2.5 to 3.6 V, V_S = 4.3 to 5.5 V)

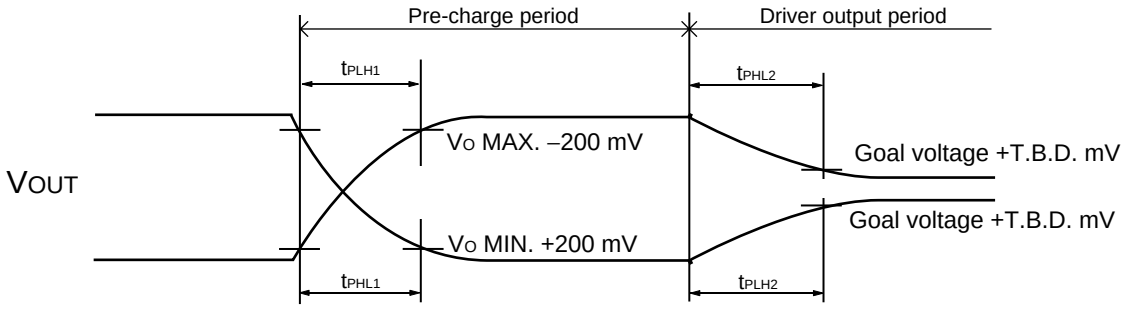
Parameter	Symbol	Condition	Specification			Unit
			MIN.	TYP. Note1	MAX.	
High level input voltage	V_{IH1}	V_{DD2}	0.8 V_{DD2}			V
	V_{IH2}	V_{DD1}	0.8 V_{DD1}			V
Low level input voltage	V_{IL1}	V_{DD2}			0.2 V_{DD2}	V
	V_{IL2}	V_{DD1}			0.2 V_{DD1}	V
High level output voltage	V_{OH1}	V_{DD2}, I_{OUT} = –100 μA	0.9 V_{DD2}			V
	V_{OH2}	V_{DD1}, I_{OUT} = –1 mA	0.8 V_{DD1}			V
	V_{OH3}	VCOUT1, VCOUT2, I_{OUT} = –100 μA	0.9 V			V
Low level output voltage	V_{OL1}	V_{DD2}, I_{OUT} = 100 μA			0.1 V_{DD2}	V
	V_{OL2}	V_{DD1}, I_{OUT} = 1 mA			0.2 V_{DD1}	V
	V_{OL3}	VCOUT1, VCOUT2, I_{OUT} = 100 μA			0.1 V_S	V
VCOM output voltage	V_{COMH}	I_{SOURCE} = 100 μA	VCOM – 0.3			V
	V_{COML}	I_{SINK} = –100 μA			VCOM – 0.3	V
High level input current	I_{IH1}	Except D_0 to D_{17}			1	μA
Low level input current	I_{IL1}	Except D_0 to D_{17}			–1	μA
High level leakage current	I_{LIH}	D_0 to D_{17}			10	μA
Low level leakage current	I_{LIL}	D_0 to D_{17}			–10	μA
High level driver output current	I_{VOH}	V_X = 3.5 V, V_{OUT} = 4.5 V, V_S = 5.0 V Note2			–100	μA
Low level driver output current	I_{VOL}	V_X = 2.0 V, V_{OUT} = 1.0 V, V_S = 5.0 V Note2	150			μA
VCOM common output voltage fluctuation parameter	ΔV_{COM}		–10		10	%
Current consumption	I_{DD1}	V_{DD1} (when non-access CPU)		0.1	2	μA
	I_{DD2}	V_{DD2} (when non-access CPU)		200	350	μA
	I_{STBY}	Stand-by mode, V_{DD2} pin		0.1	10	μA
★	I_S	260,000-color mode Note3		650	1250	μA
		8-color mode Note3		50	200	μA
Driver output Current (pre-charge)	I_{VOH}	V_{OUT} = V_S – 0.1 V, V_S = 5.0 V Note2			–5	μA
	I_{VOL}	V_{OUT} = V_{SS} + 0.1 V, V_S = 5.0 V Note2	2			μA
Output voltage deviation	ΔV_{O1}	V_O = 1.3 V to V_S – 1.3 V	–20		+20	mV
	ΔV_{O2}	V_O = 0.3 to 1.3 V V_O = V_S – 1.3 V to V_S – 0.3 V	–30		+20	mV
Output voltage period	V_O	Input data: H to H	V_{SS} + 0.2		V_S – 0.2	V

Notes 1. TYP. values are reference values when T_A = 25°C

2. V_X refers to the output voltage of analog output pins Y_1 to Y_{528}.
V_{OUT} refers to the voltage applied to analog output pins Y_1 to Y_{528}.

★ **3.** Frame frequency: 60 Hz, line inversion mode select, dot checkerboard input pattern, no load.

Switching characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = 1.7 V to V_{DD2}, V_{DD2} = 2.5 to 3.6 V, V_S = 4.3 to 5.5 V)

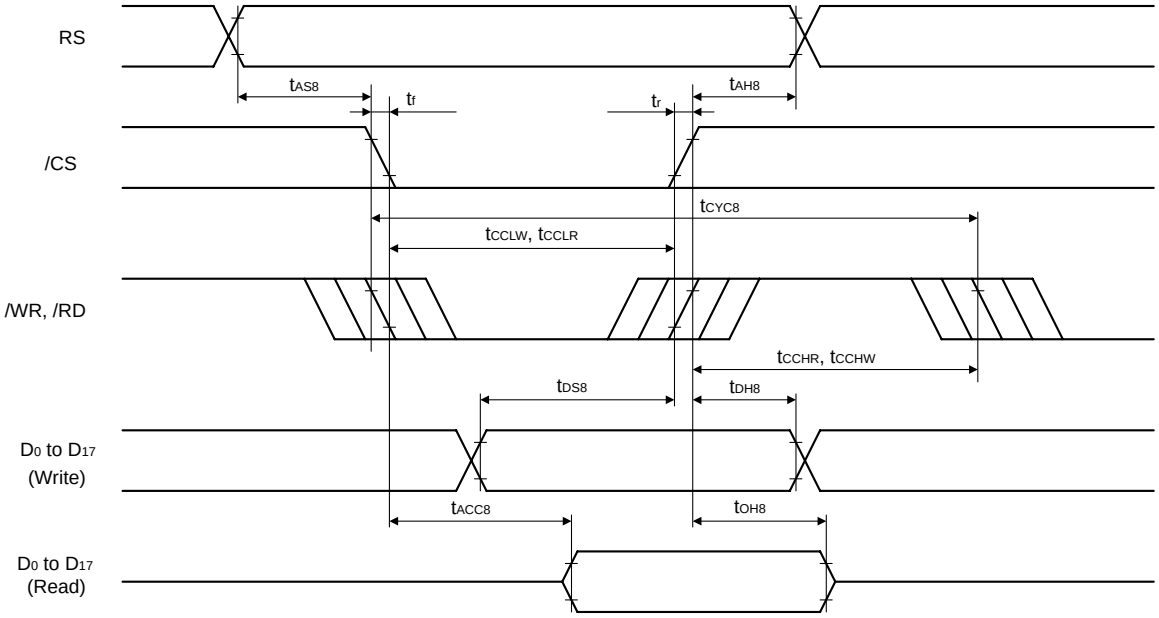


Parameter	Symbol	Condition		MIN.	TYP.[Note]	MAX.	Unit
Driver output delay time 1 (pre-charge period)	t_{PLH1}	V_S = 5.0 V, 4 kΩ +27 pF	V_O MAX. –200 mV			7.0	μs
	t_{PHL1}		V_O MIN. +200 mV			9.5	μs
Driver output delay time 2 (driver output period)	t_{PLH2}		Pre-charge completed → goal voltage			50	μs
	t_{PHL2}					52	μs

Note TYP. values are reference values when T_A = 25°C.

AC Characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{DD1} = 1.7 V to V_{DD2}, V_{DD2} = 2.5 to 3.6 V, V_S = 4.3 to 5.5 V)

(a) i80 series CPU interface



When V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (normal write mode, R114 = R115 = 01H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	140			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	60			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	80			ns
Data setup time	t_{DS8}	D_0 to D_{17}	80			ns
Data hold time	t_{DH8}	D_0 to D_{17}	0			ns
/RD access time	t_{ACC8}	D_0 to D_{17}, C_L = 100 pF			110	ns
Output disable time	t_{OH8}	D_0 to D_{17}, C_L = 100 pF	10		100	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 1.7 to 2.5 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (normal write mode, R114 = R115 = 01H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		333			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	160			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	100			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	140			ns
Data setup time	t_{DS8}	D_0 to D_{17}	100			ns
Data hold time	t_{DH8}	D_0 to D_{17}	0			ns
/RD access time	t_{ACC8}	D_0 to D_{17}, C_L = 100 pF			150	ns
Output disable time	t_{OH8}	D_0 to D_{17}, C_L = 100 pF	10		150	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		125			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	60			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	30			ns
Data setup time	t_{DS8}	D_0 to D_{17}	80			ns
Data hold time	t_{DH8}	D_0 to D_{17}	0			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 1.7 to 2.5 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$, (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

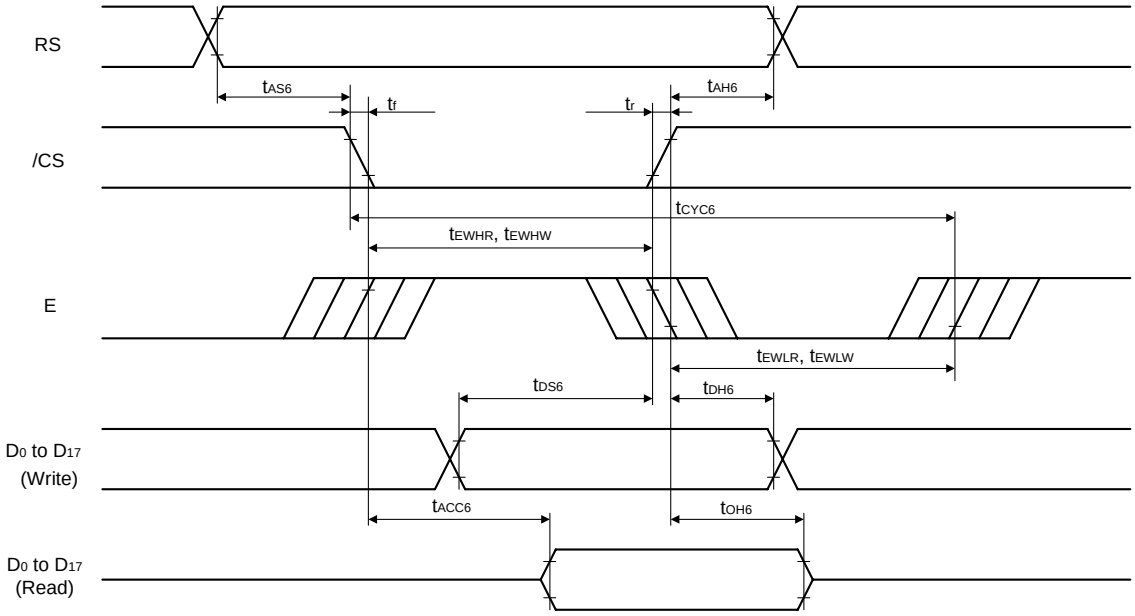
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		167			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	60			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	50			ns
Data setup time	t_{DS8}	D_0 to D_{17}	100			ns
Data hold time	t_{DH8}	D_0 to D_{17}	0			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{DD1}.

(b) M68 series CPU interface



When V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (normal mode, R114 = R115 = 01H)

Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		250			ns
Data setup time		t_{DS6}	D_0 to D_{17}	80			ns
Data hold time		t_{DH6}	D_0 to D_{17}	0			ns
Access time		t_{ACC6}	D_0 to D_{17}, C_L = 100 pF			110	ns
Output disable time		t_{OH6}	D_0 to D_{17}, C_L = 100 pF	10		100	ns
Enable high pulse width	Read	t_{EWHR}	E	140			ns
	Write	t_{EWHW}	E	120			ns
Enable low pulse width	Read	t_{EWLR}	E	80			ns
	Write	t_{EWLW}	E	60			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either ($t_r + t_f$) < (t_{CYC6}–t_{EWLR}–t_{EWHR}) or ($t_r + t_f$) < (t_{CYC6}–t_{EWLW}–t_{EWHW}).

2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 1.7 to 2.5 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (normal mode, R114 = R115 = 01H)

Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		333			ns
Data setup time		t_{DS6}	D_0 to D_{17}	100			ns
Data hold time		t_{DH6}	D_0 to D_{17}	0			ns
Access time		t_{ACC6}	D_0 to D_{17}, C_L = 100 pF			150	ns
Output disable time		t_{OH6}	D_0 to D_{17}, C_L = 100 pF	10		150	ns
Enable high pulse width	Read	t_{EWHR}	E	160			ns
	Write	t_{EWHW}	E	160			ns
Enable low pulse width	Read	t_{EWLR}	E	140			ns
	Write	t_{EWLW}	E	100			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either ($t_r + t_f$) < (t_{CYC6}–t_{EWLR}–t_{EWHR}) or ($t_r + t_f$) < (t_{CYC6}–t_{EWLW}–t_{EWHW}).

2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 2.5 to 3.6 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH6}	RS	0			ns
Address setup time	t_{AS6}	RS	0			ns
System cycle time	t_{CYC6}		125			ns
Data setup time	t_{DS6}	D_0 to D_{17}	80			ns
Data hold time	t_{DH6}	D_0 to D_{17}	0			ns
Enable high pulse width	t_{EWHR}	E	60			ns
Enable low pulse width	t_{EWLR}	E	30			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.

2. All timing is rated based on 20 to 80% of V_{DD1}.

When V_{DD1} = 1.7 to 2.5 V, V_{DD2} = 2.5 to 3.6 V, $V_{DD2} \geq V_{DD1}$ (high-speed RAM write mode, valid only for writing data, R114 = R115 = 01H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH6}	RS	0			ns
Address setup time	t_{AS6}	RS	0			ns
System cycle time	t_{CYC6}		167			ns
Data setup time	t_{DS6}	D_0 to D_{17}	100			ns
Data hold time	t_{DH6}	D_0 to D_{17}	0			ns
Enable high pulse width	t_{EWHR}	E	60			ns
Enable low pulse width	t_{EWLR}	E	50			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.

2. All timing is rated based on 20 to 80% of V_{DD1}.

(c) Common

	Parameter	Symbol	Condition	MIN.	TYP. Note1	MAX.	Unit
	Oscillation frequency	f_{OSC1}	Internal oscillator, 240 line (NGO = 0)	370	535	850	kHz
		f_{OSC2}	Internal oscillator, 220 line (NGO = 1)	300	490	760	kHz
		f_{OSC3}	External oscillator, 240 line (NGO = 0), resistance for oscillator R_L = 42 kΩ		536.2 Note5		kHz
★	Calibration setting time (frame frequency)	t_{cal1} ($f_{FRAME01}$)	Internal oscillator, 240 line (NGO = 0), **Note2**	29.7 (139.6)	69.1 (60)	162.4 (25.6)	μs (Hz)
		t_{cal2} ($f_{FRAME02}$)	Internal oscillator, 220 line (NGO = 1), **Note2**	36.7 (123.4)	69.1 (60)	181.6 (24.9)	μs (Hz)
	Frame frequency	f_{FRAME1}	Uncalibrated	40	60	95	Hz
		f_{FRAME2}	Calibrated Note3	54	60	66	Hz
		f_{FRAME3}	Calibrated Note4	56	60	64	Hz
	Input oscillation frequency	f_{OSCIN1}	External oscillator, 240 line (NGO = 0)		535		kHz
		f_{OSCIN2}	External oscillator, 220 line (NGO = 1)		490		kHz
	Reset pulse width at power on	t_{VR}	V_{DD2} or V_{DD1} to /RESET↑	100			ns
	Reset pulse width	t_{RW}		100			ns
	Reset time	t_R	/RESET↑ to interface operation	100			ns

Notes 1. TYP. values are reference values when T_A = 25°C.

★ **2.** The relationship between the frame frequency and the calibration setting time is as follows.

$$f_{FRAME01} = \frac{1}{t_{cal} \times 241} \qquad f_{FRAME02} = \frac{1}{t_{cal} \times 221}$$

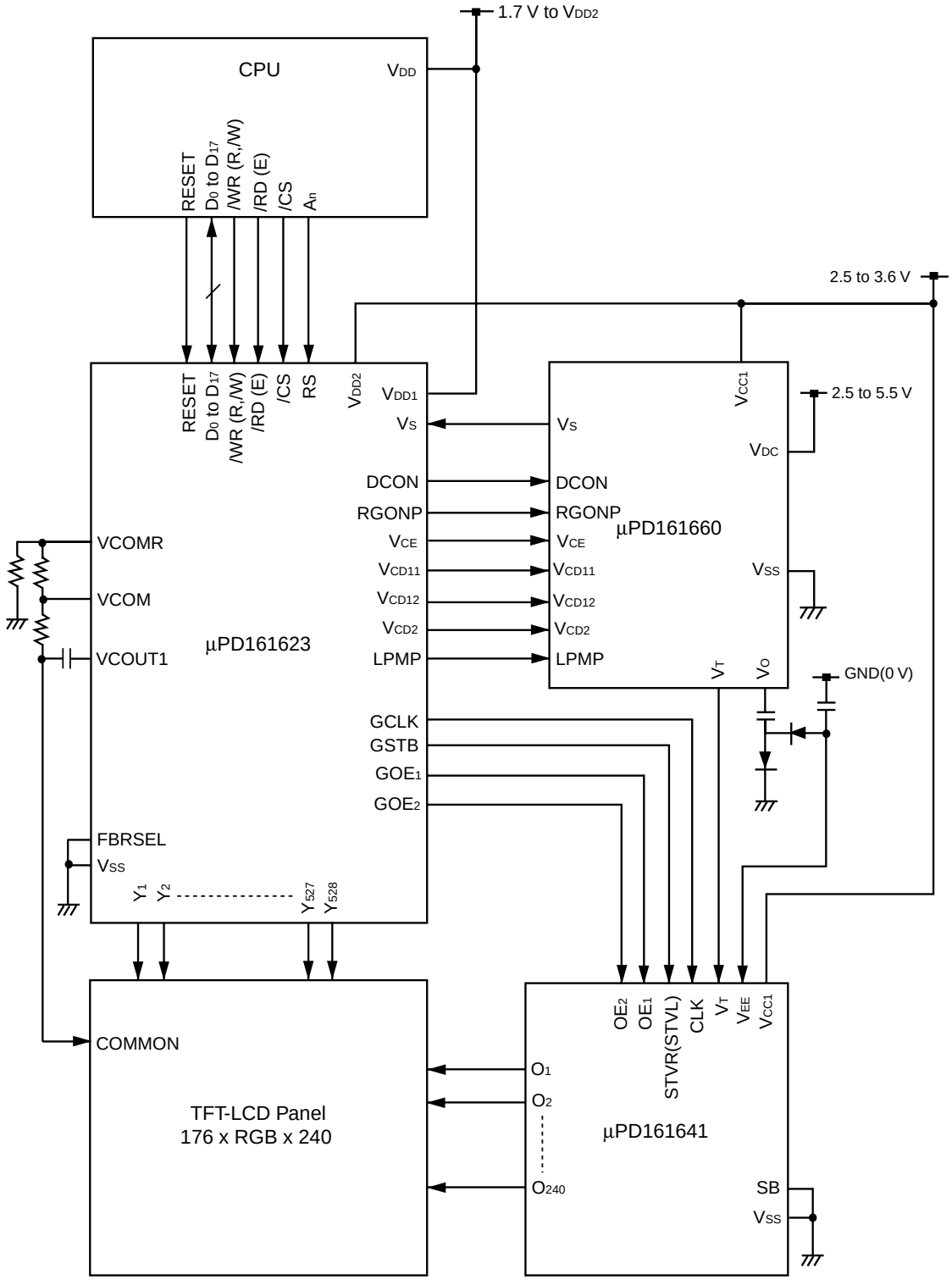
3. Measured at T_A = –40 to +85°C, after calibration at frame frequency = 60 Hz, T_A = 25°C exactly.

4. Measured at ±5°C, after calibration at frame frequency = 60 Hz exactly.

5. This value is a reference value in some measurement conditions. Note that be able to use and obtain after a real board's fully estimating.

9. μPD161623, 161641, and 161660 CONNECTION DIAGRAM EXAMPLE

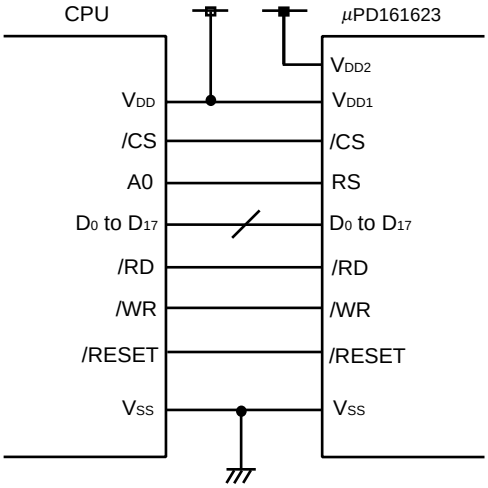
Connection diagram examples for the μPD161623, 161641, and 161660 are shown below.



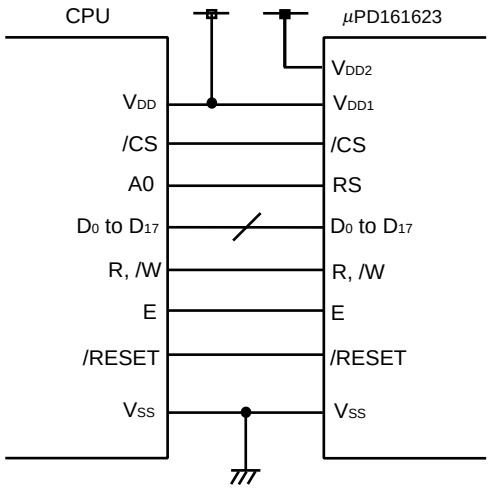
10. EXAMPLE of μPD161623 and CPU CONNECTION

Examples of μPD161623 and CPU connection are shown below. In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

(1) i80 series format



(2) M68 series format



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.