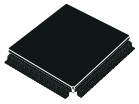
MTC20136

ADSL TRANSCEIVER CONTROLLER

- Dedicated controller for use with ADSL transceiver chips MTC20134, MTC20135 and MTC20455
  - Performs ADSL control functions :
  - Initialization procedure
  - Line monitoring during operation
  - Rate adaptive modes
- Supports the modem control interface protocol (CTRLE)
- Embedded high speed ARM microcore
- Glueless connection to MTC20135 and MTC20455
- Parallel or serial modem control interface (CTRLE) for glueless connection to management entities
- Embedded UART
- Supports code download
- External Bus Interface for 8 and 16-bit FEPROM and 16-bit SDRAM
- 144 pins PQFP



PQFP144

LFBGA160

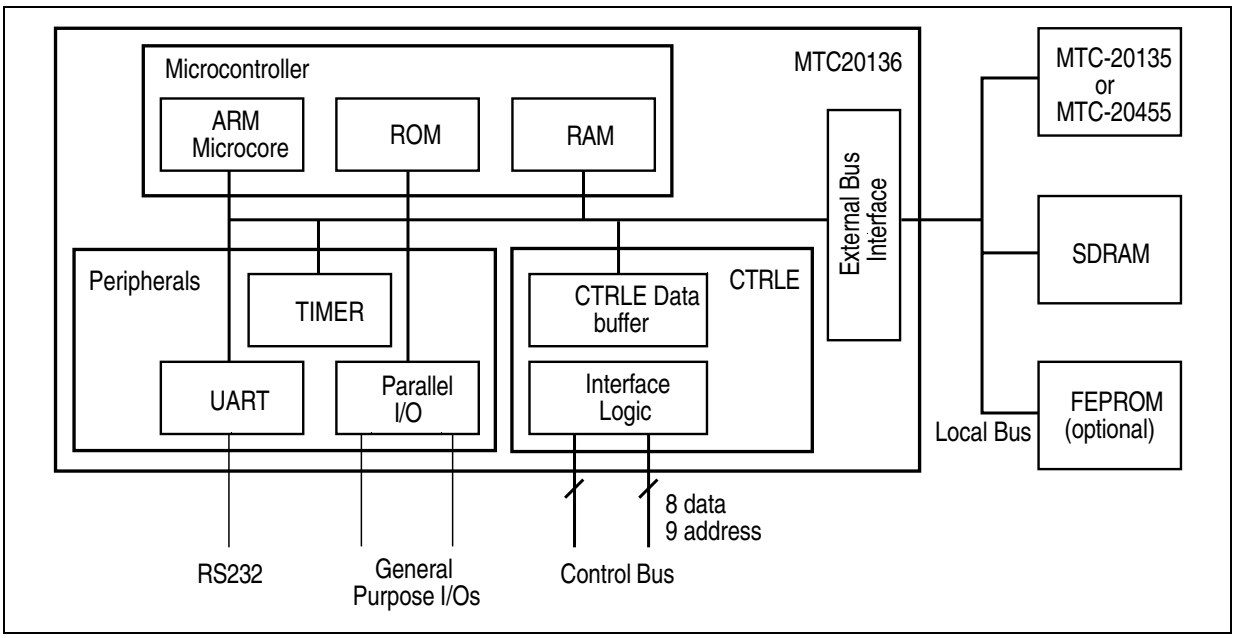
ORDERING NUMBERS:

Part number	Package	Temp.
MTC20136PQ- I1	144 pin PQFP	-40 /+85°C
MTC20136MB-I1	160 pin LBGA	-40 /+85°C
Can also be ordered using kit number MTK20131 or MTC20455		

DESCRIPTION

The MTC20136 is a dedicated controller chip, specifically designed to control operations of the ST-Microelectronics DynaMiTe chipset. The MTC20136 offers direct glueless interfaces to the MTC20135 and MTC20455 DMT/ATM transciever and implements a complete control interface for parameters and commands exchange between transceiver and system management. All real time ADSL-related functions (including EOC processing) are completely handled by the MTC20136.

Figure 1. Block Diagram



Functional Description

Figure 1 is showing the global block diagram of the MTC20136. The functions can be grouped into the following:

– Microcontroller
– External Bus Interface
– Control Interface (CTRLE)
– Peripherals
– Miscellaneous

Microcontroller

The microcontroller block includes an ARM-based microcore and its associated internal memory. 16 Kbytes on internal RAM and 128 x 32-bit words of ROM are foreseen. The ROM essentially contains the boot sequence needed for code download at startup. The use of the ROM by the microcore is defined by the state of the TROM pin during reset.

External Bus Interface

The External Bus Interface extends the internal microcontroller bus for connection of external devices. In particular, the bus is used to connect to the MTC20135 or MTC20455 modem chip and to external SDRAM (and optional FEEPROM).

The CTRLE functional block implements the ADSL modem command and data buffer and the interface logic supporting the physical interfaces of the CTRLE.

Peripherals

The peripherals block includes two UARTS for RS232 interfacing to external systems and two general = purpose parallel I/O lines.

Miscellaneous

This includes the clock circuitry, reset circuitry, test functions and configuration control signals.

CTRLE Interfaces

External Bus Interface

The external bus interface (EBI) provides a glueless interface to 8 and 16-bit asynchronous Flash EEPROM, 16 bit SDRAM devices and to slave devices with an i960-like 16 bit bus interface with multiplexed address and data (as available on DynaMiTe chips).

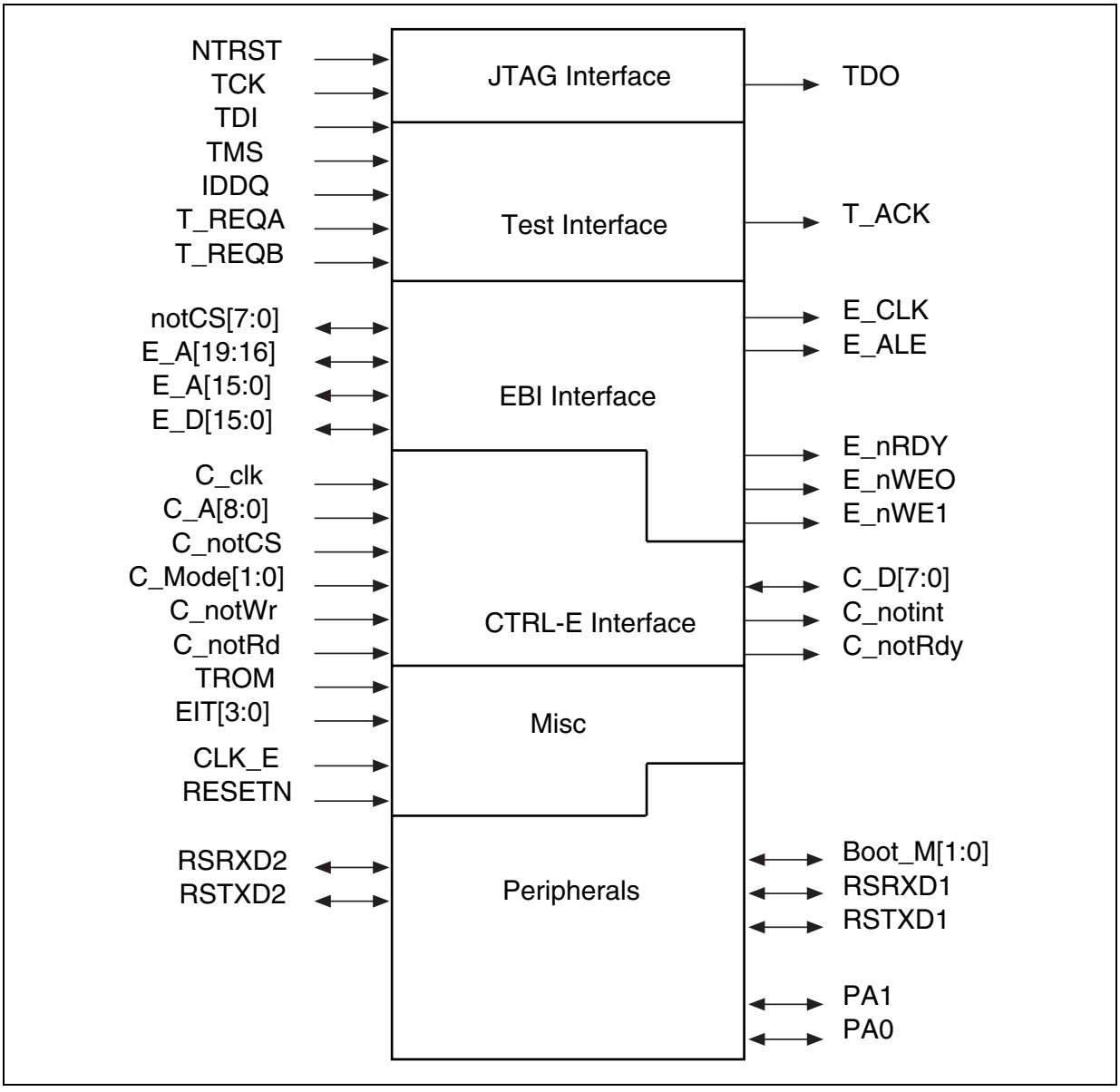
The EBI provides two chip selects (E_nCS[1:0]) to be used for memory access (SRAM-like), one dedicated SDRAM chip select ((E_nCS_S) and four chip selects (E_nCS[7:4]) to be used for access to ADSL slave devices. The chip selects all correspond to a fixed 1Mbyte memory region in the microcontroller memory map, except for SDRAM access.

PIN LAYOUT

Functional Pin Summary

The signals hereunder are grouped per functional interface.

Figure 2. Pin functional description and type per interface



The table below describes the pins, organized per interface. Some of these pins have a multiple functionality. In this case both functionalities are mentioned.

Name	I/O Type	Description
External Bus Interface		
E_A[19:16]	O	Address bus MSBs
E_A[15:0]	I/O	Address bus LSBs / Testbus MSBs
E_D[15:0]	I/O	Data bus / Testbus LSBs
E_CLK	O	EBI clock (ASIC Access)
E_ALE	O	Address latch enable (ASIC Access)
E_nCS_0	O	Chip select signal (Memory Bank 0)
E_nCS_1	O	Chip select signal (Memory Bank 1)
E_nCS_S	O	Chip select signal (SDRAM)
E_nCS_4	O	Chip select signal (ASIC 1)
E_nCS_5	O	Chip select signal (ASIC 2)
E_nCS_6	O	Chip select signal (ASIC 3)
E_nCS_7	O	Chip select signal (ASIC 4)
E_nRDYRCV	I	Data acknowledge
E_nOE	O	Output enable
E_nWE0	O	Write enable LSB / W/notR indication
E_nWE1	O	Write enable MSB
Clock Bus Interface		
CLK_IN	I	MTC20136 Master clock
Parallel Port Interface		
PA[0]	I/O	Port A bit[0]
PA[1]	I/O	Port A bit[1]
UART1 Interface		
RSTXD1	O	Serial TX port
RSRXD1	I	Serial RX port
UART2 Interface		
RSTXD2	O	Serial TX port
RSRXD2	I	Serial RX port
Interrupt Interface		
EIT_0	I	External interrupt lines
EIT_1	I	External interrupt lines
EIT_2	I	External interrupt lines
EIT_3	I	External interrupt lines
JTAG Interface		
nTRST	I-PU	Reset JTAG interface
TCK	I-PU	JTAG clock
TDI	I-PU	Test Data In
TMS	I-PU	Test Mode Select
TDO	O	Test Data Out
Reset Interface		
RESETN	I	Reset signal (Active High)
Boot Interface		
TROM	I	Boot from ROM select

Name	I/O Type	Description
Boot_M0	I/O	Download Mode .UART BaudRate.
		(Auto adjust or 9600 Bps).
Boot_M1	I/O	Download Mode Select (CTRL-E or UART1)
Ctrl-E Interface (Parallel mode only described - see above for Serial Mode)		
C_A[8:0]	I	Address bus (5 V tolerant)
C_D[7:0]	IO	Data bus (5 V tolerant)
C_nCS	I	Chip select (5 V tolerant)
C_nInt	OD	Ctrl-E external interrupt
C_mode[1:0]	I	Ctrl-E interface bus mode (5 V tolerant)
C_nWr	I	Write indication (5V tolerant)
C_nRd	I	Read indication (5V tolerant)
C_nRdy	OZ	Ready indication
C_clk	I	Serial Input clock (5V tolerant)

I = Input, CMOS levels
I-PU = Input with pull-up resistance, CMOS levels
I-PD = Input with pull-down resistance, CMOS levels
I-TTL = Input TTL levels
O = Push-pull output
OZ = Push-pull output with high-impedance state
OD = Open Drain output
IO = input / Tri-state Push-pull output

PQFP144 Pin Configuration

(Default Value between ( ))

Pin#	Name	Function
1	E_A14	EBI Address
2	E_A15	EBI Address
3	E_A16	EBI Address
4	E_A17	EBI Address
5	VDD	VDD
6	VSS	VSS
7	E_A18	EBI Address
8	E_A19	EBI Address
9	EIT0	External Interrupt In - 0
10	EIT1	External Interrupt In - 1
11	VDD	VDD
12	VSS	VSS
13	EIT2	External Interrupt In - 2
14	EIT3	External Interrupt In -3
15	I_MODE	Tracking ICE Mode Select (0)
16	E_CLK	EBI Clock Out
17	E_ALE	EBI ALE
18	VDD	VDD

PQFP144 Pin Configuration (continued)
(Default Value between ( ))

Pin#	Name	Function
19	VSS	VSS
20	E_nRDYRCV	EBI Ack in
21	E_nWE0	EBI Write Enable
22	E_nWE1	EBI Write Enable
23	E_notCS_4	EBI ASIC ChipSelect
24	VDD	VDD
25	VSS	VSS
26	Boot_M0	BootMode Select
27	Boot_M1	BootMode Select
28	PA0	General Purpose IO
29	PA1	General Purpose IO
30	TROM	Boot Mode Select
31	VDD	VDD
32	VSS	VSS
33	T_REQA	Reserved for test (0)
34	T_REQB	Reserved for test (0)
35	T_ACK	Reserved for test
36	IDDQ	Reserved for test (0)
37	RESETN	RESET (Active Low)
38	TDI	JTAG Interface
39	TDO	JTAG Interface
40	VDD	VDD
41	VSS	VSS
42	TMS	JTAG Interface
43	nTRST	JTAG Interface
44	TCK	JTAG Interface
45	RSTXD1	UART port 1 - TX
46	RSRXD1	UART port 1 - RX
47	RSTXD2	UART port 2 - TX
48	VDD	VDD
49	VSS	VSS
50	RSRXD2	UART port 2 - RX
51	TESTSE	Test Scan Enable
52	SCAN_CLK	Test Scan Clock
53	C_nInt	CTRL-E Interrupt
54	VDD	VDD
55	VSS	VSS
56	CLK_IN	Master Clock In
57	VSS	VSS
58	C_nRdy	CTRL-E Interface
59	C_nRd	CTRL-E Interface
60	VDD	VDD

PQFP144 Pin Configuration (continued)
(Default Value between ( ))

Pin#	Name	Function
61	VSS	VSS
62	C_nWr	CTRL-E Interface
63	C_Mode0	CTRL-E Interface
64	C_Mode1	CTRL-E Interface
65	C_notCS	CTRL-E Interface
66	C_CLK	CTRL-E Interface
67	VDD	VDD
68	VSS	VSS
69	C_D0	CTRL-E Interface
70	C_D1	CTRL-E Interface
71	C_D2	CTRL-E Interface
72	C_D3	CTRL-E Interface
73	C_D4	CTRL-E Interface
74	C_D5	CTRL-E Interface
75	C_D6	CTRL-E Interface
76	VDD	VDD
77	VSS	VSS
78	C_D7	CTRL-E Interface
79	C_A0	CTRL-E Interface
80	C_A1	CTRL-E Interface
81	C_A2	CTRL-E Interface
82	C_A3	CTRL-E Interface
83	C_A4	CTRL-E Interface
84	VDD	VDD
85	VSS	VSS
86	C_A5	CTRL-E Interface
87	C_A6	CTRL-E Interface
88	C_A7	CTRL-E Interface
89	C_A8	CTRL-E Interface
90	VDD	VDD
91	VSS	VSS
92	I_BP	Reserved (0)
93	I_DBGRQ	Reserved (0)
94	notCS_7	EBI - ASIC Chip Select
95	notCS_6	EBI - ASIC Chip Select
96	notCS_5	EBI - ASIC Chip Select
97	VDD	VDD
98	VSS	VSS
99	E_nCS_2	EBI - SDRAM Chip Select
100	E_nCS_1	EBI - SRAM Chip Select
101	E_nCS_0	EBI - FLASH Chip Select
102	E_nOE	EBI - OE

PQFP144 Pin Configuration (continued)
(Default Value between ( ))

Pin#	Name	Function
103	E_D15	EBI Data
104	VDD	VDD
105	VSS	VSS
106	E_D14	EBI Data
107	E_D13	EBI Data
108	E_D12	EBI Data
109	E_D11	EBI Data
110	E_D10	EBI Data
111	E_D9	EBI Data
112	VSS	VSS
113	VDD	VDD
114	E_D8	EBI Data
115	E_D7	EBI Data
116	E_D6	EBI Data
117	E_D5	EBI Data
118	E_D4	EBI Data
119	VDD	VDD
120	VSS	VSS
121	E_D3	EBI Data
122	E_D2	EBI Data
123	E_D1	EBI Data
124	E_D0	EBI Data
125	E_A0	EBI Address
126	VDD	VDD
127	VSS	VSS
128	E_A1	EBI Address
129	E_A2	EBI Address
130	E_A3	EBI Address
131	E_A4	EBI Address
132	VDD	VDD
133	VSS	VSS
134	E_A5	EBI Address
135	E_A6	EBI Address
136	E_A7	EBI Address
137	E_A8	EBI Address
138	E_A9	EBI Address
139	VDD	VDD
140	VSS	VSS
141	E_A10	EBI Address
142	E_A11	EBI Address
143	E_A12	EBI Address
144	E_A13	EBI Address

LFBGA160 Pin Configuration

Pin#	Name	Function
C4	E_A14	EBI Address
B2	E_A15	EBI Address
D4	E_A16	EBI Address
C3	E_A17	EBI Address
C2	VDD	VDD
E3	VSS	VSS
D3	E_A18	EBI Address
D2	E_A19	EBI Address
E4	EIT0	External Interrupt In - 0
E2	EIT1	External Interrupt In - 1
E1	VDD	VDD
F3	VSS	VSS
F4	EIT2	External Interrupt In - 2
F1	EIT3	External Interrupt In -3
F2	I_MODE	Tracking ICE Mode Select (0)
G3	E_CLK	EBI Clock Out
H1	E_ALE	EBI ALE
G4	VDD	VDD
G2	VSS	VSS
H3	E_nRDYRCV	EBI Ack in
H4	E_nWE0	EBI Write Enable
H2	E_nWE1	EBI Write Enable
J3	E_notCS_4	EBI ASIC ChipSelect
K2	VDD	VDD
J4	VSS	VSS
J2	Boot_M0	BootMode Select
K3	Boot_M1	BootMode Select
K4	PA0	General Purpose IO
L2	PA1	General Purpose IO
L3	TROM	Boot Mode Select
M2	VDD	VDD
M3	VSS	VSS
L4	T_REQA	Reserved for test (0)
N2	T_REQB	Reserved for test (0)
N3	T_ACK	Reserved for test
N1	IDDQ	Reserved for test (0)
P1	RESETN	RESET (Active Low)
P2	TDI	JTAG Interface
M4	TDO	JTAG Interface
P3	VDD	VDD
N4	VSS	VSS
M5	TMS	JTAG Interface
P4	nTRST	JTAG Interface

LFBGA160 Pin Configuration (continued)

Pin#	Name	Function
N5	TCK	JTAG Interface
L5	RSTXD1	UART port 1 - TX
P5	RSRXD1	UART port 1 - RX
M6	RSTXD2	UART port 2 - TX
N6	VDD	VDD
P6	VSS	VSS
L6	RSRXD2	UART port 2 - RX
N7	TESTSE	Test Scan Enable
P7	SCAN_CLK	Test Scan Clock
M7	C_nInt	CTRL-E Interrupt
L7	VDD	VDD
P8	VSS	VSS
N8	CLK_IN	Master Clock In
M8	VSS	VSS
L8	C_nRdy	CTRL-E Interface
N9	C_nRd	CTRL-E Interface
M9	VDD	VDD
P10	VSS	VSS
N10	C_nWr	CTRL-E Interface
L9	C_Mode0	CTRL-E Interface
P11	C_Mode1	CTRL-E Interface
M10	C_notCS	CTRL-E Interface
N11	C_CLK	CTRL-E Interface
P12	VDD	VDD
L10	VSS	VSS
N12	C_D0	CTRL-E Interface
P13	C_D1	CTRL-E Interface
M11	C_D2	CTRL-E Interface
N13	C_D3	CTRL-E Interface
N14	NOT CONNECTED	
P14	C_D4	CTRL-E Interface
M12	C_D5	CTRL-E Interface
M14	C_D6	CTRL-E Interface
M13	VDD	VDD
L11	VSS	VSS
L14	C_D7	CTRL-E Interface
L13	C_A0	CTRL-E Interface
L12	C_A1	CTRL-E Interface
K14	C_A2	CTRL-E Interface
K11	C_A3	CTRL-E Interface
K13	C_A4	CTRL-E Interface
J14	VDD	VDD
K12	VSS	VSS

LFBGA160 Pin Configuration (continued)

Pin#	Name	Function
J11	C_A5	CTRL-E Interface
H14	C_A6	CTRL-E Interface
J13	C_A7	CTRL-E Interface
J12	C_A8	CTRL-E Interface
H11	VDD	VDD
H13	VSS	VSS
H12	I_BP	Reserved (0)
G11	I_DBGRQ	Reserved (0)
F14	notCS_7	EBI - ASIC Chip Select
G13	notCS_6	EBI - ASIC Chip Select
G12	notCS_5	EBI - ASIC Chip Select
E14	VDD	VDD
F11	VSS	VSS
F13	E_nCS_2	EBI - SDRAM Chip Select
F12	E_nCS_1	EBI - SRAM Chip Select
E11	E_nCS_0	EBI - FLASH Chip Select
E13	E_nOE	EBI - OE
E12	E_D15	EBI Data
C14	VDD	VDD
D11	VSS	VSS
D13	E_D14	EBI Data
B14	E_D13	EBI Data
D12	E_D12	EBI Data
A14	E_D11	EBI Data
C13	E_D10	EBI Data
B13	E_D9	EBI Data
C11	VSS	VSS
C12	VDD	VDD
B12	E_D8	EBI Data
D10	E_D7	EBI Data
B11	E_D6	EBI Data
A11	E_D5	EBI Data
C10	E_D4	EBI Data
B10	VDD	VDD
A10	VSS	VSS
D9	E_D3	EBI Data
C9	E_D2	EBI Data
A9	E_D1	EBI Data
B9	E_D0	EBI Data
D8	E_A0	EBI Address
B8	VDD	VDD
C8	VSS	VSS
D7	E_A1	EBI Address

LFBGA160 Pin Configuration (continued)

Pin#	Name	Function
B7	E_A2	EBI Address
A7	E_A3	EBI Address
C7	E_A4	EBI Address
D6	VDD	VDD
A6	VSS	VSS
B6	E_A5	EBI Address
C6	E_A6	EBI Address
A4	E_A7	EBI Address
D5	E_A8	EBI Address
B5	E_A9	EBI Address
A3	VDD	VDD
C5	VSS	VSS
B4	E_A10	EBI Address
A2	E_A11	EBI Address
B3	E_A12	EBI Address
B1	E_A13	EBI Address

External pins

E_D[15:0]	16 bit data, multiplexed address/data
E_A[19:0]	20 bit address (including commands for SDRAM)
nCS[7:4]	external chip select
E_CLK	external clock
ALE	Address Latch Enable
nRDYRCV	Ready/Recover driven by selected device together with external pull-up
nOE	output enable
nWE0	Write enable for LSB byte lane E_D[7:0]
nWE1	Write enable for MSB byte lane E_D[15:8]

These physical pins are used for different logical functions, depending on the external device which is accessed. The correspondance between physical and logical functions is given in Table 1

Table 1.

Pin Name	MTC20135, MTC20455 access function	SDRAM access function	SRAM/FEPROM access function
E_A [19]	-	S_nRAS	E_A [19]
E_A [18]	-	S_nCAS	E_A [18]
E_A [17]	-	S_DQM0	E_A [17]
E_A [16]	-	S_DQM1	E_A [16]

Table 1. (continued)

Pin Name	MTC20135, MTC20455 access function	SDRAM access function	SRAM/FEPROM access function
E_A [15:0]	-	S_A [11:0]	E_A [15:0]
E_D [15:0]	AD [15:0]	S_Q [15:0]	E_D [15:0]
E_nCS [1:0]	-	-	E_nCS [1:0]
E_nCS [7:4]	nCS [7:4]	-	-
E_nCS_S	-	S_nCS	-
E_Clk	E-Clk	S_Clk	-
E_ALE	ALE	-	-
E_nRDYRCV	nRDYRCV	-	-
E_nOE	-	-	E_nOE
E_nWE0	W/nR	-	E_nWE0
E_nWE1	-	S_nWE	E_nWE1

Memory map modes

Three modes are defined :

a) Normal mode:

The internal RAM is mapped in the lower part of memory. This is the normal operating mode, it allows maximum speed access to exception vectors.

b) Normal boot mode:

If the TROM external pin is high at reset, the MTC20136 boots from an external FEPROM.

c) Internal boot mode:

If the TROM external pin is low at reset, the MTC20136 boots from its internal ROM. This mode can be used to perform code download from a host.

Boot modes are used at RESET time.

Boot_M0 andBoot_M1 on pin 26 and 27 conrol the port to be used for downloading the code into the SDRAM after Bootup. This when TROM is low.

Boot_M1 (Pin27)	Boot_M0 (Pin26)	
0	1	9600 Bps via serail port 1
1	0	Par. CTRL-E
1	1	Par.CTRL-E

MTC20135, MTC20455 access

The MTC20136 directly connects to the MTC20135 without glue logic. Following features are provided for MTC20135 access :

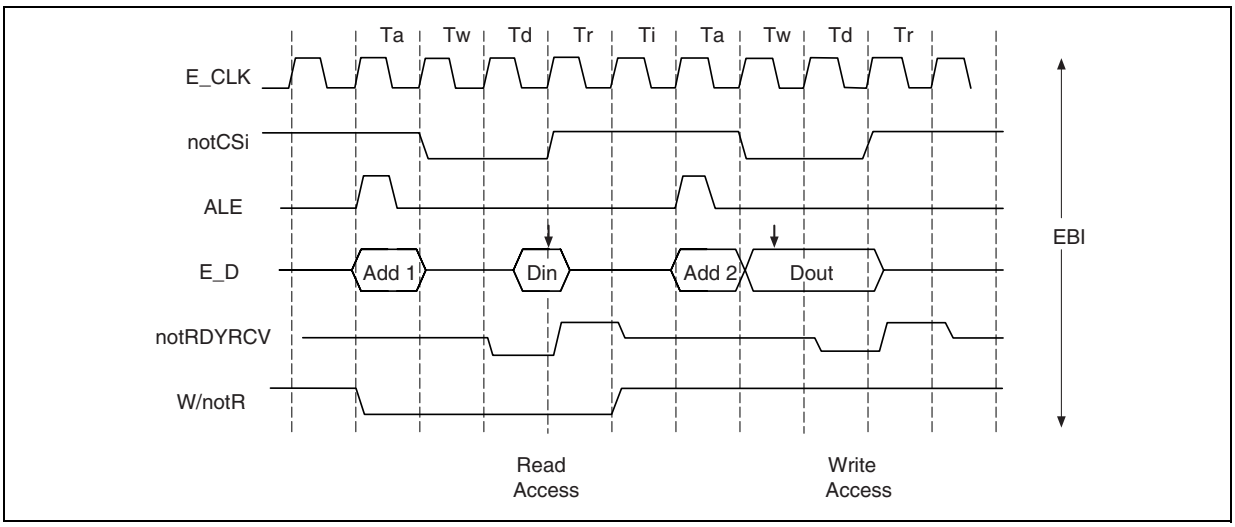
– 16 bit multiplexed address/data bus giving 64Kbyte address space per MTC20135.

– synchronous ready-controlled operation - control signals : nCS[4:7], E_CLK, ALE, W/nR, nRDYRCV

– Little endian byte ordering on 16 bit bus - nRDYRCV timeout mechanism

The timing diagram of the access to the MTC20135 or MTC20455 is shown in figure 3:

Figure 3. Access to MTC20135, MTC20455



SDRAM

The SDRAM interface allows a glue-less interconnection of 1 SDRAM. Following features are provided for SDRAM access.

– 16 bit databus and 12 bit address bus.

– control signals : S_nCS, S_nRAS, S_nCAS, S_nWE, S_DQM[1:0

Control signal timing

All SDRAM actions are triggered at the rising edge of its clock. Timing diagrams for a burst of four 16-bit accesses to 16-bit SDRAM (Figure 3 and Figure 4) show the basic behavior of the control signals.

Figure 4. SDRAM read access (CAS latency = 3; Burst length = 4)

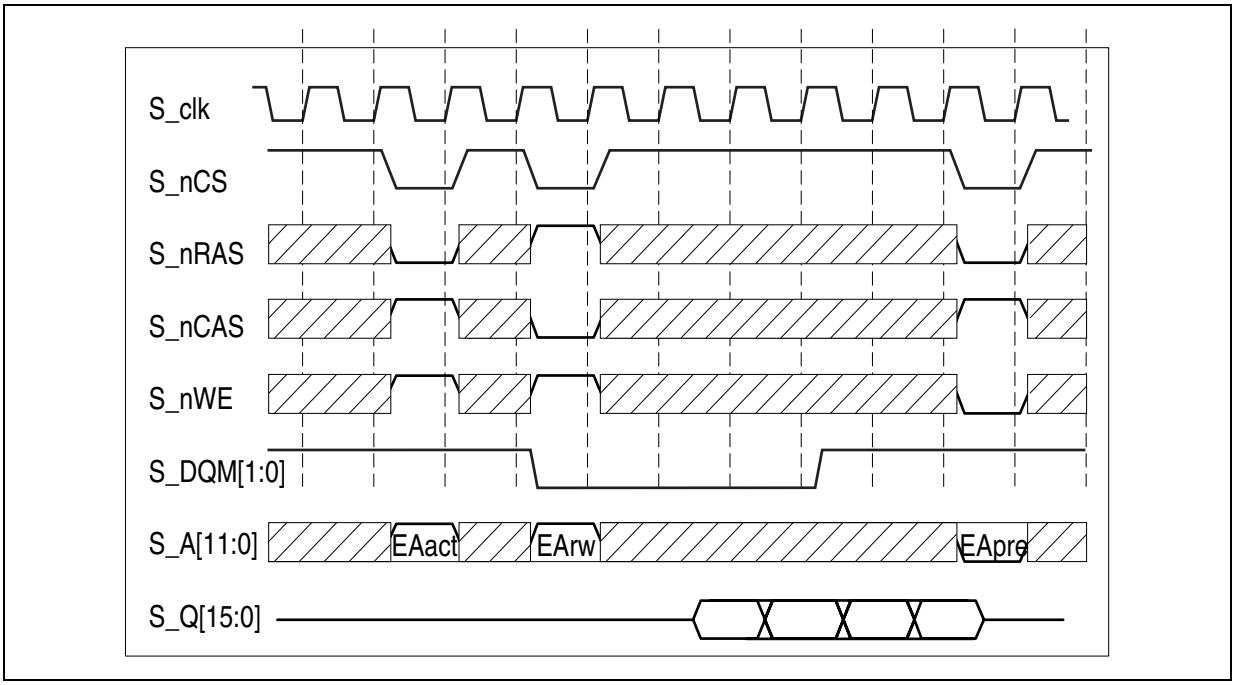
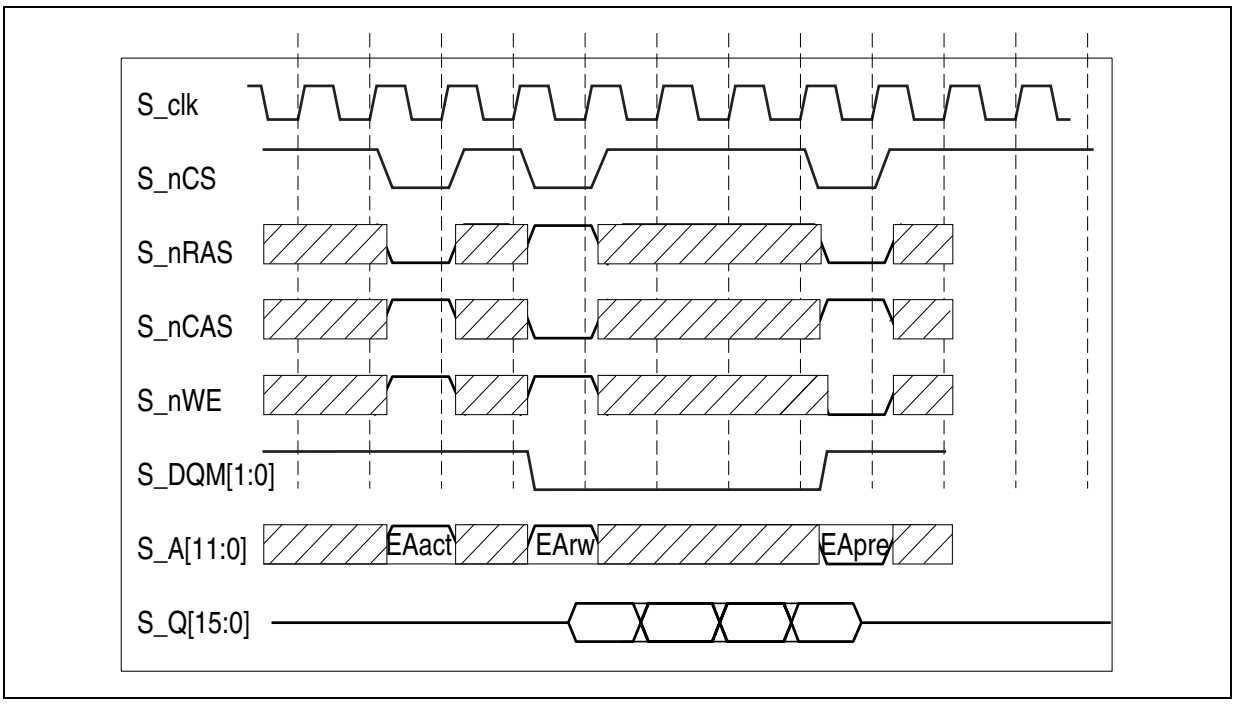


Figure 5. SDRAM write access (CAS latency = 3; Burst length = 4)

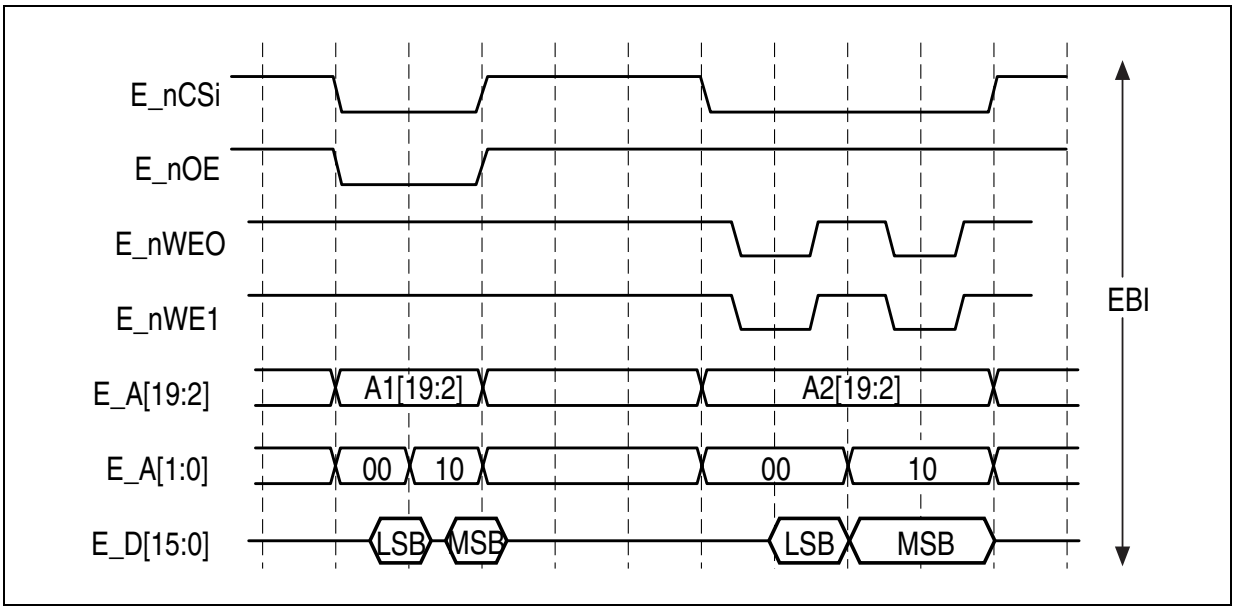


Memory

Following features are provided for memory access (SRAM or FEPROM) :

– 16 bit databus and 20 bit address bus giving 1Mbyte address space per chip select
– control signals : E_nCS[0:1], E_nOE, E_nWE0, E_nWE1
– setup and wait state insertion
– 8, 16 and 32 bit access by MTC20136 to 8 or 16 bit memory according to little endian convention

Figure 6. EBI memory access (32-bit Word R/W to 16 bit memory), maximum speed timing



EBI Interface Timing

All timing parameters are specified at a load of 100 pF, all the electrical levels are CMOS compatible.

Table 2. All signals

Symbol	Parameters	Min	Typ	Max	Unit
t_r,t_f	Rise and Fall time (10% - 90%)			3	ns
Ci	Input load			10	pF
Co	Output load			100	pF

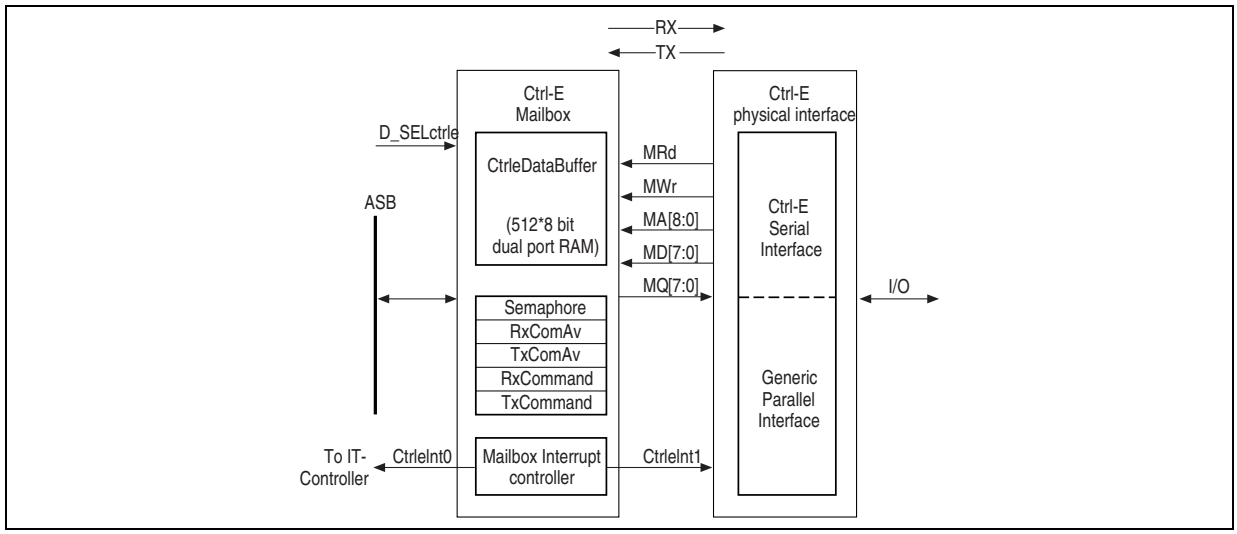
Table 3. EBI signal timing with respect to E_CLK

Symbol	Parameters	Min	Max	Unit
T_{dh}	Data input hold time from E_CLK	3		ns
T_{ds}	Data input setup time to E_CLK	10		ns
T_{dd}	Data/Address output valid/tri-state delay from E_CLK		10	ns
T_{wrd}	ALE delay from E_CLK		6	ns
T_{oed}	notOE delay from E_CLK		6	ns
T_{wed}	notWEi delay from E_CLK (falling edge)		6	ns
T_{wrd}	W/notR delay from E_CLK	3	10	ns
T_{csd}	notCSi delay from E_CLK	3	10	ns

CTRLE

The Ctrl-E interface is an ADSL-oriented mailbox system to exchange control and status messages between MTC20136 and an external controller. It consists of a mailbox and a physical interface. The mailbox has two 8-bit command registers to pass commands from the MTC20136 internal controller bus (ASB) to Ctrl-E (RxCommand) and from Ctrl-E to ASB (TxCommand), and two status registers (RxComAv and TxComAv) to indicate the status of the command register. Data associated with a command can be exchanged using a common CtrleDataBuffer. A hardware semaphore mechanism is provided to allow control of data consistency of the CtrleDataBuffer.

Figure 7. Ctrl-E interface controller principle



The Ctrl-E physical interface between the mailbox and an external controller can be used in one of two modes: as a dedicated serial bus interface or as a generic parallel bus interface. Selection between serial and parallel mode is done with an external mode strap, IO pins are shared.

Ctrl-E Mailbox

The Ctrl-E Mailbox occupies a 512 byte memory map accessible by the Ctrl-E physical interface and by the ASB bus. The mailbox memory map is given in Table 4.

An external interrupt can be generated by the Mailbox interrupt controller.

A full description of the CTRLE protocol and use of the CTRLE mailbox is available in the “CTRLE Interface Specifications” documents, available separately.

Table 4. Ctrl-E controller memory map:

Field	Acc	Mailbox Address MA[8:0]	Size(bit)	Initial	Function
TxCommand	RW	000_h	8	00_h	Command written by Ctrl-E, read by ASB
RxCommand	RW	001_h	8	00_h	Command written by ASB, read by Ctrl-E
TxComAv	RW	002_h	1	0_b	1-bit register : 1 if TX command available
RxComAv	RW	003_h	1	0_b	1-bit register : 1 if RX command available
Semaphore	PV	004_h	2	00_b	Semaphore for access to written by ASB, read by Ctrl-E
CtrleDataBuffer	RW	005_h-$1FF_h$	8	00_h	507x8 bit data buffer

Ctrl-E Semaphore

A simple semaphore mechanism is provided to allow control of the data consistency of the Ctrle-DataBuffer. One mailbox address is defined as a two-bit semaphore register protected by control logic to prevent unallowed write accesses to this register.

Before the databuffer is read or written by one of the two interfaces (ASB or Ctrl-E) this interface should perform a 'P-operation' on the semaphore. After a read or write of the databuffer the interface should do a 'V-operation' releasing the semaphore. P and V operations are performed by write and read accesses to the semaphore register. The semaphore will be updated as shown in Table 5.

Each semaphore operation (P or V) consists of two consecutive actions that don't have to be atomic :

a)Write the correct value to the semaphore address (see Table 5)

b)Read the value in the semaphore address.

If the value read is different from the value writen the P or V operation was not succesfull and should be tried again.

Table 5. Semaphore P and V operations: new value after write by ASB or Ctrl-E

semaphore operation	originator	write value	previous semaphore value		
			semaphore free	semaphore taken by ASB	Ctrl-E
			00_b	01_b	11_b
P	ASB	01_b	01_b	01_b	11_b
	Ctrl-E	11_b	11_b	01_b	11_b
V	ASB	00_b	00_b	00_b	11_b
	Ctrl-E	00_b	00_b	01_b	00_b

The databuffers can be accessed without using the semaphore mechanism if data consistency is guaranteed in another way. If other values are written to the semaphore address than the values listed the write will not be performed.

Ctrl-E Physical Interface

Two parallel bus modes are defined to support both Motorola-compatible and Intel-compatible timing and control signals. This interface specification is compliant to Utopia Level 2 Parallel Management Interface.

Selection of the Ctrl-E physical interface bus mode is done with the C_Mode[1:0] input pins :

Table 6. Bus mode selected with C_Mode[1:0] inputs

C_Mode[1]	C_Mode[0]	Description
0	0	Motorola-type parallel interface
0	1	Intel-type parallel interface
1	1	Reserved
1	0	Reserved

Generic Parallel Interface

The two parallel bus modes differ only in the definition of 3 control signals: busmode 0 provides a read/ write selector, a data strobe and a ready acknowledge. Busmode 1 provides a read strobe, a write strobe and a ready acknowledge. The signal definition is shown in following table:

Table 7. Ctrl-E interface signals in parallel interface modes

Signal name	Type	Function	PIN
C_A[8:0]	I	address bus	C_A[8:0]
C_D[7:0]	IO	byte wide bidirectional data bus	C_D[7:0]
C_notCS	I	chip select	C_notCS
C_notInt	OZ	Interrupt output, derived from CtrleInt1 signal from Mailbox : low when CtrleInt1 is low, else tri-stated	C_notInt
Mode 0 : Motorola-compatible mode			
C_Mode[1:0]	I	00_b	C_Mode[1:0]
C_Rd/notWr	I	read access if 1, write access if 0	C_notWr
C_notDS	I	Data Strobe	C_notRd
C_notDtAck	OZ	Bus cycle ready indication, indicates that data on bus can be sampled or removed	C_notRdy
Mode 1 : Intel-compatible mode			
C_Mode[1:0]	I	01_b	C_Mode[1:0]
C_notWr	I	write cycle indication	C_notWr
C_notRd	I	read cycle indication	C_notRd
C_notRdy	OZ	Bus cycle ready indication, indicates that data on bus can be sampled or removed, same as in mode 0	C_notRdy

Write cycle timing

Figure 8. Ctrl-E interface: write cycle timing in parallel modes 0 and 1

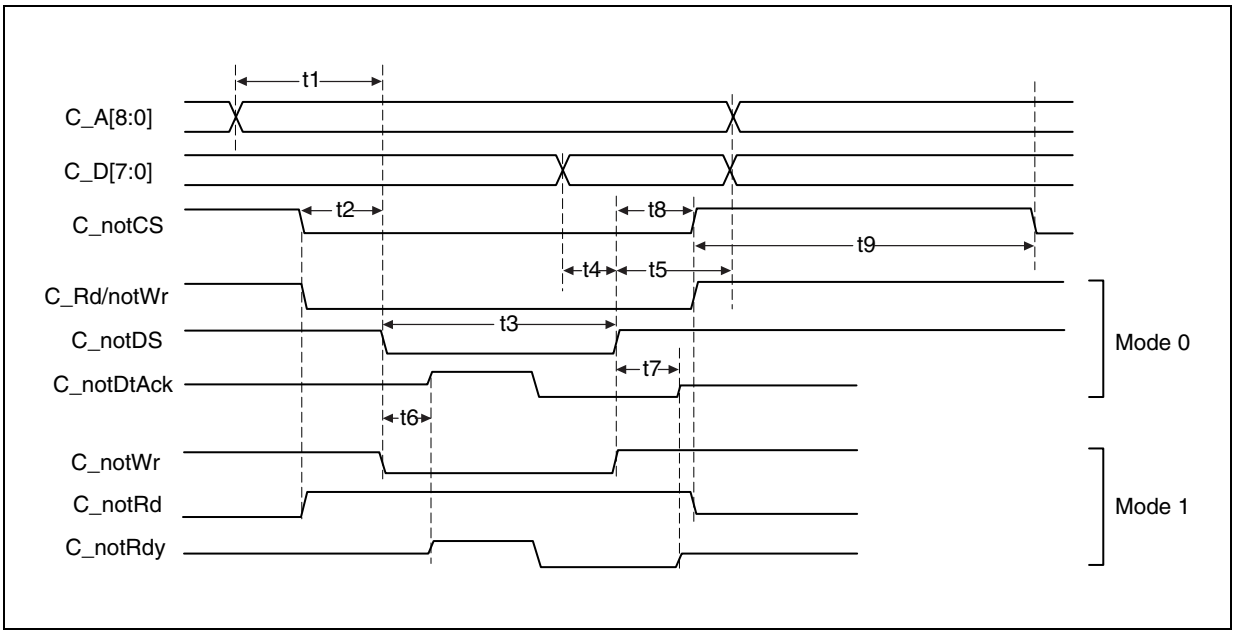


Table 8. write cycle timing in parallel modes 0 and 1

Symbol	Description	Min	Max	Unit
t1	C_A Setup to C_notDS (C_notWr) low	0		ns
t2	C_notCS, C_Rd/notWr setup to C_notDS (C_notWr) low	0		ns
t3	C_notDS (C_notWr) pulse width	215		ns
t4	C_D setup to C_notDS (C_notWr) high	15		ns
t5	C_A, C_D hold from C_notDS (C_notWr) high	5		ns
t6	C_notDtAck (C_notRdy) valid from C_notDS (C_notWr) low		15	ns
t7	C_notDtAck (C_notRdy) tri-state from C_notDS (C_notWr) high		15	ns
t8	C_notCS, C_Rd/notWr hold from C_notDS (C_notWr) high	0		ns
t9	C_notCS high to C_notCS Low	100		ns

Read cycle timing

Figure 9. Ctrl-E interface: read cycle timing in parallel modes 0 and 1

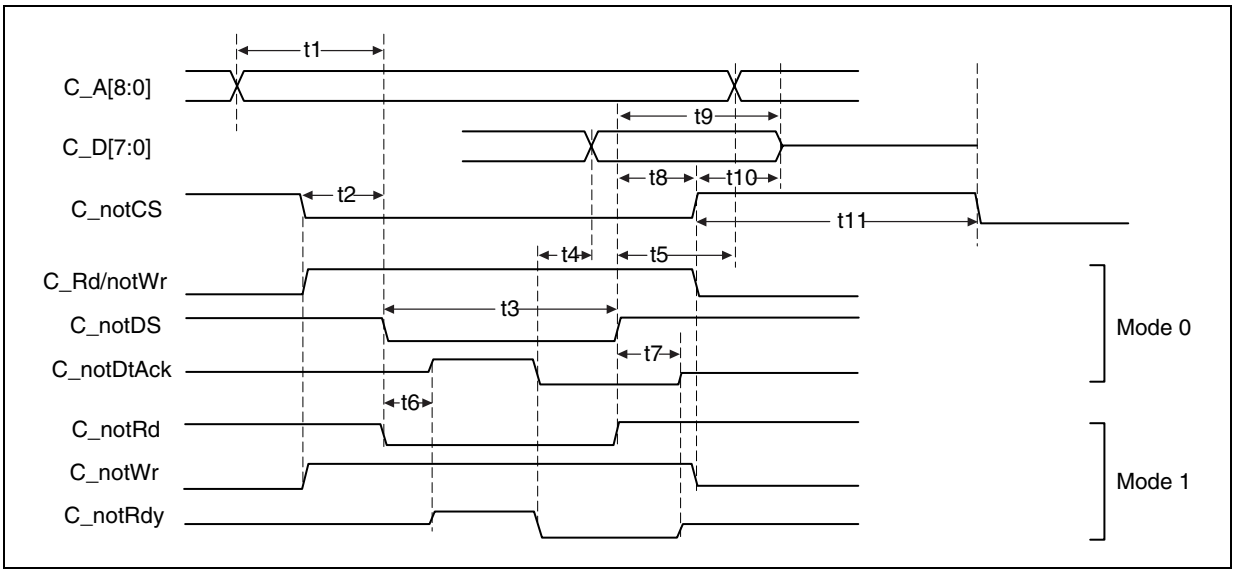


Table 9. read cycle timing in parallel modes 0 and 1

Symbol	Description	Min	Max	Unit
t1	C_A Setup to C_notDS (C_notRd) low	0		ns
t2	C_notCS, C_Rd/notWr setup to C_notDS (C_notRd) low	0		ns
t3	C_notDS (C_notRd) pulse width	215		ns
t4	C_D valid from C_notDtAck (C_notRdy) low		10	ns
t5	C_A, hold from C_notDS (C_notRd) high	0		ns
t6	C_notDtAck (C_notRdy) valid from C_notDS (C_notRd) high		15	ns
t7	C_notDtAck (C_notRdy) tri-state from C_notDS (C_notRd) high		10	ns
t8	C_notCS, C_Rd/notWr hold from C_notDS (C_notRd) high	10		ns
t9	Data tri-state from C_notDS (C_notRd) high	90	100	ns
t10	Data tri-state from C_notCS high	5	15	ns
t11	C_notCS high to C_notCS low (Min. time between 2 Accesses)	100		ns

Peripherals

UART

Two identical UARTs are implemented in MTC20136. They offer similar functionality to the standard 16C550 device. They can support bit rates of up to 115.2 K bps and contain two 16 byte FIFOs for receive and transmit.

General purpose I/Os

Four pins are available for general purpose IOs, two are used as inputs to specify the boot configuration and two are output under SW control. The latter can be used for instance to drive external LEDs.

Reset

The MTC20136 has an asynchronous, active-low reset pin. An external clock is required to leave the reset state.

Clock

The MTC20136 is operated from the 35.328MHz Master clock, also used by the other DynaMiTe chips.

ELECTRICAL SPECIFICATIONS

Generic

The values presented in the following table apply for all inputs and/or outputs unless specified otherwise. Specifically they are not influenced by the choice between CMOS or TTL levels.

Table 10. IO buffers generic DC characteristics

DC Electrical Characteristics **All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device**						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{IN}	Input leakage current	$V_{IN} = V_{SS}$, V_{DD}, no pull up/pull down	-1		1	µA
I_{OZ}	Tristate leakage current	$V_{IN} = V_{SS}$, V_{DD}, no pull up/pull down	-1		1	µA
I_{PU}	Pull up current	$V_{IN} = V_{SS}$	-25	-66	-125	µA
I_{PD}	Pull down current	$V_{IN} = V_{DD}$	25	66	125	µA
R_{PU}	Pull up resistance	$V_{IN} = V_{SS}$		50		kOhm
R_{PD}	Pull down resistance	$V_{IN} = V_{DD}$		50		kOhm

Table 11. IO buffers dynamic characteristics

DC Electrical Characteristics, important for transient but measured at (near) DC **All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device**						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
C_{IN}	Input capacitance	@f = 1MHz			5	pF
dI/dt	Current derivative	8 mA driver, slew rate control		23.5		mA/ns
		8 mA driver, no slew rate control		89		mA/ns
I_{peak}	Peak current	8 mA driver, slew rate control		85		mA
		8 mA driver, no slew rate control		100		mA
C_{OUT}	Output capacitance (also bidirectional and tristate drivers)	@f = 1MHz			7	pF

Input/Output CMOS Generic Characteristics

The values presented in the following table apply for all CMOS inputs and/ or outputs unless specified otherwise.

Table 12. CMOS IO buffers generic characteristics

DC Electrical Characteristics All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	Min	Typ	Max	Unit
V_{IL}	Low level input voltage				0.2* V_{DD}	V
V_{IH}	High level input voltage		0.8*V_{DD}			V
V_{HY}	Schmitt trigger hysteresis	slow edge < 1 V/ms, only for SCHMITx	0.8			V
V_{OL}	Low level output voltage	I_{OUT} = XmA[			0.4	V
V_{OH}	High level output voltage	I_{OUT} = -XmA[	0.85*V_{DD}			V

The reference current is dependent on the exact buffer chosen and is a part of the buffer name. The available values are 2, 4 and 8 mA.

Input/Output TTL Generic Characteristics

The values presented in the following table apply for all TTL inputs and/or outputs unless specified otherwise.

Table 13. TTL IO buffers generic characteristics

DC Electrical Characteristics All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Low level input voltage				0.8	V
V_{IH}	High level input voltage		2.0			V
V_{ILHY}	Low level threshold, falling	slow edge < 1 V/ms	0.9		1.35	V
V_{IHHY}	High level threshold, rising	slow edge < 1 V/ms	1.3		1.9	V
V_{HY}	Schmitt trigger hysteresis	slow edge < 1 V/ms	0.4		0.7	V
V_{OL}	Low level output voltage	I_{OUT} = XmA[			0.4	V
V_{OH}	High level output voltage	I_{OUT} = -XmA[	2.4			V

The reference current is dependent on the exact buffer chosen and is a part of the buffer name. The available values are currently 2, 4 and 8 mA.

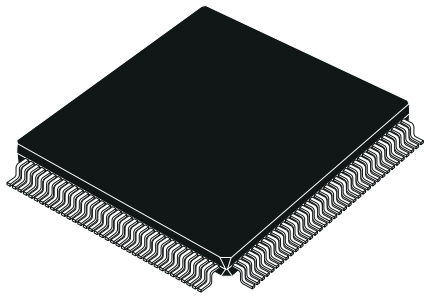
OPERATING CONDITIONS

Table 14. Operating Conditions

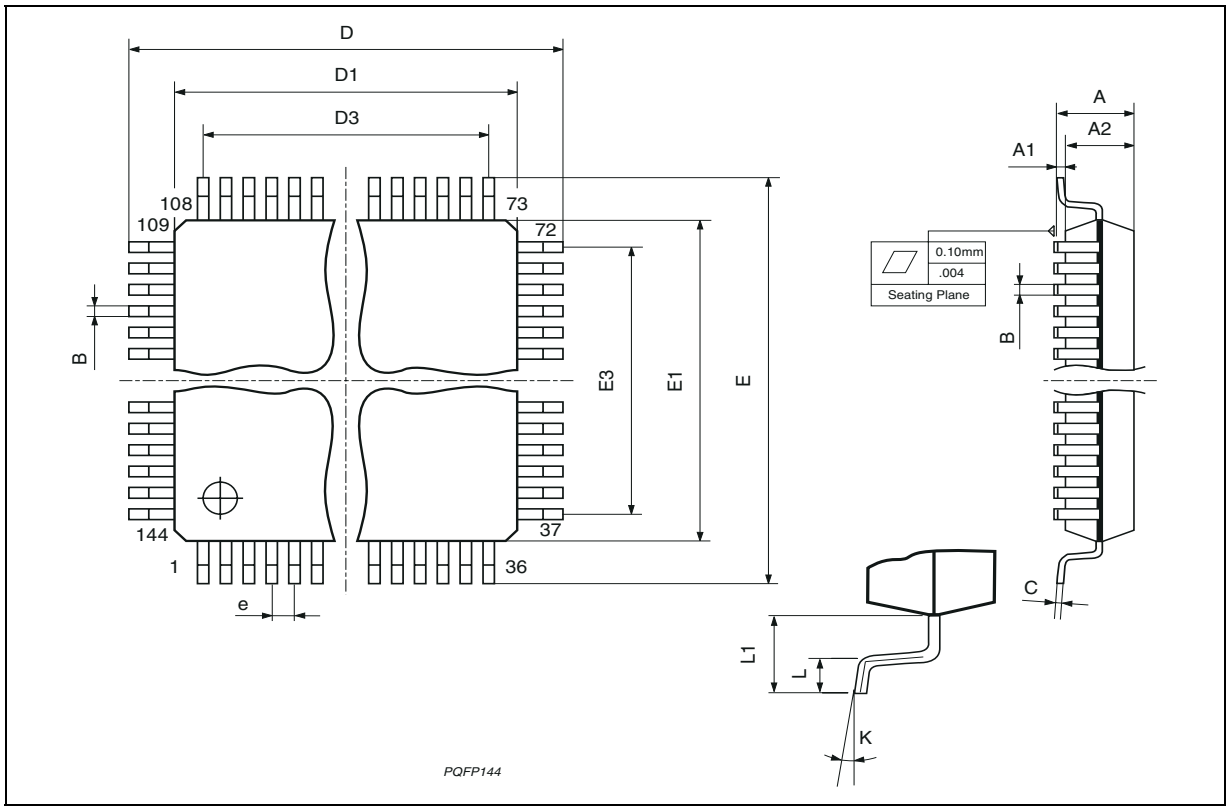
Maximum ratings						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{DD}	Supply voltage		3.0	3.3	3.6	V
T_{amb}	Ambient temperature1m/s airflow		-40		+85	°C
P	Power dissipation			300	400	mW

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.144
B	0.22		0.38	0.009		0.015
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		22.75			0.896	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		22.75			0.896	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA

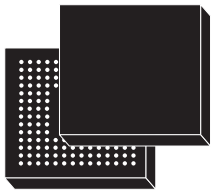


PQFP144



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.210		1.700	0.047		0.067
A1	0.270			0.010		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.02	0.021
D	11.85	12.00	12.15	0.466	0.472	0.478
D1		10.40			0.409	
E	11.85	12.00	12.15	0.466	0.472	0.478
E1		10.40			0.409	
e	0.720	0.800	0.880	0.028	0.031	0.034
f	0.650	0.800	0.950	0.025	0.031	0.037
ddd			0.120			0.004

OUTLINE AND MECHANICAL DATA



Body: 12 x 12 x 1.7mm

LFBGA160
Low Profile **F**ine Pitch **B**all **G**rid **A**rray