

# OKI Semiconductor

## MSC23B2321D-xxBS4/DS4

2,097,152-word x 32-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

### DESCRIPTION

The MSC23B2321D-xxBS4/DS4 is a fully decoded, 2,097,152-word x 32-bit CMOS dynamic random access memory module composed of four 16Mb DRAMs in SOJ packages mounted with eight decoupling capacitors on a 72-pin glass epoxy single-inline package. This module supports any application where high density and large capacity of storage memory are required.

### FEATURES

- 2,097,152-word x 32-bit organization
- 72-pin Single Inline Memory Module
  - MSC23B2321D-xxBS4 : Gold tab
  - MSC23B2321D-xxDS4 : Solder tab
- Single +5V supply  $\pm 10\%$  tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 1024cycles/16ms
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Fast page mode capability

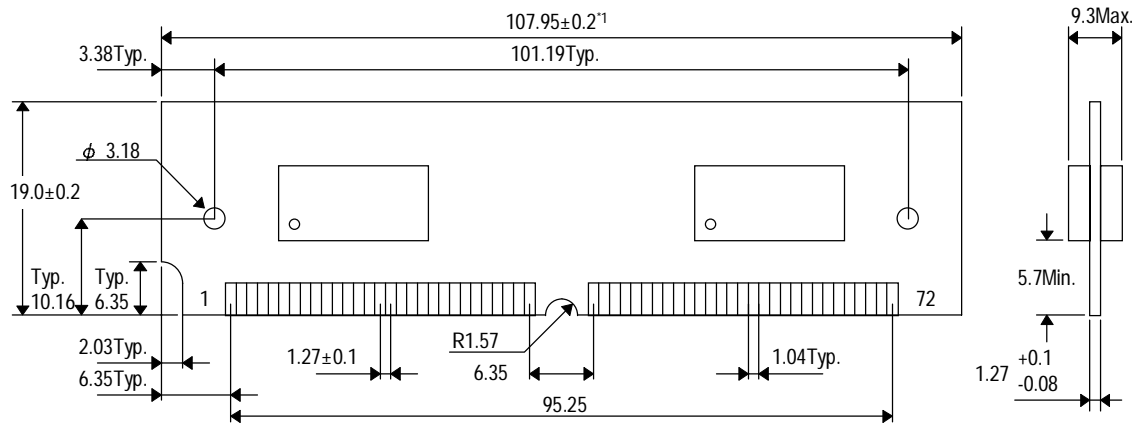
### PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>		Operating (Max.)	Standby (Max.)
MSC23B2321D-60BS4/DS4	60ns	30ns	15ns	110ns	1430mW	22mW
MSC23B2321D-70BS4/DS4	70ns	35ns	20ns	130ns	1320mW	

MODULE OUTLINE

MSC23B2321D-xxBS4/DS4

(Unit : mm)



\*1 The common size difference of the board width 12.5mm of its height is specified as  $\pm 0.2$ .  
The value above 12.5mm is specified as  $\pm 0.5$ .

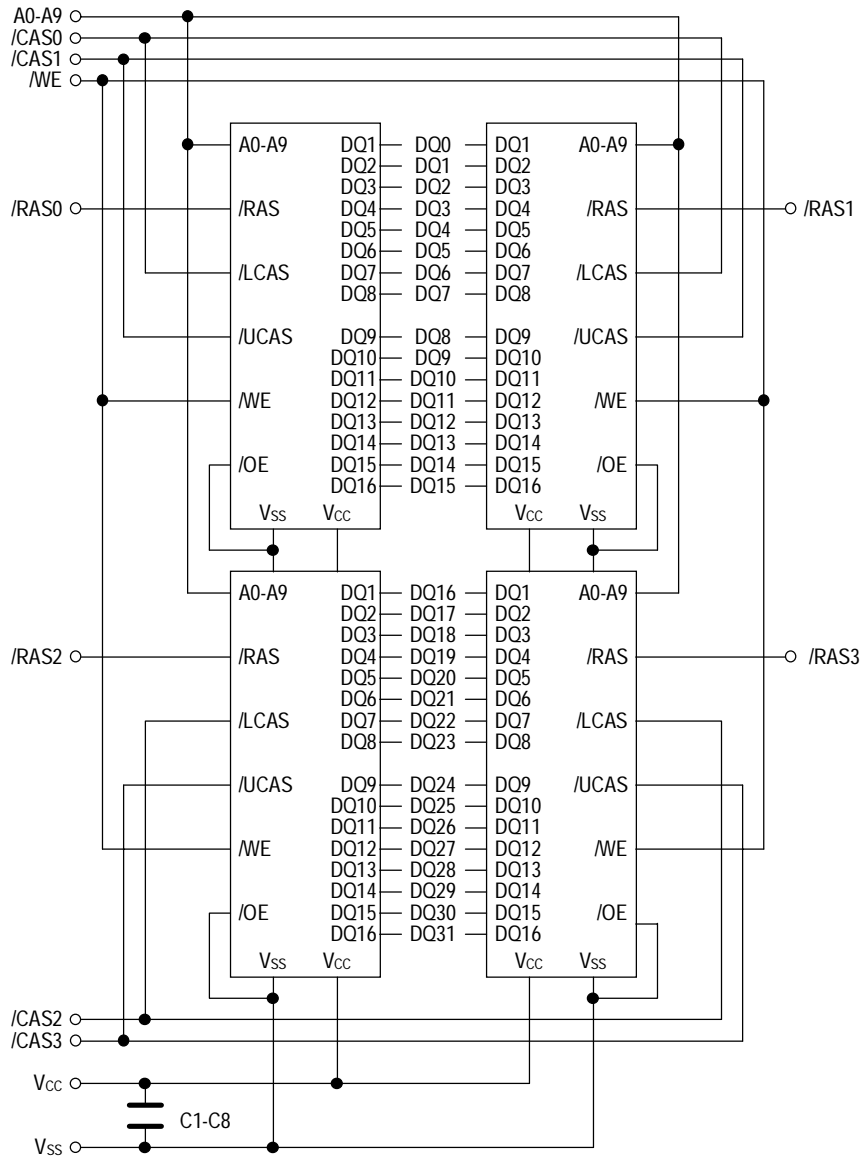
## PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>SS</sub>	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V <sub>SS</sub>	57	DQ12
4	DQ1	22	DQ5	40	/CAS0	58	DQ28
5	DQ17	23	DQ21	41	/CAS2	59	V <sub>CC</sub>
6	DQ2	24	DQ6	42	/CAS3	60	DQ29
7	DQ18	25	DQ22	43	/CAS1	61	DQ13
8	DQ3	26	DQ7	44	/RAS0	62	DQ30
9	DQ19	27	DQ23	45	/RAS1	63	DQ14
10	V <sub>CC</sub>	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	/WE	65	DQ15
12	A0	30	V <sub>CC</sub>	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	/RAS3	51	DQ9	69	PD3
16	A4	34	/RAS2	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V <sub>SS</sub>

## Presence Detect Pins

Pin No.	Pin Name	MSC23B2321D -60BS4/DS4	MSC23B2321D -70BS4/DS4
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	NC	V <sub>SS</sub>
70	PD4	NC	NC

BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 to +7.0	V
Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub>	-1.0 to +7.0	V
Short Circuit Output Current	I <sub>OS</sub>	50	mA
Power Dissipation	P <sub>D</sub> *	4	W
Operating Temperature	T <sub>OPR</sub>	0 to +70	°C
Storage Temperature	T <sub>STG</sub>	-40 to +125	°C

\* Ta = 25°C

### Recommended Operating Conditions

( Ta = 0°C to +70°C )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	6.5	V
Input Low Voltage	V <sub>IL</sub>	-1.0	-	0.8	V

### Capacitance

( V<sub>CC</sub> = 5V ± 10%, Ta = 25°C, f = 1 MHz )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C <sub>IN1</sub>	-	31	pF
Input Capacitance (/WE)	C <sub>IN2</sub>	-	35	pF
Input Capacitance (/RAS0- /RAS3)	C <sub>IN3</sub>	-	13	pF
Input Capacitance (/CAS0- /CAS3)	C <sub>IN4</sub>	-	20	pF
I/O Capacitance (DQ0 - DQ31)	C <sub>DQ</sub>	-	20	pF

Note: Capacitance measured with Boonton Meter.

## DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ C \text{ to } +70^\circ C)$ 

Parameter	Symbol	Condition	MSC23B2321D -60BS4/DS4		MSC23B2321D -70BS4/DS4		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	$I_{LI}$	$0V \leq V_{IN} \leq 6.5V$ ; All other pins not under test = 0V	-40	40	-40	40	$\mu A$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_{OUT} \leq 5.5V$	-20	20	-20	20	$\mu A$	
Output High Voltage	$V_{OH}$	$I_{OH} = -5.0mA$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2mA$	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	$I_{CC1}$	/RAS, /CAS cycling, $t_{RC} = \text{min.}$	-	260	-	240	mA	1, 2
Power supply current (Standby)	$I_{CC2}$	/RAS, /CAS = $V_{IH}$	-	8	-	8	mA	1
		/RAS, /CAS $\geq V_{CC} - 0.2V$	-	4	-	4	mA	1
Average Power Supply Current (/RAS only refresh)	$I_{CC3}$	/RAS cycling, /CAS = $V_{IH}$ , $t_{RC} = \text{min.}$	-	260	-	240	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	$I_{CC6}$	/RAS cycling, /CAS before /RAS	-	260	-	240	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	/RAS = $V_{IL}$ , /CAS cycling, $t_{PC} = \text{min.}$	-	260	-	240	mA	1, 3

- Notes: 1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.  
 2. Address can be changed once or less while /RAS =  $V_{IL}$ .  
 3. Address can be changed once or less while /CAS =  $V_{IH}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0°C to +70°C) Note: 1, 2, 3

Parameter	Symbol	MSC23B2321D -60BS4/DS4		MSC23B2321D -70BS4/DS4		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	110	-	130	-	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	40	-	45	-	ns	
Access Time from /RAS	t <sub>RAC</sub>	-	60	-	70	ns	4, 5, 6
Access Time from /CAS	t <sub>CAC</sub>	-	15	-	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	-	30	-	35	ns	4, 6
Access Time from /CAS Precharge	t <sub>CPA</sub>	-	35	-	40	ns	4
Output Low Impedance Time from /CAS	t <sub>CLZ</sub>	0	-	0	-	ns	4
/CAS to Data Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	-	16	-	16	ms	
/RAS Precharge Time	t <sub>RP</sub>	40	-	50	-	ns	
/RAS Pulse Width	t <sub>RAS</sub>	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	60	100K	70	100K	ns	
/RAS Hold Time	t <sub>RSH</sub>	15	-	20	-	ns	
/CAS Precharge Time (Fast Page Mode)	t <sub>CP</sub>	10	-	10	-	ns	
/CAS Pulse Width	t <sub>CAS</sub>	15	10K	20	10K	ns	
/CAS Hold Time	t <sub>CSH</sub>	60	-	70	-	ns	
/CAS to /RAS Precharge Time	t <sub>CRP</sub>	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge	t <sub>RHCP</sub>	35	-	40	-	ns	
/RAS to /CAS Delay Time	t <sub>RCD</sub>	20	45	20	50	ns	5
/RAS to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	-	0	-	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	-	10	-	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	-	0	-	ns	
Column Address Hold Time	t <sub>CAH</sub>	10	-	15	-	ns	
Column Address to /RAS Lead Time	t <sub>RAL</sub>	30	-	35	-	ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	-	0	-	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	-	0	-	ns	8
Read Command Hold Time referenced to /RAS	t <sub>RRH</sub>	0	-	0	-	ns	8

## AC Characteristics (2/2)

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0°C to +70°C ) Note: 1, 2, 3

Parameter	Symbol	MSC23B2321D -60BS4/DS4		MSC23B2321D -70BS4/DS4		Unit	Note
		Min.	Max.	Min.	Max.		
Write Command Set-up Time	t <sub>WCS</sub>	0	-	0	-	ns	
Write Command Hold Time	t <sub>WCH</sub>	10	-	15	-	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	-	10	-	ns	
Write Command to /RAS Lead Time	t <sub>RWL</sub>	15	-	20	-	ns	
Write Command to /CAS Lead Time	t <sub>CWL</sub>	15	-	20	-	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	-	0	-	ns	
Data-in Hold Time	t <sub>DH</sub>	10	-	15	-	ns	
/CAS Active Delay Time from /RAS Precharge	t <sub>RPC</sub>	5	-	5	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t <sub>CSR</sub>	10	-	10	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t <sub>CHR</sub>	10	-	10	-	ns	



- Notes:
1. A start-up delay of 200 $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
  2. The AC characteristics assumes  $t_T = 5$ ns.
  3.  $V_{IH}(\text{Min.})$  and  $V_{IL}(\text{Max.})$  are reference levels for measuring input timing signals. Transition time ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2TTL loads and 100pF.
  5. Operation within the  $t_{RCD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  $t_{RCD}(\text{Max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{Max.})$  limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  $t_{RAD}(\text{Max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{Max.})$  limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}(\text{Max.})$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.