Features

- **850–930 MHz Output Frequency**
- **Rx Current: 14.5 mA**
- **Low Sleep Mode Current: 1 uA**
- **DSSS Processing and BPSK Modulation/Demodulation**
- **Battery Voltage Monitoring Circuitry**
- **4 mW (6 dBm) Min. Transmit Power @ Vdd = 1.8V**
- **Serial Peripheral Interface (SPI) Control**
- **Power Supply Voltage Operating Range: 1.8V to 3.6V**
- **Low External Component Count**
- **48QFN Package**

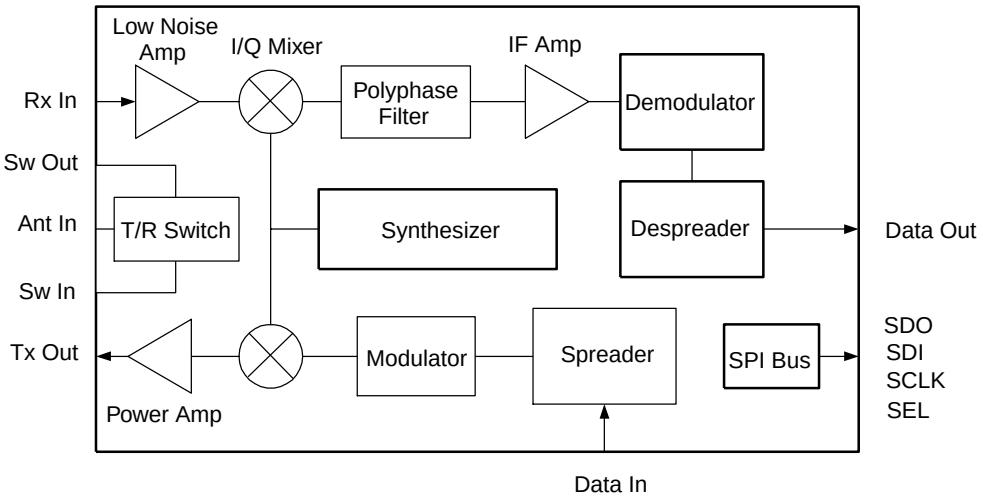
Applications

- **Low Band IEEE 802.15.4/ZigBee™-based Systems**
- **Industrial, Commercial, Home Lighting Control, Security, and HVAC**
- **Inventory Management**
- **Health Monitoring**
- **Wireless PC Peripherals such as Mouse, Keyboard, and Joystick**
- **Consumer Electronics Remote Controls and Toys**

Description

The Atmel AT86RF210 Z-Link™ Transceiver is a fully integated, low-cost ZigBee™ transceiver capable of transmitting and receiving BPSK modulated digital data over a frequency range of 868 MHz and 902–928 MHz using a minimum number of external components. It combines excellent RF performance with low cost, small size and low current consumption. The AT86RF210 includes a crystal stabilized Fractional-N synthesizer, BPSK transmitter and receiver, and full Direct Sequence Spread Spectrum Signal (DSSS) processing, including spreading and despreading. The device is fully compatable with IEEE 802.15.4 and ZigBee standards. It includes internal voltage regulation and battery monitoring circuitry and requires a minimum number of external support components.

Figure 1. Block Diagram



AT86RF210 Z-Link™ Transceiver

868/902–928 MHz Direct Sequence Spread Spectrum BPSK Transceiver

Preliminary

5033AS–WIRE–10/03

Figure 1. Functional Block Diagram

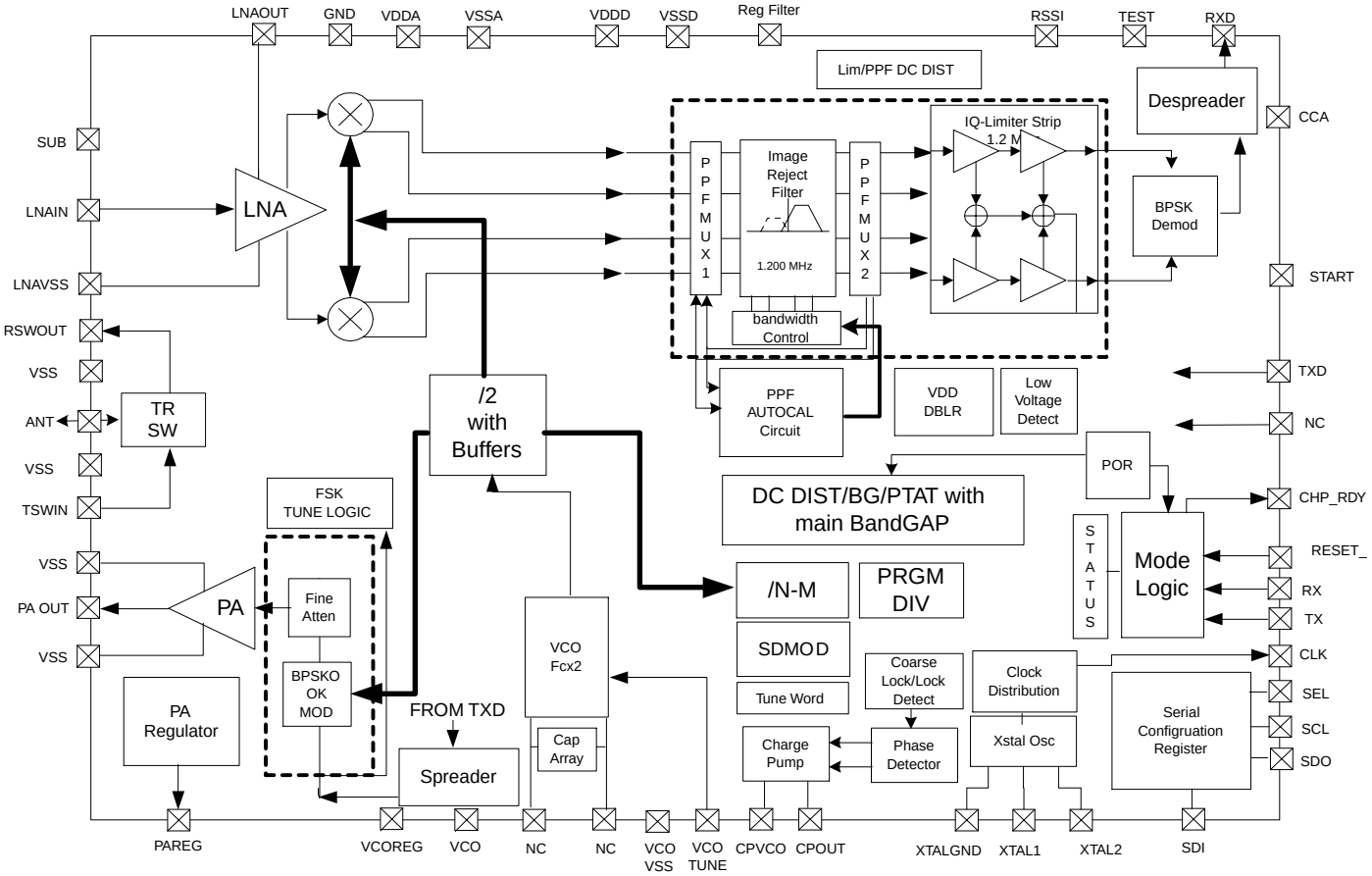


Table 1. Absolute Maximum Ratings*

Storage Temperature .....–65 to +150 Maximum Input Voltage.....VDD + 0.5V Maximum Operating Voltage (VDD) 4,5	*NOTE: Stresses beyond those listed in this table may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
TAMB	Operating temperature	–40		85	°C
VSUPPLY	Voltage supply range	1.8	2.7	3.6	V
HUMIDITY	Humidity	10		90	%

Note: Unit operation is guaranteed by design when operating within these ranges.

Table 3. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
IDDRX	Supply current, receive mode		14.5		mA
IDDTX	Supply current, transmit mode VDD = 3.3V		60		mA
IDDSleep	Supply current, sleep mode		1		uA
VPOR	Power-on reset voltage		1.5		V
VIH	Digital input voltage high	0.7*VDD			V
VIL	Digital input voltage low			0.3*VDD	V
VOH	Digital output voltage high	0.7*VDD			V
VOL	Digital output voltage low			0.3*VDD	V

Table 4. Receiver AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
FLO	Local oscillator operating range, external inductor	850		930	MHz
ZRF	Port impedance antenna input		50		Ohm
Rx Sens	Sensitivity, PER = 1% 40 kB/s, BW = 600 kHz BPSK modulation		–95		dBm
Rx NF	Receiver noise figure		6.0		dB
Rx P1dB	Receiver input 1dB compression point LNA gain max setting		–40		dBm
Rx IP3	Input IP3		–30		dBm
Rx LO Leakage	Receiver LO leakage (all possible paths)		–80		dBm
Pin	Maximum input signal; LNA gain min setting			–20	dBm
EDthresh	Default energy detection threshold (programmable)	–84			dBm
Ttx/rx	Turnaround time, transmit to receive			100	usec
Trx/tx	Turnaround time, receive to transmit			100	usec
RJAMadj	Receiver relative jamming resistance adjacent channel (desired signal = –89 dBm)	0			dB
RJAMalt	Receiver relative jamming resistance alternate channel (desired signal = –89 dBm)	30			dB
IFCF	IF center frequency		1.2		MHz
IFBW	IF bandwidth		600		KHz
Imreg	IF image rejection		–35		dB
RX IFS/N	RX IF SNR (600 KHz BW) Min input signal = –100 dBm		10		dB
Rx DR	Receiver max data rate		40		Kb/s
RSSI GN	RSSI Gain		1.0		uA/dB
RSSI RG	RSSI RANGE	–105		–30	dBm

Table 5. Transmitter AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Tx Pout	Transmitter output power: Vdd = 1.8V Vdd = 3.6V		 6 12		dBm
Rsym	Tx symbol rate 915 MHz band	40			Kbit/s
Rsym	Tx symbol rate 868 MHz band	20			Kbit/s
EVM	Transmit error vector magnitude measured over 1000 chips			35%	
PSD	Transmit power spectral density 915 MHz band; |f–fc| >1.2 MHz (absolute measured in 100 KHz resolution BW)			–20	dBm
Tx Pvar	Transmitter power variation over temperature		3		dB
Tx/Rx Z	Antenna switch impedance		50		Ohm
Tx spur	Transmit spurious within ±2 MHz		–25		dBc
Tx spur	Transmit spurious beyond ±2 MHz		–35		dBc
Tx Pcon	Transmitter power control resolution	0.25		0.75	dB
Tx Pran	Transmitter power control range		25		dB
Tx lvt	Transmitter low-voltage threshold	1.8		1.9	Volt
Tx lvpo	Transmitter low-voltage output power	0.25		0.50	mwatt
Tx tot	Transmitter turn-on time 90% full power		10		usec
Tx tofft	Transmitter turn-off time less than 10% of output power		10		usec

Table 6. Synthesizer AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F LO	Carrier frequency	850		930	MHz
LOPN	LO phase noise (integrated 10 Hz–100 KHz rms)		6		deg
Fpull	Crystal oscillator frequency pulling @ 25°C		20		ppm
Lopno	Local oscillator phase noise 2.0 MHz offset from LO		–95		dBc
TXtal	Crystal oscillator settling time		150		usec
TSynth	Phase locked loop settling time			100	usec
Synthres	Synthesizer tuning resolution		500		Hz

.

Table 7. Serial Configuration Register*

Symbol	Parameter	Min	Typ	Max	Unit
TRISE	CMOS input rise time		20		nsec
TFALL	CMOS input fall time		20		nsec
TCLKS	CLK setup time	25			nsec

Table 7. Serial Configuration Register* (Continued)

Symbol	Parameter	Min	Typ	Max	Unit
TCLKH	CLK hold time	25			nsec
TCLKW	CLK pulse width	50			nsec
TSDIS	SDI setup time	25			nsec
TSDIH	SDI hold time	25			nsec
TSDOD	SDO delay time		25		nsec

Note: *Rise and fall time is measured 10%–90%. Delay, setup, and hold times are measured 50%–50%

Table 8. Low Battery Detector Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Lvbat 0	Low voltage battery detector threshold voltage mode 0 (5 bit resolution)	1.5		3.5	Volt

Table 9. Preliminary PIN Description QFN48

PIN	Num	Type	Startup Cond	Description
SUB	1	V_I/O	GND	Substrate connection
LNARFIN	2	RF_I	NA	Low-noise amplifier RF input
LNAVSS	3	RF_I/O	NA	Analog ground for the LNA
RSWOUT	4	RF_I/O	NA	Transmit-receive switch out. Signal from ANT is routed through the TR switch to the LNA input.
VSS	5	RF_I/O	NA	Transmit-receive switch isolation ground 1.
ANT	6	RF_I/O	NA	Antenna RF input/output. Nominal impedance 50Ω, part of T/R switch. Routes signal to the LNA or from the PA.
VSS	7	RF_I/O	NA	Transmit-receive switch isolation ground 2.
TSWIN	8	RF_I/O	NA	Transmit-receive switch input. Signal from PA comes into TR switch and is routed to ANT.
PAOUT	9	RF_I/O	NA	PA signal routed into the T/R switch from the PA.
VSS	10			Pin not used
VDDA	11	V_I	NA	Secondary analog power supply input. Set in proximity to power amplifier circuits.
PAREG	12	A_O	NA	PA regulator output. Settable current source output for charging a large external capacitor during battery operation.
VCOVDD	13	V_I	NA	VCO power supply input
VCOREG	14	V_I	NA	External filter cap for the VCO regulator
No Connect	15		NA	Pin not used
No Connect	16		NA	Pin not used
VCOVSS	17	A_I/O	NA	VCO power supply ground
VCOTUNE	18	A_I	NA	LO VCO control input. An internal differential varactor diode tunes the LO frequency. The control voltage should be referenced to LOGND.

Table 9. Preliminary PIN Description QFN48 (Continued)

PIN	Num	Type	Startup Cond	Description
CPOUT	19	A_I	NA	Charge pump output
CPVSS	20	A_I/O	NA	Analog synthesizer ground
CPVDD	21	V_I	NA	Analog synthesizer power supply
XTAL1	22	A_I	NA	Crystal oscillator input 1. One side of oscillator crystal is connected to this pin.
XTAL2	23	A_I	NA	Crystal oscillator input 2. When internal oscillator is used, this pin has crystal connected. When external clock is used, the external clock is input on this pin.
XTALVSS	24	A_I/O	NA	Crystal oscillator ground
TXDAT	25	D_I	HIGH	Transmit data input from the controller
No Connect	26	D_I	LOW	Pin not used
SDI	27	D_I	NA	Serial data input Input to configuration data shift register. Data accepted at the rising edge of SCL.
SDO	28	D_O	NA	Output from configuration data shift register. Data changes at the falling edge of SCL.
SCLK	29	D_I	NA	Serial data clock
SEL	30	D_I	HIGH	SPI slave select line
SYSCLK	31	D_O	HIGH	Clock output to controller. Can be divided by 1 to 16.
TX	32	D_I	HIGH	Mode control input. TX HIGH with RX LOW causes chip to go to transmit.
RX	33	D_I	HIGH	Mode control input. RX HIGH with TX LOW causes chip to go to receive mode.
VDDDIG	34	V_I	NA	Digital power supply input
VSSDIG	35	V_I/O	NA	Digital power supply ground.
START	36	D_I	HIGH	Oscillator start. A transition on this pin will start the internal oscillator. A low on this pin allows the part to run from an external clock.
CHPRDY	37	D_O	LOW	Chip ready. Handshake signal between the controller and the chip. Also acts as fault interrupt.
RXDOUT	38	D_O	NA	Digital data from demodulator
No Connect	39		NA	Pin not used
No Connect	40		NA	Pin not used
No Connect	41			Pin not used
PPFREG	42	V_I/O	VDD	Filter cap for internal low dropout regulator for poly phase filter
RSSI	43	A_0		Logarithmic detection current
XTALMODE	44	D_IO	TBD	Test pin. Enables nand tree test or scan test.
CCA	45	D_O	LOW	Clear channel assessment. Digital signal indicates when channel activity is above a programmable threshold.

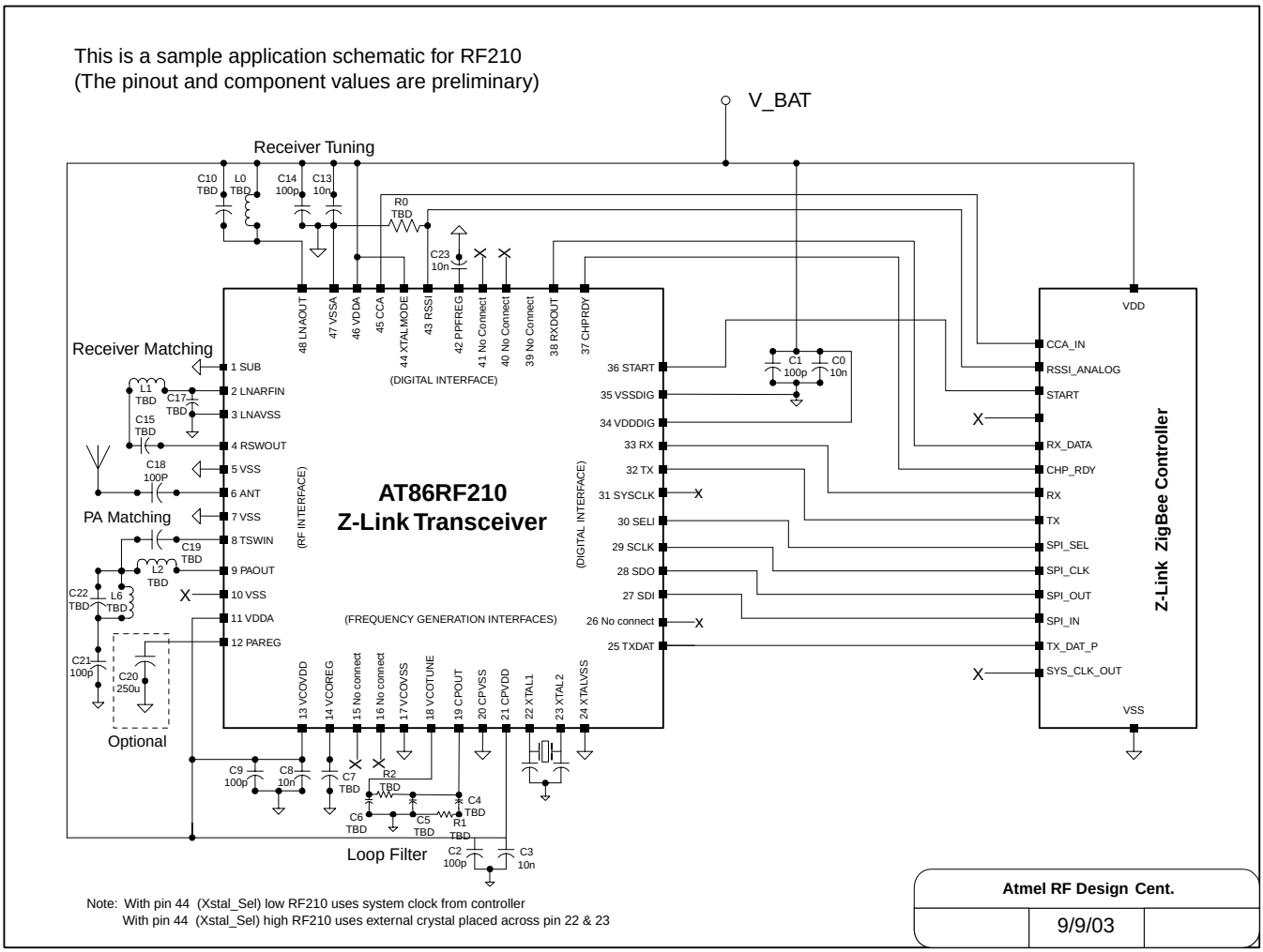
Table 9. Preliminary PIN Description QFN48 (Continued)

PIN	Num	Type	Startup Cond	Description
VDDA	46	V_I	NA	Analog (RF) power supply input
VSSA	47	V_I/O	GND	Analog (RF) power supply ground
LNAOUT	48	A_I/O		LNA external inductor. Collector inductor for LNA. P/O RF tuning network.

I/O Table Notes

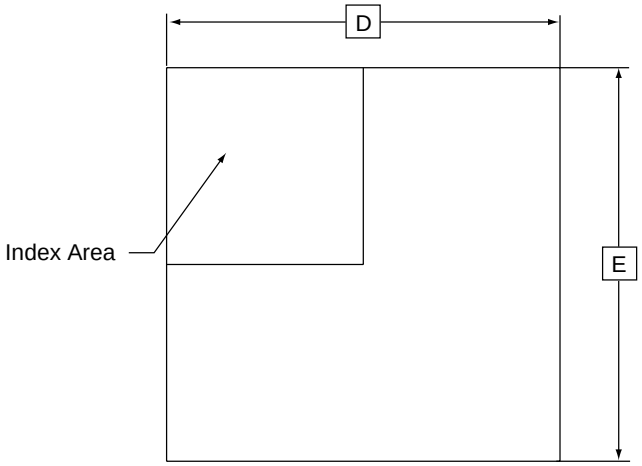
- RF_I RF input
- RF_I/O RF input/output
- Voltage_I/O Voltage input/output
- V_I Voltage input
- A_I Analog input
- A_O Analog output
- D_I Digital input
- D_O Digital output

Figure 2. Typical ZigBee Application Schematic

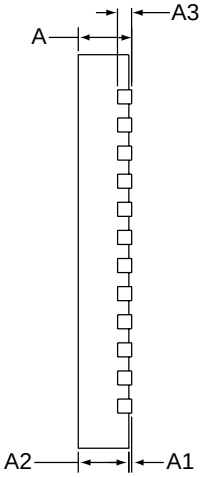


Package Drawing

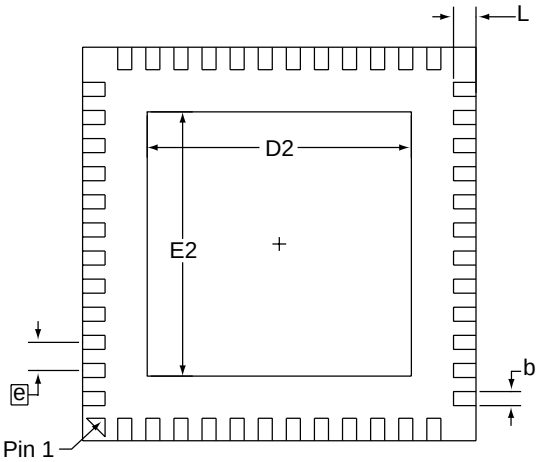
48QFN



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		7.00 BSC		
E		7.00 BSC		
D2	2.25	4.70	5.25	
E2	2.25	4.70	5.25	
A	0.80	0.90	1.00	
A1	0.0	0.02	0.05	
A2	0.0	0.65	1.00	
A3		0.20 REF		
L	0.30	0.40	0.50	
e		0.50 BSC		
b	0.18	0.23	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-2, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

12/10/02

	TITLE	DRAWING NO.	REV.
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