AMS

Austria Mikro Systeme International AG

AS8201

TTP/C-C1 Communications Controller

Data Sheet

Key Features

- First dedicated controller supporting TTP/C (time triggered protocol class C)
- Device for building up TTP/C nodes in a TTP/C local area networks (clusters).
- Suited for dependable distributed real-time systems with guaranteed response time
- application examples:
  automotive: braking, steering, vehicle dynamics control, drive train control
  industry: air plane flap control, rail way points
- Bit data rate 2 Mbits/s @ clock 20 MHz, 5.0V
- Fabricated in 0.6u CMOS process, automotive temperature range of -40 to 125deg C
- 1k x 16 RAM message, status and control area
- RAM for instruction code and configuration data
- 16 bit non-multiplexed host CPU interface
- 16 bit RISC architecture
- external firmware (FLASH memory) conforming the TTP/C specification
- automatic booting after power on
- software tools, design-in support, development boards available (http://www.tttech.com)
- 120 pin PQFP Package

Description

The TTP/C-C1 communications controller is the first integrated device supporting serial communication according to the TTP/C specification (time triggered protocol class C). It performs all communications tasks such as reception and transmission of messages in a TTP/C cluster without interaction of the host CPU.

TTP/C provides mechanisms that allow the deployment in high-dependability distributed real-time systems. It provides the following services:

- predictable transmission of messages with minimal jitter
- fault-tolerant distributed clock synchronisation
- consistent membership service with small delay
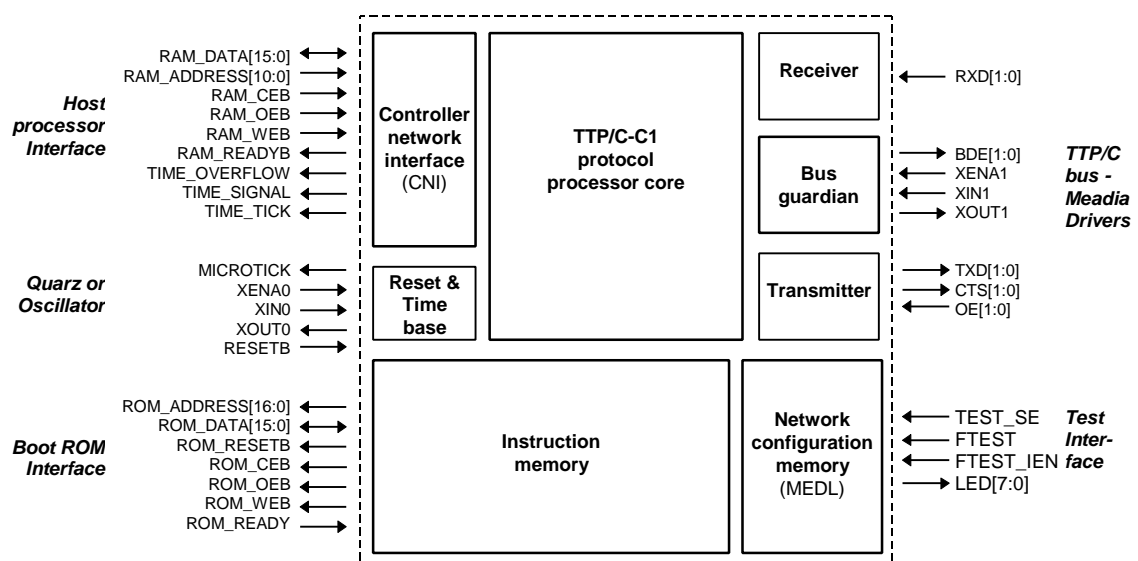- masking of single faults

Figure 1 Block Diagramm

The CNI (controller network interface) forms a temporal firewall. It decouples the controller network from the host subsystem by use of a dual ported RAM. This prevents the propagation of control errors. The interface to the host CPU is implemented as 16 bit wide non-multiplexed asynchronous bus interface.

TTP/C follows a conflict-free media access strategy called time-division-multiple access (TDMA). This means, TTP/C deploys a time slot technique based on a global time which is permanently synchronised. Each node is assigned a time slot in which it is allowed to perform transmit operation. The sequence of time slots is called TDMA round, a set of TDMA rounds forms a cluster cycle. After one cluster cycle the operation of the network repeats. The sequence of interactions forming the cluster cycle is defined in a static time schedule, called message-descriptor-list (MEDL). The definition of the MEDL in conjunction with the global time determines the response time for a service request.

The membership of all nodes in the network is evaluated by the communication controller. This information is presented in a consistent fashion to all correct cluster members. During operation, the status of every other node is propagated within one TDMA round. The MEDL is loaded into the configuration memory before run time when the system starts up.

Package and Pin Assignment
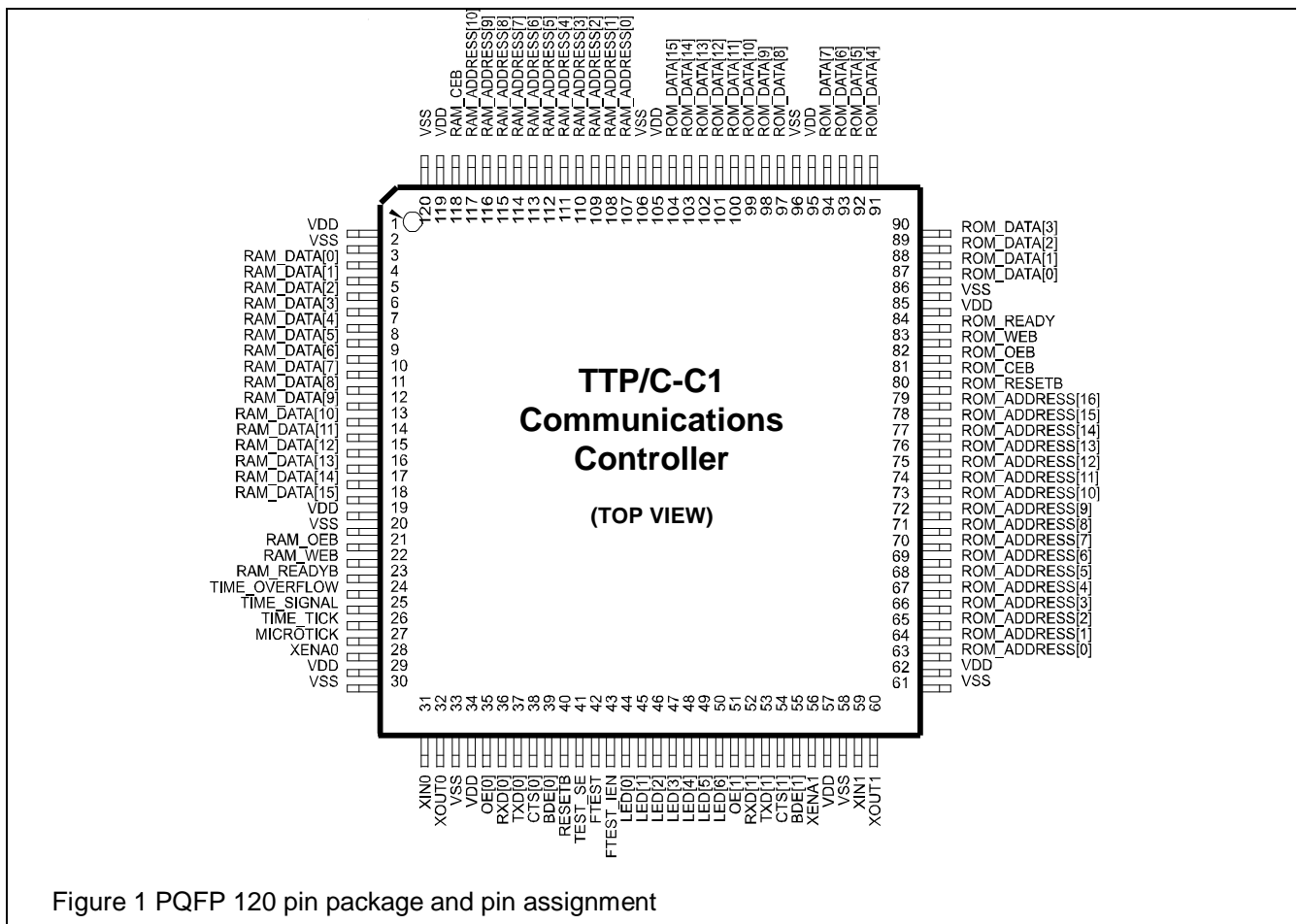
Type: PQFP 120, plastic quad flat package

Figure 1 PQFP 120 pin package and pin assignment

Pin Description

PinNr.	Pin Name	Dir	Description
1	VDD	P	positive power supply
2	VSS	P	negative power supply
3-18	RAM_DATA[0:15]	I/O	DPRAM data bus, tristate
19	VDD	P	positive power supply
20	VSS	P	negative power supply
21	RAM_OEB	I	DPRAM output enable, active low
22	RAM_WEB	I	DPRAM write enable, active low
23	RAM_READYB	O	DPRAM ready, active low, indicates read/write operation finished
24	TIME_OVERFLOW	O	CNI control signal, overflow of global time
25	TIME_SIGNAL	O	CNI control signal, CNI time signal
26	TIME_TICK	O	CNI clock signal, macrotick, typically about 1us at 20 MHz clock.
27	MICROTICK	O	output of main clock, inverted to signal applied at pin XOUT0.
28	XENA0	I	oscillator 0 (main clock) enable, active low.
29	VDD	P	positive power supply
30	VSS	P	negative power supply
31	XIN0	A	analog pad from oscillator / use as input when providing external clock
32	XOUT0	A	analog pad from oscillator / leave open when providing external clock
33	VSS	P	positive power supply
34	VDD	P	negative power supply
35	OE[0]	I	channel [0]: transmitter output enable
36	RXD[0]	I$_{PU}$	channel [0]: receiver input
37	TXD[0]	O	channel [0]: transmit data
38	CTS[0]	O	channel [0]: transmitter clear to send
39	BDE[0]	O	channel [0]: bus driver enable
40	RESETB	I	(1) main reset input signal, active low. When connected the internal power-on reset function is overridden (2) if unconnected: an internal reset is generated after power-on. Reset pulse duration typically 24 us.
41	TEST_SE	I$_{PD}$	test input: scan enable, active high
42	FTEST	I$_{PD}$	test input: functional test mode, active high
43	FTEST_IEN	I$_{PD}$	test input: instruction insertion enable, active high
44-50	LED[0:6]	O	test outputs: (1) in production test used as scan chain outputs (2) in operation: can be used as generic output port, e.g. to drive LEDs
51	OE[1]	I	channel [1]: transmitter output enable
52	RXD[1]	I$_{PU}$	channel [1]: receiver input
53	TXD[1]	O	channel [1]: transmit data
54	CTS[1]	O	channel [1]: transmitter clear to send
55	BDE[1]	O	channel [1]: bus driver enable
56	XENA1	I	oscillator 1 (bus guardian) enable, active low.
57	VDD	P	positive power supply
58	VSS	P	negative power supply
59	XIN1	A	analog pad from oscillator / use as input when providing external clock
60	XOUT1	A	analog pad from oscillator / leave open when providing external clock
61	VSS	P	positive power supply
62	VDD	P	negative power supply

63-79	ROM_ADDRESS[0:16]	O	ROM address bus, range = 2^17 = 128k
80	ROM_RESETB	O	ROM reset line, active low
81	ROM_CEB	O	ROM chip enable, active low
82	ROM_OEB	O	ROM output enable, active low
83	ROM_WEB	O	ROM write enable, active low; "read" if high.
84	ROM_READY	I$_{PU}$	ROM ready, signals read operation ready, leave open when un-used
85	VDD	P	positive power supply
86	VSS	P	negative power supply
87-94	ROM_DATA[0:7]	I/O	ROM data bus (lower byte)
95	VDD	P	positive power supply
96	VSS	P	negative power supply
97-104	ROM_DATA[8:15]	I/O	ROM data bus (higher byte)
105	VDD	P	positive power supply
106	VSS	P	negative power supply
107-117	RAM_ADDRESS[0:10]	I	DPRAM address bus, range = 2^11 = 2048
118	RAM_CEB	I	DPRAM chip enable, active low
119	VDD	P	positive power supply
120	VSS	P	negative power supply

I	Input CMOS
I$_{PU}$	Input CMOS with pull up
I$_{PD}$	Input CMOS with pull down
O	Output CMOS
I/O	Input/Output CMOS tristate
P	Power Pin
A	Analog Pin

Electrical Specifications

Absolute Maximum Ratings (Non Operating)

SYMBOL	PARAMETER	MIN	MAX	NOTE
VDD	DC Supply Voltage	-0.3 V	7.0 V	
V$_{in}$	Input Voltage on any Pin	- 0.3 V	VDD + 0.3 V	
I$_{in}$	Input Current on any Pin	-100 mA	100 mA	25°C
T$_{strg}$	Storage Temperature	-55 °C	150 °C	
T$_{sold}$	Soldering Temperature		260 °C	1)
t$_{sold}$	Soldering Time		10 sec	Reflow and Wave
H	Humidity	5 %	85 %	
ESD	Electrostatic Discharge	1000 V		HBM: R = 1.5 kΩ, C = 100 pF

1)   300 °C all ceramic packages and DIL plastic packages, 260 °C for surface mounting plastic packages

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability (e.g. hot carrier degradation).

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	NOTE
DC Supply Voltage	VDD	4.5 V	5.0 V	5.5 V	1)
Circuit Ground	VSS	0.0 V	0.0 V	0.0 V	
Static Supply Current	IDDS	----	40 µA	100 µA	2)
Operating Supply Current	IDD	----	110 mA	160 mA	fCLK = 20 MHz, VDD = 5.5 V 3)
Main clock frequency	CLK	5 MHz		20 MHz	oscillator pins XIN0, XOUT0
Bus Guardian clock frequency	CLK2	4 MHz		16 MHz	oscillatpr pins XIN1, XOUT1
Ambient Temperature	T_a	-40 ºC		+125 ºC	1)

1) The input and output parameter values in this table are directly related to ambient temperature and DC supply voltage. A temperature range other Ta_{min} to Ta_{max} or a supply voltage range other than VDD_{min} to VDD_{max} will affect these values and must be evaluated extra.

2) Static supply current IDDS is exclusive of input/output drive requirements and is measured at maximum VDD with the clocks stopped and all inputs tied to VDD or VSS, configured to draw minimum current.

3) Operating current is exclusive of input/output drive requirements and is measured at maximum VDD and maximum clock frequency 20 MHz.

DC Characteristics and Voltage Levels

CMOS I/O levels for specified voltage and temperature range unless otherwise noted.

Inputs Pins

Pin Name	Vil	Vih	Iil (1)		Iih(2)		NOTE
	max	min	min	max	min	max	
All inputs and IO pins (except: ROM_READY, RXD[0], RXD[1], FTEST, FTEST_IEN, TEST_SE)	30% VDD	70% VDD	NA	-1.0 µA	NA	1.0 µA	CMOS input (3)
ROM_READY, RXD[0], RXD[1]	30% VDD	70% VDD	-50 µA	-160 µA	NA	NA	CMOS with pull up (3)
FTEST, FTEST_IEN, TEST_SE	30% VDD	70% VDD	NA	NA	30 µA	160 µA	CMOS with pull down (3)

Notes:

1) Iil ist tested at VDDmax and Vin = 0

2) Iih ist tested at VDDmax and Vin = VDDmax

3) CMOS input levels are in percentage of VDD

4)

Output Pins

Pin Name	Vol	Voh	Iol (1)	Ioh(2)	Ioz(3)	NOTE
	V	V	mA	mA	µA	
All output pins (except XOUT0,XOUT1)	0.4	4.0	4.0	-4.0	NA	CMOS output
All I/O pins	0.4	4.0	4.0	-4.0	+/-10	CMOS output, Tristate

1) Vol, Iol is tested at VDD = 4.5V

2) Voh, Ioh is tested at VDD = 4.5V

3) Ioz is tested at VDD = 5.5V

AC Characteristics

Clock applied at XOUT0, resp. XOUT1.

PARAMETER	SYMBOL	PIN	MIN	MAX	NOTE
data in setup time	t_{setup}	all IN, all IO	20 ns		vs. Falling edge of clk @XOUT0, XOUT1
data output valid	tdav	all OUT, all IO		35 ns	vs. rising edge of clk @ XOUT0, XOUT1

Application Information

ROM Interface

Pin name	mode	width	comment
ROM_DATA	inout (tri)	16	ROM data bus
ROM_ADDRESS	out	17	ROM address bus
ROM_CEB	out	1	ROM chip enable
ROM_WEB	out	1	ROM write enable
ROM_OEB	out	1	ROM output enable
ROM_READY	in	1	ROM ready
ROM_RESETB	out	1	external reset line

Table 1 ROM Interface Ports

The timing and behaviour of the ROM Interface is designed to operate with the AM29F200 Flash EPROM or compatible devices. For detailed timing information see [AM29F200] [1]. Figure 2 shows the connection between TTP/C-C1 controller and the AM29F200 Flash. The contents of the Flash memory is loaded into the instruction memory by a boot sequencer automatically after power on.
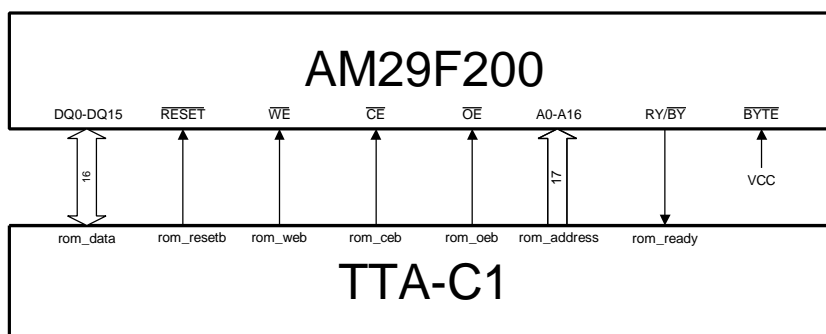

Figure 2 ROM Interface [2]

Host CPU Interface

The host CPU interface also referred as CNI (controller network interface) connects the application circuitry to the TTP/C network. As shown in Table 2 all RAM_-lines provide asynchronous read/write access to a dual ported RAM. There are no setup/hold constraints referred to the microtick (main clock "clk"). The signals have to be applied for certain duration according to Table 3. So, the applied signals get synchronised with the microtick. The TIME_-

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[1] [AMD96] Advanced Micro Devices, "Flash Memory Products - 1996 Data Book/Handbook", Advanced Micro Devices Inc., 1996.
[2] The label TTA-C1 stands for TTP/C-C1 in the following diagrams

lines signal to host CPU the global synchronous time of the TTP network and determine when to deliver, resp. to fetch data from the host interface. One of the lines may be connected to a interrupt inputs of the host CPU.

Pin Name	mode	width	comment
RAM_ADDRESS	in	11	DPRAM address bus, 11 bit
RAM_DATA	inout (tri)	16	DPRAM data bus, 16 bit
RAM_CEB	in	1	DPRAM chip enable
RAM_WEB	in	1	DPRAM write enable
RAM_OEB	in	1	DPRAM output enable
RAM_READYB	out	1	DPRAM ready
TIME_OVERFLOW	out	1	overflow of global time
TIME_SIGNAL	out	1	CNI time signal
TIME_TICK	out	1	macrotick

Table 2 Host Interface Ports

Figure 3: Read Cycle Timing

Addresses and RAM_WEB have to be stable before the falling edge of RAM_CEB. RAM_CEB has to be applied for 2 microticks. Addresses and RAM_WEB have to be applied for 3 microticks. Data can be read from RAM_DATA after 6 microticks. RAM_OEB drives the result of the (last) read operation to the RAM_DATA bus.
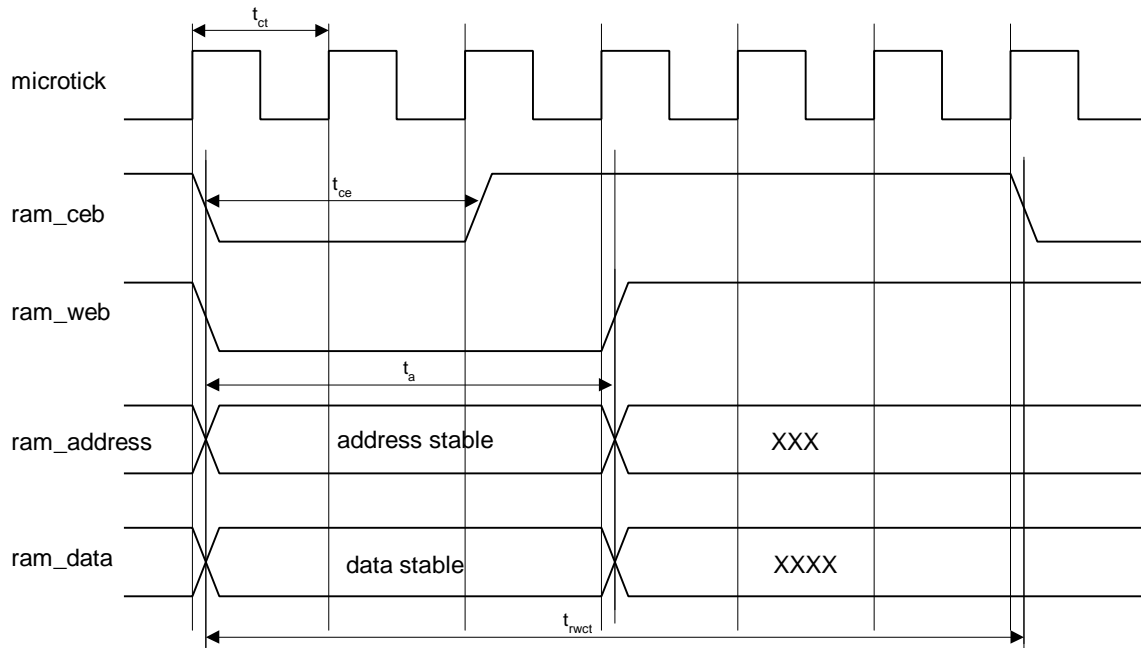
Figure 4: Write Cycle Timing

Addresses, data and RAM_WEB have to be stable before the falling edge of RAM_CEB.
RAM_CEB has to be applied for 2 microticks. Addresses, data, and RAM_WEB have to be
applied for 3 microticks.

Parameter	Symbol	Min	Typ	Max
controller cycle time	t_{ct}		50ns	
duration of chip enable	t_{ce}	87.5ns	100ns	112.5ns
address time	t_a	137.5ns	150ns	162.5ns
data valid time	t_{dv}		300ns	
read write cycle time	t_{rwct}		300ns	

Table 3: Host Interface Timing

Reset and Oscillator

Pin Name	mode	width	Comment
XIN0	in	1	controller oscillator input
XENA0	in	1	controller clock enable
XOUT0	out	1	controller oscillator output
XIN1	in	1	bus guardian oscillator input
XOUT1	out	1	bus guardian oscillator output
XENA1	in	1	bus guardian clock enable
RESETB	in	1	external reset
MICROTICK	out	1	controller clock (inverted)

Table 4: Reset and Oscillator Ports

External Reset Signal
To issue a reset of the chip the RESETB port has to be driven low for at least $200\mu s$. After
power-up the reset must overlap the build-up time of the oscillator circuit.

Integrated Power-On Reset

An internal Power-On Reset generator is integrated. When The supply voltage ramps up, the internal reset signal is kept active (low) for about 24 us typical. To activate this function the RESETB must be left unconnected.

Parameter	Symbol	Min	Typ	Max	Unit
supply voltage slope	dV/dt	250	-	-	kV/s
power on reset active time after VDD > 1,2V	t_{pon_res}	16	24	34	us
external reset low to internal high	t_{res_fall}	81	118	173	ns
external reset high to internal low	t_{reset_rise}	130	129	104	ns

Oscillator circuitry

The internal oscillator cell requires an external quartz or an external oscillator respectively (Figure 5, Figure 6). The internal controller clock is available at the port MICROTICK (inverted to clock signal applied at XOUT0).
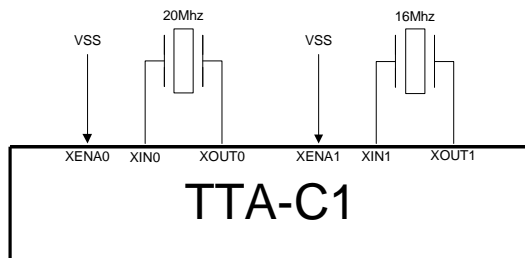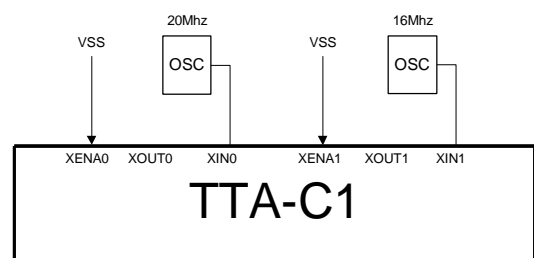

Figure 5: Quartz Circuit

Figure 6: Oscillator Circuit

TTP/C Bus Interface

Pin Name	mode	width	comment
CTS	out	2	transmitter clear to send
OE	in	2	transmitter output enable
TXD	out	2	transmit data
RXD	in	2	receiver input
BDE	out	2	bus driver enable

Table 5: TTP/C Bus Interface Ports

The controller can be connected to transceivers with recessive state and to transceivers with three-state outputs, respectively. For safe operation of the device the bus driver enable signal BDE must be connected with output enable OE. To deactivate the bus guardian the OE signal has to be tied to VCC. Applications with recessive state transceivers do not use the CTS signal.
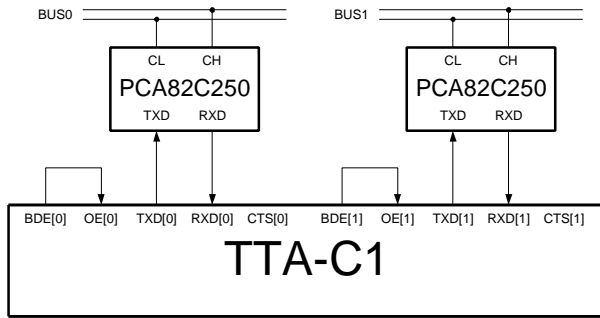
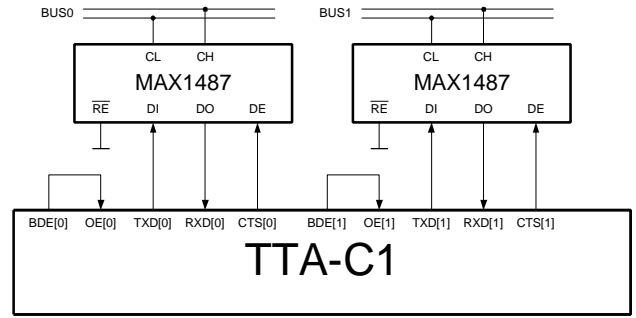Figure 7: Transceivers with Recessive State

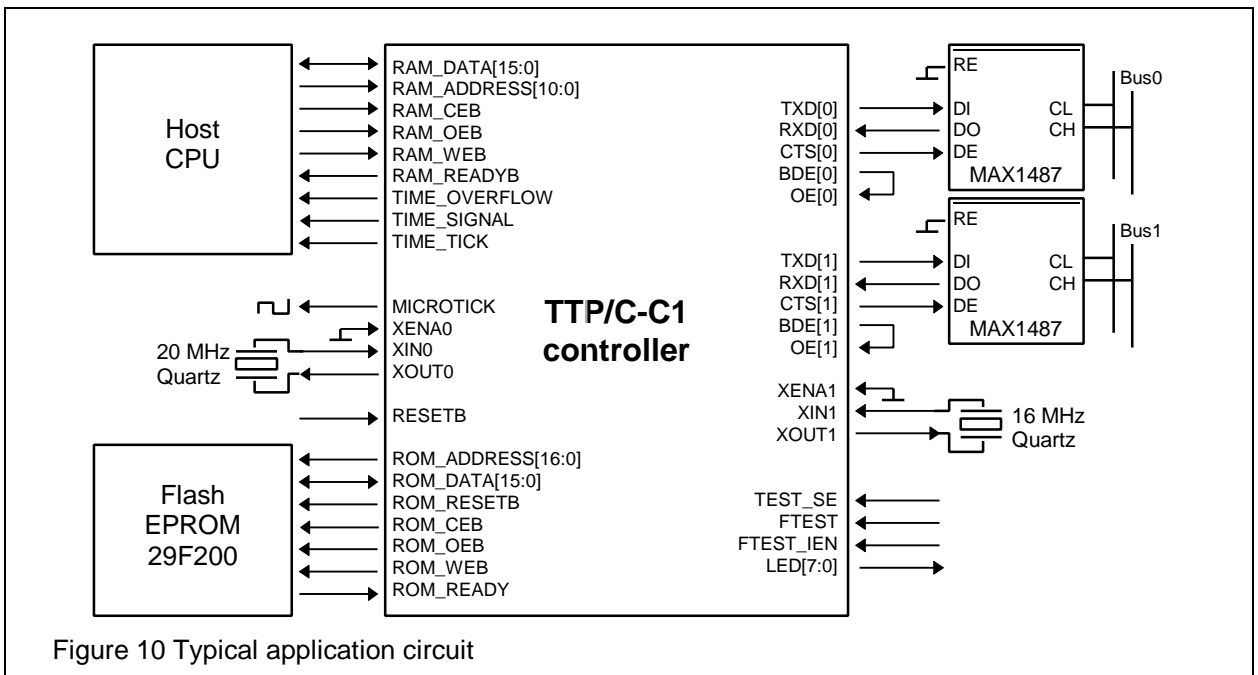Figure 8: Transceivers with Three-State Output

Test Interface

Pin Name	mode	width	comment
FTEST	in (pull down)	1	functional test mode
FTEST_EIN	in (pull down)	1	instruction insertion enable
LED	out	7	LED vector
TEST_SE	in (pull down)	1	scan enable

Table 6: Test Interface Ports

The ports of the test interface support the manufacturing test of the chip. In the application environment FTEST, FTEST_IEN, and TEST_SE are not connected. The LED bus can be used as a universal output port. The driver strength of the LED ports is 4mA.

Principles of Operation

The next 2 figures show a typical TTP/C node as it is to be deployed in a TTP/C communication cluster. The circuit example uses the MAX1487 as driver, the host CPU may be selected by the user and a 29F200 Flash memory. For detailed information the protocol on application programming refer to the manuals provided by TTTech Computer Technik GmbH.

Figure 9 Typical node in a TTP/C cluster using the TTP/C-C1

Figure 10 Typical application circuit

Ordering Information

Part Number: AS8201
Part Name: TTP/C-C1 Communications Controller
Package: PQFP 120

Support

Software tools, hardware development boards, evaluation systems and extensive support on TTP/C system integration as well as consulting is provided by

TTTech Computertechnik GmbH
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