Thermoelectric Cooler Controller

Preliminary Technical Data ADN8830

FEATURES
High Efficiency
Small Size: 5 mm × 5 mm LFCSP
Low Noise: < 0.5% TEC Current Ripple
Long Term Temperature Stability: ±0.01°C
Frequency and Phase Compensation in Control Loop
Temperature Lock Indication
Thermistor Linearity Correction Compatibility
Temperature Monitoring Output
Oscillator Synchronization with an External Signal
Clock Phase Adjustment for Multiple Controllers
Programmable Switching Frequency up to 1 MHz
Thermistor Failure Alarm
Maximum TEC Voltage Programmability

APPLICATIONS
Thermoelectric Cooler (TEC) Temperature Control
Resistive Heating Element Control
Temperature-Stabilization Substrate (TSS) Control

GENERAL DESCRIPTION

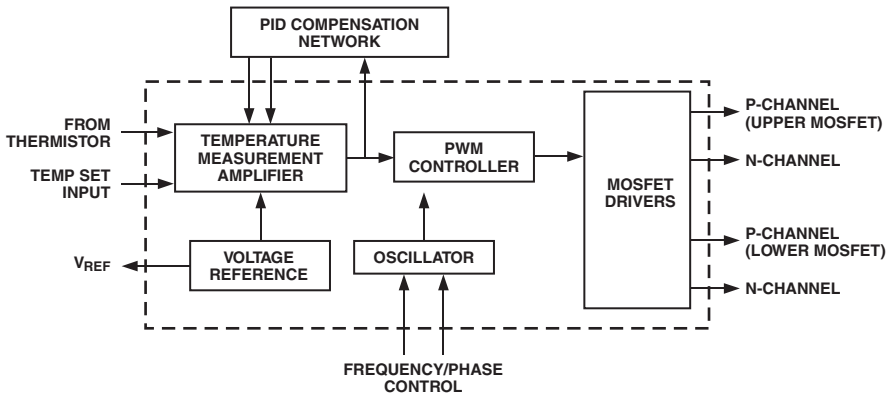
The ADN8830 is a monolithic controller that drives a Thermoelectric Cooler (TEC) to stabilize the temperature of a laser diode or a passive component used in telecommunications equipment.

This device relies on a Negative Temperature Coefficient (NTC) thermistor to sense the temperature of the object attached to the TEC. The target temperature is set with an analog input voltage either from a DAC or with an external resistor divider.

The loop is stabilized by a PID compensation amplifier with high stability and low noise. The compensation network can be adjusted by the user to optimize temperature settling time. The component values for this network can be calculated based on the thermal transfer function of the laser diode or obtained from the look-up table given in the applications notes.

Voltage outputs are provided to monitor both the temperature of the object and the voltage across the TEC. A 2.5 V voltage reference is also provided.

FUNCTIONAL BLOCK DIAGRAM



REV. PrC

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ADN8830–SPECIFICATIONS (@ V_{DD} = 3.3 V to 5.0 V, V_{GND} = 0 V, T_A = +25°C, T_{SET} = 25°C, using typical application configuration as shown in Figure 1, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TEMPERATURE STABILITY						
Long Term Stability		Using 10 kΩ thermistor with, α = –4.4% at 25°C			0.01	°C
PWM OUTPUT DRIVERS						
Output Transition Time	t_R, t_F	C_L = 3,300 pF		20		ns
Non-Overlapping Clock Delay				65		ns
Maximum Gate Drive Current	$I_{MAX(N1,P1)}$		1.0			A
Output Resistance	$R_{O(N1,P1)}$	I_L = 50 mA		6		Ω
Output Voltage Swing	OUTA	V_{LIM} = 0 V	0		V_{DD}	V
Output Voltage Ripple	ΔOUTA	f_{CLK} = 1 MHz		0.2		%
Output Current Ripple	ΔI_{TEC}	f_{CLK} = 1 MHz		0.2		%
LINEAR OUTPUT AMPLIFIER						
Capacitive Load Drive	$C_{LOAD(N2, P2)}$				10	nF
Output Resistance	$R_{0, P2}$	I_{OUT} = 2 mA		85		Ω
	$R_{0, N2}$	I_{OUT} = 2 mA		178		Ω
Output Voltage Swing	OUTB		0		V_{DD}	V
POWER SUPPLY						
Power Supply Voltage	V_{DD}		3.3		5.0	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 3.3 V to 5 V, V_{TEC} = 0 V	60	92		dB
		–40°C ≤ T_A ≤ +85°C	50			
Supply Current	I_{SY}	PWM not switching		8	12	mA
		–40°C ≤ T_A ≤ +85°C			150	mA
Shutdown Current	I_{SD}	Pin 10 = 0 V		5		μA
Soft-Start Charging Current	I_{SS}			100		μA
Undervoltage Lockout	V_{OLOCK}	Low to high threshold		2.6	2.7	V
ERROR AMPLIFIER						
Input Offset Voltage	V_{OS}	V_{CM} = 1.5 V		50	250	μV
Gain	$A_{V, IN}$			20		V/V
Input Voltage Range	V_{CM}		0.2		2.0	V
Common-Mode Rejection Ratio	CMRR	0.2 V < V_{CM} < 2.0 V		68		dB
		–40°C ≤ T_A ≤ +85°C	60			dB
Open-Loop Input Impedance	R_{IN}			1.0		GΩ
Gain-Bandwidth Product	GBW			2		MHz
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}	I_{REF} < 2 mA	2.45	2.47	2.49	V
OSCILLATOR						
Sync Range	f_{CLK}	Pin 25 connected to external clock	200		1,000	kHz
Oscillator Frequency	f_{CLK}	Pin 24 = V_{DD}; (R = 300 kΩ; Pin 25 = GND)	480	500	520	kHz
Phase Adjustment	ϕ_{CLK}		45		360	Degrees
LOGIC CONTROL[1]						
Logic Low Input Threshold					0.2	V
Logic High Input Threshold			3.0			V
Logic Low Output Level					0.2	V
Logic High Output Threshold			V_{DD} – 0.2			V

NOTE
[1]Logic inputs meet typical CMOS I/O conditions for source/sink current (~1 μA).

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +6 V
Input Voltage . . . . . GND to V_S +0.3 V
Output Short Circuit to GND Duration . . . . . TBD
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range
CP Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . +300°C

ESD RATINGS

883 (Human Body) Model . . . . . 2.0 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}[1]	θ_{JC}	Units
32-Lead LFCSP (ACP)	35	10	°C/W

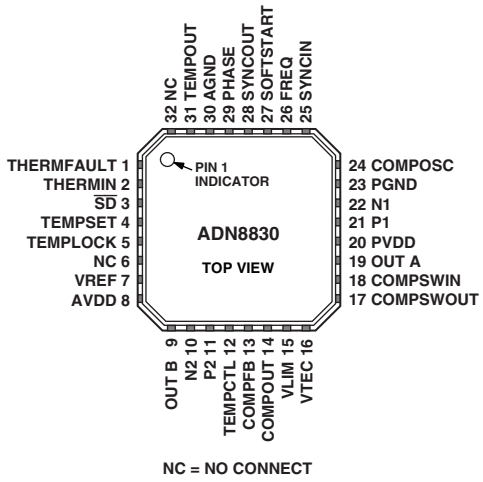
NOTE

[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device soldered in 4-layer circuit board for surface mount packages.

ORDERING GUIDE

Temperature Model	Package Range	Package Description	Package Option	Branding Information
ADN8830ACP	–40°C to +85°C	32 -Lead Chip Scale Micro-Lead Frame LFCSP	CP-32	

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN8830 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. ADN8830 Pin Descriptions

Pin #	Name	Type	Description
1	THERMFAULT	Digital Output	Indicates an open or short-circuit condition from thermistor.
2	THERMIN	Analog Input	Thermistor feedback input.
3	$\overline{SD}$	Digital Input	Puts device into low current shutdown mode. Active low.
4	TEMPSET	Analog Input	Target temperature input.
5	TEMPLOCK	Digital Output	Indicates when thermistor temperature is within ±0.1°C of target temperature as set by TEMPSET voltage.
6	NC		No connection, except as noted in applications note.
7	VREF	Analog Output	2.5 V reference voltage.
8	AVDD	Power	Power for non-driver sections. 3.3 V min; 5 V max.
9	OUT B	Analog Input	Linear output feedback. Will typically connect to TEC+ pin of TEC.
10	N2	Analog Output	Drives linear output external NMOS gate.
11	P2	Analog Output	Drives linear output external PMOS gate.
12	TEMPCTL	Analog Output	Output of error amplifier. Connects to COMPFB through feedforward section of compensation network.
13	COMPFB	Analog Input	Feedback summing node of compensation amplifier. Connects to TEMPCTL and COMPOUT through compensation network.
14	COMPOUT	Analog Output	Output of compensation amplifier. Connects to COMPFB through feedback section of compensation network.
15	VLIM	Analog Input	Sets maximum voltage across TEC.
16	VTEC	Analog Output	Indicates relative voltage across the TEC. 1.5 V corresponds to 0 V across TEC. 3.0 V indicates maximum output voltage, maximum heat transfer through TEC.
17	COMPSWOUT	Analog Output	Compensation for switching amplifier.
18	COMPSWIN	Analog Input	Compensation for switching amplifier. Capacitor connected between COMPSWIN and COMPSWOUT.
19	OUT A	Analog Input	PWM output feedback. Will typically connect to TEC- pin of TEC.
20	PVDD	Power	Power for output driver sections. 3.3 V min; 5 V max.
21	P1	Digital Output	Drives PWM output external PMOS gate.
22	N1	Digital Output	Drives PWM output external NMOS gate.
23	PGND	Ground	Power ground. External NMOS devices connect to PGND. Can be connected to digital ground as noise sensitivity at this node is not critical.
24	COMPOSC	Analog Input	Connect as indicated in applications note.
25	SYNCIN	Digital Input	Optional clock input. If not connected, clock frequency set by FREQ pin.
26	FREQ	Analog Input	Sets switching frequency.
27	SOFTSTART	Analog Input	Controls initialization time for ADN8830 with capacitor to ground.
28	SYNCOUT	Digital Output	Phase adjusted clock output. Phase set from PHASE pin. Can be used to drive SYNCIN of other ADN8830 devices.
29	PHASE	Analog Input	Sets switching and SYNCOUT clock phase relative to SYNCIN clock.
30	AGND	Ground	Analog ground. Should be low noise for highest accuracy.
31	TEMPOUT	Analog Output	Indication of thermistor temperature.
32	NC		No connection.

APPLICATIONS NOTES

Principle of Operation

The ADN8830 is a controller for a Thermoelectric Cooler (TEC) and is used to set and stabilize the temperature of the TEC. A voltage applied to the input of the ADN8830 corresponds to a target temperature set point. The appropriate current is then applied to the TEC to either pump heat to or away from the object whose temperature is being regulated. The temperature of the object is measured by a thermistor and is fed back to the ADN8830 to correct the loop and settle the TEC to the appropriate final temperature. For best stability, the thermistor should be mounted in close proximity to the object. In most laser diode modules, the TEC and thermistor are already mounted in the unit and are used to regulate the temperature of the laser diode.

For a TEC controller to provide a complete solution it requires a precision input amplifier stage to accurately measure the difference between the target temperature and the actual temperature of the object, a compensation amplifier to optimize the temperature step response of the TEC, and a high output current stage to provide the required current to the TEC. Because of the high output currents involved, a TEC controller should operate with high efficiency to minimize the heat generated from power dissipation. In addition, an effective controller should operate down to +3.3 V and have an indication of when the target temperature has been reached. The ADN8830 accomplishes all of these requirements with a minimum of external components. Figure 1 shows a reference design for a typical application.

Temperature is monitored by connecting the measurement thermistor to a precision amplifier, called the error amplifier, with a simple resistor divider. This voltage is compared against the temperature set input voltage creating an error voltage that is proportional to their difference. To maintain accurate wavelength and power from the laser diode, this difference voltage must be as accurate as possible. For this reason self correction auto-zero amplifiers are used in the input stage of the ADN8830, providing a maximum offset voltage of 250 µV over time and temperature. This results in final temperature accuracy within ±0.01°C in typical applications, eliminating the ADN8830 as an error source in the temperature control loop. A logic output is

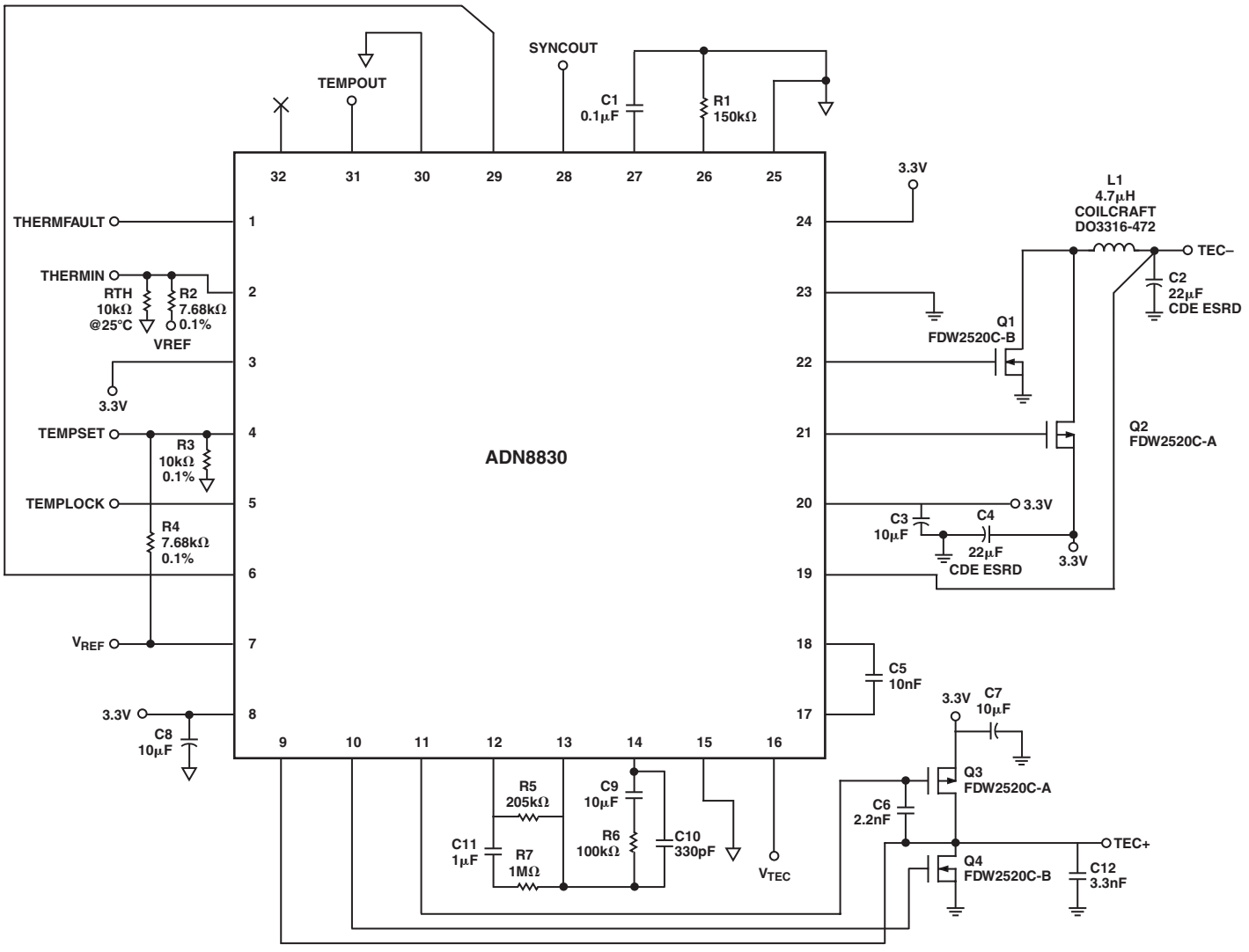


Figure 1. ADN8830 Typical Application Schematic

provided at TEMPLOCK to indicate when the target temperature has been reached.

The output of the error amplifier is then fed into a compensation amplifier. An external network consisting of a few resistors and capacitors is connected around the compensation amplifier. This network can be adjusted by the user to optimize the step response of the TEC's temperature either in terms of settling time or maximum current change. Details of how to adjust the compensation network are given in the application notes.

The ADN8830 can be easily integrated with a wavelength locker for fine-tune temperature adjustment of the laser diode for a specific wavelength. This is a useful topology for tunable wavelength lasers. Details are highlighted in the applications section.

The TEC is driven differentially using an H-bridge configuration to maximize the output voltage swing. The ADN8830 drives external transistors which are used to provide current to the TEC. These transistors can be selected by the user based on the maximum output current required for the TEC. The maximum voltage across the TEC can be set through use of the VLIM pin on the ADN8830.

To further improve the power efficiency of the system, one side of the H-bridge uses a switched output. Only one inductor and one capacitor are required to filter out the switching frequency. The output voltage ripple is a function of the output inductor and capacitor and the switching frequency. For most applications, a 4.7 µH inductor, 22 µF capacitor, and switching frequency of 1 MHz maintains less than ±0.5% worst case output voltage ripple across the TEC. The other side of the H-bridge does not require any additional circuitry.

The oscillator section of the ADN8830 controls the switched output section. A single resistor sets the switching frequency from 100 kHz to 1 MHz. The clock output is available at the SYNCOUT pin and can be used to drive another ADN8830 device by connecting to its SYNCIN pin. The phase of the clock is adjusted by a voltage applied to the PHASE pin, which can be set by a simple resistor divider. Phase adjustment allows two or more ADN8830 devices to operate from the same clock frequency and not have all outputs switch simultaneously, which could create an excessive power supply ripple. Details of how to adjust the clock frequency and phase are given in the applications section of the datasheet.

For effective indication of a catastrophic system failure, the ADN8830 alerts to open-circuit or short-circuit condition from the thermistor, preventing an erroneous and potentially damaging temperature correction from occurring. With some additional external circuitry, output over-current detection can be implemented to provide warning in the event of a TEC short circuit failure. This circuit is highlighted in the application notes.

Signal Flow Diagram

Figure A24 shows the signal flow diagram through the ADN8830. The input amplifier is fixed with a gain of 20. The voltage at TEMPCTL can be expressed as:

$$TEMPCTL = 20 \times (TEMPSET - THERMIN) + 1.5 \quad (0)$$

When the temperature is settled, the thermistor voltage will be equal to the TEMPSET voltage and the output of the input amplifier will be 1.5 V.

The voltage at TEMPCTL is then fed into the compensation amplifier whose frequency response is dictated by the compensation network. Details on the compensation amplifier can be found in the Compensation Loop section. When configured as a simple integrator or PID loop, the DC forward gain of the compensation section is equal to the open loop gain of the compensation amplifier, which is over 80 dB or 10,000. The output from the compensation loop at COMPOUT is then fed to the linear amplifier. The output of the linear amplifier at OUT_B is fed with COMPOUT into the PWM amplifier whose output is OUT_A. These two outputs provide the voltage drive directly to the TEC. Including the external transistors, the gain of the differential output section is fixed at 4. Details on the output amplifiers can be found in the Output Driver Amplifiers section of the application notes.

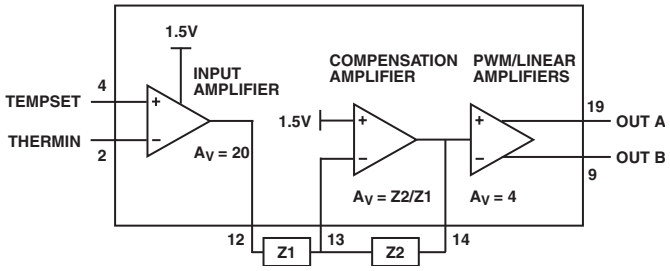


Figure 24. Signal Flow Block Diagram of ADN8830

Thermistor Setup

The temperature of the thermal object, such as a laser diode, is detected with a negative temperature coefficient (NTC) thermistor. The thermistor's resistance exhibits an exponential relationship to the inverse of temperature, meaning the resistance decreases at higher temperatures. Thus, by measuring the thermistor resistance, temperature can be ascertained.

For this application, the resistance is measured using a voltage divider. The thermistor is connected between THERMIN and AGND, Pins 7 and 30, respectively. Another resistor (R_X) is connected between V_{REF} and THERMIN, Pins 7 and 2, creating a voltage divider for the V_{REF} voltage. Figure 2 shows the schematic for this configuration.

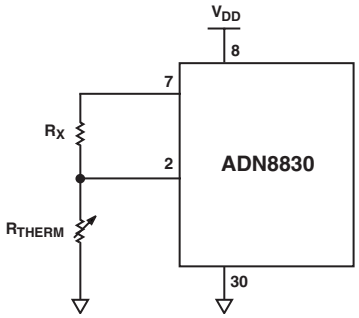


Figure 2. Connecting a Thermistor to the ADN8830

With the thermistor connected from THERMIN to AGND, the voltage at THERMIN will decrease as temperature increases. To maintain the proper input to output polarity in this configuration, Pin 19, OUT_A, should connect to the TEC– pin on the TEC and Pin 9, OUT_B, should connect to TEC+.

The thermistor can also be set up connected from V_{REF} to THERMIN with RX connecting to ground. In this case, OUT_A must connect to TEC+ with OUT_B connected to TEC– for proper operation.

Although the thermistor has a non-linear relationship to temperature, near optimal linearity over a specified temperature range can be achieved with the proper value of R_X. First, the resistance of the thermistor must be known, where:

$$\begin{aligned} R_{THERM} &= R_{T1} @ T = T_{LOW} \\ &= R_{T2} @ T = T_{MID} \\ &= R_{T3} @ T = T_{HIGH} \end{aligned} \quad (1)$$

T_{LOW} and T_{HIGH} are the end points of the temperature range and T_{MID} is the average. These resistances can be found in most thermistor datasheets. In some cases, only the coefficients corresponding to the Steinhart-Hart equation are given. The Steinhart-Hart equation is:

$$\frac{1}{T} = a + b1n(R) + c\left[1n(R)\right]^3 \quad (2)$$

Where T is the absolute temperature of the thermistor in Kelvin (°K = °C + 273.15), and R is the resistance of the thermistor at that temperature. Based on the coefficients a, b, and c, R_{THERM} can be calculated for a given T, albeit somewhat tediously, by solving the cubic roots of this equation:

$$R_{THERM} = \exp\left[\left(-\frac{\chi}{2} + \left(\frac{\chi^2}{4} + \frac{\psi^3}{27}\right)^{\frac{1}{2}}\right)^{\frac{1}{3}} + \left(-\frac{\chi}{2} - \left(\frac{\chi^2}{4} + \frac{\psi^3}{27}\right)^{\frac{1}{2}}\right)^{\frac{1}{3}}\right] \quad (3)$$

Where, $\chi = \frac{a - \frac{1}{T}}{c}$, and $\psi = \frac{b}{c}$

R_X is then found as:

$$R_X = \frac{R_{T1}R_{T2} + R_{T2}R_{T3} - 2R_{T1}R_{T3}}{R_{T1} + R_{T3} - 2R_{T2}} \quad (4)$$

For best accuracy as well as the widest selection range for resistances, R_X should be 0.1% tolerance. Naturally, the smaller the temperature range required for control, the more linear the voltage divider will be with respect to temperature. The voltage at THERMIN is:

$$V_X = V_{REF}\frac{R_{THERM}}{R_{THERM} + R_X} \quad (5)$$

Where V_{REF} has a typical value of 2.47 V.

The ADN8830 control loop will adjust the temperature of the TEC until V_X equals the voltage at TEMPSET (Pin 4), which we define as V_{SET}. Target temperature can be set by:

$$V_{SET} = m\left(T - T_{MID}\right) + V_{XMID} \quad (6)$$

Where, T equals the target temperature, and

$$m = \frac{V_{X,HIGH} - V_{X,LOW}}{T_{HIGH} - T_{LOW}} \quad (7)$$

V_X for high, mid, and low are found by using Equation 5 and substituting R_{T3}, R_{T2}, and R_{T1} respectively for R_{THERM}. The variable m is the change in V_X with respect to temperature and is expressed in V/°C.

The set point voltage can be driven from a D/A converter, or another voltage source as shown in Figure 3. The reference voltage for the DAC should be connected to the V_{REF} pin on the ADN8830 (Pin 7) to ensure best accuracy from device to device.

For a fixed target temperature, a voltage divider network can be used as shown in Figure 4. R1 is set equal to R_X and R2 is equal to the value of R_{THERM} at the target temperature.

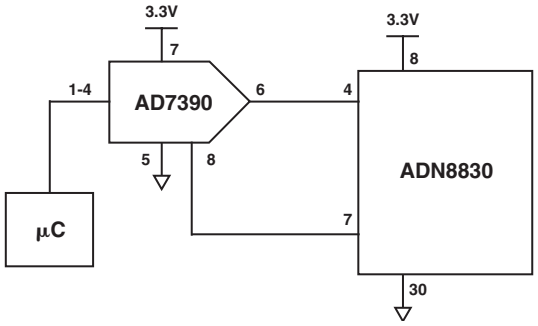


Figure 3. Using a DAC to Control the Temperature Set Point

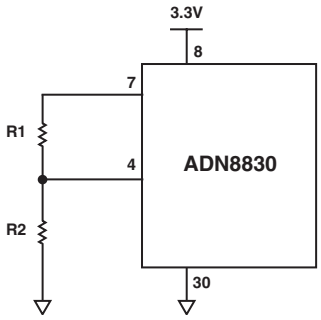


Figure 4. Using a Voltage Divider to Set a Fixed Temperature Set Point

Design Example 1:
A laser module requires a constant temperature of 25°C. From the manufacturer's datasheet, we find the thermistor in the laser module has a value of 10 kΩ at 25°C. Because the laser in not required to operate at a range of temperatures, the value of RX can be set to 10 kΩ. TEMPSET can be set by a simple resistor divider as shown in Figure 4 with R1 and R2 both equal to 10 kΩ.

Design Example 2:
A laser module requires a continuous temperature control from 5°C to 45°C. The manufacturer's datasheet shows the thermistor has a value of 10 kΩ at 25°C, 25.4 kΩ at 5°C, and 4.37 kΩ at 45°C. Using equation 4, RX is calculated to be 7.68 kΩ to yield the most linear temperature-to-voltage conversion. A D/A converter will be used to set the TEMPSET voltage.

DAC Resolution for TEMPSET
The temperature set point voltage to THERMIN can be set from a D/A converter. The DAC must have a sufficient number of bits to achieve adequate temperature resolution from the system. The voltage range for THERMIN is found by multiplying the variable m from Equation 7 by the temperature range.

$$THERMIN\ Voltage\ Range = m \times \left(T_{MAX} - T_{MIN}\right) \quad (8)$$

From Design Example 2 above, 40°C of control temperature range is achieved with a voltage range of only 1 V.

To eliminate the resolution of the DAC as the principle source of system error, the step size of each bit, V_{STEP}, should be lower than the desired system resolution. A practical value for absolute DAC resolution is the equivalent of 0.05°C. The value of V_{STEP} should be less than the value of *m* from Equation 7 multiplied by the desired temperature resolution, or

$$V_{STEP} < 0.05^{\circ}C \times m \quad (9)$$

Where, *m* is the slope of the voltage-to-temperature conversion line, as found from Equation 6. From Design Example 2, where *m* = 25 mV/°C, we see the DAC should have resolution better than 1.25 mV per step.

The minimum number of bits required is then given as:

$$\#\ of\ bits = \frac{\log\left(V_{FS}\right) - \log\left(V_{STEP}\right)}{\log\left(2\right)} \quad (10)$$

Where, V_{FS} is the full scale output voltage from the DAC, which should be equal to the reference voltage from the ADN8830, V_{REF} = 2.45 V as given in the specifications data for the reference voltage. In this example, the minimum resolution is 11 bits. A 12-bit DAC can be readily found, such as the AD7390.

It is important that the full scale voltage input to the DAC is tied to the ADN8830 reference voltage as shown in Figure 2. This eliminates errors from slight variances of V_{REF} from different ADN8830 devices.

Thermistor Fault and Temperature Lock Indications

Both the THERMFAULT and TEMPLOCK outputs at pins 1 and 5 respectively are CMOS compatible outputs that are active high. THERMFAULT will be a logic low while the thermistor is operating normally and will go to a logic high if a short or open is detected at THERMIN, pin 2. The trip voltage for THERMFAULT is when THERMIN falls below 0.2 V or exceeds 2.0 V. THERMFAULT only provides an indication of a fault condition and does not activate any shutdown or protection circuitry on the ADN8830. To shutdown the ADN8830 a logic low voltage must be asserted on pin 3 as described in the Shutdown Mode section of the datasheet.

TEMPLOCK will output a logic high when the voltage at THERMIN is within 2.5 mV of TEMPSET. This voltage can be related to temperature by solving for *m* from Equation 7. For most laser diode applications, 2.5 mV is equivalent to ±0.1°C. If the voltage difference between THERMIN and TEMPSET is greater than 2.5 mV then TEMPLOCK will output a logic low. The input offset voltage of the ADN8830 is guaranteed to within 250 mV which for most applications is within ±0.01°C.

Setting the Switching Frequency

The ADN8830 has an internal oscillator to generate the switching frequency for the output stage. This oscillator can be either set in free-run mode or synchronized to an external clock signal. For free-run operation, Pin 25 (SYNCIN) should be connected to ground and Pin 24 (COMPOSC) should be connected to AVDD. The switching frequency is then set by a single resistor connected from Pin 26 (FREQ) to ground. Table 1 shows some values for R_{FREQ} to obtain a desired switching frequency.

Table I. Switching Frequencies vs. R_{FREQ}

f_{SWITCH}	R_{FREQ}
100 kHz	1.5 MΩ
250 kHz	600 kΩ
500 kHz	300 kΩ
750 kHz	200 kΩ
1 MHz	150 kΩ

For other frequencies, the value for this resistor, R_{FREQ}, should be set to:

$$R_{FREQ} = \frac{150 \times 10^9}{f_{SWITCH}} \quad (11)$$

Where f_{SWITCH} is the switching frequency in Hz.

Highger switching frequencies reduce the voltage ripple across the TEC. However, high switch frequencies will create more power dissipation in the external transistors. This is due to the more frequent charging and discharging of the transistors' gate capacitances. If large transistors are needed for a high output current application, faster switching frequencies could reduce the overall power efficiency of the circuit. This is covered in detail in the Switched Output section of the application notes.

The switching frequency of the ADN8830 can be synchronized with an external clock by connecting the clock signal to Pin 25, SYNCIN. Pin 24 should also be connected to an R-C network as shown in Figure 11A. This network is simply used to compensate a PLL to lock on to the external clock. To ensure the quickest synchronization lock-in time, RFREQ should be set to 1.5 MΩ.

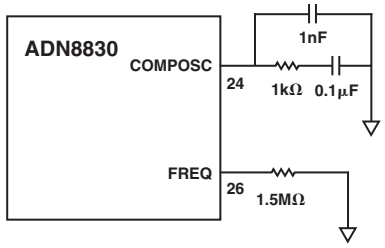


Figure 11. Using an R-C Network on Pin 24 with an External Clock

The relative phase of the ADN8830 internal oscillator compared to the external clock signal can be adjusted. This is accomplished by adjusting the voltage to Pin 29, the PHASE pin according to Figures XX and XX. The phase shift versus voltage can be approximated as:

$$Phase\ shift^{\circ} = 360^{\circ} \times \frac{V_{PHASE}}{V_{REF}} \quad (12)$$

Where, V_{PHASE} is the voltage at Pin 29, and V_{REF} has a typical value of 2.47 V.

To ensure the oscillator operates correctly, VPHASE should remain higher than 100 mV and lower than 2.3 V. This is required for either internal clock or external sync operation. A resistor divider from V_{REF} to ground can establish this voltage easily, although any voltage source, such as a DAC, could be used as well. If phase is not a consideration, for example with a single

ADN8830 being used, then Pin 29 can be tied to Pin 6, which provides a 1.5 V reference voltage.

The phase adjusted output from the ADN8830 is available at Pin 28, SYNCOUT. This pin can be used as a master clock signal for driving other ADN8830 devices. Multiple ADN8830 devices can be either driven from a single master ADN8830 device by connecting its SYNCOUT pin to each slave's SYNCIN pin, or daisy-chained by connecting each device's SYNCOUT to the next device's SYNCIN pin.

Phase shifting is useful in systems that use more than one ADN8830 TEC controller. It ensures the ADN8830 devices will not all switch at the same time, which could create too much ripple on the power supply voltage. By adjusting the phase of each device, the switching can be spread out equally over the clock period, reducing potential supply ripple and easing the instantaneous current demand from the supply.

Using a single master clock, each slave ADN8830 should have a different value phase shift. For example, with four TEC controllers, one slave device should be set for 90° of phase shift, another for 180°, and the last slave for 270°. In a daisy-chain configuration, each slave device would be set with equal phase. Using the previous example, each slave would be set to 90° with its SYNCOUT pin connected to the next device's SYNCIN pin. Examples are shown in Figures A5 and A6.

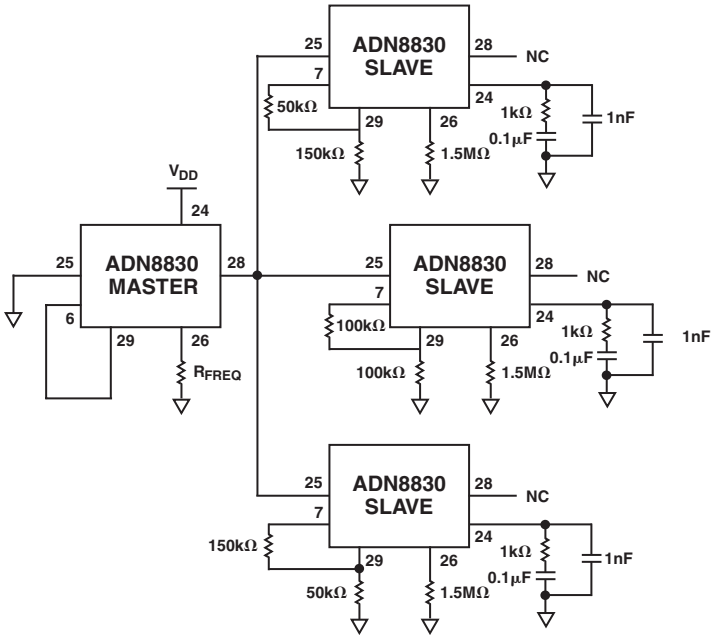


Figure 5. Multiple ADN8830 Devices Driven from a Master Clock

Soft Start on Power Up

The ADN8830 can be programmed to ramp up for a specified time after the power supply is applied or after shutdown is de-asserted. This feature, known as soft start, is useful for gradually increasing the duty cycle of the PWM amplifier. The soft start time is set with a single capacitor connected from Pin 27 to ground according to Equation 13:

$$\tau_{SS} = 150 \times C_{SS} \quad (13)$$

Where, C_{SS} is the value of the capacitor in microfarads, and t_{SS} is the soft start time in milliseconds. To set a soft start time of 15 ms, C_{SS} should equal 0.1 μF. A minimum soft start time of 10 ms is recommended to ensure proper initialization of the ADN8830 on power up.

Shutdown Mode

The ADN8830 has a shutdown mode which deactivates the output stage and puts the device into a low current standby state. The current draw for the ADN8830 in shutdown is less than 100 μA. The shutdown input, Pin 3, is active low. To shut the device down, Pin 3 should be driven to logic low. Once a logic high is applied, the ADN8830 will reactivate after the delay set by the soft start circuitry. Refer to the Soft Start on Power Up section for more details on this feature.

Pin 3 should not be left floating as there are no internal pull-up or pull-down resistors. If the shutdown function is not required, Pin 3 should be tied to V_{DD} to ensure the device is always active.

Compensation Loop

The ADN8830 TEC controller has a built-in amplifier dedicated for loop compensation. The exact compensation network is set by the user and can vary from a simple integrator, to PI, PID, or any other type of network. The type of compensation and component values should be determined by the user as it will depend on the thermal response of the object and the TEC. One method for determining these values empirically is to input a step function to TEMPSET, thus changing the target temperature, and adjusting the compensation network to minimize the settling time of the object's temperature.

A typical compensation network used for temperature control of a laser module is a PID loop, which consists of a very low frequency pole and two separate zeros at higher frequencies. Figure 7 shows a simple network for implementing PID compensation. An additional pole is added at a higher frequency than the zeros to reduce the noise sensitivity of the control loop. The bode plot of the magnitude is shown in Figure 8.

The unity-gain crossover frequency of the feed forward amplifier is given as:

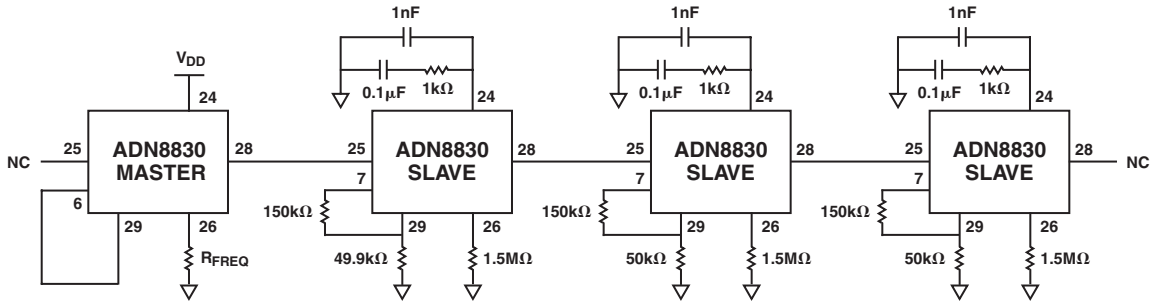


Figure 6. Multiple ADN8830 Devices Using a Daisy-Chain

$$f_{0dB} = \frac{1}{2\pi R3C1} \times 80 \times TEC\ GAIN \qquad (14)$$

To ensure stability, the unity-gain crossover frequency should be lower than the thermal time constant of the TEC and thermistor. However, this thermal time constant may not be specified and can be difficult to characterize.

There are many texts written on loop stabilization and it is beyond the scope of this datasheet to discuss all methods and trade-offs in optimizing compensation networks. A simple method that can be used to empirically determine a PID compensation loop as shown in Figure A7 involves the following procedure:

1. Connect thermistor and TEC to ADN8830 application circuit. Power does not need to be applied to the laser diode for this procedure. Monitor output voltage across the TEC with an oscilloscope.
2. Short C1 and open C2, leaving just R1 and R3 as a simple proportional-only compensation loop.
3. While maintaining a constant TEMPSET voltage, increase the ratio of R1/R3 thus increasing the gain until loop oscillation starts to occur. Decrease this ratio by a factor of 2 from the point of oscillation. The R1/R3 ratio will likely be less than unity for most laser modules.
4. Add C1 capacitor and decrease value until oscillation starts, then increase by a factor of 2. A good initial starting value for C1 is to create a unity-gain crossover of 0.1 Hz based on Equation 14.
5. Short R2 and increase C2 until oscillation starts. At this point, either C2 can be decreased or R2 can be added to regain stability. Generally speaking, R2 will be greater than R3 and C2 will be one or more orders of magnitude less than C1.
6. TEMPSET should be adjusted with a step change while observing the output voltage settling time. A step change of 100 mV should suffice. From here, C2, R2 and even C1 can be decreased to minimize settling time at the expense of additional output voltage overshoot.
7. An additional feedback capacitor in parallel with R1 and C1 can be added to add another high frequency pole. In many cases, this improves the stability of the system without increasing settling time as out-of-band noise is filtered out of the control signal. A 330 pF to 1 nF capacitor should suffice, if required.

The typical values shown in typical application circuit in Figure 1 have R1 = 100 kΩ, R2 = 1 MΩ, R3 = 205 kΩ, C1 = 10 µF, C2 = 1 µF, and an additional feedback capacitor of 330 pF. For most pump laser modules, this results in a 10°C TEMPSET step settling time to within 0.1°C in less than 5 seconds.

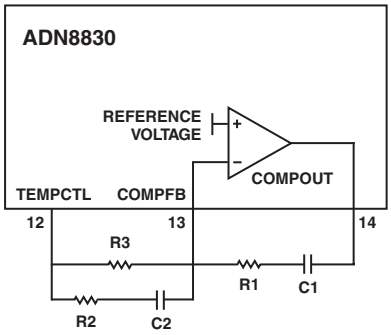


Figure 7. Implementing a PID Compensation Loop

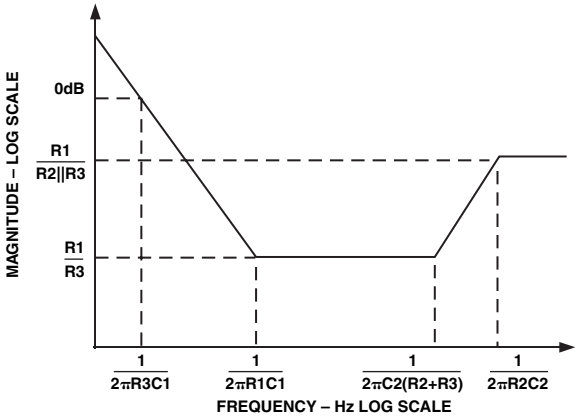


Figure 8. Bode Plot for PID Compensation

Using TEC Controller ADN8830 with a Wave Locker

Many optical applications require precision control of laser wavelength. The wavelength of the laser diode can be adjusted by adjusting its temperature, which is done through temperature control of the TEC. Wavelength control can be done by feeding a wave locker or etalon output back to the microprocessor and using the microprocessor to calculate and re-instruct the TEC controller with a new target temperature. However, this method is computationally expensive and has time delays before the adjustment is done. A faster responding and simpler method is to feed the wave locker signal back to the TEC controller for direct temperature control.

The ADN8830 is designed to be compatible with a wave locker controller. Figure 9 shows the basic schematic. The TEMPCTL output from ADN8830 is proportional to the object's actual temperature. This voltage is fed to the wave locker controller. Also fed to the wave locker controller are the photodiode outputs from the wave locker, as well as the laser diode power and a digital signal indicating a functional laser diode, both of which come from the CW controller. The output of the wave locker controller is then connected to the input of the compensation network. This allows the wave locker controller to adjust the TEC temperature based on the current temperature of the object, the current wavelength of the laser diode, and the target wavelength. Once the target wavelength is reached, the wave locker

controller sends a signal to the micro-controller indicating the laser signal is good.

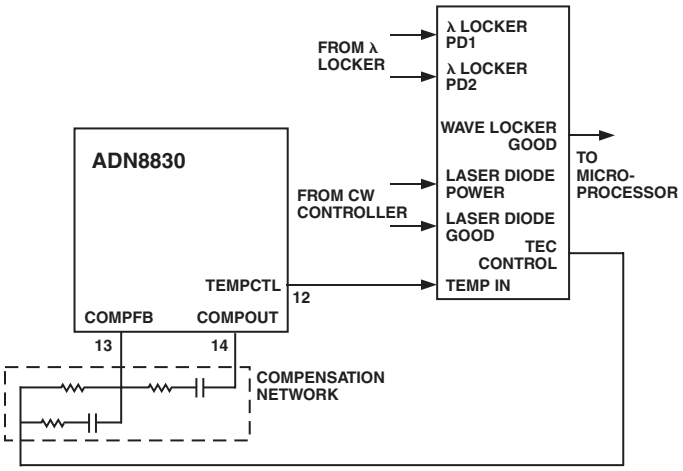


Figure 9. Using the ADN8830 with a Wave Locker

Using TEMPOUT to Measure Temperature

The TEMPOUT pin is a voltage that is proportional to difference between the target temperature and the measured thermistor temperature. The full equation for the voltage at TEMPOUT is:

$$TEMPOUT = 1.5 + 3 \times \left(THERMIN - TEMPSET\right) \quad (16)$$

The voltage range of TEMPOUT is 0 V to 3.0 V and is independent of power supply voltage.

Setting the Maximum TEC Voltage and Current

The ADN8830 can be programmed for a maximum output voltage to protect the TEC. A voltage from 0 V to 1.5 V applied to the VLIM input to the ADN8830, Pin 15, sets the maximum TEC voltage, $V_{TEC,MAX}$. This voltage can be set with either a resistor divider or from a DAC. Because the output of the ADN8830 is bi-directional, this voltage sets both the upper and lower limits of the TEC voltage. The equation governing $V_{TEC,MAX}$ is given in equation 15 and the graph of this equation is shown in Fig A10:

$$V_{TEC,MAX} = \left(1.5\ V - V_{LIM}\right) \times 4 \quad (15)$$

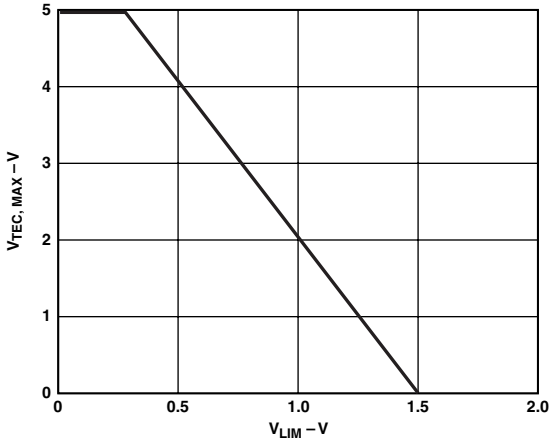


Figure A10: Graph of V_{LIM} Voltage vs. Maximum TEC Voltage

If the supply voltage is lower than $V_{TEC,MAX}$, then the maximum TEC voltage will obviously be equal to the supply voltage. The voltage to V_{LIM} should not exceed 1.5 V as this causes improper operation of the output voltage limiting circuitry. Setting V_{LIM} to 1.5 V can be used to deactivate the TEC current without shutting down the ADN8830 in the event of a system failure. If a maximum TEC voltage is not required, then V_{LIM} should be connected to ground. It is not advisable to leave V_{LIM} floating as this would cause unpredictable output behavior.

This feature should be used to limit the maximum output current to the TEC as specified in the TEC datasheet. For example, if the maximum TEC voltage is specified at 2 V, then V_{LIM} should be set to 1 V. The maximum output voltage is then set to ±2 V.

Output Driver Amplifiers

The output voltage across the TEC as measured from Pin 19 to Pin 9 can be monitored at Pin 16. This is labeled as VTEC in the typical application schematic in Figure 1. The voltage at VTEC can vary from 0 V to 3 V independent of the power supply voltage. Its equation is given as:

$$V_{TEC} = 0.25\text{x}\left(V_{OUT\_A} - V_{OUT\_B}\right) + 1.5 \quad (17)$$

Where V_{OUT_A} and V_{OUT_B} are the voltages at Pins 19 and 9 respectively. The ripple voltage at pin 19 is filtered out internally and does not appear at VTEC, leaving it as an accurate dc output of the TEC voltage.

The TEC is driven with a differential voltage allowing current to flow in either direction through the TEC. This can provide heat transfer either to or from the object being regulated without the use of a negative voltage rail. The maximum output voltage across the TEC is set by the voltage at VLIM, Pin 15. Refer to the Setting the Maximum TEC Voltage section for details on this operation. With V_{LIM} set to ground the maximum output voltage is the power supply voltage, V_{SY}.

To achieve a differential output, the ADN8830 has two separate output stages. OUT_A from a switched output, or pulse width modulated (PWM), amplifier and OUT_B is from a high gain linear amplifier. Although they achieve the same result, to pro-

vide constant voltage and high current, their operations are different. The exact equations for the two outputs are:

$$OUT\_A = 4 \times (COMPOUT - 1.5) + OUT\_B \quad (18)$$

$$OUT\_B = -14 \times (COMPOUT - 1.5) + 1.5 \quad (19)$$

Where COMPOUT is the voltage at Pin 13. The voltage at COMPOUT is determined by the compensation network which is fed by the input amplifier, which receives its input voltage from TEMPSET and THERMIN. Equation 19 is only valid in the linear region of the linear amplifier. OUT_B has a lower limit of 0 V and an upper limit of the power supply.

Because the COMPOUT voltage is not readily known, equation 19 can be rewritten in terms of the TEC voltage, V_{TEC} which is defined as OUT_B – OUT_A.

$$OUT\_B = 3.5 \times V_{TEC} + 1.5 \quad (20)$$

Referring to Figure 1, Pins 10 and 11 provide the gate drive for Q3 and Q4, which complete the linear output amplifier. This output voltage is fed back to Pin 9, OUT_B, to close its loop. The gate-to-drain capacitance of Q3 and Q4 provide the compensation for the linear amplifier. If using the recommended FDW2520C transistors, it will be necessary to add an additional 2.2 nF of capacitance from the gate to the drain of the PMOS transistor to maintain stability. A 3.3 nF capacitor should also be connected from the drain to ground to prevent small oscillations when there is very little or no current through the TEC.

These extra capacitors are specified only when using FDW2520C transistors in the linear amplifier. If other transistors are used, these values may need to be adjusted. To ensure the linear amplifier is stable, the total gate-to-source capacitance for both Q3 and Q4 should be at least 2.5 nF. Refer to the transistor's datasheet for their typical gate-to-drain capacitance values.

The output of the linear amplifier is proportional to the voltage at Pin 13, COMPOUT. Because the linear amplifier operates with a gain of 14, its output will typically be at either ground or V_{SY} if there is more than about 100 mA of current flowing through the TEC. This ensures Q3 and Q4 will not be a dominant source of power dissipation at high output currents.

Inductor Selection

In addition to the external transistors, the PWM amplifier requires an inductor and capacitor at its output to filter the switched output waveform. Proper inductor selection is important to achieve the best efficiency. The duty cycle of the PWM sets the OUT_A output voltage and is:

$$D = \frac{OUT\_A}{V_{SY}} \quad (21)$$

The average current through the inductor is equal to the TEC current. The ripple current through the inductor, ΔI_L, varies with the duty cycle and is equal to:

$$\Delta I_L = \frac{V_{SY} \times D \times (1 - D)}{L \times f_{CLK}} \quad (22)$$

Where f_{CLK} is the clock frequency as set by the resistor R_{FREQ} at Pin 26 or an external clock frequency. Refer to the Setting the Switching Frequency section for more information. Selecting a faster switching frequency or a larger value inductor will reduce the ripple current through the inductor. The waveform of the inductor current is shown in Figure 12A.

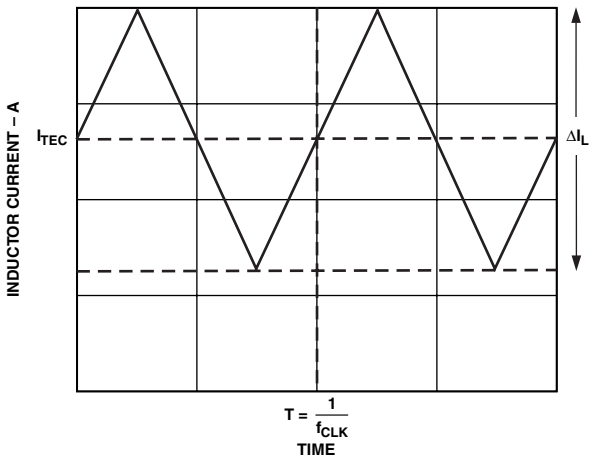


Figure A12. Current Waveform Through Inductor

It is important to select an inductor that can tolerate the maximum possible current that could pass through it. Most TECs are specified with a maximum voltage and current for proper and reliable operation. The maximum instantaneous inductor current can be found as:

$$I_{L,MAX} = I_{TEC,MAX} + 0.5 \times \Delta I_L \quad (23)$$

Table II. Partial List of Inductors and Key Specifications

Inductance (µH)	I_{MAX} (A)	$R_{S,TYP.}$ (mΩ)	Height (mm)	Part Number	Manufacturer	Web site
4.7	1.1	200	1	LPO1704-472M	Coilcraft	http://www.coilcraft.com
4.7	1.59	55	2	A918CY-4R7M	Toko	http://www.toko.com
4.7	3.9	48	2.8	UP2.8B-4R7	Cooper	http://cooperet.com
4.7	1.5	90	3	DO1608C-472	Coilcraft	
4.7	1.32	56	3	CDRH4D28 4R7	Sumida	http://www.sumida.com
4.7	7.5	12	4.5	892NAS-4R7M	Toko	
4.7*	5.4	18	5.2	DO3316P-472	Coilcraft	
10	2.7	80	2.8	UP2.8B-100	Cooper	
15	8	32	8	DO5022P-153HC	Coilcraft	
47	4.5	86	7.1	DO5022P-473	Coilcraft	

*Recommend inductor in typical application circuit Figure 1.

Where ΔI_L can be found from equation 22 with the appropriate duty cycle calculated from equation 21 with OUT_A = $V_{TEC,MAX}$.

Design Example 3: A TEC is specified with a maximum current of 1.5 A and maximum voltage of 2.5 V. The ADN8830 will be operating from a 3.3 V supply voltage with a 200 kHz clock and a 4.7 µH inductor. The duty cycle of the PWM amplifier at 2.5 V is calculated to be 75.8%. Using equation 22, the inductor ripple current is found to be 664 mA. From equation 23, the maximum inductor current will be 1.82 A and should be considered when selecting the inductor. Notice that increasing the clock frequency to 1 MHz would reduce $I_{L,MAX}$ to 1.56 A.

Design Example 4: Using the same TEC as above, the ADN8830 will be powered from 5.0 V instead. Here, the duty cycle is 50%, which happens to be the worst case duty cycle for inductor current ripple. Now, ΔI_L equals 1.33 A with a 200 kHz clock, and $I_{L,MAX}$ is 2.83 A. Reducing the inductor ripple current is another compelling reason to operate the ADN8830 from a 3.3 V supply instead.

Table 2 lists some inductor manufacturers and part numbers along with some key specifications. The column I_{MAX} refers to the maximum current the inductor is rated at to remain linear. Although higher currents can be pushed through the inductor, efficiency and ripple voltage will be dramatically degraded.

This is by no means a complete list of manufacturers or inductors that can be used in the application. More information on these inductors is available at their web sites. Note the trade-offs between inductor height, maximum current, and series resistance. Smaller inductors cannot handle as much current and therefore require higher clock speeds to reduce their ripple current. They also have higher series resistance which can lower the overall efficiency of the ADN8830.

PWM Output Filter Requirements

The switching of Q1 and Q2 creates a pulse-width modulated (PWM) square wave from 0 V to V_{DD}. This square wave must be filtered sufficiently to create a steady voltage that will drive the TEC. The ripple voltage across the TEC is a function of the inductor ripple current, the L-C filter cutoff frequency, and the equivalent series resistance (ESR) of the filter capacitor. The equivalent circuit for the PWM side is given in Figure 13A.

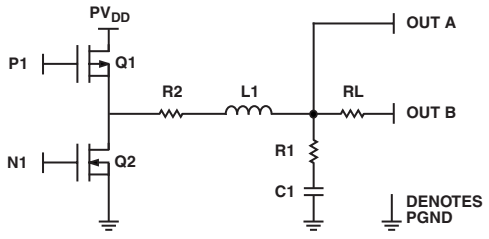


Figure A13. Equivalent Circuit for PWM Amplifier and Filter

In this circuit, RL is the TEC resistance, R2 is the parasitic resistance of the inductor combined with the equivalent $r_{DS,ON}$ of Q1 and Q2, and R1 is the ESR of C1. The voltage V_X is the a pulse width modulated waveform that switches between V_{SY} and ground. This is a second-order low pass filter with an exact cutoff frequency of:

$$f_C = \frac{1}{2\pi}\sqrt{\frac{R2+RL}{(R1+RL)C1L1}} \quad (24)$$

Practically speaking, R1 and R2 are several tens of milliohms and are much smaller than the TEC resistance, which can be a few ohms. The cutoff frequency can be roughly approximated as:

$$f_C = \frac{1}{2\pi}\sqrt{\frac{1}{C1L1}} \quad (25)$$

This cutoff frequency should be much lower than the clock frequency to achieve adequate filtering of the switched output waveform. Also of importance is the damping factor ζ of the L-C filter. Too low a damping factor will result in a longer settling time and could potentially cause stability problems for the temperature control loop. Neglecting R1 and R2 again, the damping factor is simply:

$$\zeta = \frac{1}{2RL}\sqrt{\frac{L1}{C1}} \quad (26)$$

Using the recommended values of L1 = 4.7 µH and C1 = 22 µF results in a cutoff frequency of 15.7 kHz. With a TEC resistance of 2 Ω, the damping factor is 0.12. The cutoff frequency can be decreased to lower the output voltage ripple with slower clock frequencies by increasing L1 or C1. Increasing C1 may appear to be a simpler approach as it would not increase the physical size of the inductor, but there is a potential stability danger in lowering the damping factor too far. It is recommended ζ remain greater than 0.05 to provide a reasonable settling time for the TEC. Increasing ζ also makes finding the proper PID compensation easier as there is less ringing in the L-C output filter. To allow adequate phase and gain margin for the PWM amplifier, the following table should be used to find the lower limit of cutoff frequency for a given damping factor.

Table III. Minimum L-C Filter Cutoff Frequency vs. Damping Factor

ζ	$f_{C,MIN}$ (kHz)
0.05	8
0.1	4
0.2	2
0.3	1.9
0.5	1.6
>0.707	1.5

Calculating PWM Output Ripple Voltage

Although it may seem that f_C can be arbitrarily lowered to reduce output ripple, the ripple voltage is also dependent on the ESR of C1, shown as R1 in Figure 12A. This resistance creates a zero which turns the second-order filter into a first-order filter at high frequencies. The location of this zero is:

$$Z1 = \frac{1}{2\pi R1C1} \quad (27)$$

With a clock frequency greater than Z1, and presumably greater than f_C, the output voltage ripple is:

$$\Delta OUT\_A = \Delta I_L \times R1 \quad (28)$$

$$\Delta OUT\_A = \frac{V_{SY} D(1-D) R1}{L1 f_{CLK}} \quad for\ \left(f_{CLK} > Z1\right) \quad (29)$$

The worst-case voltage ripple occurs when the duty cycle of the PWM output is exactly 50%, or when OUT_A = 0.5 × V_{SY}. As shown in equation 30:

$$\Delta OUT\_A_{MAX} \approx \frac{V_{SY} R1}{4 f_{CLK} L1} \quad for\ \left(f_{CLK} > Z1\right) \quad (30)$$

Here it can be directly seen that increasing the inductor value or clock frequency will reduce the ripple. Choosing a low ESR capacitor will ensure R1 remains low. Operating from a lower supply voltage will also help reduce the output ripple voltage from the L-C filter. With a clock frequency equal to Z1 but presumably greater than f_C, the worst-case output voltage ripple is:

$$\Delta OUT\_A_{MAX} = V_{DD} \frac{\left(16 R1^2 C1^2 {f_{CLK}}^2 + 1\right)}{32 L1 C1 f_{CLK}} \quad for\ \left(f_{CLK} = Z1\right) \quad (31)$$

Which, if f_{CLK} < Z1, can be further simplified to:

$$\Delta OUT\_A_{MAX} \approx \frac{V_{DD}}{2 L1 C1 {f_{CLK}}^2} \quad for\ \left(f_{CLK} < Z1\right) \quad (32)$$

A typical 100 µF surface mount electrolytic capacitor can have an ESR of over 100 mΩ, pulling this zero to below 16 kHz, resulting in an excess of ripple voltage across the TEC. Low ESR capacitors such as ceramic or polymer aluminum capacitors are recommended instead. Polymer aluminum capacitors can provide more bulk capacitance per unit area over ceramic ones saving board space. Table IV shows a limited list of capacitors with their equivalent series resistances.

This is by no means a complete list of all capacitor manufacturers or capacitors types that can be used in the application. The 22 µF capacitor recommended has a maximum ESR of 35 mΩ, which puts Z1 at 207 kHz. Using a 3.3 V supply with the recommended inductor and capacitor listed with a 1 MHz clock frequency will yield a worst-case ripple voltage at OUT_A of about 6 mV.

External FET Requirements

External FETs are required for both the PWM and linear amplifiers that drive OUT_A and OUT_B from the ADN8830. Although it is important to select FETs that can supply the maximum current required to the TEC, they should also have a low enough resistance ($r_{DS,ON}$) to prevent excessive power dissipation and improve efficiency. Other key requirements from these FET pairs are slightly different for the PWM and linear outputs.

The gate drive outputs for the PWM amplifier at P1 and N1, Pins 21 and 22 respectively, have a typical non-overlap delay of 80 ns. This is done to ensure one FET is completely off before the other FET is turned on preventing current from shooting through both simultaneously. Such shoot-through current could reach in excess of 50 A, which although would only for a brief period, would occur during every switching transition and could quickly burn up the FET pair.

The input capacitance (C_{ISS}) of the FET should not exceed 6 nF. The P1 and N1 outputs from the ADN8830 have a typical output impedance of 5 Ω. This creates a time constant in combination with CISS of the external FETs equal to 5 Ω × C_{ISS}. To ensure shoot-through does not occur through these FETs, this time constant should remain less than 30 ns.

The linear output from the ADN8830 uses N2 and P2, pins 10 and 11 respectively, to drive the gates of the linear side FETs, shown as Q3 and Q4 in Figure 1A. Local compensation for the linear amplifier is achieved through the gate-to-drain capacitances (C_{GD}) of Q3 and Q4. The value of C_{GD} can be determined from the datasheet as is usually referred to as C_{RSS}, the reverse transfer capacitance. The exact C_{RSS} value should be determined from a graph that shows capacitance versus drain-to-source voltage, using the power supply voltage as the appropriate V_{DS}.

To ensure stability of the linear amplifier, the total CGD of the PMOS device, Q3, should be greater than 2.5 nF and the total CGD of the NMOS should be greater than 150 pF. External capacitance can be added around the FET to increase the effective CGD of the transistor. This is the function of C6 in the typical application schematic shown in Figure 1A. If external capacitance must be added, it will generally only be required around the PMOS transistor.

In the event of zero output current through the TEC, there will be no current flowing through Q3 and Q4. In this condition,

Table IV. Partial List of Capacitors and Key Specifications

Value (µF)	ESR (mΩ)	Voltage Rating (V)	Part Number	Manufacturer	Web Site
10	60	6.3	NSP100M6.3D2TR	NIC Components	http://www.niccomp.com
22*	35	8	ESRD220M08B	Cornell Dubilier	http://www.cornell-dubilier.com
22	35	8	NSP220M8D5TR	NIC Components	
22	35	8	EEFFD0K220R	Panasonic	http://www.maco.panasonic.co.jp
47	25	6.3	NSP470M6.3D2TR	NIC Components	
68	18	8	ESRD680M08B	Cornell Dubilier	
100	95	10	594D107X_010C2T	Vishay	http://www.vishay.com

* Recommend capacitor in typical application circuit Figure 1.

these FETs will not provide any small signal gain and hence no negative feedback for the linear amplifier. This leaves only a feedforward signal path through C_{GD}, which could cause a settling problem at OUT_B. This is often seen as a small signal oscillation at OUT_B, but only when the TEC is at or very near zero current.

The remedy for this potential minor instability is to add additional capacitance from OUT_B to ground. This may need to be determined empirically, but a good starting point is 1.5 times the total C_{GD}. This is the function of C12 in Figure 1A. Note that while adding additional C_{GD} around Q3 and Q4 will help ensure stability, it could potentially increase instability in the zero current dead-band region, requiring additional capacitance from OUT_B to ground.

Bear in mind the addition of these capacitors is only for local stabilization. The stability of the entire TEC application may need adjustment, which should be done around the compensation amplifier. This is covered in the Adjusting the Compensation Network section.

One additional consideration for selecting both the linear output FETs: They must have a minimum threshold voltage (VT) of 0.6 V. Lower threshold voltages could cause shoot-through current in the linear output transistors.

Table V shows the recommended FETs that can be used for the linear output in the ADN8830 application. The table includes the appropriate external gate-to-drain capacitance (Ext. C_{GD}) and snubber capacitor value (C_{SNUB}) connected from OUT_B to ground that should be added to ensure local stability. Table VI shows the recommended PWM output FETs. Although other transistors can be used, these combinations have been tested and are proved stable and reliable for typical applications.

Datasheets for these devices can be found at their respective web sites:

Fairchild - www.fairchildsemi.com
Vishay Siliconix - www.vishay.com
International Rectifier - www.irf.com

Calculating Power Dissipation and Efficiency

The total efficiency of the ADN8830 application circuit is simply the ratio of output power to the TEC divided by total power delivered from the supply. The idea in minimizing power dissipation is to avoid both drawing additional power and reducing heat generated from the circuit. The dominant sources of power dissipation will include resistive losses, gate charge loss, core loss from the inductor, and the current used by the ADN8830 itself.

The on-channel resistance of both the linear and PWM output FETs will affect efficiency primarily at high output currents. Because the linear amplifier operates in a high gain configuration, it will be at either at ground or V_{DD} when significant current is flowing through the TEC. In this condition, the power dissipation through the linear output FET will be:

$$P_{FET,LIN} = r_{DS,ON} \times I_{TEC}^{2} \quad (34)$$

Using either the $r_{DS,ON}$ for the NMOS or the PMOS depending on the direction of the current flow. In the typical application setup in Figure 1, if the TEC is cooling the target object then the PMOS is sourcing the current. If the TEC is heating the object, the NMOS will be sinking current.

Although the FETs that drive OUT_A switch between Q1 and Q2 being on, they have an equivalent series resistance that is equal to a weighted average of their $r_{DS,ON}$ values.

$$R_{EQIV} = D \times r_{DS,P1} + (D-1) \times r_{DS,N1} \quad (35)$$

Table V. Recommended FETs for Linear Output Amplifier

Part Number	Type	C_{GD} (nF)	Ext. C_{GD} (nF)	C_{SNUB} (nF)	$r_{DS,ON}$ (mΩ)	I_{MAX} (A)	Manufacturer
FDW2520C*	NMOS	0.17	–	–	18	6.0	Fairchild
	PMOS	0.15	2.2	3.3	35	4.5	
IRF7401	NMOS	0.5	–	–	22	8.7	International Rectifier
IRF7233	PMOS	2.2	1.0	3.3	20	9.5	International Rectifier
FDR6674A	NMOS	0.23	–	–	9.5	11.5	Fairchild
FDR840P	PMOS	0.6	1.0	3.3	12	10	Fairchild

* Recommend transistors in typical application circuit Figure 1.

Table VI. Recommended FETs for PWM Output Amplifier

Part Number	Type	C_{ISS} (nF)	$r_{DS,ON}$ (mΩ)	Continuous I_{MAX} (A)	Manufacturer
FDW2520C*	NMOS	1.33	18	6.0	Fairchild
	PMOS	1.33	35	4.5	
Si7904DN	NMOS	1.0	30	5.3	Vishay Siliconix
Si7401DN	PMOS	3.5	17	7.3	Vishay Siliconix
IRF7401	NMOS	1.6	22	8.7	International Rectifier
IRF7404	PMOS	1.5	40	6.7	International Rectifier

* Recommend transistors in typical application circuit Figure 1.

The resistive power loss from the PWM transistors is then:

$$P_{FET,PWM} = R_{EQIV} \times I_{TEC}^{2} \quad (36)$$

There is also a power loss from the continuing charging and discharging of the gate capacitances on Q1 and Q2. The power dissipated due to gate charge loss (P_{GCL}) is:

$$P_{GCL} = \frac{1}{2} C_{ISS} V_{DD}^{2} f_{CLK} \quad (37)$$

Using the appropriate input capacitance (C_{ISS}) for the NMOS and PMOS. Both transistors are switching, so P_{GCL} should be calculated for each one and will be added to find the total power dissipated from the circuit.

The series resistance of the inductor, R2 from Figure A13, will also exhibit a power dissipation equal to:

$$P_{R2} = R2 \times I_{TEC}^{2} \quad (38)$$

Core loss from the inductor arises as a result of non-idealities of the inductor. Although this is difficult to calculate explicitly, is can be estimated as 80% of P_{RL} at 1 MHz switching frequencies and 50% of P_{RL} at 100 kHz. Judging conservatively:

$$P_{LOSS} = 0.8 \times P_{RL} \quad (39)$$

Finally, the power dissipated by the ADN8830 is equal to the current used by the device multiplied by the supply voltage. Again, this exact equation is difficult to determine as we have already taken into account some of the current while finding the gate charge loss. A reasonable estimate is to use 40 mA as the total current used by the ADN8830. The power dissipated from the device itself is:

$$P_{ADN8830} = V_{DD} \times 10\,mA \quad (40)$$

There are certainly other mechanisms for power dissipation in the circuit, including some external transistor shoot-through current. However, a rough estimate of the total power dissipated can be found by summing the above power dissipation equations. Efficiency is then found by comparing the power dissipated with the required output power to the load.

$$Efficiency = \frac{P_{LOAD}}{P_{LOAD} + P_{DISS,TOT}} \quad (41)$$

Where $P_{LOAD} = I_{LOAD} \times V_{LOAD}$.

The measured efficiency of the system will likely be less than the calculated efficiency. Measuring the efficiency of the application circuit is fairly simple but must be done in a exact manner to ensure the correct numbers are being measured. Using two high current, low impedance ammeters and two voltmeters, the circuit should be setup as shown in Figure A14.

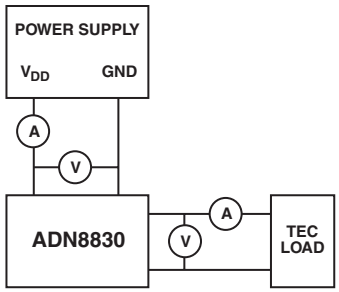


Figure A14. Measuring Efficiency of the ADN8830 Circuit

The voltmeter to the TEC or output load should include the series ammeter as the power delivered to the ammeter is considered part of the total output power. However, the voltmeter measuring the voltage delivered to the ADN8830 circuit should not include the series ammeter from the power supply. This prevents a false supply voltage power measurement as we are only interested in the supply voltage power delivered to the ADN8830 circuit. Figure A15 and A16 show some efficiency measurements using the typical application circuit shown in Figure A1.

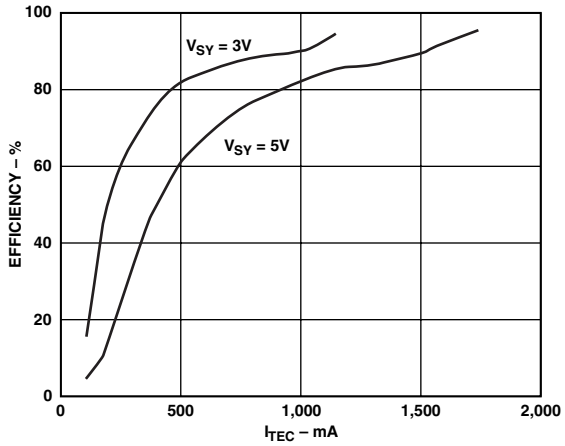


Figure A15. ADN8830 Efficiency with f_{CLK} = 1 MHz

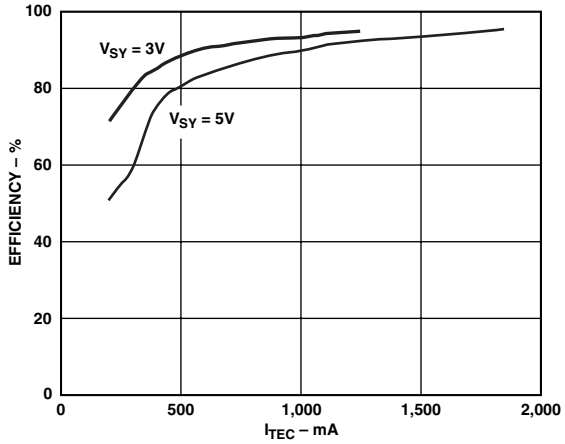


Figure A16. ADN8830 Efficiency with f_{CLK} = 200 kHz

Note that higher efficiency can be achieved using a lower supply voltage or a slower clock frequency. This is due to the fact that the dominant source of power dissipation at high clock frequencies is the gate charge loss on the PWM transistors.

Layout Considerations

The two key considerations for laying out the board for the ADN8830 is to minimize both the series resistance in the output and the potential noise pickup in the precision input section. The best way to accomplish both of these objectives is to divide the layout into two sections, one for the output components and the other for the remainder of the circuit. These sections should have independent power supply and ground current paths which are each connected together at a single point near the power supply. This is used to minimize power supply and ground voltage bounce on the more sensitive input stages to the ADN8830 caused by the switching of the PWM output. Such a layout technique is referred to as a "star" ground and supply connection. Figure A17 shows a block diagram of the concept.

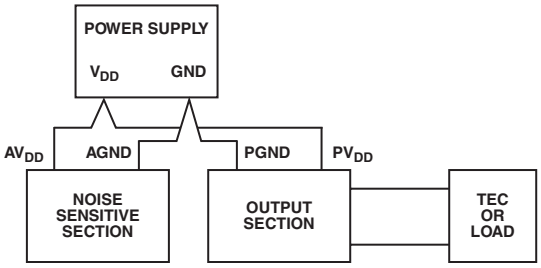


Figure A17. Using Star Connections to Minimize Noise Pickup from Switched Output

The low noise power and ground are referred to as AV_{DD} and A_{GND}, with the output supply and ground paths labeled PV_{DD} and P_{GND}. These pins are labeled on the ADN8830 and should be connected appropriately. Both sets of external FETs should be connected to PV_{DD} and P_{GND}. All output filtering and PV_{DD} supply bypass capacitors should be connected to P_{GND}.

All remaining connections to ground and power supply should be done through AV_{DD} and A_{GND}. A 4-layer board layout is recommended for best performance with split power and ground planes between the top and bottom layers. This provides the lowest impedance for both supply and ground points. Setting the ADN8830 above the A_{GND} plane will reduce the potential noise injection into the device. Figure A18 shows the top layer of the layout used for the ADN8830 demo boards, highlighting the power and ground split planes.

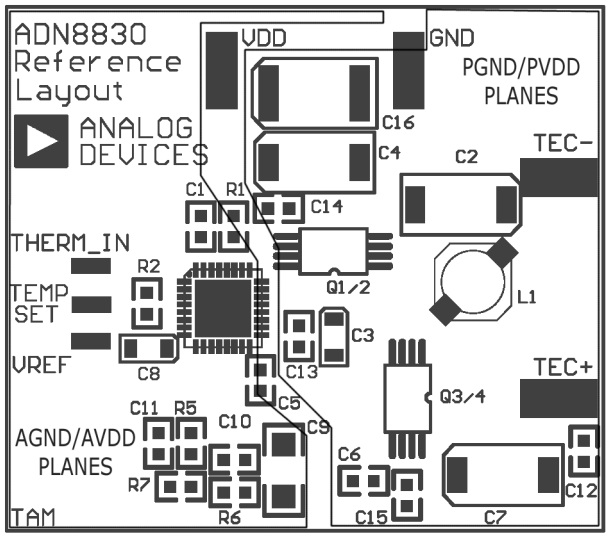


Figure A18. Top Layer Reference Layout for ADN8830

Proper supply voltage bypassing should be taken into consideration as well to minimize the ripple voltage on the power supply. A minimum bypass capacitance of 10 µF should be placed in close proximity to each component connected to the power supply. This includes Pins 8 and 20 on the ADN8830 and both external PMOS transistors. An additional 0.1 µF capacitor should be placed in parallel to each 10 µF cap to provide bypass for high frequency noise. Using a large bulk capacitor, 100 µF or greater, in parallel with a low ESR capacitor where AV_{DD} and PV_{DD} connect will further improve voltage supply ripple. This is covered in more detail in the Power Supply Ripple section.

Power Supply Ripple

Minimizing ripple on the power supply voltage can be an important consideration, particularly in signal source laser applications. If the laser diode is operated from the same supply rail as the TEC controller, ripple on the supply voltage could cause inadvertent modulation of the laser frequency. As most laser diodes are driven from a 5 V supply, it is recommended to operate the ADN8830 from a separate 3.3 V regulated supply unless higher TEC voltages are required. Operation from 3.3 V also improves efficiency thus minimizing power dissipation.

The power supply ripple is primarily a function of the supply bypass capacitance, also called bulk capacitance, and the inductor ripple current. Similar to the L-C filter at the PWM amplifier output, using more capacitance with low equivalent series resistance (ESR) will lower the supply ripple. A larger inductor value will reduce the inductor ripple current, but this may not be practical in the application. A recommended approach is to use a standard electrolytic capacitor in parallel with a low ESR capacitor. A surface mount 220 µF electrolytic in parallel with a 22 µF polymer aluminum low ESR cap can occupy an approximate total board area only of 0.94 square inches or 61 square millimeters. Using these capacitors along with a 4.7 µH inductor can yield a supply ripple of less than 5 mV.

High frequency transient spikes may appear on the supply voltage as well. This is due to the fast switching times on the PWM transistors and the sharp edges of their gate voltages. Although these transient spikes can reach several tens of millivolts at their peak, they typically last for less than 20 ns and have a resonance greater than 100 MHz. Additional bulk capacitance will not

appreciably affect the level of these spikes as such capacitance is not reactive at these frequencies. Adding 0.01 μF ceramic capacitors on the supply line near the PWM PMOS transistor can reduce this switching noise. Inserting an RF inductor with a high-Q around 100 MHz in series with PV_{DD} will also block this noise from traveling back to the power supply.

Setting Maximum Output Current and Short Circuit Protection
Although the maximum output voltage can be programmed through VLIM to protect the TEC from overvoltage damage, the user may wish to protect the ADN8830 circuit from a possible short circuit at the output. Such a short could quickly damage the external FETs or even the power supply as they would attempt to drive excessive current. Figure A19 shows a simple modification that will protect the system from an output short circuit.

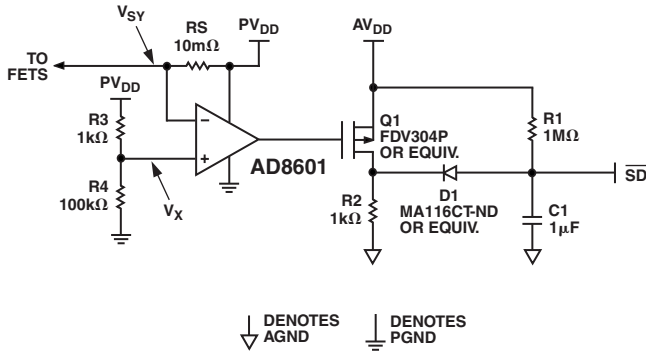


Figure 19. Implementing Output Short Circuit Protection

A 10 mΩ resistor placed in series with the PVDD supply line creates a voltage drop proportional to the absolute value of the output current. The AD8601 is a CMOS amplifier that is configured as a comparator. As long as the voltage at its inverting input (VS) exceeds the voltage set by the resistor divider at the non-inverting input (VX), the gate of Q1 will remain at ground. This leaves Q1 on, effectively connecting D1 to the positive rail and leaving the voltage on C1 at VDD. Should enough current flow through RS to drop VS below VX, Q1 will turn off and C1 will discharge through R2 down to a logic low to activates the ADN8830 shutdown. Once VS returns to a voltage greater than VX, Q1 will turn back on and C1 will charge back to VDD through R1. The shutdown and re-activation time constants are approximately:

$$\tau_{SD} = C1 \times R1$$
$$\tau_{ON} = C1 \times R1 \quad (42)$$

The shutdown time constant should be a minimum of ten clock cycles to ensure high current switching transients do not trigger a false activation. If powered from 5 V, the circuit shown will shutdown the ADN8830 should PVDD deliver over 5 A for more than 1 ms. After shutdown, the circuit will reactivate the ADN8830 in about 1 second.

The current from the power supply and through the shunt resistor is less than the current delivered to the load due to the efficiency of the PWM amplifier. The voltage drop across RS is found as:

$$V_{RS} = \frac{I_{OUT}{}^2 R_L R_S}{\eta V_{DD}}$$

Where R_L is the load resistance or resistance of the TEC and η is the efficiency of the system. An estimate of efficiency can either calculated from the Calculating Power Dissipation and Efficiency section or from figures A15 and A16. A reasonable approximation is η = 0.85. Although the exact resistance of a TEC varies with temperature, an estimation can be made by dividing the maximum voltage rating of the TEC by its maximum current rating.

In addition to providing protection against a short at the output, this circuit will also protect the FETs against shoot-thru current. Shoot-through will not occur when using the recommended transistors and additional capacitance shown in Tables 5 and 6.

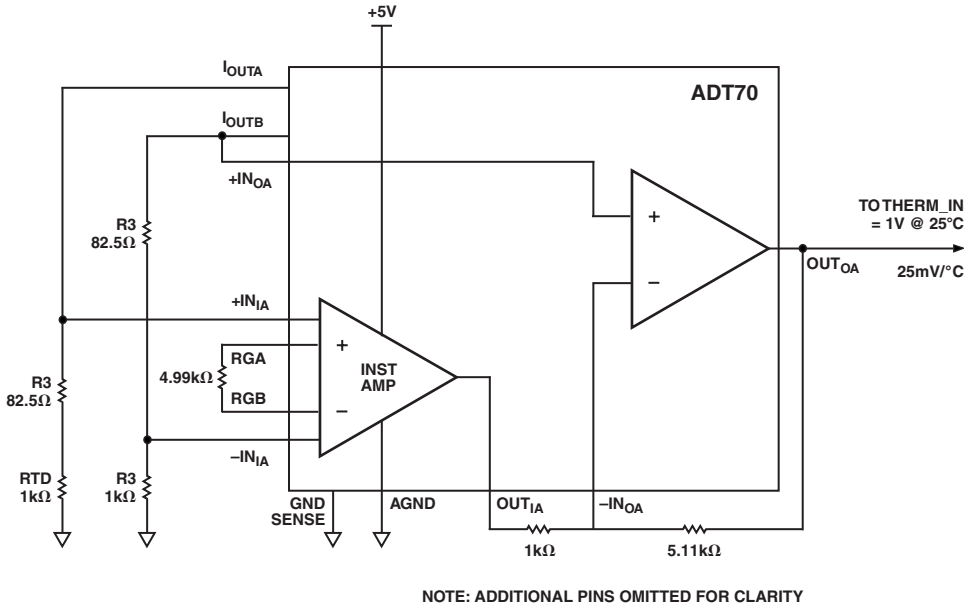


Figure A20. Using an RTD for Temperature Feedback to the ADN8830

However, if different transistors are used where their shoot-through potential is unknown, implementing the short circuit protection circuit will unconditionally protect these transistors.

To set a maximum output current limit, use the circuit in Figure A25. This circuit can share the 10 mΩ power supply shunt resistor as the short-circuit protection circuit to sense the output current. In normal operation Q1 is on, pulling the ADN8830 VLIM pin down to the voltage set by VLIMIT. This sets the maximum output voltage limit as described in the Setting the Maximum TEC Voltage section.

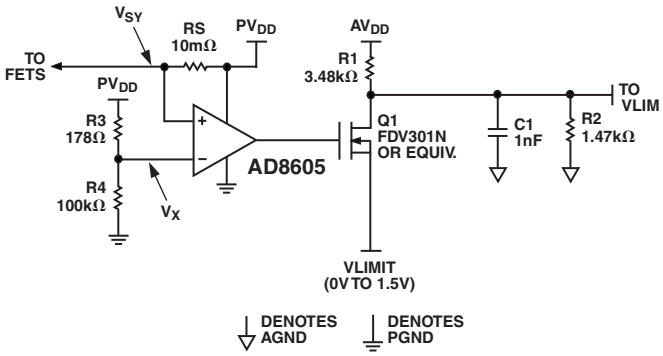


Figure A25. Setting a Maximum Output Current Limit

If the voltage at VSY drops below VX, then Q1 is turned off and the VLIM pin will be set to 1.5 V, effectively setting the maximum voltage across the outputs to 0 V. The voltage divider for VX is calculated from Equation 43.

Design Example 5

A maximum output current limit needs to be set at 1.5 A for a TEC with a maximum voltage rating of 2.5 V. The ADN8830 is powered from 5 V. The TEC resistance is estimated at 1.67 Ω and efficiency at 85%. Using Equation 43, the voltage drop across RS will be 8.8 mV when 1.5 A is delivered to the TEC. The trip voltage VX is set to 4.991 V with R3 = 178 Ω and R4 = 100 kΩ as shown in Figure A25. To set the output voltage limit to 2.5 V, the voltage at VLIMIT should be set to 0.875 V according to Equation 15.

The C1 capacitor is added to smooth the voltage transitions at VLIM. Once an over-current condition is detected, the output voltage will turn down to 0 V within 30 ms.

For a more exact measurement of the output current, place a sense resistor in series with the output load as shown in Figure A26. The AD626 instrumentation amplifier is set for a gain of 100 with a reference voltage of 2.47 V from VREF. The output of the AD626 is equal to 100 x RS x IL and is fed to the AD8602 which is set up as a window comparator. With VX greater than VLO but less than VHI, VLIM will be pulled down to the voltage at VLIMIT. Should VX fall outside the voltage window, VLIM will be pulled to 1.5 V as in Figure A25. The trip points should be set according to:

$$VHI = V_{REF} + 100 \times R_S I_{LIMIT+}$$
$$VLO = V_{REF} - 100 \times R_S I_{LIMIT-} \quad (44)$$

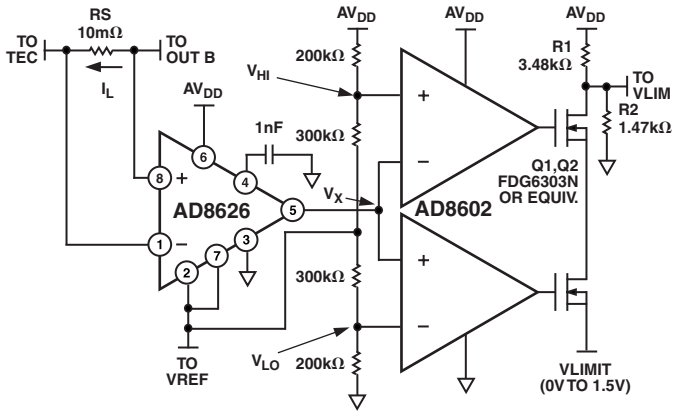


Figure 26: A High Accuracy Output Current Limit

The upper and lower trip point voltages can be set independently allowing different maximum output current limits depending on the direction of the current. The resistor divider for VHI and VLO is tapped to VREF to maintain window accuracy with any changes in VREF. Using the values from Figure A26 with a 5 V supply, the output current will not exceed 1.5 A in either direction.

Adding the current sensing resistor will slightly reduce efficiency. The power dissipated by this resistor is equal to I_{TEC}^2 x R_S, and should be included when calculating efficiency as described in the section titled Calculating Power Dissipation and Efficiency.

Using an RTD for Temperature Sensing

The ADN8830 can be used with a resistive-temperature device (RTD) as the temperature feedback sensor. The resistance of an RTD is linear with respect to temperature, offering an advantage over thermistors which have an exponential relationship to temperature. A constant current applied through an RTD will yield a voltage proportional to temperature. However, this voltage could be on the order of only 0.5 mV per °C, thus requiring the use of additional amplification to achieve a usable signal level.

The ADT70 from Analog Devices can be used to bias and amplify the voltage across an RTD, which can then be fed directly to the THERM_IN pin on the ADN8830 to provide temperature feedback for the TEC controller. The ADT70 uses a 0.9 mA current source to drive the RTD and an instrumentation amplifier with adjustable gain to boost the RTD voltage. Application notes and typical schematics for this device can be found in the ADT70 datasheet.

Most RTDs have a positive temperature coefficient, also called tempco, as opposed to thermistors which have a negative tempco. For the OUT_A output to drive the TEC- input as shown in Figure 1A, the signal from an RTD must be conditioned to create a negative tempco. This can be easily done using an inverting amplifier. Alternately, OUT_A can be connected to drive TEC+ with OUT_B driving TEC- with a positive tempco at THERMIN. This is highlighted in the Output Driver Amplifiers section.

For ADN8830 proper operation care should be taken to ensure the voltage at THERMIN remain within 0.4 V and 2.0 V. Using a 1 kΩ RTD with the ADT70 will yield a THERMIN voltage of 0.9 V at 25°C. Using the application circuit shown in Figure A20 will provide a nominal output voltage of 1.0 V at 25°C and a total gain of 66.7 mV/Ω. Using an RTD with a temperature coefficient of 0.375 Ω/°C will give a THERMIN voltage swing from 1.5 V at 5°C to 0.5 V at 45°C, well within the input range of the ADN8830.

Using a Resistive Load as a Heating Element

The ADN8830 can be used in applications that do not necessarily drive a TEC, but require only a high current output into a load resistance. Such applications generally only require heating above ambient temperature only and simply use the power dissipated by the load element to accomplish this. Because the power dissipated by such an element is proportional to the square of the output voltage, the ADN8830 application circuit must be modified. Figure A21 shows the preferred method for driving a heating element load.

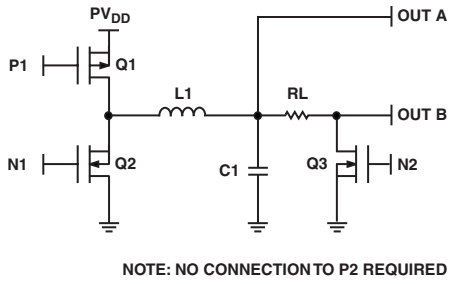


Figure A21. Using the ADN8830 to Drive a Heating Element

Current is delivered from the PWM amplifier through Q3 when the voltage at THERMIN is lower than TEMPSET. If the object temperature is greater than the target temperature, Q3 will turn off and the current through the load goes to zero, allowing the object to cool back towards the ambient temperature. As the target temperature is approached, a steady output current should be reached. Naturally, a proper compensation network must be found to ensure stability and adequate temperature settling time. The P2 output from the ADN8830 should be left unconnected.

Boosting the Output Voltage

Although the ADN8830 is designed for operation only up to 5 V, the output circuit can be modified to boost the output voltage up to 14 V. This may be required for higher voltage TECs or when more current is required from a resistive heating element. Additional circuitry is required to increase the gate drive voltage to the PMOS transistors. Figure A22 shows the modification for the PWM output. The ADP3414 takes a 0 V to 3 V input signal and converts it to the appropriate levels for both the external FETs.

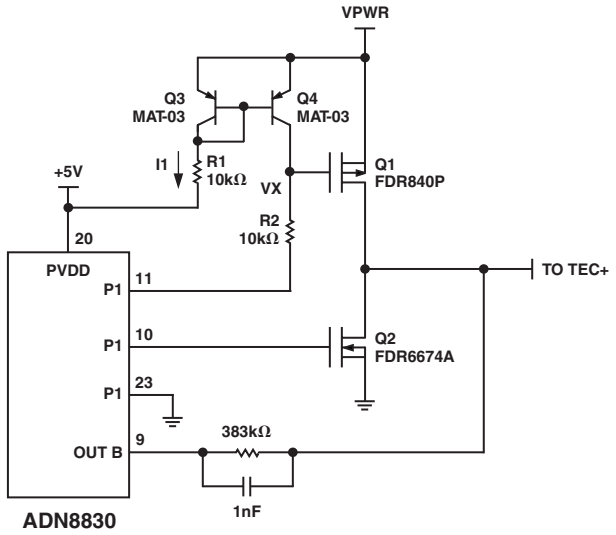


Figure A23. Boosting Linear Output Voltage up to 14 V

Note that both external FETs on the outputs of the ADP3414 must be NMOS. A PMOS transistor cannot be substituted when using this voltage boosting circuit. Larger transistors may be required to handle higher output currents to the TEC or heating element. The ADP3414 ensures one FET is completely off before turning the other FET on, thereby protecting against possible shoot through current.

The P1 output from the ADN8830 is inverted using a high speed CMOS logic gate, providing the input signal to the ADP3414. The N1 output can be left with no connection. The L-C filter can be calculated as described in the PWM Output Filter Requirements section. A 402 kΩ feedback resistor must be placed in series to the OUT_A input to ensure the voltage at Pin 19 does not exceed 5 V.

The maximum output voltage to the load can still be limited by the V_{LIM} pin on the ADN8830. The limited boosted differential output voltage is set as:

$$V_{OUT,MAX} = 4 \times \frac{V_{PWR}}{V_{DD}} \times \left(1.5 - V_{LIM}\right) \qquad (43)$$

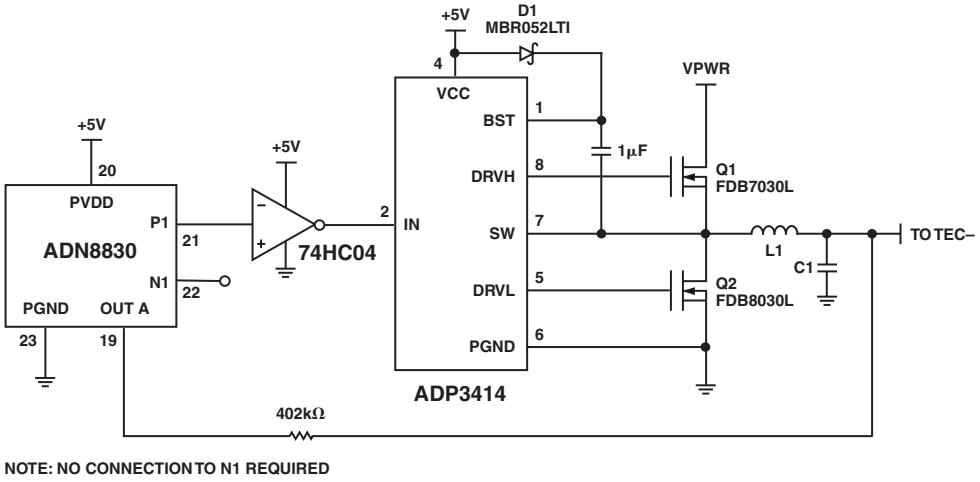


Figure A22. Boost PWM Output Voltage up to 14 V

To set the maximum output voltage to ±10 V with V_{PWR} = 12 V and PV_{DD} = 5 V, V_{LIM} should be set to 0.46 V. The input signal to the ADP3414 should never reach 100% duty cycle or the device will not operate properly. To prevent the ADN8830 P1 output from reaching a 100% duty cycle, the V_{LIM} voltage pin should be set according to Equation 15, or Figure A10, to ensure $V_{TEC,MAX}$ is less than PV_{DD}. For example: With PV_{DD} = 5 V, V_{LIM} must be set to a minimum of 0.25 V for the boosting circuit to operate correctly. Additional applications information on the ADP3414 can be found on the Analog Devices website at **www.analog.com.**

No modification is required to the external NMOS FET connected to N2 for the linear amplifier output. If the output load is a resistive heating element, then do not connect a PMOS transistor to the P2 output from the ADN8830 as shown in Figure A21. If the load is a TEC, then connect the PMOS as shown in Figure A23. Here, a voltage level shift must be added to provide the correct gate drive voltage for Q1. This is done by using a current mirror where I1 sets up the reference current and I2 equals I1. The voltage at VX will be approximately:

$$VX \approx V_{P1} + V_{PWR} - V_{DD} - V_{BE,Q3} \quad (44)$$

Where V_{P1} is the output voltage at P1. The typical V_{BE} for the MAT03 will a collector current of 840 mA is about 0.58 V. Using the supply voltages as shown in Figure A23,

$$VX \approx V_{P1} + 8.42\ V \quad (45)$$

When P1 is driven low the gate-to-source voltage of Q1 is about 5.58 V, which is enough to turn Q1 on in a low-resistance state. When the P1 output goes high to 5 V, V_{GS} of Q1 is approximately 0.58 V, the V_{BE} drop across Q3. This turns Q1 off. Other bipolar transistors and PMOS FETs can be used provided the threshold voltage (V_T) for Q1 is higher than the V_{BE} drop across Q1. Otherwise, Q1 will never fully turn off and excessive shoot-thru current could occur through Q1 and Q2.

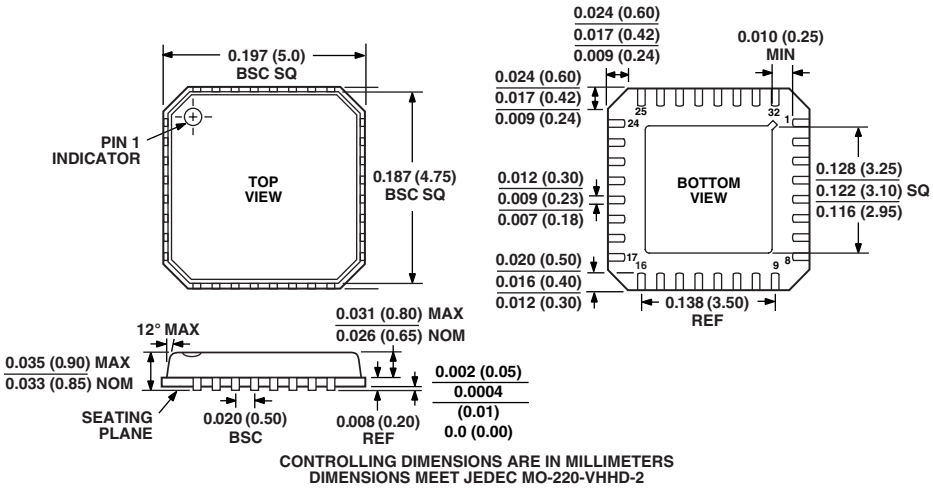
A feedback resistor between TEC+ and OUT_B of 383 kΩ must be used to prevent more than 5 V from reaching OUT_B. A 1 nF capacitor is placed in parallel to improve the linear amplifier stability and loop response time.

Although these voltage boosting circuits can be used with lower voltages, VPWR cannot exceed 14 V for both the linear and the PWM boosting circuits.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

32-Lead LFCSP
(CP Suffix)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS MEET JEDEC MO-220-VHHD-2