Datasheet

VSC7126

1.0625 Gbits/sec Fibre Channel Transceiver

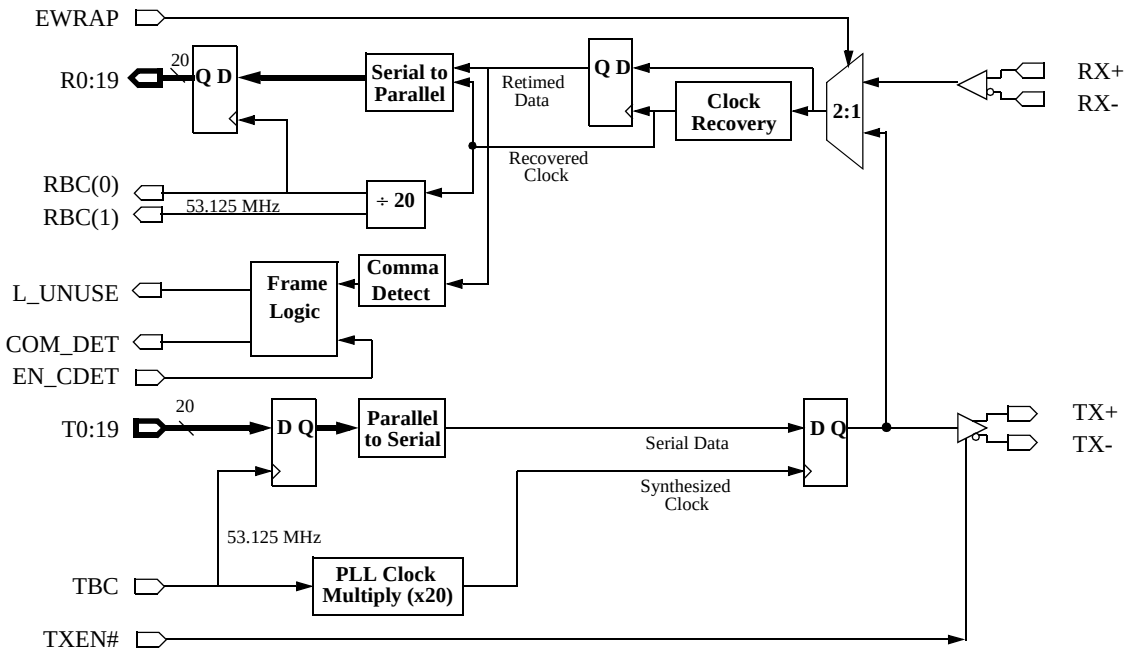
Features

- ANSI X3T11 Fibre Channel Compatible 1.0625 Gbps Full-duplex Transceiver
- GLM Compatible (FCSI-301-Rev 1.0)
- 20 Bit TTL Interface For Transmit And Receive Data
- Monolithic Clock Synthesis And Clock Recovery - No External Components
- 53.125 MHz TTL Reference Clock
- Automatic Lock-to-Reference Function
- Suitable For Both Copper And Fiber Optical Link Applications
- Low Power Operation - 850 mW
- 80 Pin, 14x14 mm PQFP
- Single +3.3V Power Supply

General Description

The VSC7126 is a full-speed Fibre Channel Transceiver optimized for Host Adapter and other space- constrained applications. It accepts two 10-bit 8B/10B encoded transmit characters, latches them on the rising edge of TBC and serializes the data onto the TX+/- PECL differential outputs at a baud rate which is twenty times the TBC frequency. It also samples serial receive data on the RX+/- PECL differential inputs, recovers the clock and data, deserializes it onto two 10-bit receive characters, outputs a recovered clocks at one twentieth of the incoming baud rate and detects Fibre Channel “Comma” characters. The VSC7126 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream. These circuits are fully monolithic and require no external components.

VSC7126 Block Diagram



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Functional Description

Clock Synthesizer:

The VSC7126 clock synthesizer multiplies the 53.125 MHz reference frequency provided on the TBC pin by 20 to achieve a baud rate clock at nominally 1.0625 GHz. The clock synthesizer contains a fully monolithic PLL which does not require any external components.

Serializer:

The VSC7126 accepts TTL input data as two parallel 10 bit characters on the T0:19 bus which is latched into the input latch on the rising edge of TBC. This data will be serialized and transmitted on the TX PECL differential outputs at a baud rate of twenty times the frequency of the TBC input, with bit T0 transmitted first. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification, or an equivalent, edge rich, DC-balanced code. If either EWRAP or TXEN# is HIGH the transmitter will be disabled with TX+ HIGH and TX- LOW. If both EWRAP and TXEN# are LOW, the transmitter outputs serialized data.

Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. The 20 bit interface on the VSC7126 corresponds to two transmission characters. This mapping is illustrated in Figure 1.

Figure 1: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a
Valid Comma Position														1	1	1	1	1	0	0

Last Data Bit Transmitted

First Data Bit Transmitted

Clock Recovery:

The VSC7126 accepts differential high speed serial inputs on the RX+/RX- pins, (when EWRAP is LOW), extracts the clock and retimes the data. The serial bit stream should be encoded to provide DC balance and limited run length by a Fibre Channel compatible 8B/10B transmitter or equivalent. The VSC7126 clock recovery circuitry is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within 200 ppm of twenty times the TBC frequency. This allows oscillators on either end of the link to be 53.125 MHz +/- 100ppm.

Deserializer:

The retimed serial bit stream is converted into two 10-bit parallel output characters. The VSC7126 provides a TTL recovered clock, RBC(0) and its complement RBC(1), at one-twentieth of the serial baud rate. The clocks are generated by dividing down the high-speed clock which is phase locked to the serial data. The serial data is retimed by the internal high-speed clock, and deserialized. The resulting parallel data will be captured

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by the adjoining protocol logic on the falling edge of RBC(0). In order to maximize the setup and hold times available at this interface, the parallel data is loaded into the output register at a point nominally midway between the falling edges of RBC(0).

If serial input data is not present, or does not meet the required baud rate, the VSC7126 will continue to produce a recovered clock so that downstream logic may continue to function. In the absence of a signal, the RBC(0)/RBC(1) output clocks will immediately lock to the TBC reference clock.

Word Alignment:

The VSC7126 provides 7-bit Fibre Channel comma character recognition and data word alignment. Word synchronization is enabled by asserting EN_CDET HIGH. When synchronization is enabled, the VSC7126 constantly examines the serial data for the presence of the Fibre Channel “comma” character. This pattern is “0011111XXX”, where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined specifically for synchronization in Fibre Channel systems. Improper alignment of the comma character is defined as any of the following conditions:

1) The comma is not aligned within the 10-bit transmission character such that T0...T6 = “0011111”

2) The comma straddles the boundary between two 10-bit transmission characters.

When EN_CDET is HIGH and an improperly aligned comma is encountered, the internal data is shifted in such a manner that the comma character is aligned properly in R0:6 as shown in Figure 1. This results in proper character and word alignment. When the parallel data alignment changes in response to an improperly aligned comma pattern, some data which would have been presented on the parallel output port may be lost. However, the synchronization character and subsequent data will be output correctly and properly aligned. When EN_CDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, COM_DET is driven HIGH to inform the user that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the comma character and has a duration equal to the data. The COM_DET signal is timed such that it can be captured by the adjoining protocol logic on the falling edge of RBC(0). Functional waveforms for synchronization are given in Figure 2 and Figure 3. Figure 2 shows the case when a comma character is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the comma character on R0:6. Figure 3 shows the case where the K28.5 is detected, but it is out of phase and a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.

Signal Detection:

An output, LUNUSE, is provided to signal when the link is open or down. This signal is asserted if R0:19 are all either LOW or HIGH and EWRAP is LOW.

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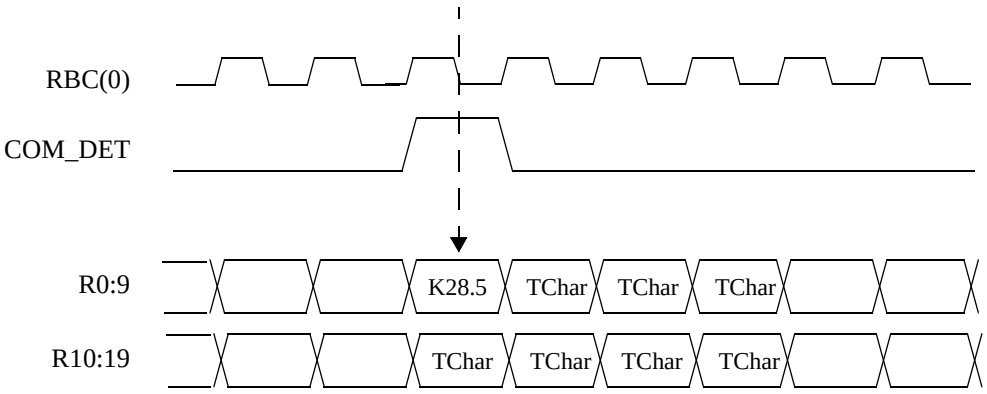
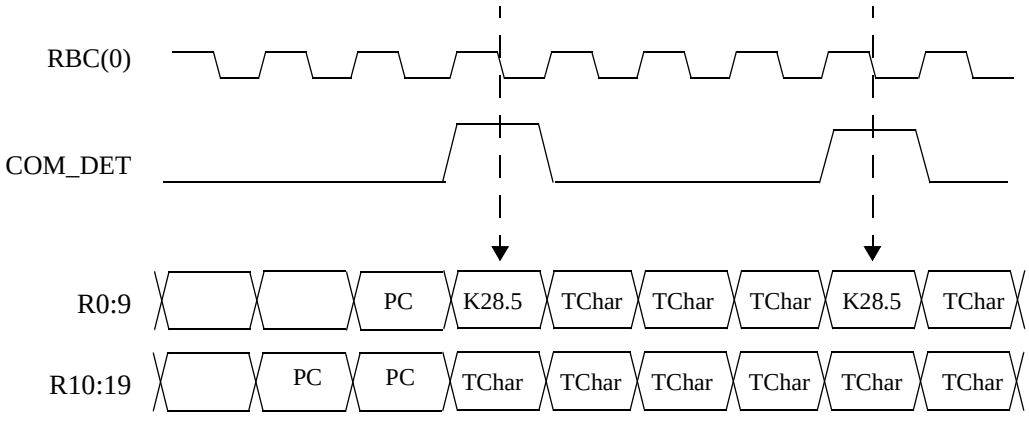
Figure 2: Detection of a Properly Aligned Comma Character



TChar: 10 bit Transmission Character

Figure 3: Detection and Resynchronization of an Improperly Aligned Comma

Receiving Two Consecutive K28.5+TChar Transmission Words



PC = Potentially Corrupted

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AC Characteristics

Figure 4: Transmit Timing Waveforms

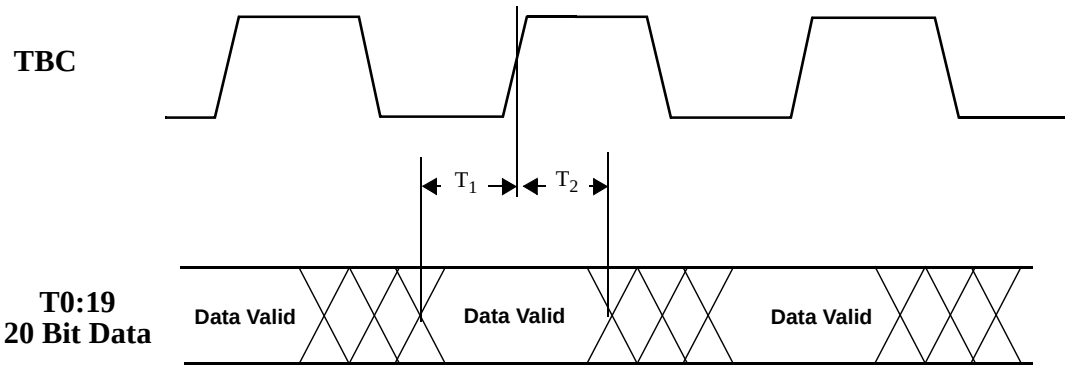

Table 1: Transmit AC Characteristics

Parameters	Description	Min	Max	Units	Conditions
T_1	T0:19 Setup time to the rising edge of TBC	1.5	—	ns.	Measured between the valid data level of T0:19 to the 1.4V point of TBC
T_2	T0:19 hold time after the rising edge of TBC	2.5	—	ns.	
T_{SDR},T_{SDF}	TX+/TX- rise and fall time	—	300	ps.	20% to 80%, 75 Ohm load to Vdd-2V Tested on a sample basis
T_{LAT}	Latency from rising edge of TBC to T0 appearing on TX+/TX-	20 bc - 4 ns		ns.	bc = Bit Clock Periods
Transmitter Output Jitter Allocation					
T_{RJ}	Serial data output random jitter (RMS)	—	20	ps.	RMS, tested on a sample basis (refer to Figure 8)
T_{DJ}	Serial data output deterministic jitter (p-p)	—	120	ps.	Peak to peak, tested on a sample basis (refer to Figure 8)

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Figure 5: Receive Timing Waveforms

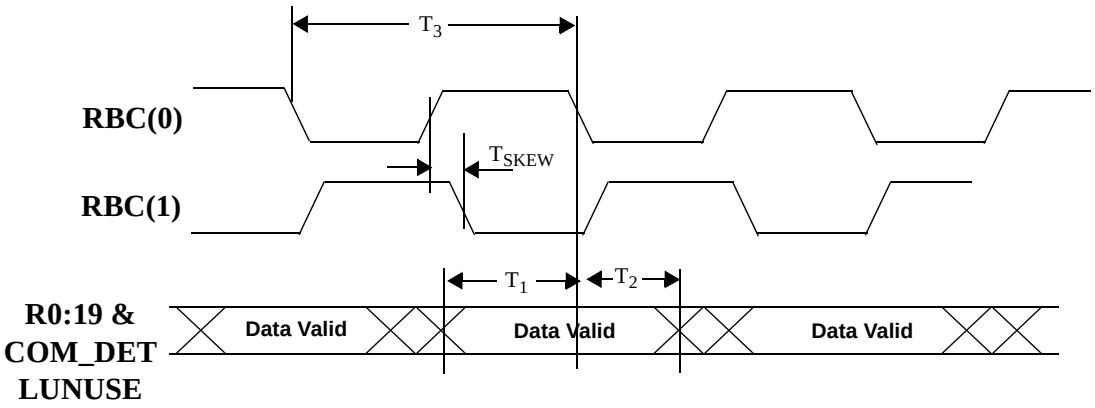

Table 2: Receive AC Characteristics

Parameters	Description	Min.	Max.	Units	Conditions
T_1	Data or COM_DET Valid prior to RBC(0) fall	4	—	ns.	Measured between the 1.4V point of RBC(0) and a valid level of R0:19 or COM_DET. All outputs driving 10pF load.
T_2	Data or COM_DET Valid after RBC(0) fall	6.0	—	ns.	
T_4	Deviation of RBC(0) falling edge to falling edge delay from nominal.	-500	500	ps.	Nominal delay is 20 bit times. Tested on sample basis
T_R, T_F	R0:19, COM_DET, RBC(0) rise and fall time	0.7	2.4	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$, into 10 pf. load.
R_{lat}	Latency from RX to RBC(0) falling and RO valid.	40 bc + 10 ns	59 bc + 10 ns	Bit Clocks	bc = bit clock periods
T_{SKEW}	Skew between edges of RBC(0) and RBC(1)	----	1.5	ns	
T_{LOCK}	Data acquisition lock time @ 1.0625Gb/s	—	2.4	µs.	8B/10B IDLE pattern. Tested on a sample basis

NOTE: Probability of Recovery for data acquisition is 95% per section 5.3 of the FC-PH rev 4.3.

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Figure 6: TBC Timing Waveforms

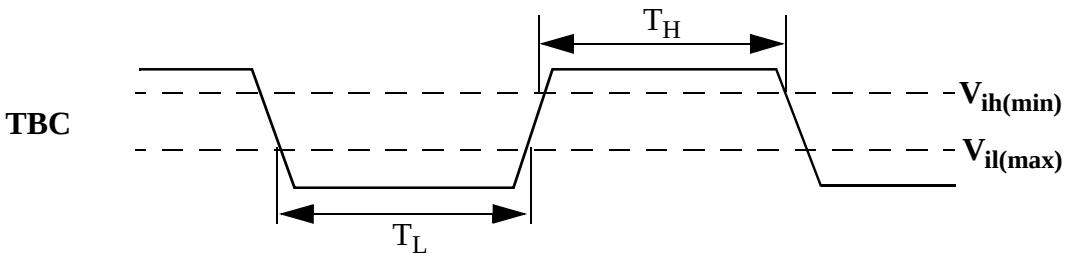

Table 3: Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FR	Frequency Range	50	55	MHz	Range over which both transmit and receive reference clocks on any link may be centered
FO	Frequency Offset	-200	200	ppm.	Mean frequency offset between transmit and receive reference clocks on one link
T_L,T_H	Pulse Width, Low / High	4.5	----	ns	Low is measured from V_{il}(max) to V_{il}(max), High is measured from V_{ih}(min) to V_{ih}(min)
DC	TBC duty cycle	30	70	%	Measured at 1.5V
T_{RCR},T_{RCF}	TBC rise and fall time	----	2.0	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$
J_T	Total jitter tolerance on REFCLK	----	120	ps	Peak-to-peak total jitter for frequencies between 50KHz and 7MHz

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DC Characteristics *(Over recommended operating conditions).*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	2.9	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
ΔV_{OUT75}	Serial Output voltage differential peak-to-peak swing (TX+/TX-)	1200	—	2200	mV	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	Serial Output voltage differential peak-to-peak swing (TX+/TX-)	1000	—	2200	mV	50Ω to V_{DD} – 2.0 V
ΔV_{IN}	Serial Input voltage differential peak-to-peak swing (RX+/RX-)	400	—	3200	mV	
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.14	—	3.47	V	3.3V±5%
P_D	Power dissipation	—	850	1560	mW	Outputs open, $V_{DD} = V_{DD}$ max
I_{DD}	Supply Current	—	245	450	mA	Outputs open, $V_{DD} = V_{DD}$ max

Absolute Maximum Ratings *(1)*

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C
Storage Temperature ..... -65^{o}C to $+150^{o}$C
Maximum Input ESD (Human Body Model) 1500V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range ..... 0^{o}C Ambient to 90^{o}C Case Temperature

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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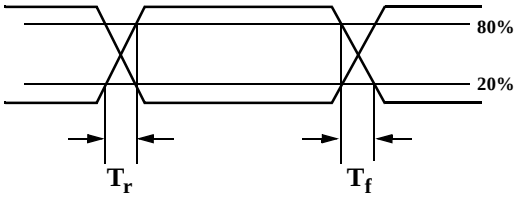
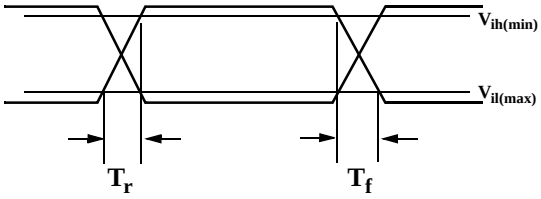
Figure 7: Parametric Measurement Information

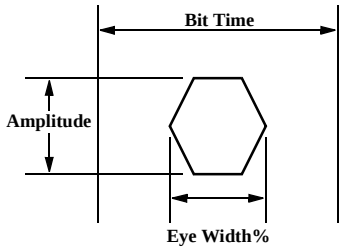
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time



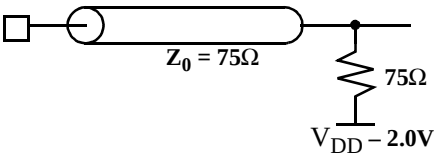
Receiver Input Eye Diagram Jitter Tolerance Mask



Total jitter tolerance is 0.7UI, according to Fibre Channel 4.3 Annex J

Parametric Test Load Circuit

Serial Output Load



TTL A.C. Output Load

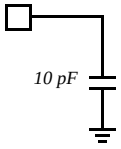


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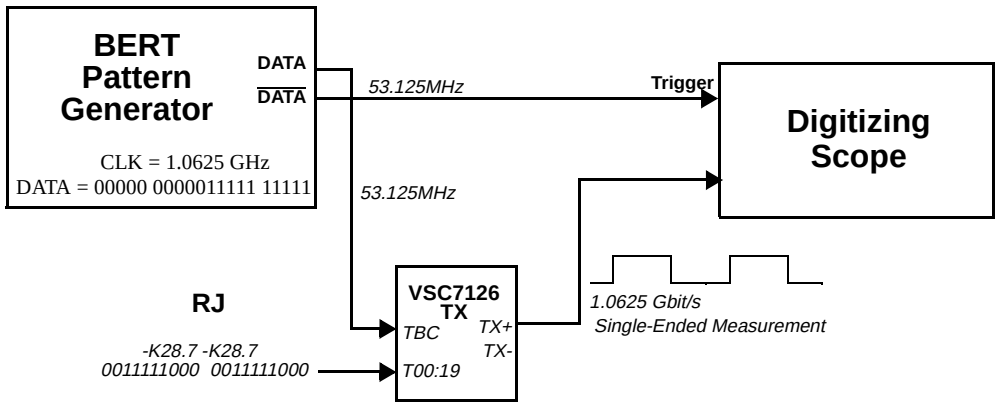
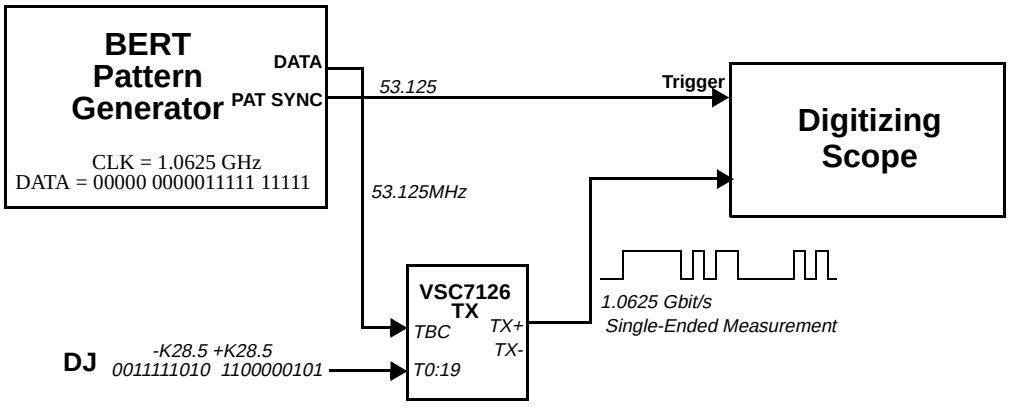
Figure 8: Transmitter Jitter Measurement Method

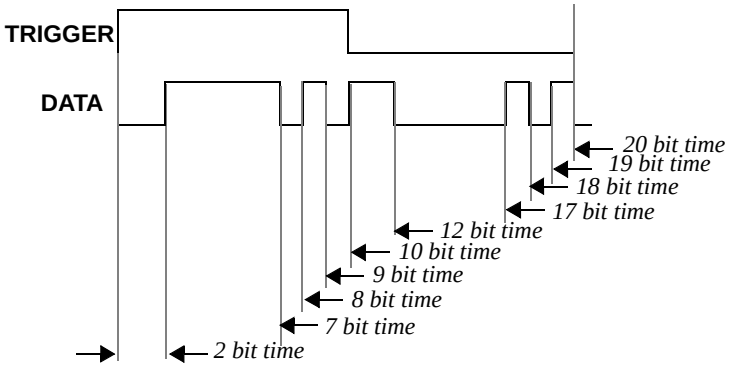
Random Jitter Measurement



Random jitter (RJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ± 7 sigma of distribution.

Deterministic Jitter Measurement





Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variation from expected.

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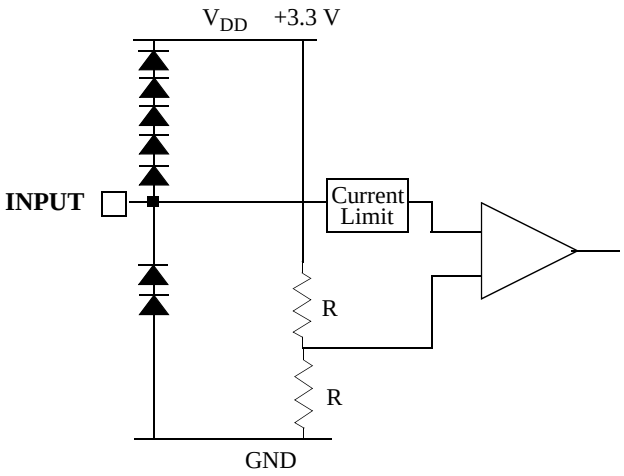
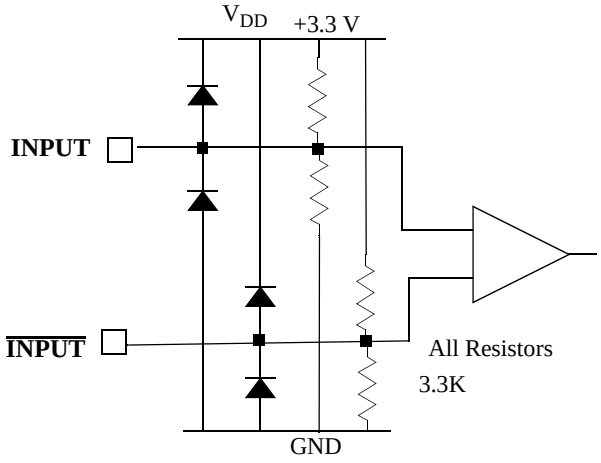
Input Structures

Figure 9: Input Structures



TBC and TTL Inputs

A



High Speed Differential Input (RX+/RX-)

B

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Package Pin Descriptions

Figure 10: Pin Diagram

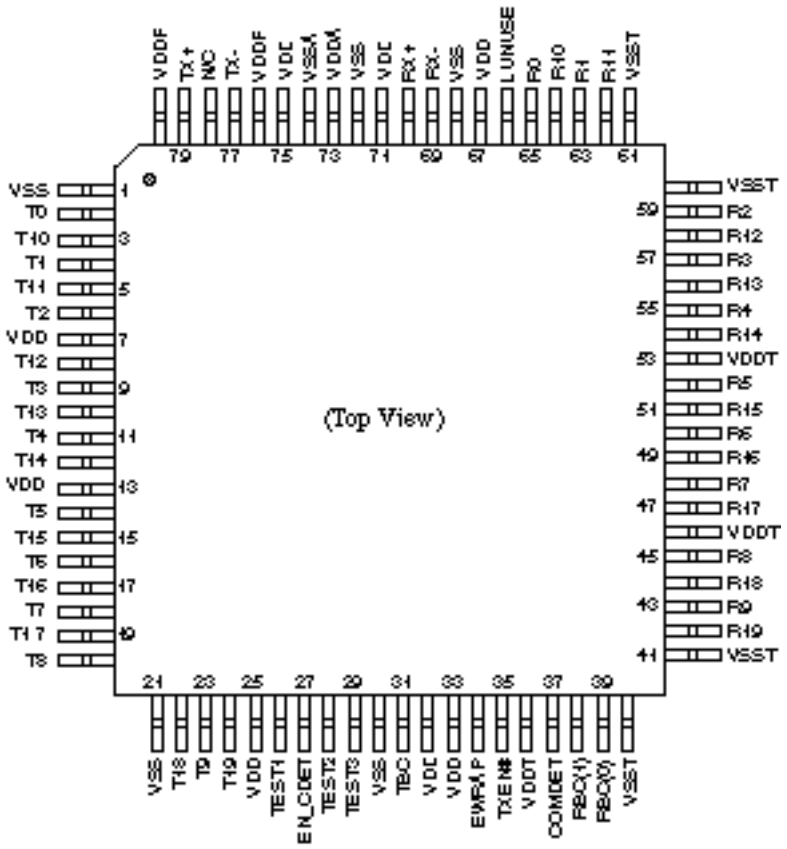

Table 4: Pin Identification

Pin #	*Name*	*Description*
2,4,6,9,11,14, 16,18,20,23,3, 5,8,10,12,15, 17,19,22,24	T0:19	**T**ransmit Data Bus, Bits **0** thru **19**. INPUTS - TTL 20-bit transmit character. Parallel data on this bus is clocked in on the rising edge of TBC. The data bit corresponding to T0 is transmitted first.
31	TBC	**T**ransmit **B**yte **C**lock. INPUT - TTL This rising edge of this clock latches T0:9 into the input register. It also provides the reference clock, at one twentieth of the baud rate to the PLL.
79 77	TX+ TX-	**T**ransmitter Serial Outputs. OUTPUTS - Differential PECL These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX- is LOW. (AC Coupling recommended)

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Pin #	*Name*	*Description*
65,63,59,57, 55,52,50,48, 45,43,64,62, 58,56,54,51, 49,47,44,42	R0:19	**R**eceive Data Bus, Bits **0** thru **19** OUTPUTS - TTL 20-bit received character. Parallel data on this bus is clocked out on the rising edge of RBC(0). R0 is the first bit received on RX+/RX-.
34	EWRAP	**E**nable Internal **WRAP** Mode. INPUT - TTL LOW for Normal Operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled, TX+ = HIGH and TX- is LOW.
70 69	RX+ RX-	**R**eceive Serial Inputs INPUTS - Differential PECL The receiver inputs when EWRAP is LOW. Internally biased to VDD/2, with 3.3KΩ resistors to VDD and GND. (AC Coupling recommended)
39 38	RBC(0) RBC(1)	**R**ecovered **B**yte **C**lock and Complement OUTPUT - TTL Recovered clock and complement derived from one twentieth of the RX+/- data stream. The rising edge of RBC(0) corresponds to a new word on R0:19.
27	EN_CDET	**EN**able **C**omma **DET**ect. INPUT - TTL Enables comma detection and word resynchronization when HIGH. When LOW, keeps current word alignment and disables comma detection.
37	COMDET	**COM**ma **DET**ect OUTPUT - TTL This output goes HIGH to indicate that R0:6 contains a Comma Character (‘0011111’). COMDET will go HIGH only during a cycle when RBC(0) is falling. COMDET is enabled by EN_CDET being HIGH.
35	TXEN#	**T**ransmitter **EN**able INPUT - TTL When LOW, the TX outputs transmit serial data. When HIGH, the TX+ is HIGH and the TX- is LOW.
66	LUNUSE	Link **UNUSE** OUTPUT - TTL Normally is LOW. If R0:19 is all LOW or all HIGH and EWRAP is LOW, this output will be asserted HIGH to indicate an open link on RX+/-.
26 28 29	TEST1 TEST2 TEST3	TEST Mode Pins INPUT - TTL Factory test pins. Tie to VDD for normal operation.
1,21,30,68,72	VSS	Digital Ground
40,41,60,61	VSST	Digital Ground for TTL Outputs
74	VSSA	Analog Ground
7,13,25,32,33, 67,71,75	VDD	Digital Power (3.3V)
36,46,53	VDDT	Digital Power for TTL outputs (3.3V)
76,80	VDDP	Digital Power for PECL outputs (3.3V)
73	VDDA	Analog Power (3.3V)
78	N/C	Not Internally Connected.

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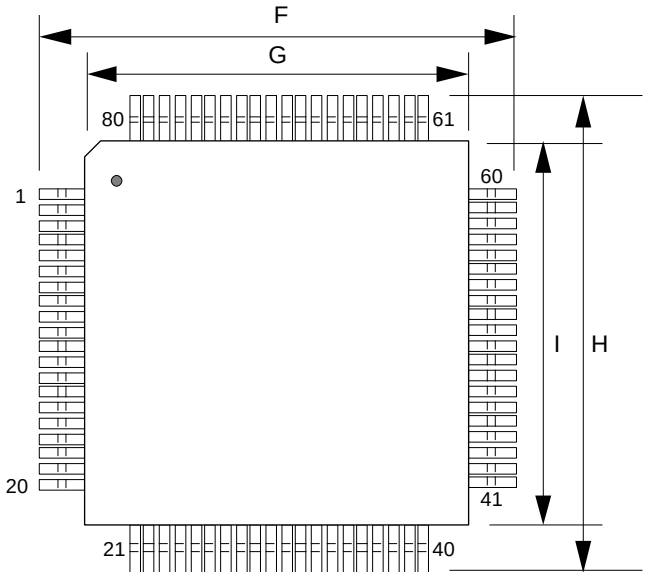
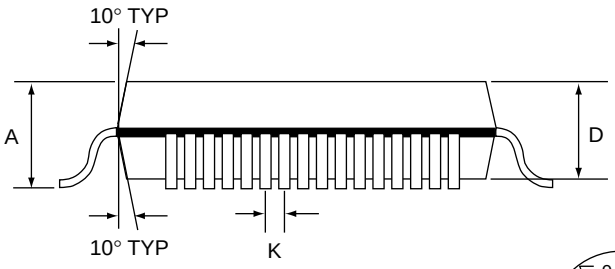
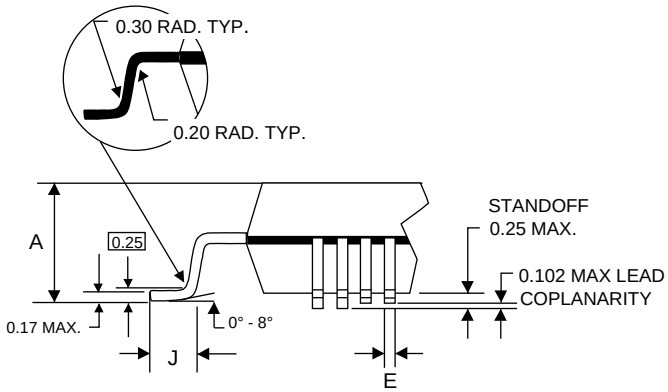
Package Information

80-pin PQFP Package Drawing



Item	14 mm	Tolerance
A	2.35	MAX
D	2.00	+0.10/-0.05
E	0.30	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15/-.10
K	0.65	BASIC





NOTES:
Drawing not to scale.
All units in mm unless otherwise noted.

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Package Thermal Characteristics

The VSC7126 is packaged in a 14 mm PQFP with an integrated heat spreader. These packages use industry-standard EIAJ footprints, but have been enhanced to improve thermal dissipation. The construction of the packages is as shown in Figure 11.

Figure 11: Package Cross Section - 14 mm package

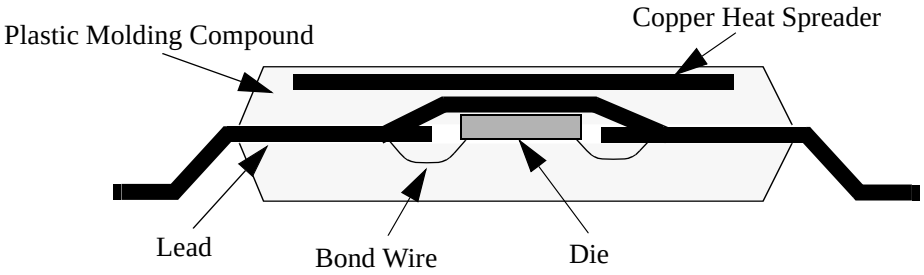

Table 5: Thermal Resistance

Symbol	*Description*	*14mm Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	17	^{o}C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	32	^{o}C/W
θ_{ca-100}	Thermal resistance from case to ambient with 100 LFM airflow	28	^{o}C/W
θ_{ca-200}	Thermal resistance from case to ambient with200 LFM airflow	25	^{o}C/W
θ_{ca-400}	Thermal resistance from case to ambient with 400 LFM airflow	22	^{o}C/W
θ_{ca-600}	Thermal resistance from case to ambient with 600 LFM airflow	20	^{o}C/W

The VSC7126 is designed to operate with a case temperature up to 90^{o}C. The user must guarantee that the temperature specification is not violated. With the Thermal Resistances shown above, the 14x14 PQFP can operate in still air ambient temperatures of 40^{o}C (40°C = 90°C - 1.56W * 32°C/W). If the ambient air temperature exceeds these limits, then some form of cooling through a heatsink or an increase in airflow will be needed.

Moisture Sensitivity Level

This device is rated with a moisture sensitivity level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC7126 QX

Device Type
VSC7126: 1.0625 Gbps Transceiver

Package Style
QX: 80-pin, 14 x 14 mm PQFP

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products, specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirmation that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

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