System Reset (with built-in watchdog timer)
Monolithic IC MM1135, MM1136

Outline

These ICs were developed to drive low voltage batteries, and have a watchdog timer with built-in microcomputer reset voltage detection circuit and low battery detection circuit.
A single reference voltage is used for low battery voltage detection and microcomputer reset voltage detection, so detection voltage difference is uniform (≒ 0.2V). Further, there is a built-in watchdog timer for operation diagnosis, which prevents the system from running wild by generating an intermittent reset pulse during system mis-operation.

Features

1. Accurate voltage drop detection voltage
   1. Low battery detection 3.4V±3%
   2. Power supply voltage detection 3.2V±3%
   3. Detection voltage error 0.2V±20mV 1-2
   4. Hysteresis Both 50mV typ.
2. Watchdog function stop pin (can be made to function only as reset IC during V_{CC} rise)
3. Low current consumption 150μA typ.

Package

SOP-8C (MM1135XF, MM1136XF)

Applications

1. 3V cordless telephones
2. Various types of small, handy equipment

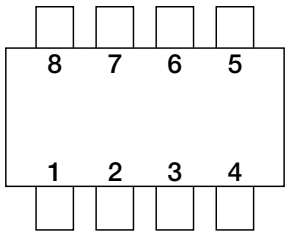
Series Table

Model	V_{SLB}	V_{SLR}	T_{PR}	T_{WD}	T_{WR}
MM1135	3.4V	3.2V	100mS	10mS	2mS
MM1136			100mS	100mS	2mS

*C_T=0.02μF

T_{PR} : Reset hold time during V_{CC} rise
T_{WD} : Timer monitoring time
T_{WR} : Reset time
V_{SLB} : Battery check detection voltage
V_{SLR} : Reset detection voltage

Pin Assignment



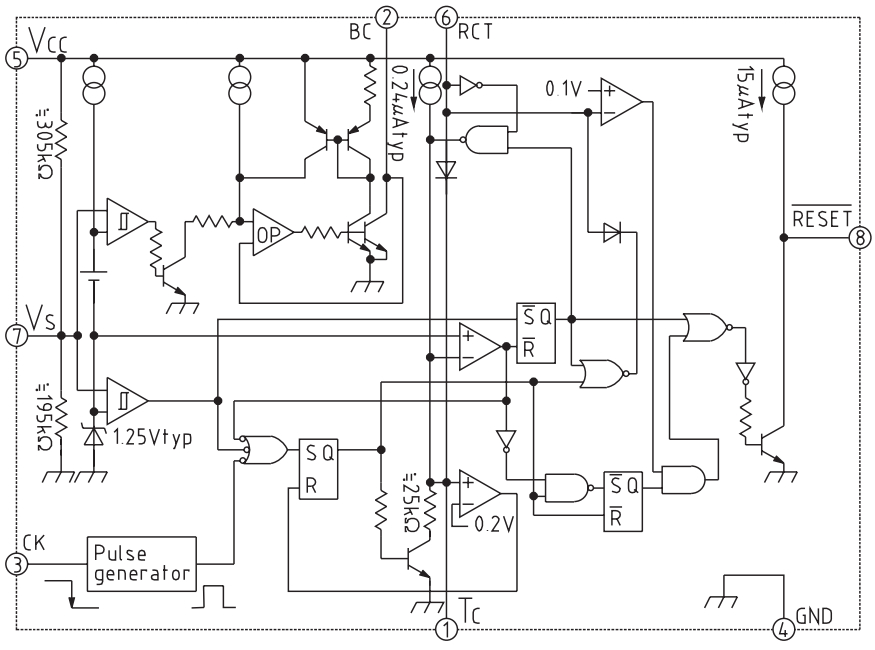
SOP-8C

1	TC
2	BC ($\overline{\text{RESET}}$)
3	CK
4	GND
5	V_{CC}
6	RCT
7	V_S
8	$\overline{\text{RESET}}$

Pin Description

Pin No.	Pin name	Function
1	TC	T_{WD}, T_{WR}, T_{PR} time setting pins.
2	BC ($\overline{\text{RESET}}$)	Battery check output pin (RESET low level output) for 3.4V
3	CK	Clock input pin
4	GND	GND pin
5	V_{CC}	Power supply voltage input pin
6	RCT	Watchdog timer stop pin Operation → OPEN, Stop → connect to GND
7	V_S	Detection voltage fine adjustment pin
8	$\overline{\text{RESET}}$	Reset output pin (low output)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V_{CC} max.	–0.3~+7	V
Voltage applied to input pin	V_{IN}	–0.3~V_{CC}+0.3 (≦ +7)	V
Voltage applied to output pin	V_{OUT}	–0.3~V_{CC}+0.3 (≦ +7)	V
Allowable loss	Pd	450	mW
Storage temperature	T_{STG}	–40~+125	℃

Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V_{CC}	+2.5~+6.5	V
$\overline{\text{RESET}}$ sync current	I_{OLR}	0~1.5	mA
BC sync current	I_{OLC}	0~1.5	mA
Clock input high level voltage	V_{CKH}	1.4<	V
Clock input low level voltage	V_{CKL}	<0.4	V
Clock monitoring time setting	T_{WD}	1~1000	mS
Clock rise and fall times	t_{RCK}, t_{FCK}	<100	µS
Power supply voltage rise times	t_{RVCC}	100<	µS
Power supply voltage fall times	t_{FVCC}	50<	µS
TC pin capacitance	C_T	0.002~2	µF
Operating temperature	T_{OP}	–25~+75	°C

Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc=3.8V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	I_{CC}	No load		200	280	µA
RESET detection voltage	V_{SLR}	V_{CC} : High→Low RCT : GND, V_{TC}=OPEN	3.10	3.20	3.30	V
Detection voltage temperature coefficient R	$\frac{\Delta V_{SR}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage R	V_{HYSR}	V_{CC} : Low→High RCT : GND, V_{TC}=OPEN	25	50	100	mV
BC detection voltage	V_{SLB}	V_{CC} : High→Low, R_{LB}=10kΩ	3.30	3.40	3.50	V
Detection voltage temperature coefficient B	$\frac{\Delta V_{SB}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage B	V_{HYSB}	V_{CC} : Low→High, R_{LB}=10kΩ	25	50	100	mV
Detection voltage difference	ΔV_{SL}	$\Delta V_{SL}=V_{SLB}-V_{SLR}$	0.18	0.20	0.22	V
CK input threshold	V_{TH}		0.8	1.2	2	V
CK input current	I_{IH}	V_{CK}=3.8V		0	1	µA
	I_{IL}	V_{CK}=0.0V	–15	–6	–2	
Output voltage RH	V_{OHR}	$I_{\overline{RESET}}$=–5µA	3.0	3.4		V
Output voltage BH	V_{OHB}	R_{LB}=10kΩ	3.2	3.6		V
Output voltage RL	V_{OLR}	$I_{\overline{RESET}}$=1mA, V_{CC}=3.0V		0.3	0.5	V
Output voltage BL	V_{OLB}	I_{BC}=5mA, V_{CC}=3.0V		0.3	0.5	V
Output sync current R	I_{OLR}	$V_{\overline{RESET}}$=0.5V, V_{CC}=3.0V	1	2		mA
Output sync current B	I_{OLB}	V_{BC}=0.5V, V_{CC}=3.0V	5	10		mA
Output source current R	I_{OHR}	$V_{\overline{RESET}}$=3.4V	8	15		µA
C_T charge current	$I_{CT}1$	V_{TC}=1.0V during watchdog timer operation	–0.48	–0.24	–0.16	µA
	$I_{CT}2$	V_{TC}=1.0V during power ON reset operation	–0.48	–0.24	–0.16	µA
Minimum operating power supply voltage to ensure $\overline{RESET}$	V_{CC}	$V_{\overline{RESET}}$=0.4V $I_{\overline{RESET}}$=0.1mA		0.8	1.0	V

V_{CC} input pulse width	T_{PI}	V_{CC} 3.8V / 2.8V, T_{PI}	8			µS
CK input pulse width	T_{CKW}	CK, T_{CKW} or	3			µS
CK input cycle	T_{CK}	CK, T_{CK}	20			µS
Watchdog timer monitoring time *1	T_{WD}	C_T=0.02µF	50	100	150	mS
Watchdog timer reset time *2	T_{WR}	C_T=0.02µF	1	2	3	mS
Reset hold time for power supply rise *3	T_{PR}	C_T=0.02µF	50	100	150	mS
$\overline{RESET}$ delay time	t_{PDR}	V_{CC} : High→Low, R_{LR}=10kΩ, C_{LR}=15pF		10		µS
BC delay time	t_{PDB}	V_{CC} : High→Low, R_{LB}=4.7kΩ, C_{LB}=15pF		10		µS
$\overline{RESET}$ rise time	t_{RR}	R_{LR}=10kΩ, C_{LR}=15pF		10		µS
$\overline{RESET}$ fall time	t_{FR}	R_{LR}=10kΩ, C_{LR}=15pF		2		µS
BC rise time	t_{RB}	R_{LB}=4.7kΩ, C_{LB}=15pF		10		µS
BC fall time	t_{FB}	R_{LB}=4.7kΩ, C_{LB}=15pF		2		µS

Notes:

*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output.
In other words, reset output is output if a clock pulse is not input during this time.

*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

*3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SHR}) during power ON reset until reset release ($\overline{RESET}$ output high).

*4 Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. The times are expressed by the following formulae.

T_{PR} (mS) ≒ 5000×C_T (µF)

T_{WD} (mS) ≒ 5000×C_T (µF)

T_{WR} (mS) ≒ 100×C_T (µF)

Example : When C_T=0.02µF

T_{PR} ≒ 100mS

T_{WD} ≒ 100mS

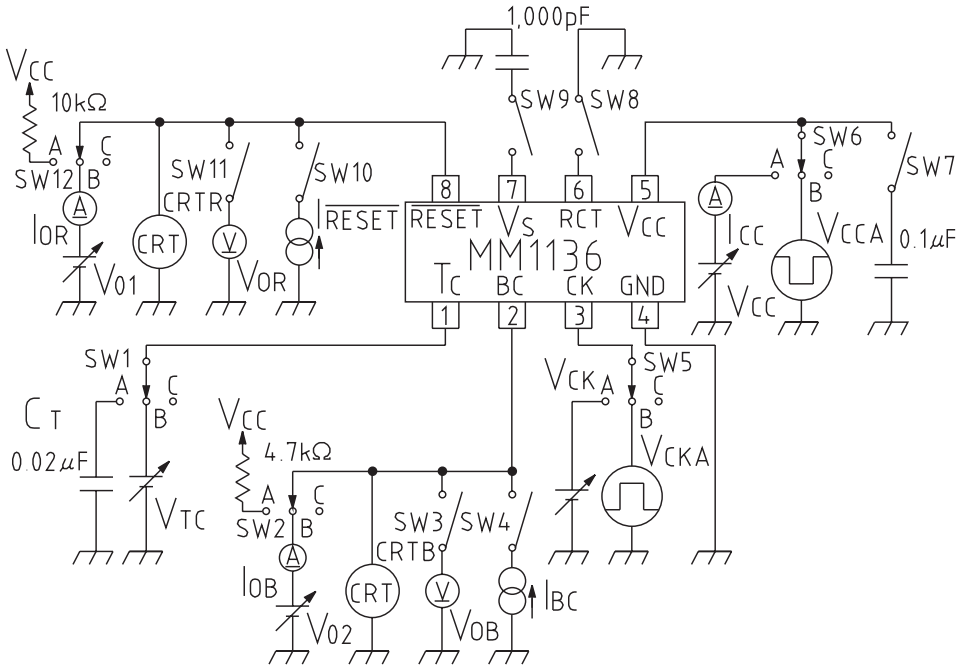
T_{WR} ≒ 2mS

*5 T_{WD} can be varied by placing a resistor (1MEGΩ or more) between the RCT pin and V_{CC}.

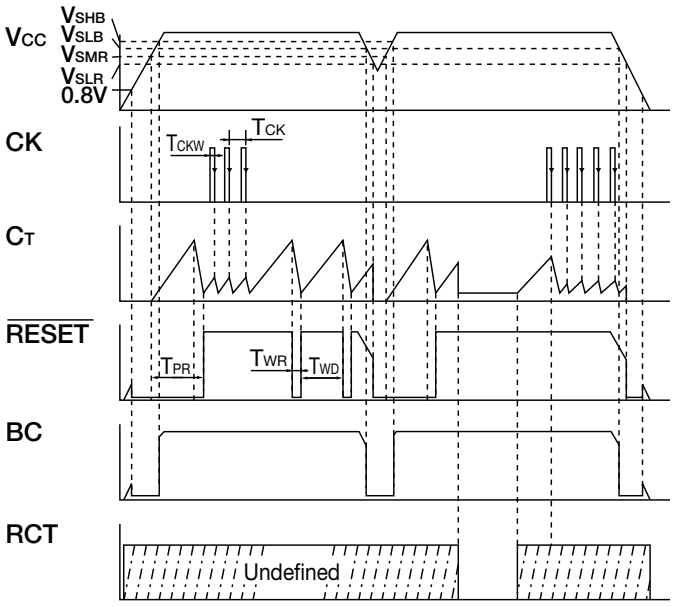
*6 The voltage range when measuring output rise and fall time is 10~90%.

*7 V_{CC} rise time should be 100µS or more, and fall time should be 50µS or more.

Measuring Circuit



Timing Chart



Basic Circuit Diagram