ELECTRICAL CHARACTERISTICS

15.1 Absolute maximum ratings

This chapter describes electrical characteristics of the M37702M2BXXXFP and M37702M2AXXXFP.
For the low voltage version, refer to section **"18.4 Electrical characteristics."**
The 7703 Group's available pins varies from that of the 7702 Group. Refer to **"Chapter 20. 7703 GROUP."**
For the latest data, inquire of addresses described last (☞**"CONTACT ADDRESSES FOR FURTHER INFORMATION").**

In a part of the standard indicated in this chapter, there are the limits depending on each microcomputer product or used external clock input frequency. Distinguish it described below.

•Limits depending on each microcomputer
(Example) M37702M2BXXXFP
- B: When this sign is 'A,' refer to the column of "16 MHz."
- B: When this sign is 'B,' refer to the column of "25 MHz."

•Limits depending on used external clock input frequency
The calculation formula is described in the table. When the microcomputer is 16 MHz version, the limits is the value in the case of $f(X_{IN})$ = 16 MHz. When the microcomputer is 25 MHz version, the limits is the value in the case of $f(X_{IN})$ = 25 MHz.

15.1 Absolute maximum ratings

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage		−0.3 to 7	V
AV_{CC}	Analog power source voltage		−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}, BYTE		−0.3 to 12	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}, X_{IN}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}, $\overline{E}$		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25 °C	300 **(Note)**	mW
T_{opr}	Operating temperature		−20 to 85	°C
T_{stg}	Storage temperature		−40 to 150	°C

Note: In the 7703 Group, this value is 1000 mW.

15.2 Recommended operating conditions

Recommended operating conditions (V_{CC} = 5 V±10%, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		4.5	5.0	5.5	V
AV_{CC}	Analog power source voltage			V_{CC}		V
V_{SS}	Power source voltage			0		V
AV_{SS}	Analog power source voltage			0		V
V_{IH}	High-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0.5V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16V_{CC}	V
$I_{OH\ (peak)}$	High-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–10	mA
$I_{OH\ (avg)}$	High-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–5	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			10	mA
$I_{OL\ (avg)}$	Low-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			5	mA
$f(X_{IN})$	External clock input frequency	M37702M2BXXXFP			25	MHz
		M37702M2AXXXFP			15	

Notes 1: Average output current is the average value of a 100 ms interval.

2: The sum of I_{OL}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL}(peak) for ports P4, P5, P6, and P7 must be 80 mA or less, and the sum of I_{OH}(peak) for ports P4, P5, P6, and P7 must be 80 mA or less.

15.3 Electrical characteristics

Electrical characteristics (V_{CC} = 5 V, V_{SS} = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OH} = −10 mA		3			V
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OH} = −400 μA		4.7			V
V_{OH}	High-level output voltage	$P3_2$	I_{OH} = −10 mA		3.1			V
			I_{OH} = −400 μA		4.8			
V_{OH}	High-level output voltage	$\overline{E}$	I_{OH} = −10 mA		3.4			V
			I_{OH} = −400 μA		4.8			
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 10 mA				2	V
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OL} = 2 mA				0.45	V
V_{OL}	Low-level output voltage	$P3_2$	I_{OL} = 10 mA				1.9	V
			I_{OL} = 2 mA				0.43	
V_{OL}	Low-level output voltage	$\overline{E}$	I_{OL} = 10 mA				1.6	V
			I_{OL} = 2 mA				0.4	
V_{T+}–V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$–$TA4_{IN}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{INT_0}$–$\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1			0.4		1	V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.2		0.5	V
V_{T+}–V_{T-}	Hysteresis	X_{IN}			0.1		0.3	V
I_{IH}	High-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I = 5 V				5	μA
I_{IL}	Low-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I = 0 V				−5	μA
V_{RAM}	RAM hold voltage		When clock is stopped.		2			V
I_{CC}	Power source current		In single-chip mode, output pins are open, and the other pins are connected to V_{SS}.	$f(X_{IN})$ = 25 MHz		19	38	mA
				$f(X_{IN})$ = 16 MHz		12	24	
				Ta = 25 °C,when clock is stopped			1	μA
				Ta = 85 °C,when clock is stopped			20	μA

15.4 A-D converter characteristics

A-D CONVERTER CHARACTERISTICS (V_{CC} = AV_{CC} = 5 V ± 10%, V_{SS} = AV_{SS} = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}			8	Bits
—	Absolute accuracy	V_{REF} = V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}	2		10	kΩ
t_{CONV}	Conversion time	f(X_{IN}) = 25 MHz	9.12			μs
		f(X_{IN}) = 16 MHz	14.25			
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

15.5 Internal peripheral devices

Timing requirements (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

Timer A input (count input in event counter mode)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	125		80		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	62		40		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	62		40		ns

Timer A input (gating input in timer mode)

Symbol	Parameter	Data formula	Limits				Unit
			16 MHz		25 MHz		
			Min.	Max.	Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{f(X_{IN})}$	500		320		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns

Note: TAi_{IN} input cycle time must be 4 cycles or more of count source,
TAi_{IN} input high-level pulse width must be 2 cycles or more of count source,
TAi_{IN} input low-level pulse width must be 2 cycles or more of count source.

Timer A input (external trigger input in one-shot pulse mode)

Symbol	Parameter	Data formula	Limits				Unit
			16 MHz		25 MHz		
			Min.	Max.	Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width		150		80		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width		150		80		ns

Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	125		80		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	125		80		ns

Timer A input (up-down input in event counter mode)

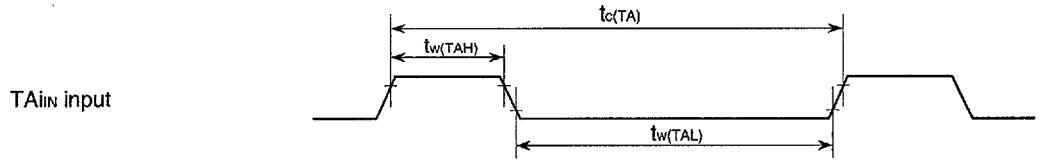
Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2500		2000		ns
$t_{w(UPH)}$	TAi_{OUT} input high-level pulse width	1250		1000		ns
$t_{w(UPL)}$	TAi_{OUT} input low-level pulse width	1250		1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	500		400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	500		400		ns

Timer A input (Two-phase pulse input in event counter mode)

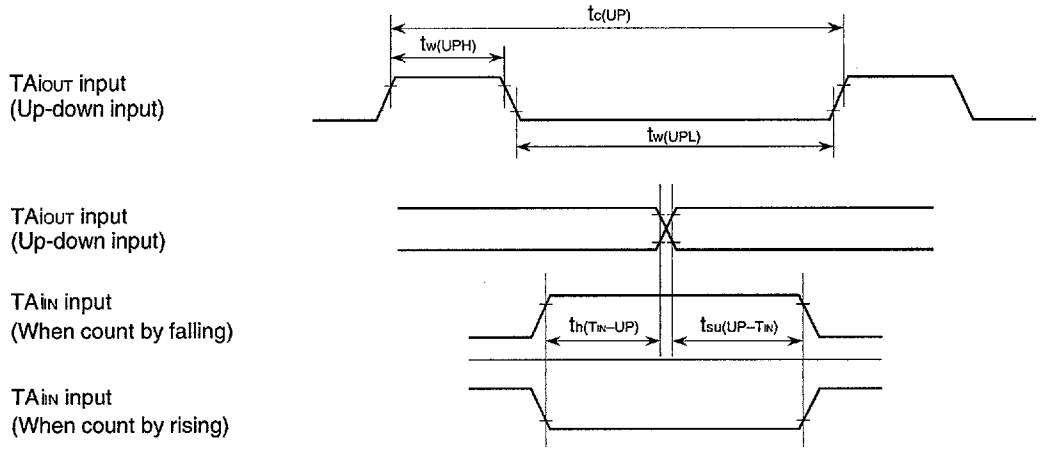
Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{c(TA)}$	TAjIN input cycle time	1000		800		ns
$t_{su(TAjIN-TAjOUT)}$	TAjIN input setup time	250		200		ns
$t_{su(TAjOUT-TAjIN)}$	TAjOUT input setup time	250		200		ns

Internal peripheral devices

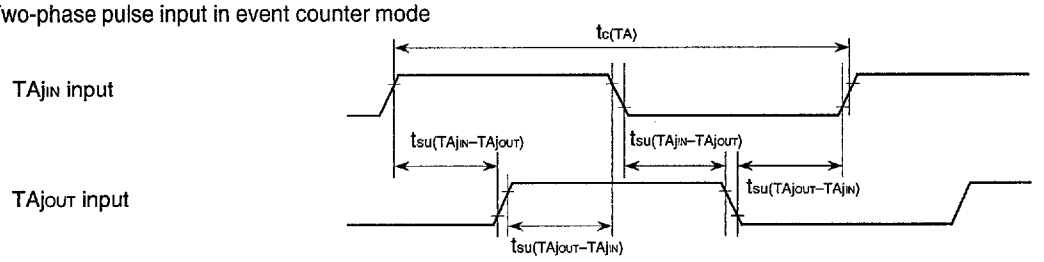
- Count input in event counter mode
- Gating input in timer mode
- External trigger input in one-shot pulse mode
- External trigger input in pulse width modulation mode



- Up-down input, count input in event counter mode



- Two-phase pulse input in event counter mode



Test conditions

•V_{CC} = 5 V ± 10%

•Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V

Timer B input (count input in event counter mode)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (one edge count)	125		80		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	62		40		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	62		40		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (both edges count)	250		160		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	125		80		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	125		80		ns

Timer B input (pulse period measurement mode)

Symbol	Parameter	Data formula	Limits				Unit
			16 MHz		25 MHz		
			Min.	Max.	Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{f(X_{IN})}$	500		320		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns

Note: TBi_{IN} input cycle time must be 4 cycles or more of count source,
TBi_{IN} input high-level pulse width must be 2 cycles or more of count source,
TBi_{IN} input low-level pulse width must be 2 cycles or more of count source.

Timer B input (pulse width measurement mode)

Symbol	Parameter	Data formula	Limits				Unit
			16 MHz		25 MHz		
			Min.	Max.	Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{f(X_{IN})}$	500		320		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{f(X_{IN})}$	250		160		ns

Note: TBi_{IN} input cycle time must be 4 cycles or more of count source,
TBi_{IN} input high-level pulse width must be 2 cycles or more of count source,
TBi_{IN} input low-level pulse width must be 2 cycles or more of count source.

A-D trigger input

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)	1000		1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	125		125		ns

ELECTRICAL CHARACTERISTICS

15.5 Internal peripheral devices

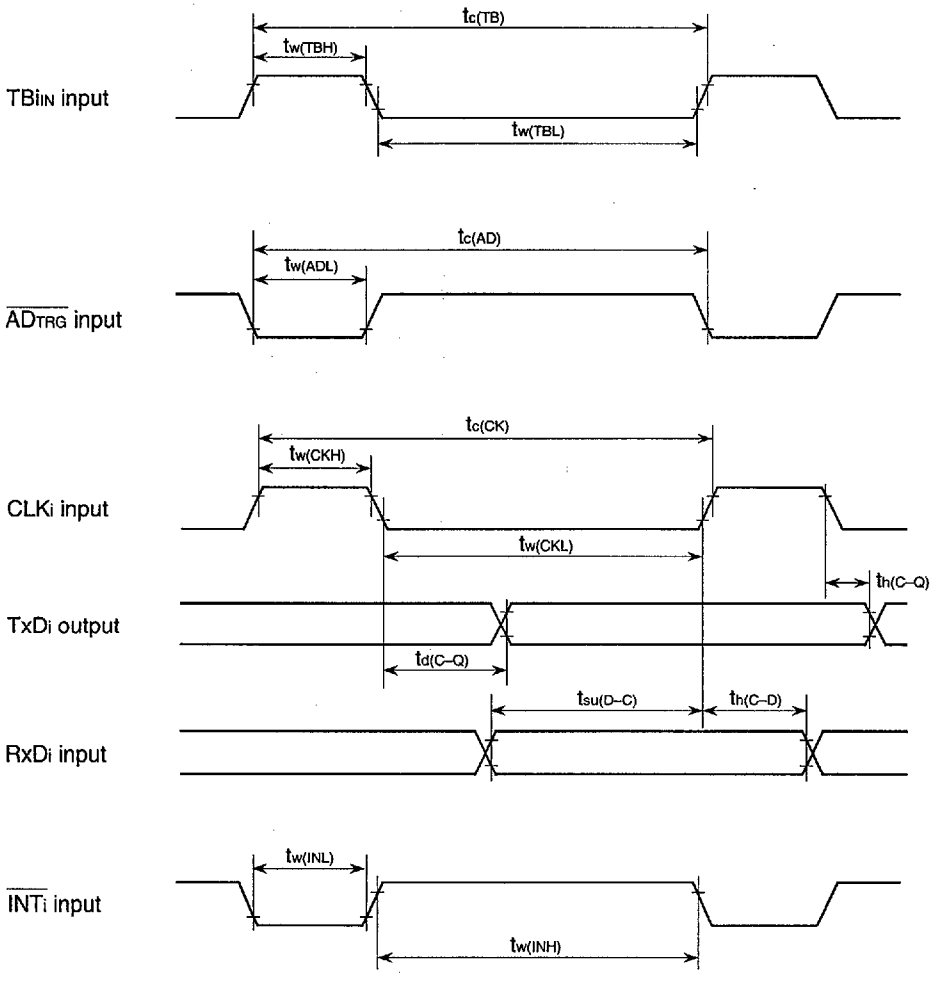
Serial I/O

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	250		200		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	125		100		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	125		100		ns
$t_{d(C-Q)}$	TxDi output delay time		90		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		0		ns
$t_{su(D-C)}$	RxDi input setup time	30		30		ns
$t_{h(C-D)}$	RxDi input hold time	90		90		ns

External interrupt $\overline{INT_i}$ input

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		250		ns

Internal peripheral devices



Test conditions

- V_{CC} = 5 V ± 10%
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.6 Ready and Hold

Timing requirements (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{su(RDY-\phi)}$	$\overline{RDY}$ input setup time	60		55		ns
$t_{su(HOLD-\phi)}$	$\overline{HOLD}$ input setup time	60		55		ns
$t_{h(\phi-RDY)}$	$\overline{RDY}$ input hold time	0		0		ns
$t_{h(\phi-HOLD)}$	$\overline{HOLD}$ input hold time	0		0		ns

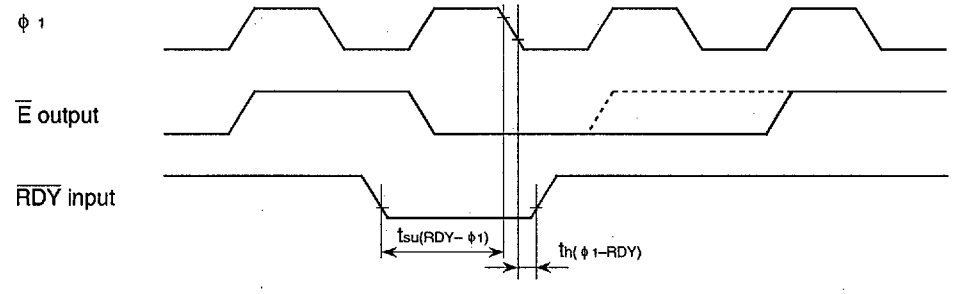
Switching characteristics (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{d(\phi-HLDA)}$	$\overline{HLDA}$ output delay time		50		50	ns

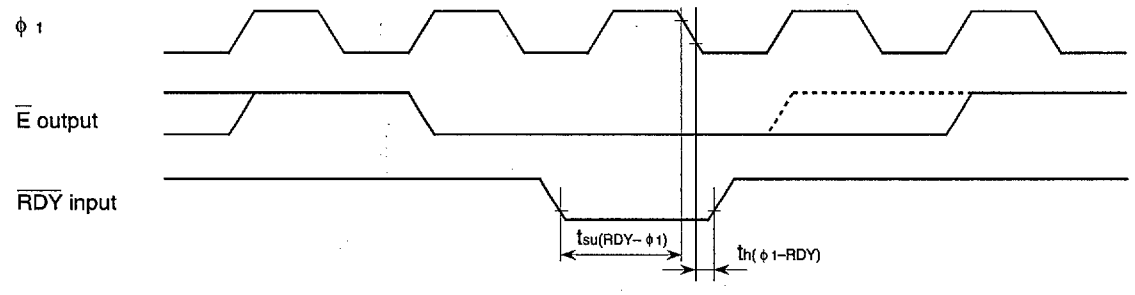
Note: For test conditions, refer to Figure 15.10.1.

● Ready function

With no Wait



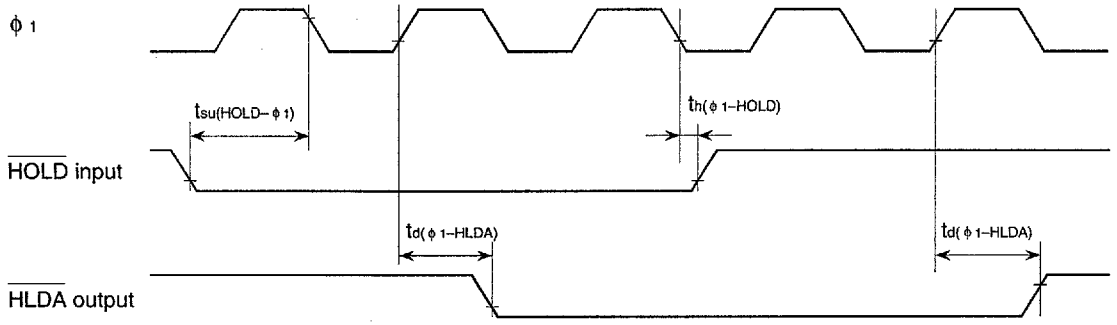
With Wait



Test conditions

- V_{CC} = 5 V±10%
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

● Hold function



Test conditions

- V_{CC} = 5 V±10%
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.7 Single-chip mode

Timing requirements (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

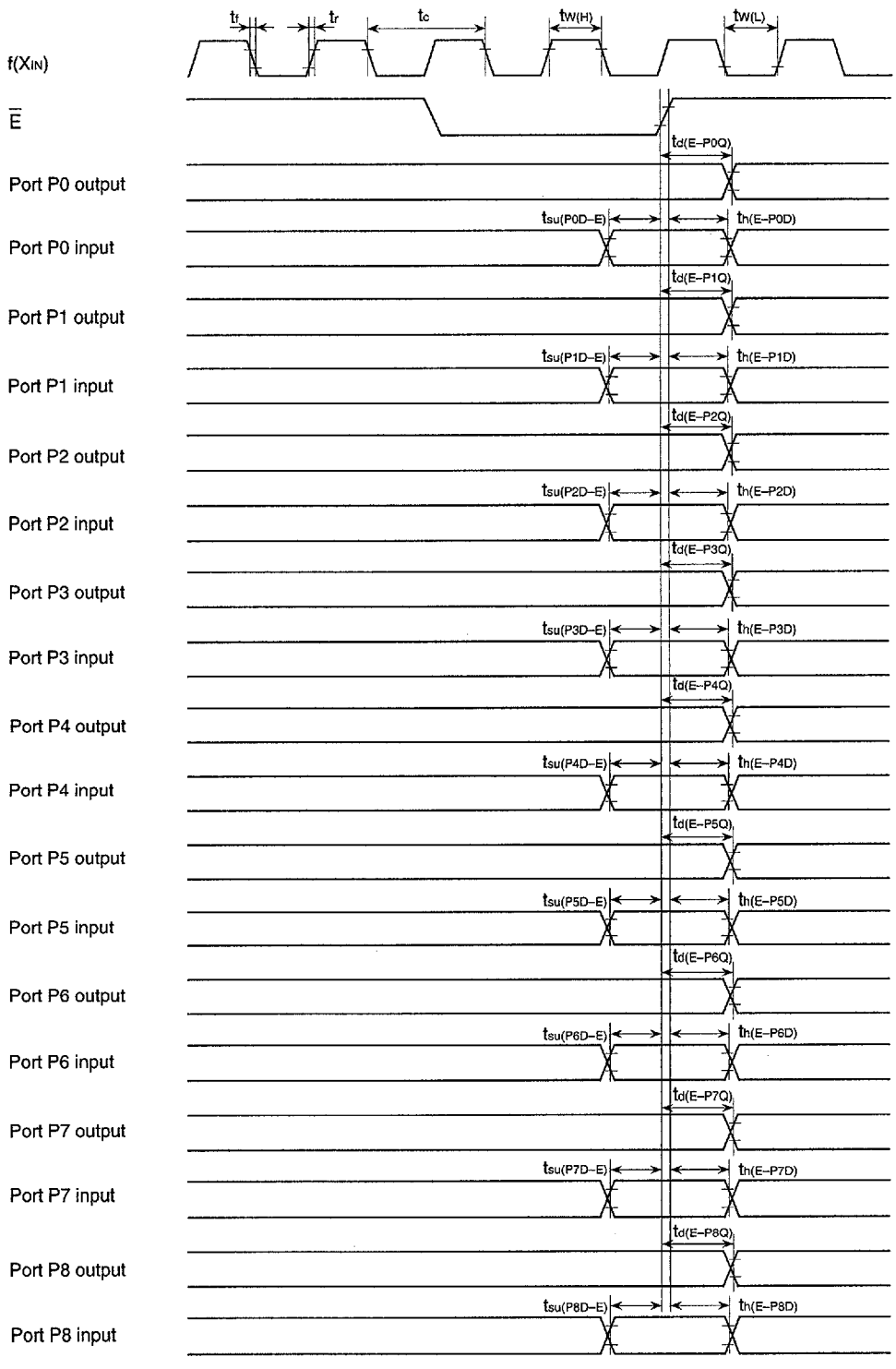
Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
t_c	External clock input cycle time	62		40		ns
$t_{w(H)}$	External clock input high-level pulse width	25		15		ns
$t_{w(L)}$	External clock input low-level pulse width	25		15		ns
t_r	External clock rise time		10		8	ns
t_f	External clock fall time		10		8	ns
$t_{su(P0D-E)}$	Port P0 input setup time	100		60		ns
$t_{su(P1D-E)}$	Port P1 input setup time	100		60		ns
$t_{su(P2D-E)}$	Port P2 input setup time	100		60		ns
$t_{su(P3D-E)}$	Port P3 input setup time	100		60		ns
$t_{su(P4D-E)}$	Port P4 input setup time	100		60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	100		60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	100		60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	100		60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	100		60		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		0		ns

Switching characteristics (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time		100		80	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time		100		80	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time		100		80	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time		100		80	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time		100		80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time		100		80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time		100		80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time		100		80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time		100		80	ns

Note: For test conditions, refer to Figure 15.10.1.

Single-chip mode



Test conditions

- V_{CC} = 5 V ±10%
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.8 Memory expansion mode and microprocessor mode : with no Wait

Timing requirements (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
t_c	External clock input cycle time	62		40		ns
$t_{w(H)}$	External clock input high-level pulse width	25		15		ns
$t_{w(L)}$	External clock input low-level pulse width	25		15		ns
t_r	External clock rise time		10		8	ns
t_f	External clock fall time		10		8	ns
$t_{su(P1D-E)}$	Port P1 input setup time	45		30		ns
$t_{su(P2D-E)}$	Port P2 input setup time	45		30		ns
$t_{su(P4D-E)}$	Port P4 input setup time	100		60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	100		60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	100		60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	100		60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	100		60		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		0		ns

Switching characteristics (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{d(E-P4Q)}$	Port P4 data output delay time		100		80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time		100		80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time		100		80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time		100		80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time		100		80	ns
$t_{d(E-\phi)}$	ϕ_1 output delay time	0	20	0	18	ns
$t_{w(EL)}$	$\overline{E}$ low-level pulse width	95 *		50 *		ns
$t_{d(P0A-E)}$	Port P0 address output delay time	30 *		12 *		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE = "L")		70		45	ns
$t_{pxz(E-P1Z)}$	Port P1 floating start delay time (BYTE = "L")		5		5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time	30 *		12 *		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time	24 *		5 *		ns
$t_{h(E-P2Q)}$	Port P2 data output delay time		70		45	ns
$t_{pxz(E-P2Z)}$	Port P2 floating start delay time		5		5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time	30 *		12 *		ns
$t_{h(P2A-ALE)}$	Port P2 address output delay time	24 *		5 *		ns
$t_{d(ALE-E)}$	ALE output delay time	4		4		ns
$t_{w(ALE)}$	ALE pulse width	35 *		22 *		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time	30 *		20 *		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time	30 *		20 *		ns

Note: For test conditions, refer to Figure 15.10.1.
* This is the value depending on f(X_{IN}). For data formula, refer to Table 15.8.1.

ELECTRICAL CHARACTERISTICS

15.8 Memory expansion mode and microprocessor mode : with no Wait

Switching characteristics (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{h(E-P0A)}$	Port P0 address hold time	25*		18 *		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE = "L")	9		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE = "L")	25*		18 *		ns
$t_{pzx(E-P1Z)}$	Port P1 floating release delay time (BYTE = "L")	36*(Note 1)		18 *		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE = "H")	25*		18 *		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time	9		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time	25*		18 *		ns
$t_{pzx(E-P2Z)}$	Port P2 floating release delay time	36*(Note 1)		18 *		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time	18		18		ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time	18		18		ns

Notes 1: For the M37702E2AXXXFP, M37702E2AFS, M37702E4AXXXFP, and M37702E4AFS, refer to section **"19.5.4 Bus timing and EPROM mode."** For the M37703E2AXXXSP and M37703E4AXXXSP, refer to section **"20.6.2 Bus timing and EPROM mode."**

2: For test conditions, refer to Figure 15.10.1.

*: This is the value depending on f(X_{IN}). For data formula, refer to Table 15.8.1.

Table 15.8.1 Bus timing data formula

Sign \ f(X_{IN})	f(X_{IN}) ≤ 8 MHz	8 MHz < f(X_{IN}) ≤ 16 MHz	16 MHz < f(X_{IN}) ≤ 25 MHz
$t_{w(EL)}$	$\frac{2 \times 10^9}{f(X_{IN})} - 30$		
$t_{d(P0A-E)}$ $t_{d(P1A-E)}$ $t_{d(P2A-E)}$	$100 + \frac{1 \times 10^9}{f(X_{IN})} - 125$	$30 + \frac{1.2 \times 10^9}{f(X_{IN})} - 75$	$12 + \frac{1 \times 10^9}{f(X_{IN})} - 40$
$t_{d(P1A-ALE)}$ $t_{d(P2A-ALE)}$	$\frac{1 \times 10^9}{f(X_{IN})} - 45$	$\frac{1 \times 10^9}{f(X_{IN})} - 38.5$	$\frac{1 \times 10^9}{f(X_{IN})} - 35$
$t_{w(ALE)}$	$\frac{1 \times 10^9}{f(X_{IN})} - 35$	$\frac{1 \times 10^9}{f(X_{IN})} - 27.5$	$\frac{1 \times 10^9}{f(X_{IN})} - 18$
$t_{d(BHE-E)}$ $t_{d(R/W-E)}$	$100 + \frac{1 \times 10^9}{f(X_{IN})} - 125$	$30 + \frac{1.2 \times 10^9}{f(X_{IN})} - 75$	$20 + \frac{1 \times 10^9}{f(X_{IN})} - 40$
$t_{h(E-P0A)}$ $t_{h(E-P1A)}$ $t_{h(E-P1Q)}$ $t_{h(E-P2Q)}$	$\frac{1 \times 10^9}{2 \times f(X_{IN})} - 12.5$	$\frac{1 \times 10^9}{2 \times f(X_{IN})} - 6.25$	$\frac{1 \times 10^9}{2 \times f(X_{IN})} - 2$
$t_{pzx(E-P1Z)}$ $t_{pzx(E-P2Z)}$ **(Note)**	$\frac{1 \times 10^9}{f(X_{IN})} - 30$	$\frac{1 \times 10^9}{f(X_{IN})} - 26$	$\frac{1 \times 10^9}{f(X_{IN})} - 22$

Note: For the M37702E2AXXXFP, M37702E2AFS, M37702E4AXXXFP, and M37702E4AFS, refer to section **"19.5.4 Bus timing and EPROM mode."** For the M37703E2AXXXSP and M37703E4AXXXSP, refer to section **"20.6.2 Bus timing and EPROM mode."**

Memory expansion mode and microprocessor mode ; With no Wait

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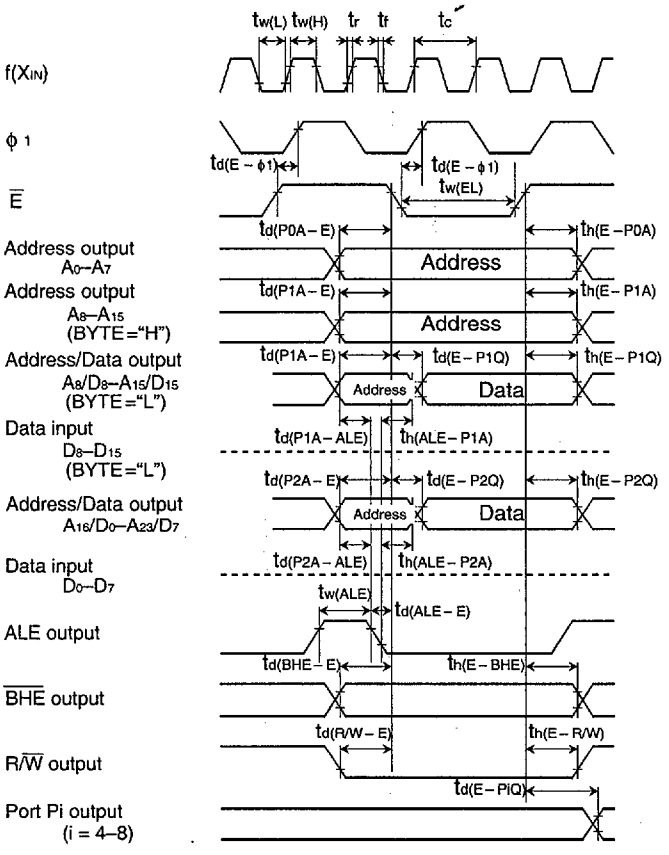

Test conditions (ϕ1, E, P0–P3)

- V_{CC} = 5 V ± 10%
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Test conditions (P4–P8)

- V_{CC} = 5 V ± 10%
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0V

15.8 Memory expansion mode and microprocessor mode : with no Wait

Memory epxansion mode and microprocessor mode ; With no Wait

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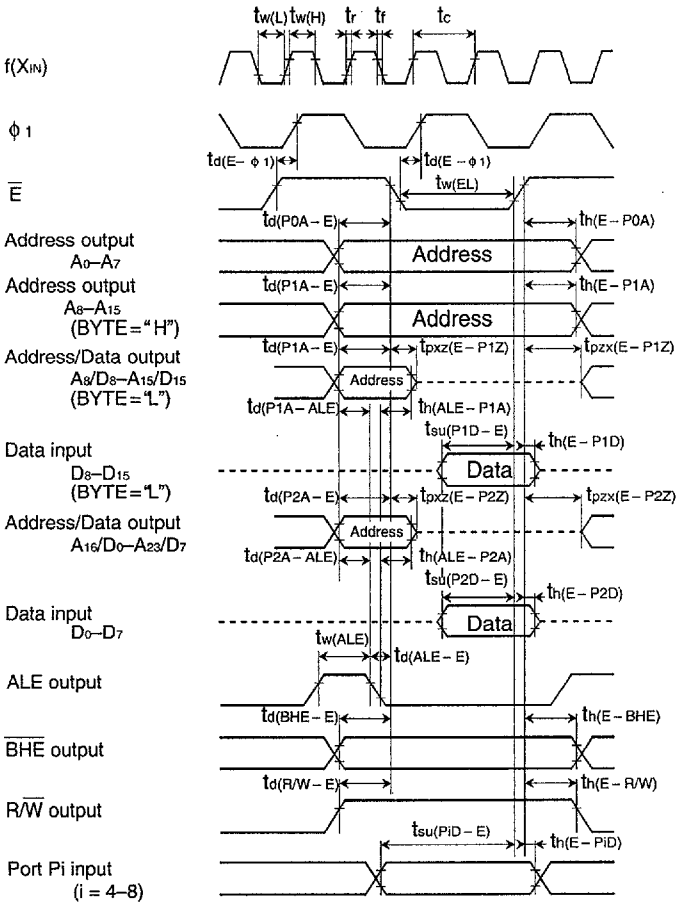

Test conditions (φ1, E, P0–P3)

- Vcc = 5 V ± 10%
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (P4–P8)

- Vcc = 5 V ± 10%
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V

15.9 Memory expansion mode and microprocessor mode : with Wait

Timing requirements (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
t_c	External clock input cycle time	62		40		ns
$t_{w(H)}$	External clock input high-level pulse width	25		15		ns
$t_{w(L)}$	External clock input low-level pulse width	25		15		ns
t_r	External clock rise time		10		8	ns
t_f	External clock fall time		10		8	ns
$t_{su(P1D-E)}$	Port P1 input setup time	45		30		ns
$t_{su(P2D-E)}$	Port P2 input setup time	45		30		ns
$t_{su(P4D-E)}$	Port P4 input setup time	100		60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	100		60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	100		60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	100		60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	100		60		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		0		ns

Switching characteristics (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{d(E-P4Q)}$	Port P4 data output delay time		100		80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time		100		80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time		100		80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time		100		80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time		100		80	ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time	0	20	0	18	ns
$t_{w(EL)}$	$\overline{E}$ low-pulse width	220 *		130 *		ns
$t_{d(P0A-E)}$	Port P0 address output delay time	30 *		12 *		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE = "L")		70		45	ns
$t_{pxz(E-P1Z)}$	Port P1 floating start delay time (BYTE = "L")		5		5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time	30 *		12 *		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time	24 *		5 *		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time		70		45	ns
$t_{pxz(E-P2Z)}$	Port P2 floating start delay time		5		5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time	30 *		12 *		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time	24 *		5 *		ns
$t_{d(ALE-E)}$	ALE output delay time	4		4		ns
$t_{w(ALE)}$	ALE pulse width	35 *		22 *		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time	30 *		20 *		ns
$t_{d(R/W-E)}$	$R/\overline{W}$ output delay time	30 *		20 *		ns

Note: For test conditions, refer to Figure 15.10.1.

*: This is the value depending on f(X_{IN}). For data formula, refer to Table 15.9.1.

ELECTRICAL CHARACTERISTICS

15.9 Memory expansion mode and microprocessor mode : with Wait

Switching characteristics (V_{CC} = 5 V±10%, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		16 MHz		25 MHz		
		Min.	Max.	Min.	Max.	
$t_{h(E-P0A)}$	Port P0 address hold time	25*		18*		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE = "L")	9		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE = "L")	25*		18*		ns
$t_{pzx(E-P1Z)}$	Port P1 floating release delay time (BYTE = "L")	36*(Note 1)		18*		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE = "H")	25*		18*		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time	9		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time	25*		18*		ns
$t_{pzx(E-P2Z)}$	Port P2 floating release delay time	36*(Note 1)		18*		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time	18		18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time	18		18		ns

Notes 1: For the M37702E2AXXXFP, M37702E2AFS, M37702E4AXXXFP, and M37702E4AFS, refer to section **"19.5.4 Bus timing and EPROM mode."** For the M37703E2AXXXSP and M37703E4AXXXSP, refer to section **"20.6.2 Bus timing and EPROM mode."**

2: For test conditions, refer to Figure 15.10.1.

*: This is the value depending on $f(X_{IN})$. For data formula, refer to Table 15.9.1.

Table 15.9.1 Bus timing data formula

Sign \ $f(X_{IN})$	$f(X_{IN}) \leq 8$ MHz	8 MHz < $f(X_{IN}) \leq 16$ MHz	16 MHz < $f(X_{IN}) \leq 25$ MHz
$t_{w(EL)}$	$\frac{4 \times 10^9}{f(X_{IN})} - 30$		
$t_{d(P0A-E)}$ $t_{d(P1A-E)}$ $t_{d(P2A-E)}$	$100 + \frac{1 \times 10^9}{f(X_{IN})} - 125$	$30 + \frac{1.2 \times 10^9}{f(X_{IN})} - 75$	$12 + \frac{1 \times 10^9}{f(X_{IN})} - 40$
$t_{d(P1A-ALE)}$ $t_{d(P2A-ALE)}$	$\frac{1 \times 10^9}{f(X_{IN})} - 45$	$\frac{1 \times 10^9}{f(X_{IN})} - 38.5$	$\frac{1 \times 10^9}{f(X_{IN})} - 35$
$t_{w(ALE)}$	$\frac{1 \times 10^9}{f(X_{IN})} - 35$	$\frac{1 \times 10^9}{f(X_{IN})} - 27.5$	$\frac{1 \times 10^9}{f(X_{IN})} - 18$
$t_{d(BHE-E)}$ $t_{d(R/W-E)}$	$100 + \frac{1 \times 10^9}{f(X_{IN})} - 125$	$30 + \frac{1.2 \times 10^9}{f(X_{IN})} - 75$	$20 + \frac{1 \times 10^9}{f(X_{IN})} - 40$
$t_{h(E-P0A)}$ $t_{h(E-P1A)}$ $t_{h(E-P1Q)}$ $t_{h(E-P2Q)}$	$\frac{1 \times 10^9}{2 \times f(X_{IN})} - 12.5$	$\frac{1 \times 10^9}{2 \times f(X_{IN})} - 6.25$	$\frac{1 \times 10^9}{2 \times f(X_{IN})} - 2$
$t_{pzx(E-P1Z)}$ $t_{pzx(E-P2Z)}$ **(Note)**	$\frac{1 \times 10^9}{f(X_{IN})} - 30$	$\frac{1 \times 10^9}{f(X_{IN})} - 26$	$\frac{1 \times 10^9}{f(X_{IN})} - 22$

Note: For the M37702E2AXXXFP, M37702E2AFS, M37702E4AXXXFP, and M37702E4AFS, refer to section **"19.5.4 Bus timing and EPROM mode."** For the M37703E2AXXXSP and M37703E4AXXXSP, refer to section **"20.6.2 Bus timing and EPROM mode."**

15.9 Memory expansion mode and microprocessor mode : with Wait

Memory expansion mode and microprocessor mode ; With Wait

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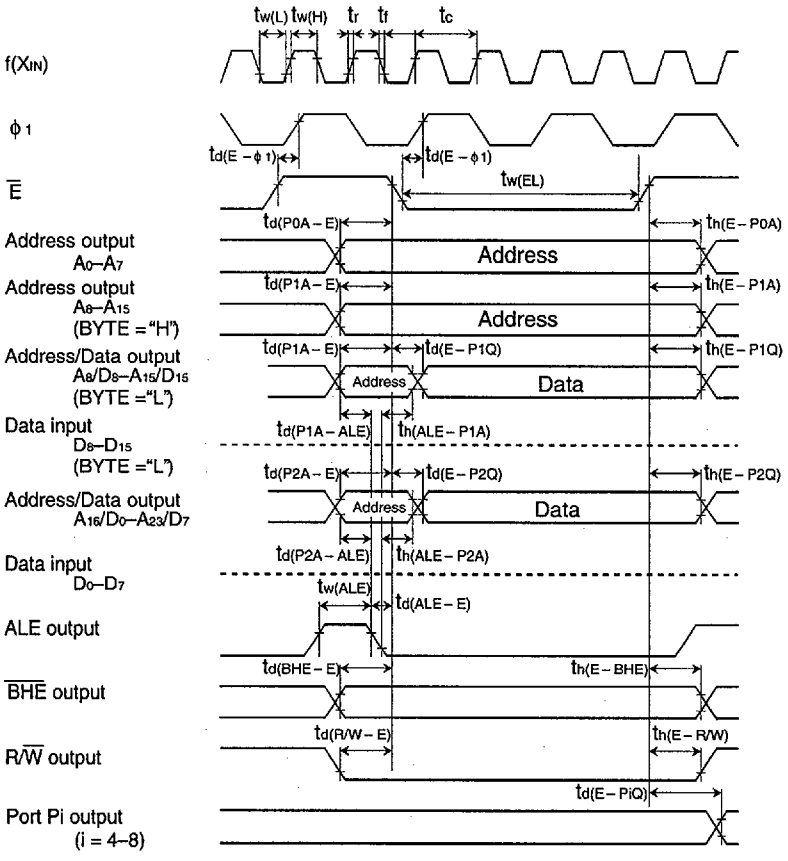

Test conditions (φ1, E, P0–P3)

- Vcc = 5 V ± 10%
- Output timing voltage : VOL = 0.8 V, VOH = 2.0V
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (P4–P8)

- Vcc = 5V ± 10%
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V

ELECTRICAL CHARACTERISTICS

15.9 Memory expansion mode and microprocessor mode : with Wait

Memory expansion mode and microprocessor mode ; With Wait

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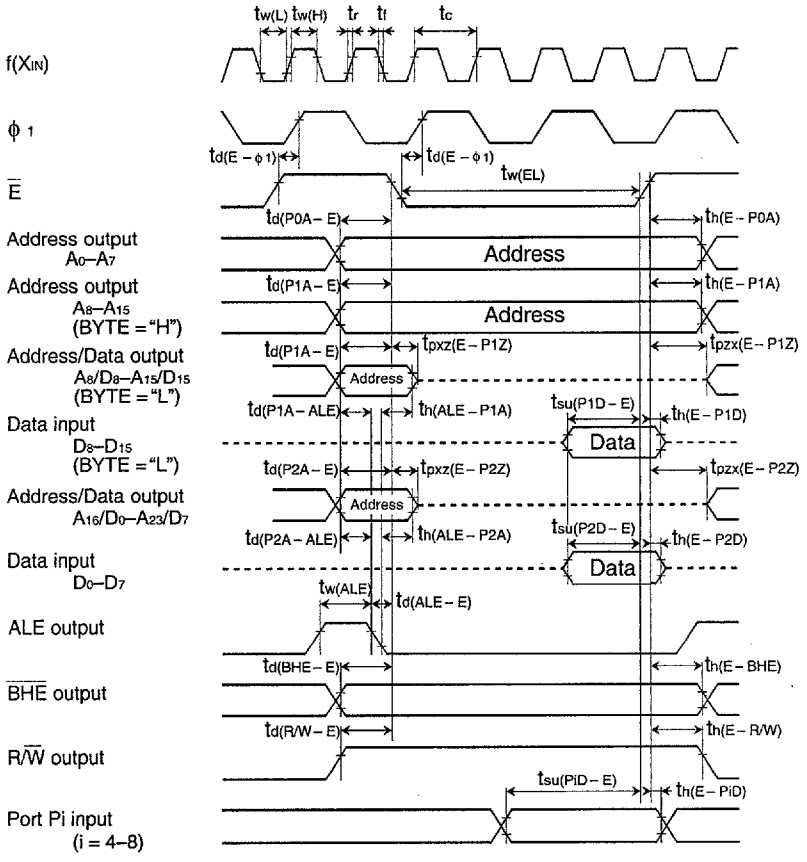

Test conditions (φ1, E, P0–P3)

- V_{CC} = 5 V ± 10%
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Test conditions (P4–P8)

- V_{CC} = 5 V ± 10%
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.10 Testing circuit for ports P0 to P8, ϕ_1, and $\overline{E}$

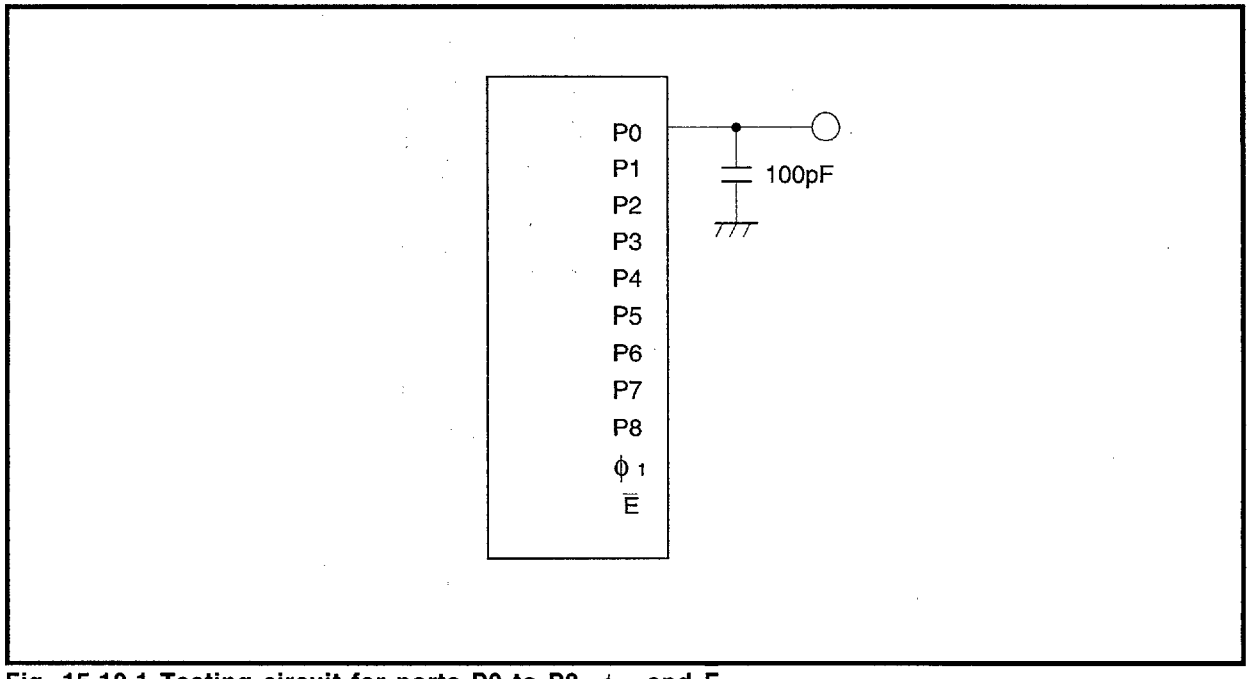

Fig. 15.10.1 Testing circuit for ports P0 to P8, ϕ_1, and E