Section 14 Electrical Characteristics

14.1 Absolute Maximum Ratings

Table 14-1 lists the absolute maximum ratings.

Table 14-1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		V_{CC}	–0.3 to +7.0	V
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V
Programming voltage		V_{PP}	–0.3 to +13.0	V
Input voltage	Ports other than ports B and C	V_{in}	–0.3 to V_{CC} +0.3	V
	Ports B and C	AV_{in}	–0.3 to AV_{CC} +0.3	V
Operating temperature		T_{opr}	–20 to +75	°C
Storage temperature		T_{stg}	–55 to +125	°C

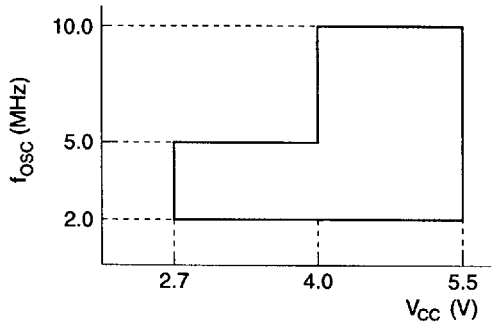
Note: Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

14.2 H8/3834 Electrical Characteristics

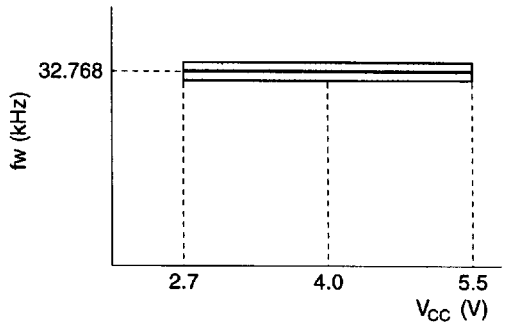
14.2.1 Power Supply Voltage and Operating Range

The power supply voltage and operating range are indicated by the shaded region in the figures below.

1. Power supply voltage vs. oscillator frequency range

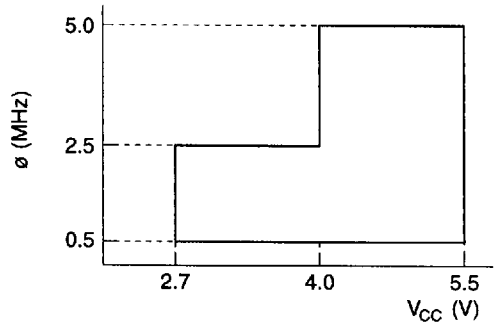


• Active mode (high speeds)
• Sleep mode

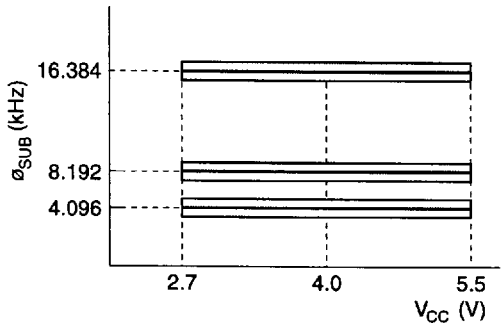


• All operating modes

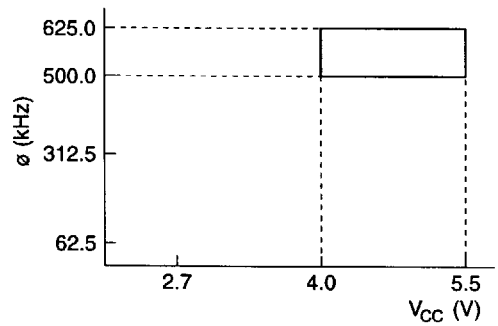
2. Power supply voltage vs. clock frequency range



- Active mode (high speed)
- Sleep mode (except CPU)

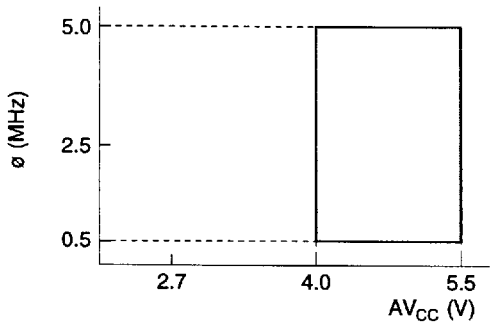


- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

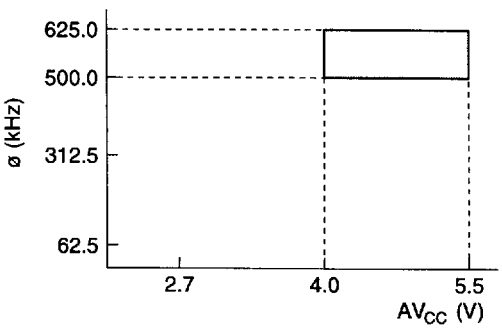


- Active mode (medium speed)

3. Analog power supply voltage vs. A/D converter operating range



- Active (high speed) mode
- Sleep mode



- Active (medium speed) mode

14.2.2 DC Characteristics

Table 14-2 lists the DC characteristics.

Table 14-2 DC Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$\overline{RES}$, MD0, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, TMIB, TMIC, TMIF	0.8 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
		$\overline{CS}$, TMIG, SCK_1, SCK_2, SCK_3, $\overline{ADTRG}$	0.9 V_{CC}	—	V_{CC} +0.3			
		UD, SI_1, SI_2, RXD	0.7 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} +0.3			
		OSC_1	V_{CC} –0.5	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			V_{CC} –0.3	—	V_{CC} +0.3			
		$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_3$ $P5_0$ to $P5_7$	0.7 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
		$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	0.8 V_{CC}	—	V_{CC} +0.3			
		PB_0 to PB_7 PC_0 to PC_3	0.7 V_{CC}	—	AV_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	AV_{CC} +0.3			
Input low voltage	V_{IL}	$\overline{RES}$, MD0, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, TMIB, TMIC, TMIF,	–0.3	—	0.2 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
		$\overline{CS}$, TMIG, SCK_1, SCK_2, SCK_3, $\overline{ADTRG}$	–0.3	—	0.1 V_{CC}			
		UD, SI_1, SI_2, RXD	–0.3	—	0.3 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.2 V_{CC}			
		OSC_1	–0.3	—	0.5	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.3			

Note: Connect pin TEST to V_{SS}.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input low voltage	V_{IL}	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_3$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$	–0.3	—	0.3 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
		$P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3 PB_0 to PB_7 PC_0 to PC_3	–0.3	—	0.2 V_{CC}			
Output high voltage	V_{OH}	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$	V_{CC} – 1.0	—	—	V	V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 1.0 mA	
		$P4_0$ to $P4_2$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$	V_{CC} – 0.5	—	—		V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 0.5 mA	
		$P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	V_{CC} – 0.5	—	—		$-I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$P1_0$ to $P1_7$ $P4_0$ to $P4_2$	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	—	—	0.5		I_{OL} = 0.4 mA	
		$P2_0$ to $P2_7$ $P3_0$ to $P3_7$	—	—	1.5		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	

Note: Connect pin TEST to V_{SS}.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input leakage current	$\|I_{IL}\|$	$\overline{RES}$, $P4_3$	—	—	20	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	2
			—	—	1			1
		OSC_1, MD0 $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_2$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	—	—	1	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7 PC_0 to PC_3	—	—	1		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_P$	$P1_0$ to $P1_7$ $P3_0$ to $P3_7$	50	—	300	µA	V_{CC} = 5 V, V_{IN} = 0 V	
		$P5_0$ to $P5_7$ $P6_0$ to $P6_7$	—	35	—	µA	V_{CC} = 2.7 V, V_{IN} = 0 V	Reference value
Input capacitance	C_{IN}	All input pins except power supply $\overline{RES}$, $P4_3$ pin	—	—	15	pF	f = 1 MHz, V_{IN} = 0 V, T_a = 25°C	
		$\overline{RES}$	—	—	60			2
			—	—	15			1
		$P4_3$	—	—	30			2
			—	—	15			1

Notes: 1. Applies to HD6433834.
2. Applies to HD6473834.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Active mode current dissipation	I_{OPE1}	V_{CC}	—	12	24	mA	Active mode (high speed), V_{CC} = 5 V, f_{osc} = 10 MHz	1, 2
	I_{OPE2}	V_{CC}	—	2.5	5	mA	Active mode (medium speed), V_{CC} = 5 V, f_{osc} = 10 MHz	1, 2
Sleep mode current dissipation	I_{SLEEP}	V_{CC}	—	5	10	mA	V_{CC} = 5 V, f_{osc} = 10 MHz	1, 2
Subactive mode current dissipation	I_{SUB}	V_{CC}	—	50	130	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/2)	1, 2
			—	40	—	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/8)	Reference value 1, 2
Subsleep mode current dissipation	I_{SUBSP}	V_{CC}	—	40	90	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/2)	1, 2
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	—	6	µA	V_{CC} = 2.7 V, LCD not used, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/8)	1, 2
Standby mode current dissipation	I_{STBY}	V_{CC}	—	—	5	µA	32-kHz crystal oscillator not used	1, 2
RAM data retaining voltage	V_{RAM}	V_{CC}	2	—	—	V		1, 2

Notes: 1. Pin states during current measurement

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active mode (high and medium speed)	V_{CC}	Operates	V_{CC}	Open	System clock oscillator: Crystal Subclock oscillator: Pin X_1 = V_{CC}
Sleep mode	V_{CC}	Only timer operates	V_{CC}	Open	
Subactive mode	V_{CC}	Operates	V_{CC}	Open	System clock oscillator: Crystal Subclock oscillator: Crystal
Subsleep mode	V_{CC}	Only timer operates, CPU stops	V_{CC}	Open	
Watch mode	V_{CC}	Only time-base clock operates, CPU stops	V_{CC}	Open	
Standby mode	V_{CC}	CPU and timers all stop	V_{CC}	Open	System clock oscillator: Crystal Subclock oscillator: Pin X_1 = V_{CC}

2. Excludes current in pull-up MOS transistors and output buffers.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, $V_{SS} = AV_{SS}$ = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition
Allowable output low current (per pin)	I_{OL}	Output pins except in ports 2 and 3	—	—	2	mA	V_{CC} = 4.0 V to 5.5 V
		Ports 2 and 3	—	—	10		V_{CC} = 4.0 V to 5.5 V
		All output pins	—	—	0.5		
Allowable output low current (total)	ΣI_{OL}	Output pins except in ports 2 and 3	—	—	40	mA	V_{CC} = 4.0 V to 5.5 V
		Ports 2 and 3	—	—	80		V_{CC} = 4.0 V to 5.5 V
		All output pins	—	—	20		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	—	—	2	mA	V_{CC} = 4.0 V to 5.5 V
			—	—	0.2		
Allowable output high current (total)	$\Sigma-I_{OH}$	All output pins	—	—	15	mA	V_{CC} = 4.0 V to 5.5 V
			—	—	10		

14.2.3 AC Characteristics

Table 14-3 lists the control signal timing, and tables 14-4 and 14-5 list the serial interface timing.

Table 14-3 Control Signal Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2	—	10	MHz	V_{CC} = 4.0 V to 5.5 V	
			2	—	5			
OSC clock ($ø_{OSC}$) cycle time	t_{OSC}	OSC_1, OSC_2	100	—	1000	ns	V_{CC} = 4.0 V to 5.5 V	1
			200	—	1000			Figure 14-1
System clock (ø) cycle time	t_{cyc}		2	—	16	t_{OSC}		1
			—	—	2000	ns		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.678	—	kHz		
Watch clock cycle time	t_W	X_1, X_2	—	30.5	—	µs		
Subclock ($ø_{SUB}$) cycle time	t_{subcyc}		2	—	8	t_W		2
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time (crystal oscillator)	t_{rc}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 4.0 V to 5.5 V	
			—	—	60			
Oscillation stabilization time	t_{rc}	X_1, X_2	—	—	2	s		
External clock high width	t_{CPH}	OSC_1	40	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			80	—	—			
External clock low width	t_{CPL}	OSC_1	40	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			80	—	—			
External clock rise time	t_{CPr}		—	—	15	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			—	—	20			
External clock fall time	t_{CPf}		—	—	15	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			—	—	20			
Pin $\overline{RES}$ low width	t_{REL}	$\overline{RES}$	10	—	—	tcyc		Figure 14-2

Notes: 1. A frequency between 1 MHz to 10 MHz is required when an external clock is input.
2. Selected with SA1 and SA0 of system clock control register 2 (SYSCR2).

Table 14-3 Control Signal Timing (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input pin high width	t_{IH}	$\overline{IRQ_0}$ to $\overline{IRQ_4}$ $\overline{WKP_0}$ to $\overline{WKP_7}$ $\overline{ADTRG}$ TMIB, TMIC TMIF, TMIG	2	—	—	t_{cyc} t_{subcyc}		Figure 14-3
Input pin low width	t_{IL}	$\overline{IRQ_0}$ to $\overline{IRQ_4}$ $\overline{WKP_0}$ to $\overline{WKP_7}$ $\overline{ADTRG}$ TMIB, TMIC TMIF, TMIG	2	—	—	t_{cyc} t_{subcyc}		Figure 14-3
Pin UD minimum modulation width	t_{UDH} t_{UDL}	UD	4	—	—	t_{cyc} t_{subcyc}		Figure 14-4

Table 14-4 Serial Interface (SCI1, SCI2) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input serial clock cycle time	t_{scyc}	SCK_1, SCK_2	2	—	—	t_{cyc}		Figure 14-5
Input serial clock high width	t_{SCKH}	SCK_1, SCK_2	0.4	—	—	t_{scyc}		Figure 14-5
Input serial clock low width	t_{SCKL}	SCK_1, SCK_2	0.4	—	—	t_{scyc}		Figure 14-5
Input serial clock rise time	t_{SCKr}	SCK_1, SCK_2	—	—	60	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			—	—	80			
Input serial clock fall time	t_{SCKf}	SCK_1, SCK_2	—	—	60	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			—	—	80			
Serial output data delay time	t_{SOD}	SO_1, SO_2	—	—	200	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			—	—	350			
Serial input data setup time	t_{SIS}	SI_1, SI_2	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			400	—	—			
Serial input data hold time	t_{SIH}	SI_1, SI_2	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			400	—	—			
$\overline{CS}$ setup time	t_{CSS}	$\overline{CS}$	2	—	—	t_{cyc}		Figure 14-6
$\overline{CS}$ hold time	t_{CSH}	$\overline{CS}$	2	—	—	t_{cyc}		Figure 14-6

Table 14-5 Serial Interface (SCI3) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc}		Figure 14-7
	Synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 14-7
Transmit data delay time (synchronous mode)		t_{TXD}	—	—	1	t_{cyc}	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			—	—	1			
Receive data setup time (synchronous mode)		t_{RXS}	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			400	—	—			
Receive data hold time (synchronous mode)		t_{RXH}	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			400	—	—			

14.2.4 A/D Converter Characteristics

Table 14-6 shows the A/D converter characteristics.

Table 14-6 A/D Converter Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog power supply voltage	AV_{CC}	AV_{CC}	4.0	—	5.5	V		1
Analog input voltage	AV_{IN}	AN_0 to AN_{11}	–0.3	—	AV_{CC} + 0.3	V		
Analog power supply current	AI_{OPE}	AV_{CC}	—	—	1.5	mA	AV_{CC} = 5.0 V	
	AI_{STOP1}	AV_{CC}	—	150	—	µA		2 Reference value
	AI_{STOP2}	AV_{CC}	—	—	5	µA		3
Analog input capacitance	C_{AIN}	AN_0 to AN_{11}	—	—	30	pF		
Allowable signal source impedance	R_{AIN}		—	—	10	kΩ		
Resolution (data length)			—	—	8	bit		
Non-linearity error			—	—	±2.0	LSB		
Quantization error			—	—	±0.5	LSB		
Absolute accuracy			—	—	±2.5	LSB		
Conversion time			12.4	—	124	µs	AV_{CC} = 4.5 V to 5.5 V	
			24.8	—	124			

Notes: 1. Set AV_{CC} = V_{CC} when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby, watch, subactive, and subsleep modes while the A/D converter is idle.

14.2.5 LCD Characteristics

Table 14-7 lists the LCD characteristics, and table 14-8 lists the AC characteristics for external segment expansion.

Table 14-7 LCD Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Segment driver voltage drop	V_{DS}	SEG_1 to SEG_{40}	—	—	0.6	V	I_D = 2 µA	1
Common driver voltage drop	V_{DC}	COM_1 to COM_4	—	—	0.3	V	I_D = 2 µA	1
LCD power supply voltage divider resistance	R_{LCD}		50	300	900	kΩ	Between V_1 and V_{SS}	
LCD power supply voltage	V_{LCD}	V_1	2.7	—	V_{CC}	V		2

Notes: 1. These are the voltage drops between the voltage supply pins V1, V2, V3, and Vss, and the segment pins or common pins.
2. When V_{LCD} is supplied from an external source, the following relation must hold: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$

Table 14-8 AC Characteristics for External Segment Expansion

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Clock high width	t_{CWH}	CL_1, CL_2	800	—	—	ns	*	Figure 14-9
Clock low width	t_{CWL}	CL_2	800	—	—	ns	*	Figure 14-9
Clock setup time	t_{CSU}	CL_1, CL_2	500	—	—	ns	*	Figure 14-9
Data setup time	t_{SU}	DO	300	—	—	ns	*	Figure 14-9
Data hold time	t_{DH}	DO	300	—	—	ns	*	Figure 14-9
M delay time	t_{DM}	M	–1000	—	1000	ns		Figure 14-9
Clock rise and fall times	t_{CT}	CL_1, CL_2	—	—	100	ns		Figure 14-9

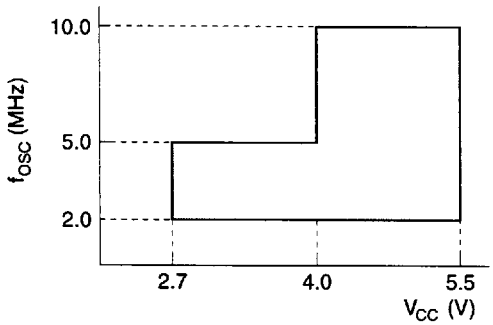
Note: * Value when the frame frequency is set to between 30.5 Hz and 488 Hz.

14.3 H8/3836, H8/3837 Electrical Characteristics

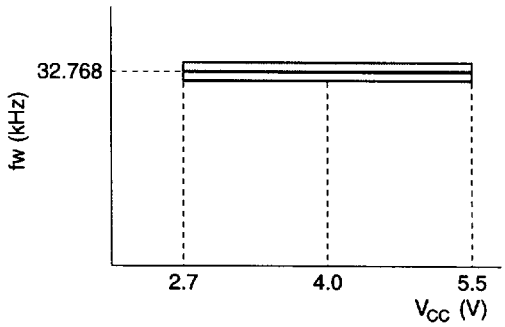
14.3.1 Power Supply Voltage and Operating Range

The power supply voltage and operating range are indicated by the shaded region in the figures below.

1. Power supply voltage vs. oscillator frequency range

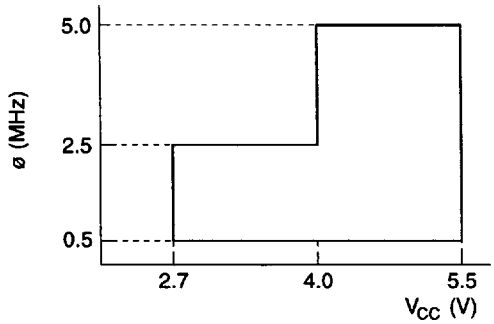


• Active mode (high speeds)
• Sleep mode

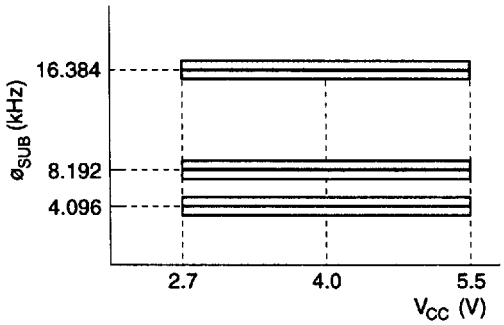


• All operating modes

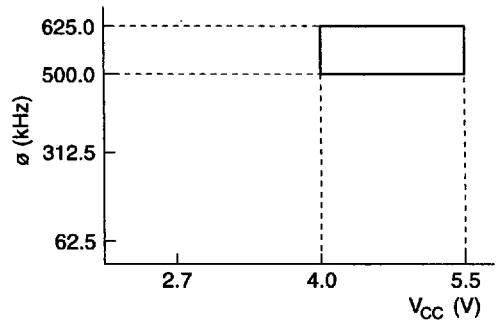
2. Power supply voltage vs. clock frequency range



- Active mode (high speed)
- Sleep mode (except CPU)

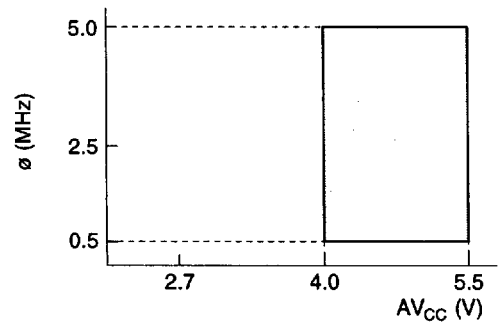


- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

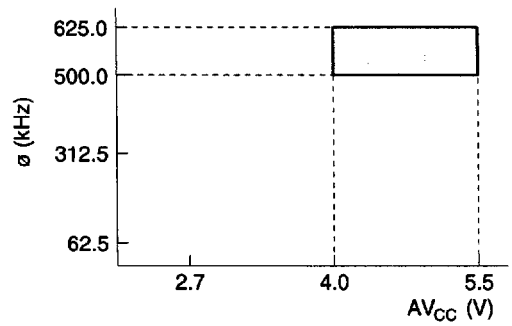


- Active mode (medium speed)

3. Analog power supply voltage vs. A/D converter operating range



- Active (high speed) mode
- Sleep mode



- Active (medium speed) mode

14.3.2 DC Characteristics

Table 14-9 lists the DC characteristics.

Table 14-9 DC Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$\overline{RES}$, MD0, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, TMIB, TMIC, TMIF	0.8 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
		$\overline{CS}$, TMIG, SCK_1, SCK_2, SCK_3, $\overline{ADTRG}$	0.9 V_{CC}	—	V_{CC} +0.3			
		UD, SI_1, SI_2, RXD	0.7 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} +0.3			
		OSC_1	V_{CC} –0.5	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			V_{CC} –0.3	—	V_{CC} +0.3			
		$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_3$ $P5_0$ to $P5_7$	0.7 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
		$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	0.8 V_{CC}	—	V_{CC} +0.3			
		PB_0 to PB_7 PC_0 to PC_3	0.7 V_{CC}	—	AV_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	AV_{CC} +0.3			
Input low voltage	V_{IL}	$\overline{RES}$, MD0, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, TMIB, TMIC, TMIF,	–0.3	—	0.2 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
		$\overline{CS}$, TMIG, SCK_1, SCK_2, SCK_3, $\overline{ADTRG}$	–0.3	—	0.1 V_{CC}			
		UD, SI_1, SI_2, RXD	–0.3	—	0.3 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.2 V_{CC}			
		OSC_1	–0.3	—	0.5	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.3			

Note: Connect pin TEST to V_{SS}.

Table 14-9 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input low voltage	V_{IL}	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_3$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$	–0.3	—	0.3 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
		$P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3 PB_0 to PB_7 PC_0 to PC_3	–0.3	—	0.2 V_{CC}			
Output high voltage	V_{OH}	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$	V_{CC} – 1.0	—	—	V	V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 1.0 mA	
		$P4_0$ to $P4_2$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$	V_{CC} – 0.5	—	—		V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 0.5 mA	
		$P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	V_{CC} – 0.5	—	—		$-I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$P1_0$ to $P1_7$ $P4_0$ to $P4_2$	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	—	—	0.5		I_{OL} = 0.4 mA	
		$P2_0$ to $P2_7$ $P3_0$ to $P3_7$	—	—	1.5		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	

Note: Connect pin TEST to V_{SS}.

Table 14-9 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input leakage current	$\|I_{IL}\|$	$\overline{RES}$, $P4_3$	—	—	20	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	2
			—	—	1			1
		OSC_1, MD0 $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_2$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3	—	—	1	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7 PC_0 to PC_3	—	—	1		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_P$	$P1_0$ to $P1_7$ $P3_0$ to $P3_7$	50	—	300	µA	V_{CC} = 5 V, V_{IN} = 0 V	
		$P5_0$ to $P5_7$ $P6_0$ to $P6_7$	—	35	—	µA	V_{CC} = 2.7 V, V_{IN} = 0 V	Reference value
Input capacitance	C_{IN}	All input pins except power supply $\overline{RES}$ $P4_3$ pin	—	—	15	pF	f = 1 MHz, V_{IN} = 0 V, T_a = 25°C	
		$\overline{RES}$	—	—	60			2
			—	—	15			1
		$P4_3$	—	—	30			2
			—	—	15			1

Notes: 1. Applies to HD6433836, and HD6433837.
2. Applies to HD6473837.

Table 14-9 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Active mode current dissipation	I_{OPE1}	V_{CC}	—	14.4	28.8	mA	Active mode (high speed), V_{CC} = 5 V, f_{osc} = 10 MHz	1, 2
	I_{OPE2}	V_{CC}	—	3.0	6.0	mA	Active mode (medium speed), V_{CC} = 5 V, f_{osc} = 10 MHz	1, 2
Sleep mode current dissipation	I_{SLEEP}	V_{CC}	—	6.0	12.0	mA	V_{CC} = 5 V, f_{osc} = 10 MHz	1, 2
Subactive mode current dissipation	I_{SUB}	V_{CC}	—	60.0	156.0	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/2)	1, 2
			—	48.0	—	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/8)	Reference value 1, 2
Subsleep mode current dissipation	I_{SUBSP}	V_{CC}	—	48.0	108.0	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/2)	1, 2
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	—	6	µA	V_{CC} = 2.7 V, LCD not used, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/8)	1, 2
Standby mode current dissipation	I_{STBY}	V_{CC}	—	—	5	µA	32-kHz crystal oscillator not used	1, 2
RAM data retaining voltage	V_{RAM}	V_{CC}	2	—	—	V		1, 2

Notes: 1. Pin states during current measurement

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active mode (high and medium speed)	V_{CC}	Operates	V_{CC}	Open	System clock oscillator: Crystal Subclock oscillator: Pin X_1 = V_{CC}
Sleep mode	V_{CC}	Only timer operates	V_{CC}	Open	
Subactive mode	V_{CC}	Operates	V_{CC}	Open	System clock oscillator: Crystal Subclock oscillator: Crystal
Subsleep mode	V_{CC}	Only timer operates, CPU stops	V_{CC}	Open	
Watch mode	V_{CC}	Only time-base clock operates, CPU stops	V_{CC}	Open	
Standby mode	V_{CC}	CPU and timers all stop	V_{CC}	Open	System clock oscillator: Crystal Subclock oscillator: Pin X_1 = V_{CC}

2. Excludes current in pull-up MOS transistors and output buffers.

Table 14-9 DC Characteristics (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, $V_{SS} = AV_{SS}$ = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition
Allowable output low current (per pin)	I_{OL}	Output pins except in ports 2 and 3	—	—	2	mA	V_{CC} = 4.0 V to 5.5 V
		Ports 2 and 3	—	—	10		V_{CC} = 4.0 V to 5.5 V
		All output pins	—	—	0.5		
Allowable output low current (total)	ΣI_{OL}	Output pins except in ports 2 and 3	—	—	40	mA	V_{CC} = 4.0 V to 5.5 V
		Ports 2 and 3	—	—	80		V_{CC} = 4.0 V to 5.5 V
		All output pins	—	—	20		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	—	—	2	mA	V_{CC} = 4.0 V to 5.5 V
			—	—	0.2		
Allowable output high current (total)	$\Sigma-I_{OH}$	All output pins	—	—	15	mA	V_{CC} = 4.0 V to 5.5 V
			—	—	10		

14.3.3 AC Characteristics

Table 14-10 lists the control signal timing, and tables 14-11 and 14-12 list the serial interface timing.

Table 14-10 Control Signal Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2	—	10	MHz	V_{CC} = 4.0 V to 5.5 V	
			2	—	5			
OSC clock ($ø_{OSC}$) cycle time	t_{OSC}	OSC_1, OSC_2	100	—	1000	ns	V_{CC} = 4.0 V to 5.5 V	1
			200	—	1000			Figure 14-1
System clock (ø) cycle time	t_{cyc}		2	—	16	t_{OSC}		1
			—	—	2000	ns		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.678	—	kHz		
Watch clock cycle time	t_W	X_1, X_2	—	30.5	—	µs		
Subclock ($ø_{SUB}$) cycle time	t_{subcyc}		2	—	8	t_W		2
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time (crystal oscillator)	t_{rc}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 4.0 V to 5.5 V	
			—	—	60			
Oscillation stabilization time	t_{rc}	X_1, X_2	—	—	2	s		
External clock high width	t_{CPH}	OSC_1	40	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			80	—	—			
External clock low width	t_{CPL}	OSC_1	40	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			80	—	—			
External clock rise time	t_{CPr}		—	—	15	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			—	—	20			
External clock fall time	t_{CPf}		—	—	15	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-1
			—	—	20			
Pin $\overline{RES}$ low width	t_{REL}	$\overline{RES}$	10	—	—	tcyc		Figure 14-2

Notes: 1. A frequency between 1 MHz to 10 MHz is required when an external clock is input.
2. Selected with SA1 and SA0 of system clock control register 2 (SYSCR2).

Table 14-10 Control Signal Timing (cont)

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input pin high width	t_{IH}	$\overline{IRQ_0}$ to $\overline{IRQ_4}$ $\overline{WKP_0}$ to $\overline{WKP_7}$ $\overline{ADTRG}$ TMIB, TMIC TMIF, TMIG	2	—	—	t_{cyc} t_{subcyc}		Figure 14-3
Input pin low width	t_{IL}	$\overline{IRQ_0}$ to $\overline{IRQ_4}$ $\overline{WKP_0}$ to $\overline{WKP_7}$ $\overline{ADTRG}$ TMIB, TMIC TMIF, TMIG	2	—	—	t_{cyc} t_{subcyc}		Figure 14-3
Pin UD minimum modulation width	t_{UDH} t_{UDL}	UD	4	—	—	t_{cyc} t_{subcyc}		Figure 14-4

Table 14-11 Serial Interface (SCI1, SCI2) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input serial clock cycle time	t_{scyc}	SCK_1, SCK_2	2	—	—	t_{cyc}		Figure 14-5
Input serial clock high width	t_{SCKH}	SCK_1, SCK_2	0.4	—	—	t_{scyc}		Figure 14-5
Input serial clock low width	t_{SCKL}	SCK_1, SCK_2	0.4	—	—	t_{scyc}		Figure 14-5
Input serial clock rise time	t_{SCKr}	SCK_1, SCK_2	—	—	60	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			—	—	80			
Input serial clock fall time	t_{SCKf}	SCK_1, SCK_2	—	—	60	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			—	—	80			
Serial output data delay time	t_{SOD}	SO_1, SO_2	—	—	200	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			—	—	350			
Serial input data setup time	t_{SIS}	SI_1, SI_2	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			400	—	—			
Serial input data hold time	t_{SIH}	SI_1, SI_2	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-5
			400	—	—			
$\overline{CS}$ setup time	t_{CSS}	$\overline{CS}$	2	—	—	t_{cyc}		Figure 14-6
$\overline{CS}$ hold time	t_{CSH}	$\overline{CS}$	2	—	—	t_{cyc}		Figure 14-6

Table 14-12 Serial Interface (SCI3) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc}		Figure 14-7
	Synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 14-7
Transmit data delay time (synchronous mode)		t_{TXD}	—	—	1	t_{cyc}	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			—	—	1			
Receive data setup time (synchronous mode)		t_{RXS}	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			400	—	—			
Receive data hold time (synchronous mode)		t_{RXH}	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			400	—	—			

14.3.4 A/D Converter Characteristics

Table 14-13 shows the A/D converter characteristics.

Table 14-13 A/D Converter Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, $AV_{SS} = V_{SS}$ = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog power supply voltage	AV_{CC}	AV_{CC}	4.0	—	5.5	V		1
Analog input voltage	AV_{IN}	AN_0 to AN_{11}	AV_{SS} – 0.3	—	AV_{CC} + 0.3	V		
Analog power supply current	AI_{OPE}	AV_{CC}	—	—	1.5	mA	AV_{CC} = 5.0 V	
	AI_{STOP1}	AV_{CC}	—	150	—	µA		2 Reference value
	AI_{STOP2}	AV_{CC}	—	—	5	µA		3
Analog input capacitance	C_{AIN}	AN_0 to AN_{11}	—	—	30	pF		
Allowable signal source impedance	R_{AIN}		—	—	10	kΩ		
Resolution (data length)			—	—	8	bit		
Non-linearity error			—	—	±2.0	LSB		
Quantization error			—	—	±0.5	LSB		
Absolute accuracy			—	—	±2.5	LSB		
Conversion time			12.4	—	124	µs	AV_{CC} = 4.5 V to 5.5 V	
			24.8	—	124			

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby, watch, subactive, and subsleep modes while the A/D converter is idle.

14.3.5 LCD Characteristics

Table 14-14 lists the LCD characteristics, and table 14-15 lists the AC characteristics for external segment expansion.

Table 14-14 LCD Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Segment driver voltage drop	V_{DS}	SEG_1 to SEG_{40}	—	—	0.6	V	I_D = 2 µA	1
Common driver voltage drop	V_{DC}	COM_1 to COM_4	—	—	0.3	V	I_D = 2 µA	1
LCD power supply voltage divider resistance	R_{LCD}		50	300	900	kΩ	Between V_1 and V_{SS}	
LCD power supply voltage	V_{LCD}	V_1	2.7	—	V_{CC}	V		2

Notes: 1. These are the voltage drops between the voltage supply pins V1, V2, V3, and Vss, and the segment pins or common pins.
2. When V_{LCD} is supplied from an external source, the following relation must hold: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$

Table 14-15 AC Characteristics for External Segment Expansion

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Clock high width	t_{CWH}	CL_1, CL_2	800	—	—	ns	*	Figure 14-9
Clock low width	t_{CWL}	CL_2	800	—	—	ns	*	Figure 14-9
Clock setup time	t_{CSU}	CL_1, CL_2	500	—	—	ns	*	Figure 14-9
Data setup time	t_{SU}	DO	300	—	—	ns	*	Figure 14-9
Data hold time	t_{DH}	DO	300	—	—	ns	*	Figure 14-9
M delay time	t_{DM}	M	–1000	—	1000	ns		Figure 14-9
Clock rise and fall times	t_{CT}	CL_1, CL_2	—	—	100	ns		Figure 14-9

Note: * Value when the frame frequency is set to between 30.5 Hz and 488 Hz.

14.4 Operation Timing

Figures 14-1 to 14-10 show timing diagrams.

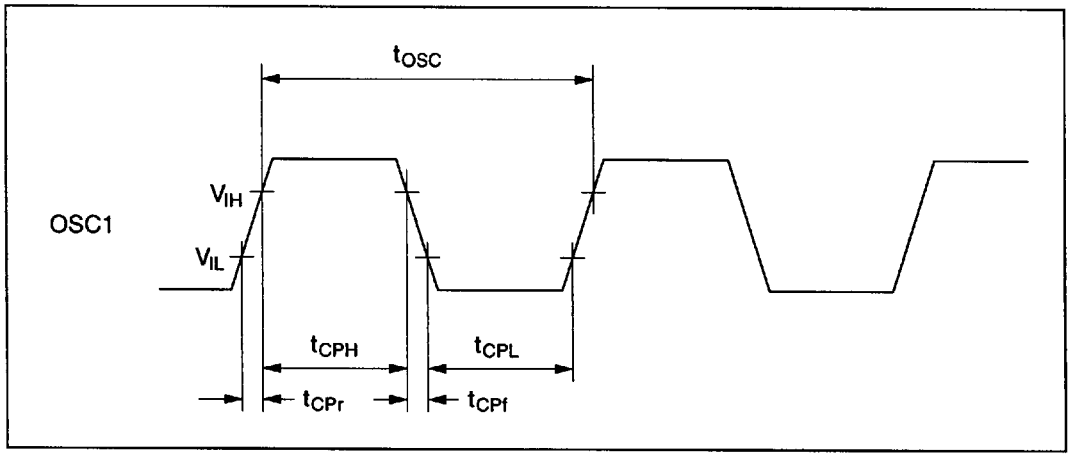


Figure 14-1 System Clock Input Timing

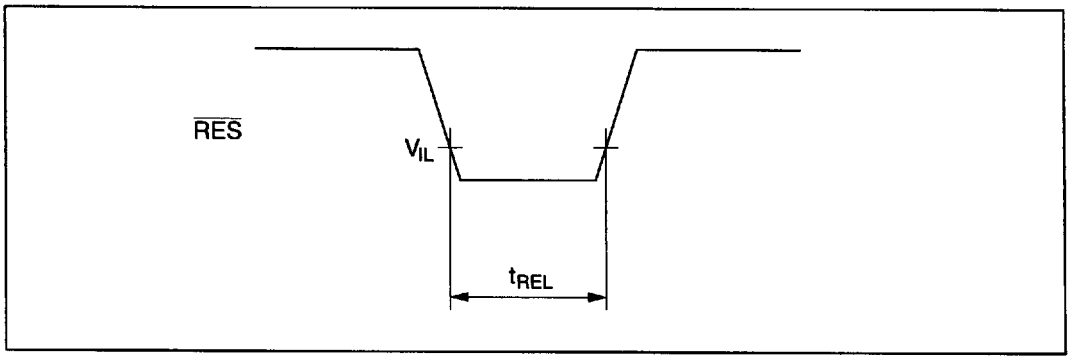


Figure 14-2 $\overline{\text{RES}}$ Low Width

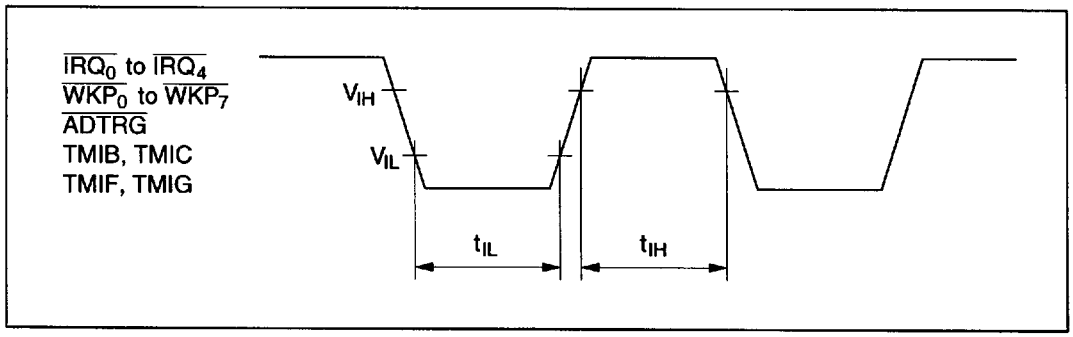


Figure 14-3 Input Timing

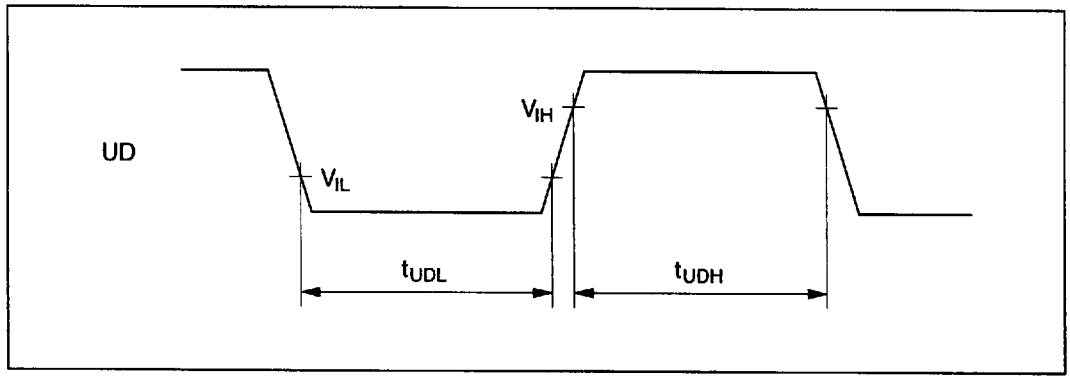
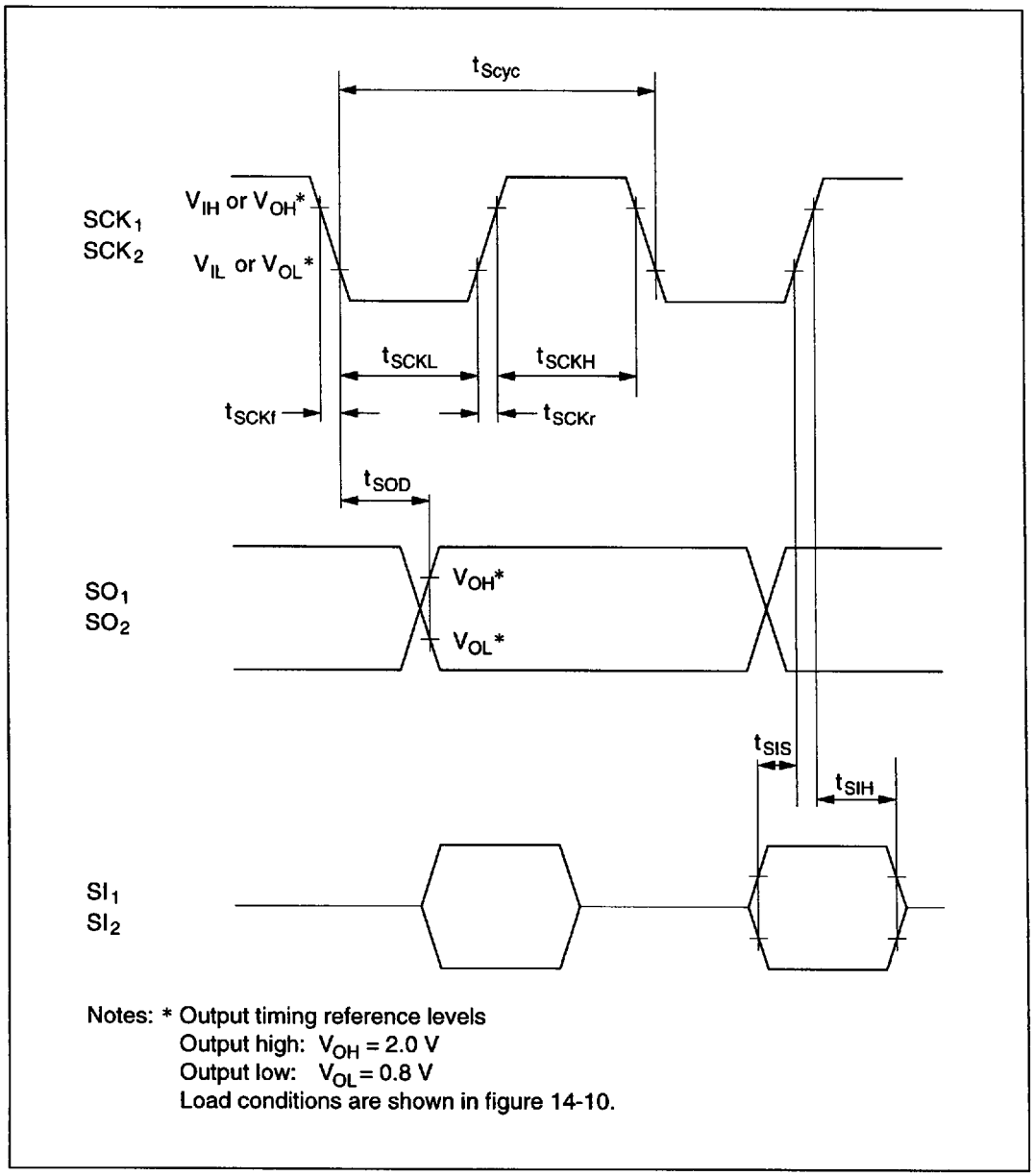


Figure 14-4 Minimum UD High and Low Width



Notes: * Output timing reference levels
Output high: V_{OH} = 2.0 V
Output low: V_{OL} = 0.8 V
Load conditions are shown in figure 14-10.

Figure 14-5 Serial Interface 1 and 2 Input/Output Timing

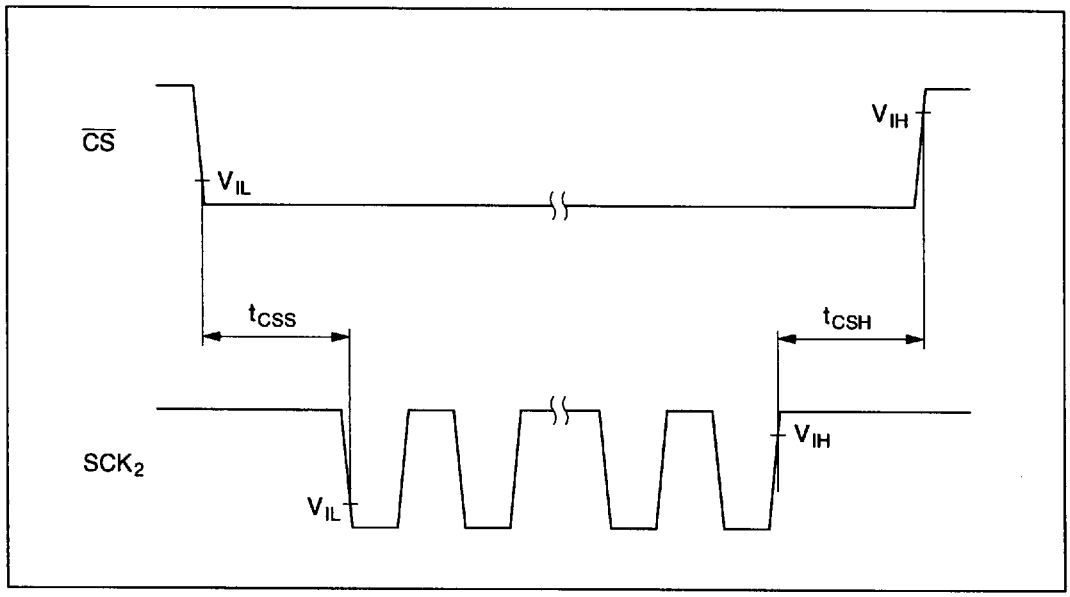


Figure 14-6 Serial Interface 2 Chip Select Timing

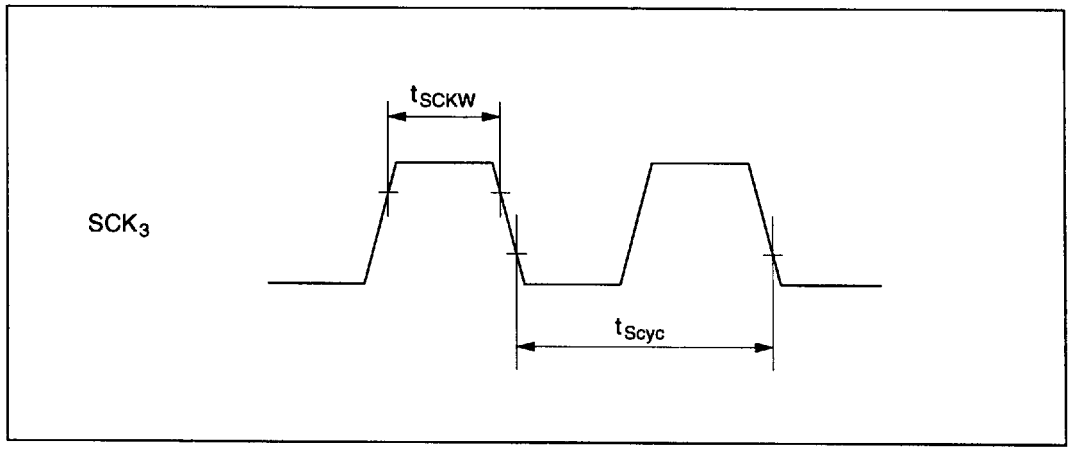


Figure 14-7 SCK_3 Input Clock Timing

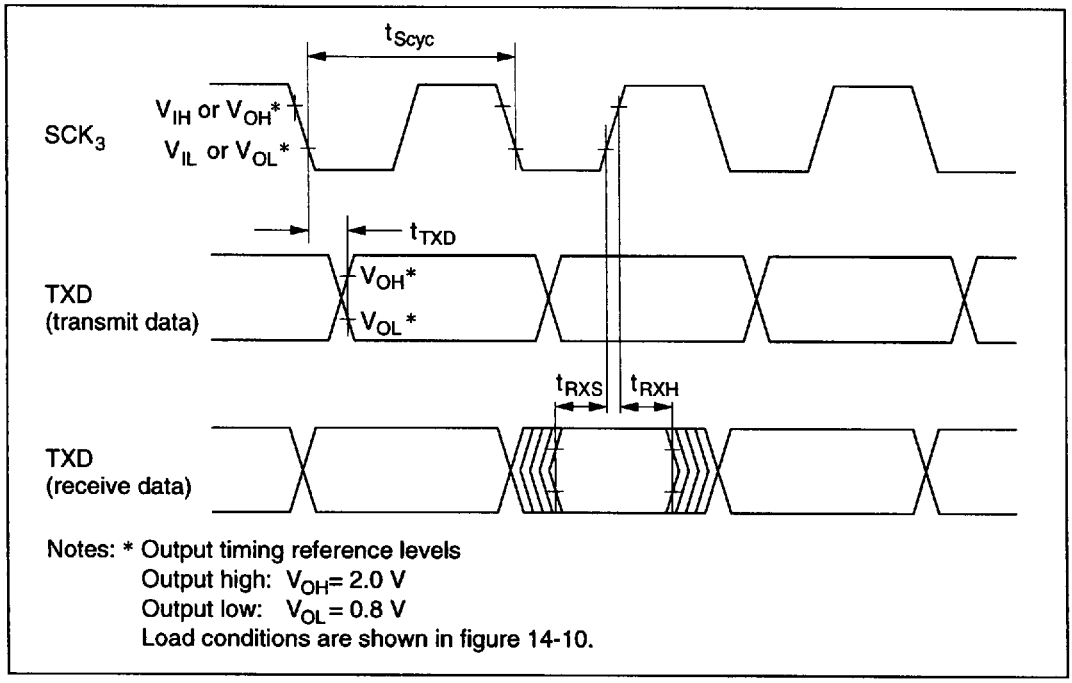


Figure 14-8 Input/Output Timing of Serial Interface 3 in Synchronous Mode

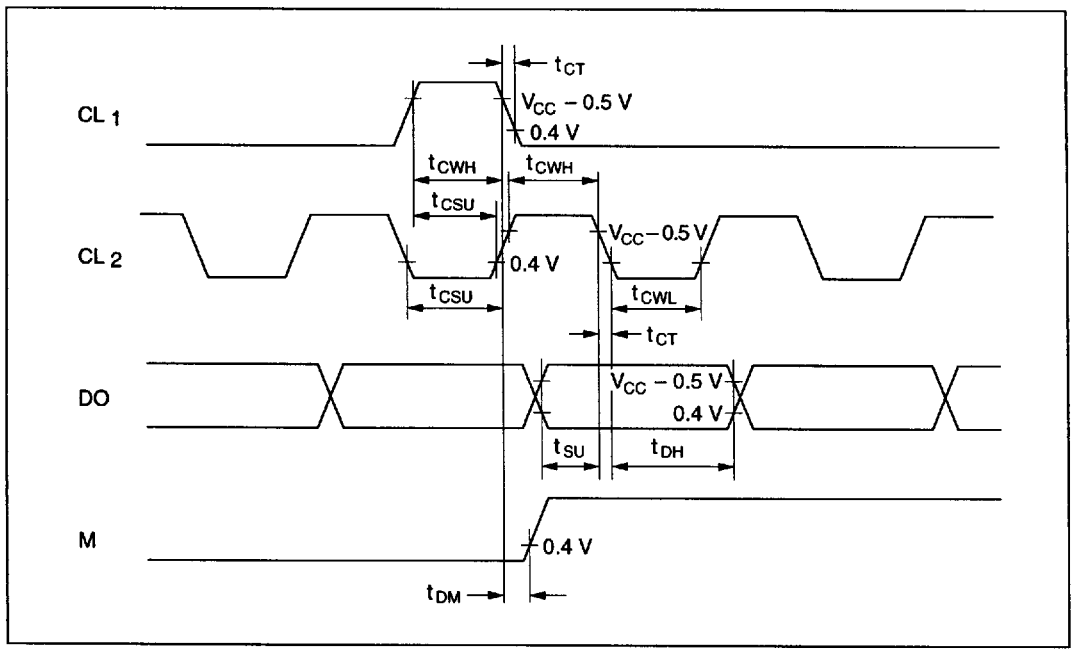


Figure 14-9 Segment Expansion Signal Timing

14.5 Output Load Circuit

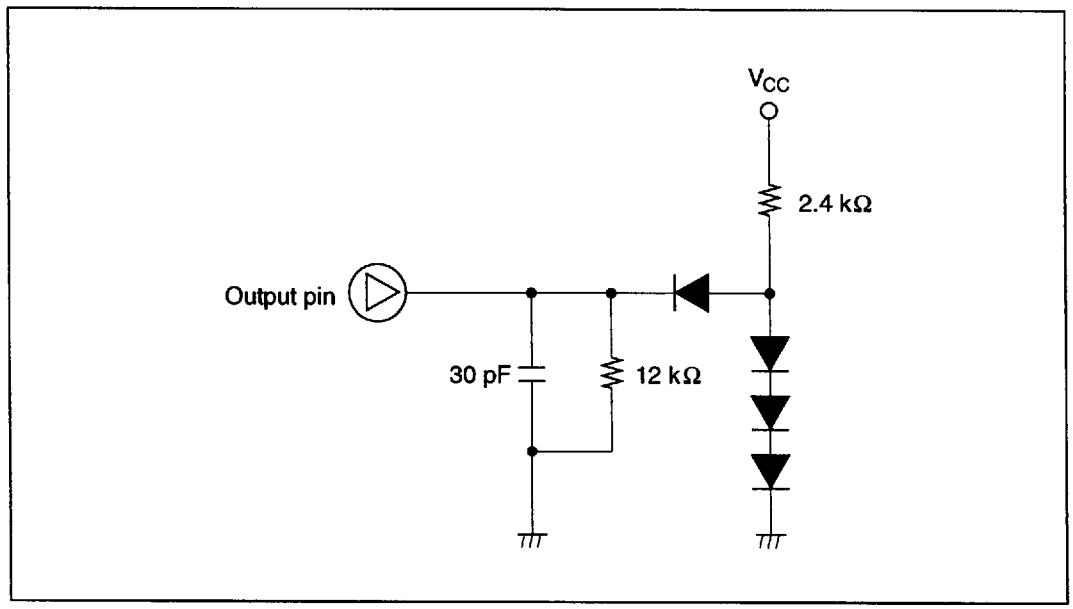


Figure 14-10 Output Load Condition