12-Bit R/D Converter with Reference Oscillator

Preliminary Technical Data

AD2S1205

FEATURES

Complete monolithic R/D converter
Parallel and serial 12-bit data ports
System fault detection
Absolute position and velocity outputs
Differential inputs
±11 arc minutes of accuracy
1,250 rps maximum tracking rate, 12-bit resolution
Incremental encoder emulation (1,024 pulses/rev)
Programmable sinusoidal oscillator on-board
Compatible with DSP and SPI® interface standards
204.8 kHz square wave output
Single-supply operation (5.00 V ± 5%)
−40°C to +125°C temperature rating
44-lead LQFP package
4 kV ESD protection

GENERAL DESCRIPTION

The AD2S1205 is a complete 12-bit resolution tracking resolver-to-digital converter, integrating an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers. An external crystal is recommended to provide a precision time reference.

The converter accepts 3.15 V p-p ± 27% input signals, in the range of 10 kHz to 20 kHz on the Sin and Cos inputs. A Type II servo loop is employed to track the inputs and convert the input Sin and Cos information into a digital representation of the input angle and velocity. The maximum tracking rate of the converter is set internally by the input clock frequency. The nominal clock frequency is 8.192MHz which allows a tracking rate of 1,000rps. However by increasing the clock frequency to 10.24MHz a maximum tracking rate of 1,250 rps can be achieved.

FUNCTIONAL BLOCK DIAGRAM

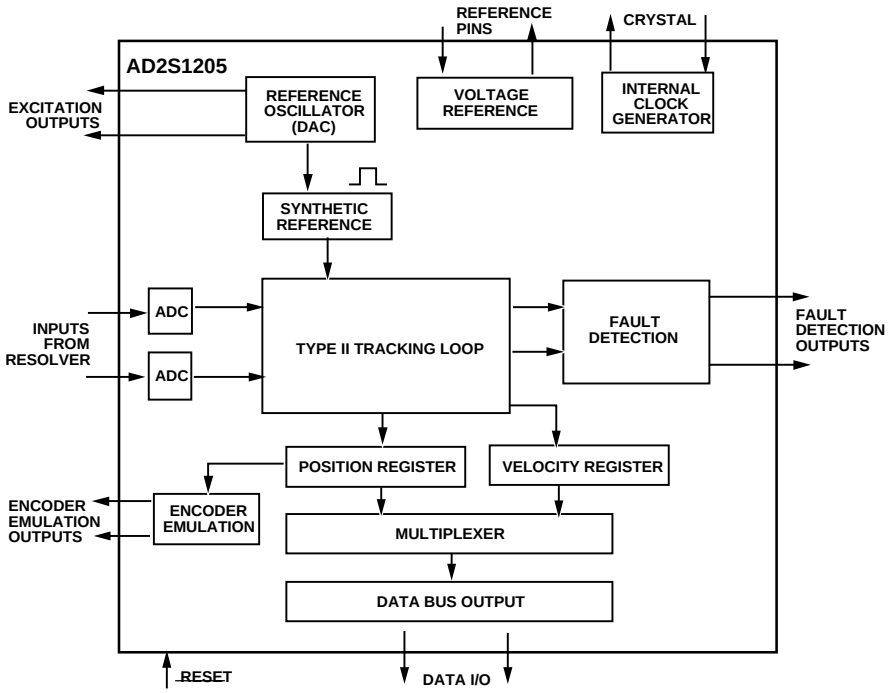

Figure 1.

Rev. PrB_10/06

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APPLICATIONS

Electric power steering
Electric vehicles
Integrated starter generator/alternator
Encoder emulation
Automotive motion sensing and control

PRODUCT HIGHLIGHTS

- **Complete Resolver-to-Digital Interface:** The AD2S1205 provides the complete solution for digitizing resolver signals (12-bit resolution) with on-board programmable sinusoidal oscillator.
- **Ratiometric Tracking Conversion:** This technique provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.
- **Triple Format Position Data:** Absolute 12-bit angular binary position data accessed either via a 12-bit parallel port or via a 3-wire serial interface. Incremental encoder emulation in standard A QUAD B format, with direction output is available.
- **Digital Velocity Output:** 12-bit signed digital velocity, twos complement format, accessed either via a 12-bit parallel port or via a 3-wire serial interface.
- **Programmable Excitation Frequency:** Excitation frequency easily programmable to 10 kHz, 12 kHz, 15 kHz, or 20 kHz by using the frequency select pins.
- **System Fault Detection:** A fault detection circuit will detect any loss of resolver signals, out of range input signals, input signal mismatch, or loss of position tracking.

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AD2S1205–SPECIFICATIONS

Table 1. (AV_{DD} = DV_{DD} = 5.0 V ± 5% @ −40°C to +125°C CLKIN 6.144MHz to 10.24MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Sin, Cos INPUTS[1]					
Voltage	2.3	3.15	4.0	V p-p	Sinusoidal waveforms, Sin-SinLO, Cos-CosLO, differential inputs
Input Bias Current			2	µA	V_{IN} = 3.96 V p-p
Input Impedance	1.0			MΩ	V_{IN} = 3.96 V p-p
Common Mode Volts			100	mV Peak	CMV with respect to REFOUT/2 @ 10 kHz
Phase Lock Range	−45		+45	Degrees	Sin/Cos vs. EXC output
ANGULAR ACCURACY					
Angular Accuracy			±11	arc min	Zero acceleration Y Grade
			±22	arc min	Zero acceleration W Grade
Resolution		12		Bits	Guaranteed no missing codes
Linearity INL			2	LSB	Zero acceleration, 0 to 1,000 rps
Linearity DNL			0.3	LSB	Guaranteed monotonic
Repeatability			1	LSB	
Hysteresis		1		LSB	
VELOCITY OUTPUT					
Velocity Accuracy			2	LSB	Zero acceleration
Resolution		11		Bits	
Linearity		1		LSB	Guaranteed by design 2 LSB max
Offset		0	1	LSB	Zero acceleration
Dynamic Ripple		1		LSB	Zero acceleration
DYNAMIC PERFORMANCE					
Bandwidth	1,160	1,600	2,000	Hz	Fixed
Tracking Rate			1,250	rps	CLKIN 10.24MHz. Guaranteed by design. Tested to 800 rps.
Acceleration Error		30		arc min	At 10,000 rps[2]
Settling Time 179° Step Input			5.2	ms	To within stated accuracy
Settling Time 179° Step Input			4.0	ms	To within one degree
EXC, $\overline{EXC}$ OUTPUTS					
Voltage	3.34	3.6	3.83	V p-p	Load ±100 µA
Center Voltage	2.39	2.47	2.52	V	
Frequency		10		kHz	FS1 = high, FS2 = high
		12		kHz	FS1 = high, FS2 = low
		15		kHz	FS1 = low, FS2 = high
		20		kHz	FS1 = low, FS2 = low
EXC/$\overline{EXC}$ DC Mismatch			35	mV	
THD		−60	−55	dB	First five harmonics
FAULT DETECTION BLOCK					
LOS					
Sin/Cos Threshold	2.18	2.24	2.3	V p-p	DOS and LOT go low when Sin or Cos fall below threshold.
Angular Accuracy (Worst Case)			57	Degrees	LOS indicated before angular output error exceeds limit (4.0 V p-p input signal and 2.2 V LOS threshold).
Angular Latency (Worst Case)			114	Degrees	Maximum electrical rotation before LOS is indicated (4.0 V p-p input signal and 2.2 V LOS threshold).
Time Latency			125	µs	

[1] The voltages Sin, SinLO, Cos, and CosLO relative to AGND must always be between 0.2 V and AV_{DD}.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
FAULT DETECTION BLOCK (CONT.)					
DOS					
Sin/Cos Threshold	4.0	4.09	4.2	V p-p	DOS goes low when Sin or Cos exceeds threshold.
Sin/Cos Mismatch		385	420	mV	DOS latched low when Sin/Cos amplitude mismatch exceeds the threshold.
Angular Accuracy (Worst Case)			33	Degrees	DOS indicated before angular output error exceeds limit.
Angular Latency (Worst Case)			66	Degrees	Maximum electrical rotation before DOS is indicated.
Time Latency			125	µs	
LOT					
Tracking Threshold		5		Degrees	LOT goes low when internal error signal exceeds threshold. Guaranteed by design.
Time Latency			1.1	ms	
Hysteresis	4			Degrees	Guaranteed by design
VOLTAGE REFERENCE					
REFOUT	2.39	2.47	2.52	V	±IOUT = 100 µA
Drift		70		ppm/°C	
PSRR		−60		dB	
CHARGE PUMP OUTPUT (CPO)					
Frequency		204.8		kHz	Square wave output
Duty Cycle		50		%	
POWER SUPPLY					
I_{DD} Dynamic			18	mA	
ELECTRICAL CHARACTERISTICS					
V_{IL} Voltage Input Low			0.8	V	
V_{IH} Voltage Input High	2.0			V	
V_{OL} Voltage Output Low			0.4	V	2 mA load
V_{OH} Voltage Output High	4.0			V	−1 mA load
I_{IL} Low Level Input Current			10	µA	
I_{IH} High Level Input Current	−10			µA	
I_{OZH} High Level Three-State Leakage	−10			µA	
I_{OZL} Low Level Three-State Leakage			10	µA	

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	−0.3 V to +7.0 V
Supply Voltage (AV_{DD})	−0.3 V to + 7.0 V
Input Voltage	−0.3 V to V_{DD} + 0.3 V
Output Voltage Swing	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

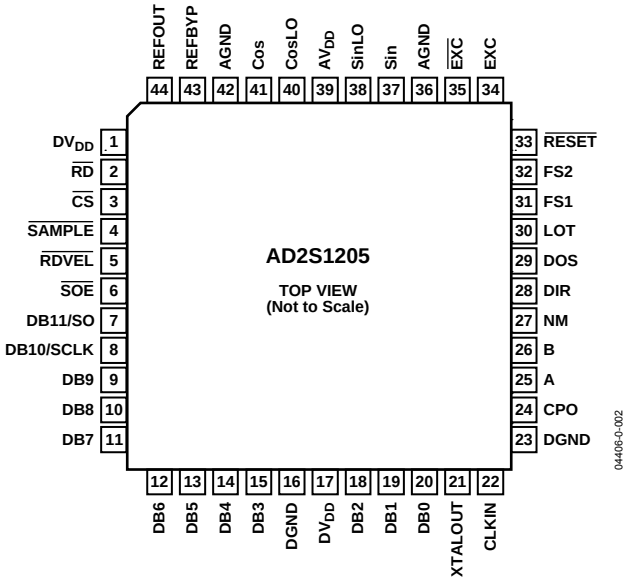

Figure 2. Pin Configuration
44-Lead Low Profile Quad Flat Package [LQFP] (ST-44)

Table 3. Pin Function Descriptions

Pin No.	Pin Name	Pin Type
1	DV_{DD}	Supply
2	$\overline{RD}$	Input
3	$\overline{CS}$	Input
4	$\overline{SAMPLE}$	Input
5	$\overline{RDVEL}$	Input
6	$\overline{SOE}$	Input
7	DB11/SO	Output
8	DB10/SCLK	Input, output
9–15	DB9–DB3	Output
16	DGND	Ground
17	DV_{DD}	Supply
18–20	DB2–DB0	Output
21	XTALOUT	Output
22	CLKIN	Input
23	DGND	Ground
24	CPO	Output
25	A	Output
26	B	Output
27	NM	Output
28	DIR	Output
29	DOS	Output
30	LOT	Output
31	FS1	Input
32	FS2	Input
33	$\overline{RESET}$	Input
34	EXC	Output
35	$\overline{EXC}$	Output
36	AGND	Ground
37	Sin	Input
38	SinLO	Input
39	AV_{DD}	Supply
40	CosLO	Input
41	Cos	Input
42	AGND	Ground
43	REFBYP	Input
44	REFOUT	Output

RESOLVER FORMAT SIGNALS

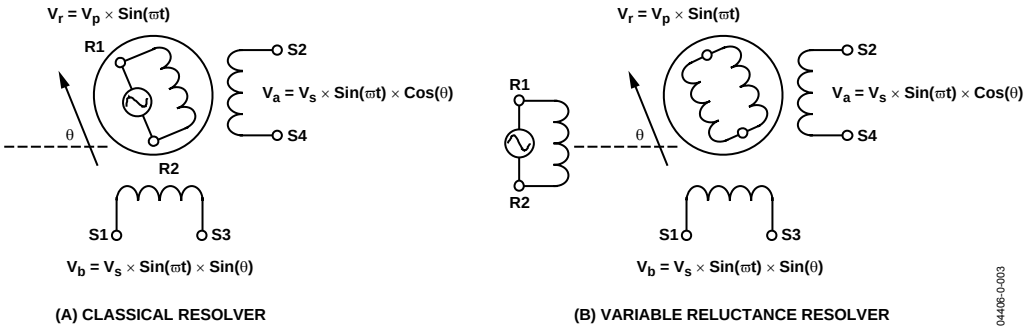

Figure 3. Classical Resolver vs. Variable Reluctance Resolver

A resolver is a rotating transformer typically with a primary winding on the rotor and two secondary windings on the stator. In the case of a variable reluctance resolver, there are no windings on the rotor as shown in Figure 3. The primary winding is on the stator as well as the secondary windings, but the saliency in the rotor design provides the sinusoidal variation in the secondary coupling with the angular position. Either way, the resolver output voltages (S3–S1, S2–S4) will have the same equations as shown in Equation 1.

$$S3 - S1 = E_0 \, Sin\omega t \times Sin\theta$$
$$S2 - S4 = E_0 \, Sin\omega t \times Cos\theta$$
$$\theta = Shaft\ Angle$$
$$Sin\omega t = Rotor\ Excitation\ Frequency$$
$$E_0 = Rotor\ Excitation\ \ Amplitude$$

Equation 1.

The stator windings are displaced mechanically by 90° (see Figure 3). The primary winding is excited with an ac reference. The amplitude of subsequent coupling onto the stator secondary windings is a function of the position of the rotor (shaft) relative to the stator. The resolver, therefore, produces two output voltages (S3–S1, S2–S4) modulated by the Sine and Cosine of shaft angle. Resolver format signals refer to the signals derived from the output of a resolver as shown in Equation 1. Figure 4 illustrates the output format.

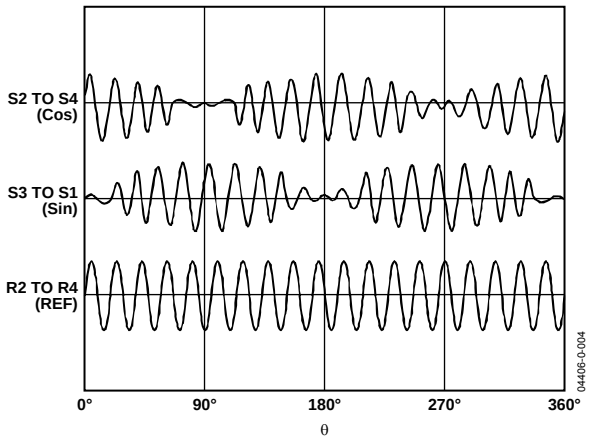

Figure 4. Electrical Resolver Representation

PRINCIPLE OF OPERATION

The AD2S1205 operates on a Type II tracking closed-loop principle. The output continually tracks the position of the resolver without the need for external convert and wait states. As the resolver moves through a position equivalent to the least significant bit weighting, the output is updated by one LSB.

The converter tracks the shaft angle θ by producing an output angle ϕ that is fed back and compared to the input angle θ, and the resulting error between the two is driven towards 0 when the converter is correctly tracking the input angle. To measure the error, S3–S1 is multiplied by Cosϕ and S2–S4 is multiplied by Sinϕ to give

$$E_0 Sin\omega t \times Sin\theta Cos\phi \qquad S1\ to\ S3$$
$$E_0 Sin\omega t \times Cos\theta Sin\phi \qquad S2\ to\ S4$$

The difference is taken, giving

$$E_0 Sin\omega t \times (Sin\theta Cos\phi - Cos\theta Sin\phi)$$

Equation 2.

This signal is demodulated using the internally generated synthetic reference, yielding

$$E_0 (Sin\theta Cos\phi - Cos\theta Sin\phi)$$

Equation 3.

Equation 3 is equivalent to E_0 Sin (θ − ϕ), which is approximately equal to E_0 (θ − ϕ) for small values of θ − ϕ, where θ − ϕ = angular error.

The value E_0 (θ − ϕ) is the difference between the angular error of the rotor and the converter's digital angle output.

A phase-sensitive demodulator, integrators, and a compensation filter form a closed-loop system that seeks to null the error signal. When this is accomplished, ϕ equals the resolver angle θ within the rated accuracy of the converter. A Type II tracking loop is used so that constant velocity inputs can be tracked without inherent error.

For more information about the operation of the converter, see the Circuit Dynamics section.

FAULT DETECTION CIRCUIT

The AD2S1205 fault detection circuit will detect loss of resolver signals, out of range input signals, input signal mismatch, or loss of position tracking. In these cases, the position indicated by the AD2S1205 may differ significantly from the actual shaft position of the resolver.

Monitor Signal

The AD2S1205 generates a monitor signal by comparing the angle in the position register to the incoming Sin and Cos signals from the resolver. The monitor signal is created in a similar fashion to the error signal described in the Principle of Operation section. The incoming signals Sinθ and Cosθ are multiplied by the Sin and Cos of the output angle, respectively, and then added together as shown below:

$$Monitor = A1 \times Sin\theta\ x\ Sin\phi + A2 \times Cos\theta \times Cos\phi$$

Equation 4.

Where A1 is the amplitude of the incoming Sin signal (A1 × Sinθ), A2 is the amplitude of the incoming Cos signal (A2 × Cosθ), θ is the resolver angle, and ϕ is the angle stored in the position register. Note that Equation 4 is shown after demodulation, with the carrier signal Sinωt removed. Also note that for matched input signal (i.e., no-fault condition), A1 = A2.

When A1 = A2 and the converter is tracking (θ = ϕ), the monitor signal output has a constant magnitude of A1 (Monitor = A1 × (Sin^2 θ + Cos^2 θ) = A1), independent of shaft angle. When A1 ≠ A2, the monitor signal magnitude varies between A1 and A2 at twice the rate of shaft rotation. The monitor signal is used as described in the following sections to detect degradation or loss of input signals.

Loss of Signal Detection

Loss of signal (LOS) is detected when either resolver input (Sin or Cos) falls below the specified LOS Sin/Cos threshold by comparing the monitor signal to a fixed minimum value. LOS is indicated by both DOS and LOT latching as logic low outputs. The DOS and LOT pins are reset to the no fault state by a rising edge of $\overline{\text{SAMPLE}}$. The LOS condition has priority over both the DOS and LOT conditions, as shown in Table 4. LOS is indicated within 45° of angular output error worst case.

Signal Degradation Detection

Degradation of signal (DOS) is detected when either resolver input (Sin or Cos) exceeds the specified DOS Sin/Cos threshold by comparing the monitor signal to a fixed maximum value. DOS is also detected when the amplitude of the input signals Sin and Cos mismatch by more than the specified DOS Sin/Cos mismatch by continuously storing the minimum and maximum magnitude of the monitor signal in internal registers, and calculating the difference between the minimum and maximum. DOS is indicated by a logic low on the DOS pin, and is not latched when the input signals exceed the maximum input level. When DOS is indicated due to mismatched signals, the output is latched low until a rising edge of $\overline{\text{SAMPLE}}$ resets the stored minimum and maximum values. The DOS condition has priority over the LOT condition, as shown in Table 4. DOS is indicated within 30° of angular output error worst case.

Loss of Position Tracking Detection

Loss of tracking (LOT) is detected for three separate conditions:

- When the internal error signal of the AD2S1205 has exceeded 5°
- When the input signal exceeds the maximum tracking rate of 60,000 rpm (1,000 rps)
- When the internal position (at the position integrator) differs from the external position (at the position register) by more than 5°

LOT is indicated by a logic low on the LOT pin, and is not latched. LOT has a 4° hysteresis, and is not cleared until the internal error signal or internal/external position mismatch is less than 1°. When the maximum tracking rate is exceeded, LOT is cleared when both the velocity is less than 1,000 rps and the internal/external position mismatch is less than 1°. LOT can be indicated for step changes in position (such as after a $\overline{\text{RESET}}$ signal is applied to the AD2S1205), or for accelerations >~85,000 rps^2. LOT is useful as a built-in test (BIT) that the tracking converter is functioning properly. The LOT condition has lower priority than both the DOS and LOS conditions as shown in Table 4. The LOT and DOS conditions cannot be indicated at the same time.

Table 4. Fault Detection Decoding

Condition	DOS	LOT	Priority
Loss of Signal	0	0	1
Degradation of Signal	0	1	2
Loss of Tracking	1	0	3
No Fault	1	1	

Responding to a Fault Condition

If any fault condition (LOS, DOS, or LOT) is indicated by the AD2S1205, the output data must be presumed to be invalid. This means that even if a $\overline{\text{RESET}}$ or $\overline{\text{SAMPLE}}$ pulse releases the fault condition, the output data may be corrupted, even though a fault may not be immediately indicated after the $\overline{\text{RESET}}$/$\overline{\text{SAMPLE}}$ event. As discussed earlier, there are some fault conditions with inherent latency. If the device fault is cleared, there could be some latency in the resolver's mechanical position before the fault condition is re-indicated.

When a fault is indicated, all output pins will still provide data, although the data may or may not be valid. The fault condition will not force the parallel, serial, or encoder outputs to a known state.

Response to specific fault conditions is a system-level requirement. The fault outputs of the AD2S1205 indicate that the device has sensed a potential problem with either the internal or external signals of the AD2S1205. It is the responsibility of the system designer to implement the appropriate fault-handling schemes within the control hardware and/or algorithm of a given application based on the indicated fault(s) and the velocity or position data provided by the AD2S1205.

False Null Condition

Resolver-to-digital converters that employ Type II tracking loops based on the error equation (Equation 3) presented in the Principle of Operation section can suffer from a condition known as "false null." This condition is caused by a metastable solution to the error equation when $\theta - \phi = 180°$. The AD2S1205 is not susceptible to this condition because its hysteresis is implemented externally to the tracking loop. Because of the loop architecture chosen for the AD2S1205, the internal error signal always has some movement (1 LSB per clock cycle), and so, in a metastable state, the converter will always move to an unstable condition within one clock cycle, causing the tracking loop to respond to the false null condition as if it were a 180° step change in input position (the response time is the same as specified in Dynamic Performance section of Table 1). Therefore, it is impossible to enter the metastable condition any time after the startup sequence as long as the resolver signals are valid.

CONNECTING THE CONVERTER

Refer to Figure 5. Ground should be connected to the AGND pin and DGND pin. Positive power supply V_{DD} = +5 V dc ± 5% should be connected to the AV_{DD} pin and DV_{DD} pin. Typical values for the decoupling capacitors are 10 nF and 4.7 µF, respectively. These capacitors should be placed as close to the device pins as possible, and should be connected to both AV_{DD} and DV_{DD}. If desired, the reference oscillator frequency can be changed from the nominal value of 10 kHz using FS1 and FS2. Typical values for the oscillator decoupling capacitors are 20 pF. Typical values for the reference decoupling capacitors are 10 µF and 0.01 µF, respectively.

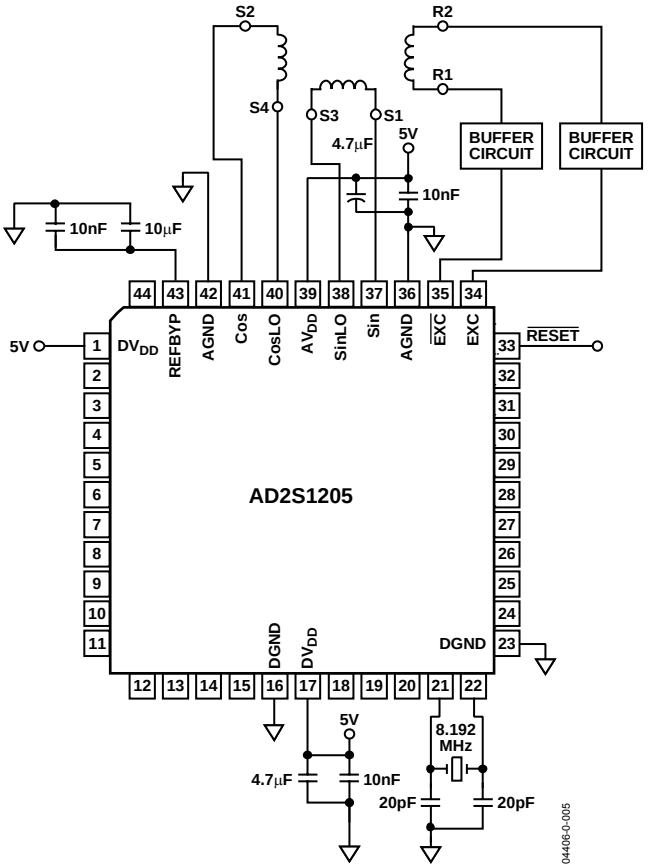

Figure 5. Connecting the AD2S1205 to a Resolver

The gain of the buffer depends on the type of resolver used. Since the specified excitation output amplitudes are matched to the specified Sin/Cos input amplitudes, the gain of the buffer is determined by the attenuation of the resolver.

In this recommended configuration, the converter introduces a $V_{REF}/2$ offset in the Sin, Cos signals coming from the resolver. Of course, the SinLO and CosLO signals may be connected to a different potential relative to ground, as long as the Sin and Cos signals respect the recommended specifications. Note that since the EXC/$\overline{\text{EXC}}$ outputs are differential, there is an inherent gain of 2×.

For example, if the primary to secondary turns ratio is 2:1, the buffer will have unity gain. Likewise, if the turns ratio is 5:1, the gain of the buffer should be 2.5×. Figure 6 suggests a buffer circuit. The gain of the circuit is

$$Gain = -(R2/R1)$$

$$\text{and } V_{OUT} = \left(V_{REF} \times \left(1 + \frac{R2}{R1}\right)\right) - \left(\frac{R2}{R1} \times V_{IN}\right)$$

V_{REF} is set so that V_{OUT} is always a positive value, eliminating the need for a negative supply.

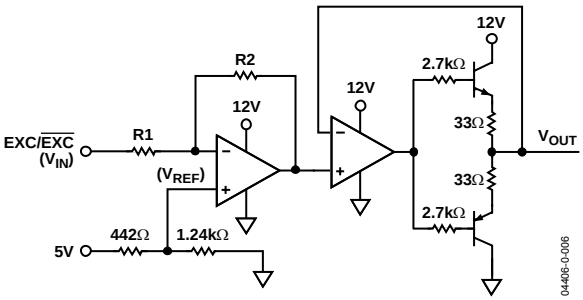

Figure 6. Buffer Circuit

Separate screened twisted cable pairs are recommended for analog inputs Sin/SinLO and Cos/CosLO. The screens should terminate to REFOUT. To achieve the dynamic performance specified, an 8.192 MHz crystal must be used.

ABSOLUTE POSITION AND VELOCITY OUTPUT

The angular position and angular velocity are represented by binary data and can be extracted either via a 12-bit parallel interface or a 3-wire serial interface that operates at clock rates up to 25 MHz. The chip select pin, $\overline{CS}$, must be held low to enable the device. Angular position and velocity can be selected using a dedicated polarity input, $\overline{RDVEL}$.

$\overline{SOE}$ Input

The serial output enable pin, $\overline{SOE}$, is held high to enable the parallel interface. The $\overline{SOE}$ pin is held low to enable the serial interface, which places pins (DB0–DB9) in the high impedance state, while DB11 is the serial output (SO), and DB10 is the serial clock input (SCLK).

Data Format

The digital angle signal represents the absolute position of the resolver shaft as a 12-bit unsigned binary word. The digital velocity signal is a 12-bit twos complement word, which represents the velocity of the resolver shaft rotating in either a clockwise or a counterclockwise direction.

Finally, the $\overline{RD}$ input is used to read the data from the output register and to enable the output buffer. The timing requirements for the read cycle are illustrated in Figure 7.

$\overline{SAMPLE}$ Input

Data is transferred from the position and velocity integrators respectively to the position and velocity registers following a high to low transition of the $\overline{SAMPLE}$ signal. This pin must be held low for at least t_1 ns to guarantee correct latching of the data. $\overline{RD}$ should not be pulled low before this time. Also, a rising edge of $\overline{SAMPLE}$ resets the internal registers that contain the minimum and maximum magnitude of the monitor signal.

PARALLEL INTERFACE

The angular position and angular velocity are available on the AD2S1205 in two 12-bit registers, which can be accessed via the 12-bit parallel port. The parallel interface is selected holding the $\overline{SOE}$ pin high. Data is transferred from the velocity and position integrators, respectively, to the position and velocity registers following a high-to-low transition on the $\overline{SAMPLE}$ pin. The $\overline{RDVEL}$ polarity pin selects which register from the position or the velocity registers is transferred to the output register. The $\overline{CS}$ pin must be held low to transfer the selected data register to the output register. Finally, the $\overline{RD}$ input is used to read the data from the output register and to enable the output buffer. The timing requirements for the read cycle are shown in Figure 7.

$\overline{SAMPLE}$ Input

Data is transferred from the position and velocity integrators, respectively, to the position and velocity registers following a high-to-low transition on the $\overline{SAMPLE}$ signal. This pin must be held low for at least t_1 ns to guarantee correct latching of the data. $\overline{RD}$ should not be pulled low before this time since data would not be ready. The converter will continue to operate during the read process. Also, a rising edge of $\overline{SAMPLE}$ resets the internal registers that contain the minimum and maximum magnitude of the monitor signal.

$\overline{CS}$ Input

The device will be enabled when $\overline{CS}$ is held low.

$\overline{RDVEL}$ Input

$\overline{RDVEL}$ input is used to select between the angular position and velocity registers as shown in Figure 7. $\overline{RDVEL}$ is held high for angular position and low for angular velocity. The $\overline{RDVEL}$ pin must be set (stable) at least t_4 ns before the $\overline{RD}$ pin is pulled low.

$\overline{RD}$ Input

The 12-bit data bus lines are normally in a high impedance state. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. A falling edge of the $\overline{RD}$ signal transfers data to the output buffer. The selected data is made available to the bus to be read within t_6 ns of the $\overline{RD}$ pin going low. The data pins will return to high impedance state when the $\overline{RD}$ returns to high state, within t_7 ns. If the user is reading data continuously, $\overline{RD}$ can be reapplied a minimum of t_3 ns after it was released.

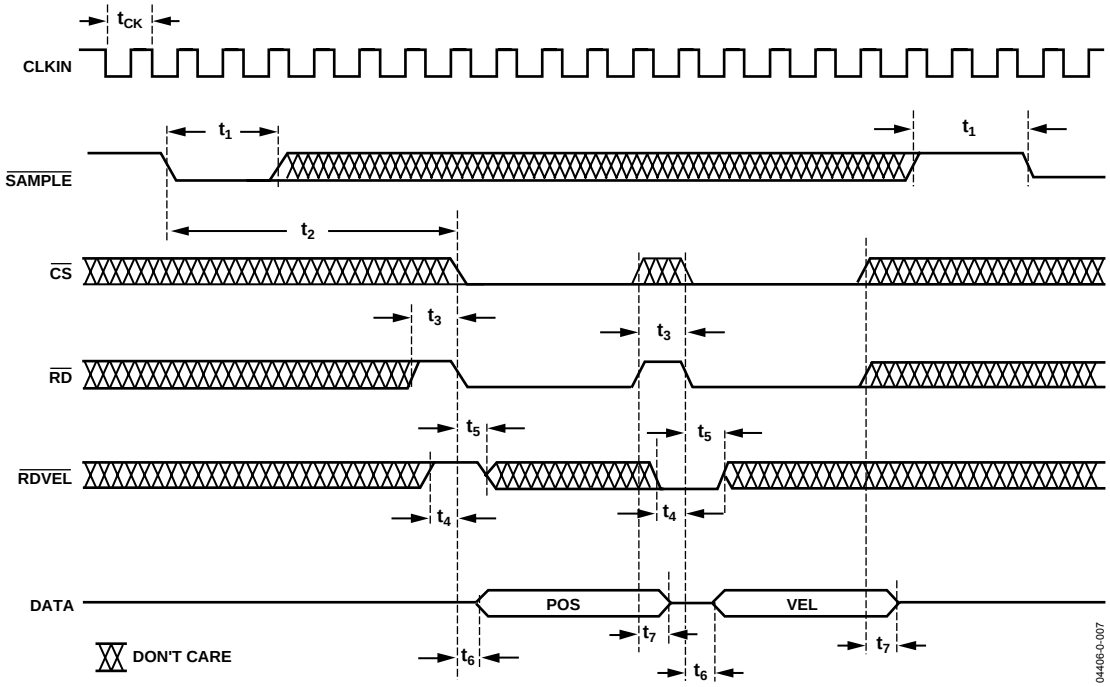

Figure 7. Parallel Port Read Timing

Table 5. Parallel Port Timing

Parameter	Description	Min	Typ	Max
t_{CK}	*Clock Period (= 1/8.192 MHz)*		*~122 ns*	
t_1	$\overline{\text{SAMPLE}}$ Pulse Width	$2 \times t_{CK} + 20$ ns		
t_2	Delay from $\overline{\text{SAMPLE}}$ before $\overline{\text{RD}}/\overline{\text{CS}}$ Low	$6 \times t_{CK} + 20$ ns		
t_3	$\overline{\text{RD}}$ Pulse Width	18 ns		
t_4	Set Time $\overline{\text{RDVEL}}$ before $\overline{\text{RD}}/\overline{\text{CS}}$ Low	5 ns		
t_5	Hold Time $\overline{\text{RDVEL}}$ after $\overline{\text{RD}}/\overline{\text{CS}}$ Low	7 ns		
t_6	Enable Delay $\overline{\text{RD}}/\overline{\text{CS}}$ Low to Data Valid			12 ns
t_7	Disable Delay $\overline{\text{RD}}/\overline{\text{CS}}$ Low to Data High Z			18 ns

SERIAL INTERFACE

The angular position and angular velocity are available on the AD2S1205 in two 12-bit registers. These registers can be accessed via a 3-wire serial interface, SO, $\overline{RD}$, and SCLK, that operates at clock rates up to 25 MHz and is compatible with SPI and DSP interface standards. The serial interface is selected by holding low the $\overline{SOE}$ pin. Data from the position and velocity integrators are first transferred to the position and velocity registers, using the $\overline{SAMPLE}$ pin. The $\overline{RDVEL}$ polarity pin selects which register from the position or the velocity registers is transferred to the output register. The $\overline{CS}$ pin must be held low to transfer the selected data register to the output register. Finally, the $\overline{RD}$ input is used to read the data that will be clocked out of the output register and will be available on the serial output pin, SO. When the serial interface is selected, DB11 is used as the serial output pin, SO, and DB10 is used as the serial clock input, SCLK, while pins DB0–DB9 are placed in the high impedance state. The timing requirements for the read cycle are described in Figure 8.

SO Output

The output shift register is 16-bit wide. Data is shifted out of the device as a 16-bit word under the control of the serial clock input, SCLK. The timing diagram for this operation is shown in Figure 8. The 16-bit word consists of 12 bits of angular data (position or velocity depending on $\overline{RDVEL}$ input), one $\overline{RDVEL}$ status bit and three status bits, a parity bit, degradation of signal bit, and loss of tracking bit. Data is read out MSB first (bit 15) on the SO pin. Bit 15 through bit 4 correspond to the angular information. The angular position data format is unsigned binary, with all zeros corresponding to 0 degrees and all ones corresponding to 360 degrees –l LSB. The angular velocity data format instead is twos complement binary, with the MSB representing the rotation direction. Bit 3 is the $\overline{RDVEL}$ status bit, 1 indicating position and 0 indicating velocity. Bit 2 is DOS, the degradation of signal flag (refer to the Fault Detection Circuit section). Bit 1 is LOT, the loss of tracking flag (refer to the Fault Detection Circuit section). Bit 0 is PAR, the parity bit: both position and velocity data are odd parity format; the data read out will always contain an odd number of logic highs (1s).

$\overline{SAMPLE}$ Input

Data is transferred from the position and velocity integrators, respectively, to the position and velocity registers following a high-to-low transition on the $\overline{SAMPLE}$ signal. This pin must be held low for at least t_1 ns to guarantee correct latching of the data. $\overline{RD}$ should not be pulled low before this time since data would not be ready. The converter will continue to operate during the read process.

$\overline{CS}$ Input

The device will be enabled when $\overline{CS}$ is held low.

$\overline{RD}$ Input

The 12-bit data bus lines are normally in a high impedance state. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. The $\overline{RD}$ input is an edge-triggered input that acts as frame synchronization signal and output enable. A falling edge of the $\overline{RD}$ signal transfers data to the output buffer and data will be available on the serial output pin, SO. $\overline{RD}$ must be held low for t_9 before the data is valid on the outputs. After $\overline{RD}$ goes low, the serial data will be clocked out of the SO pin on the falling edges of the SCLK (after a minimum of t_{10} ns): the MSB will be already available at the SO pin on the very first falling edge of the SCLK. Each other bit of the data word will be shifted out on the rising edge of SCLK and will be available at the SO pin on the falling edge of SCLK for the next 15 clock pulses.

The high-to-low transition of $\overline{RD}$ must happen during the high time of the SCLK to avoid MSB being shifted on the first rising edge of the SCLK and lost. $\overline{RD}$ may rise high after the falling edge of the last bit transmitted. Subsequent negative edges greater than the defined word length will clock zeros from the data output if $\overline{RD}$ remains in a low state. If the user is reading data continuously, $\overline{RD}$ can be reapplied a minimum of t_5 ns after it is released.

$\overline{RDVEL}$ Input

$\overline{RDVEL}$ input is used to select between the angular position and velocity registers. $\overline{RDVEL}$ is held high for angular position and low for angular velocity. The $\overline{RDVEL}$ pin must be set (stable) at least t_4 ns before the $\overline{RD}$ pin is pulled low.

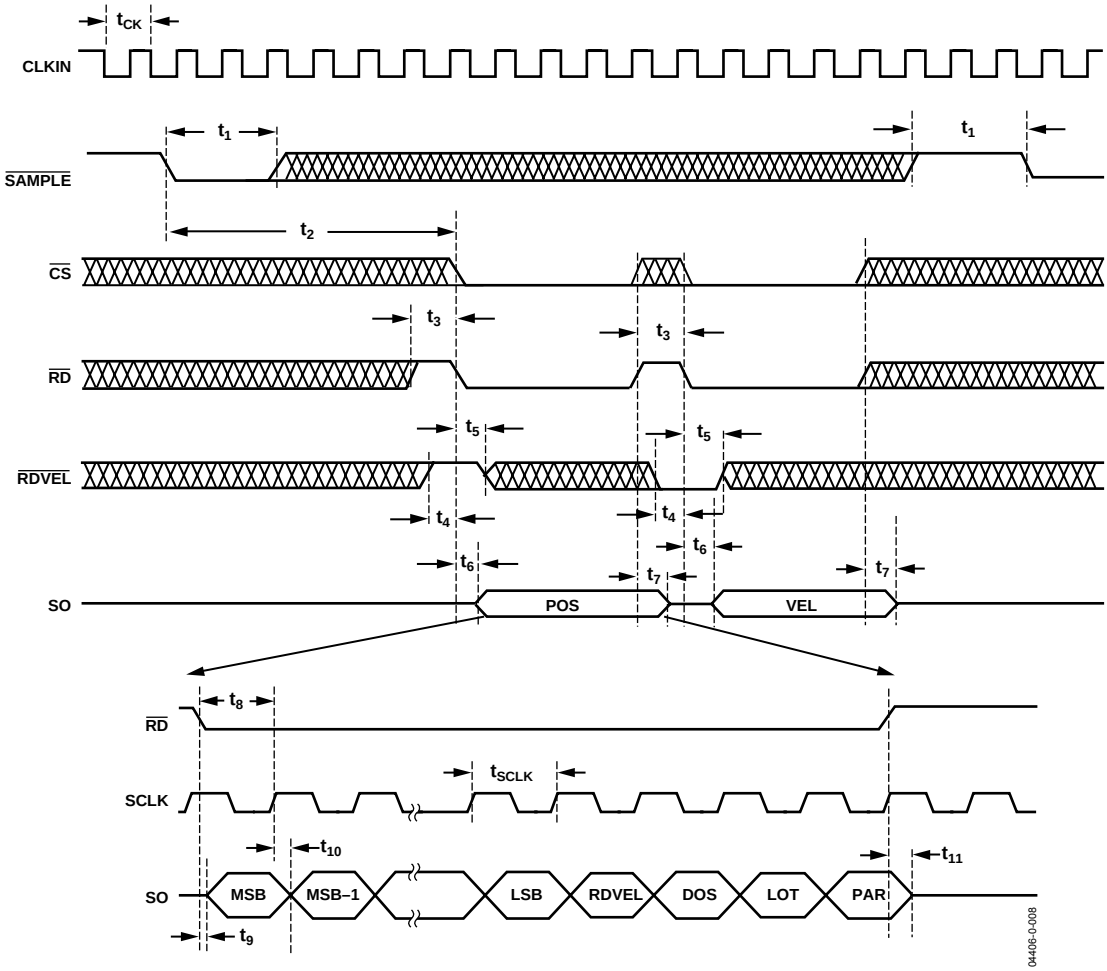

Figure 8. Serial Port Read Timing

Table 6. Serial Port Timing

Parameter	Description	Min	Typ	Max
t_8	MSB Read Time from $\overline{RD}/\overline{CS}$ to SCLK	15 ns		t_{SCLK}
t_9	Enable Time $\overline{RD}/\overline{CS}$ to DB Valid			12 ns
t_{10}	Delay SCLK to DB Valid			14 ns
t_{11}	Disable Time $\overline{RD}/\overline{CS}$ to DB High Z			18 ns
t_{SCLK}	Serial Clock Period (25 MHz Max)	40 ns		

INCREMENTAL ENCODER OUTPUTS

The incremental encoder emulation outputs A, B, and NM are free running and are always valid, providing that valid resolver format input signals are applied to the converter.

The AD2S1205 emulates a 1024-line encoder. Relating this to converter resolution means one revolution produces 1,024 A, B pulses. A leads B for increasing angular rotation (i.e., clockwise direction). The addition of the DIR output negates the need for external A and B direction decode logic. The DIR output indicates the direction of the input rotation and it is high for increasing angular rotation. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This occurs when the direction of rotation of the input changes but the magnitude of the rotation is less than 1 LSB.

The north marker pulse is generated as the absolute angular position passes through zero. The north marker pulse width is set internally for 90° and is defined relative to the A cycle. Figure 9 details the relationship between A, B, and NM.

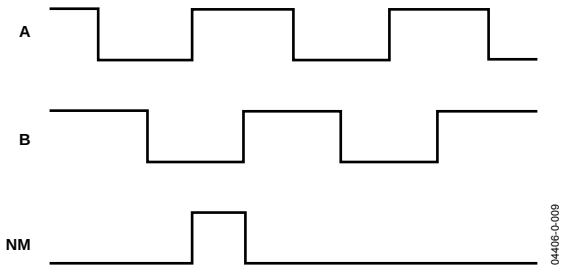

Figure 9. A, B, and NM Timing for Clockwise Rotation

Unlike incremental encoders, the AD2S1205 encoder output is not subject to error specifications such as cycle error, eccentricity, pulse and state width errors, count density, and phase ϕ. The maximum speed rating, n, of an encoder is calculated from its maximum switching frequency, f_{MAX}, and its pulses per revolution (PPR).

$$n = \frac{60 \times f_{MAX}}{PPR}$$

The AD2S1205 A, B pulses are initiated from XTALOUT, which has a frequency of 4.096 MHz. The equivalent encoder switching frequency is

$$1/4 \times 4.096\,MHz = 1.024\,MHz\ (4Updates = 1Pulse)$$

Rev. PrB_10/06

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At 12 bits, the PPR = 1,024. Therefore, the maximum speed, *n*, of the AD2S1205 is

$$n = \frac{60 \times 1{,}024{,}000}{1{,}024} = 60000\ rpm$$

To get a maximum speed of 60,000 rpm, an external crystal of 8.192 MHz has to be chosen in order to produce an internal CLOCKOUT equal to 4.096 MHz.

This compares favorably with encoder specifications where f_{MAX} is specified from 20 kHz (photo diodes) to 125 kHz (laser based) depending on the light system used. A 1,024 line laser-based encoder will have a maximum speed of 7,300 rpm.

The inclusion of A, B outputs allows the AD2S1205 plus resolver solution to replace optical encoders directly without the need to change or upgrade existing application software.

ON-BOARD PROGRAMMABLE SINUSOIDAL OSCILLATOR

An on-board oscillator provides the sinusoidal excitation signal (EXC) to the resolver as well as its complemented signal ($\overline{EXC}$). The frequency of this reference signal is programmable to four standard frequencies (10 kHz, 12 kHz, 15 kHz, or 20 kHz) using the FS1 and FS2 pins (see Table 7). FS1 and FS2 have internal pull-ups, so the default frequency is 10 kHz. The amplitude of this signal is centered on 2.5 V and has an amplitude of 3.6 V p-p.

Table 7. Excitation Frequency Selection

Frequency Selection (kHz)	FS1	FS2
10	1	1
12	1	0
15	0	1
20	0	0

The reference output of the AD2S1205 will need an external buffer amplifier to provide gain and the additional current to drive a resolver. Refer to Figure 6 for a suggested buffer circuit.

The AD2S1205 also provides an internal synchronous reference signal that is phase locked to its Sin and Cos inputs. Phase errors between the resolver primary and secondary windings could degrade the accuracy of the RDC and are compensated by this synchronous reference signal. This also compensates the phase shifts due to temperature and cabling and eliminates the need of an external preset phase compensation circuits.

Synthetic Reference Generation

When a resolver undergoes a high rotation rate, the RDC tends to act as an electric motor and produces speed voltages, along with the ideal Sin and Cos outputs. These speed voltages are in quadrature to the main signal waveform. Moreover, nonzero resistance in the resolver windings causes a non-zero phase shift between the reference input and the Sin and Cos outputs. The combination of speed voltages and phase shift causes a tracking error in the RDC that is approximated by

$$Error = Phase\,Shift \times \frac{Rotation\,Rate}{Reference\,Frequency}$$

To compensate for the described phase error between the resolver reference excitation and the Sin/Cos signals, an internal synthetic reference signal is generated in phase with the reference frequency carrier. The synthetic reference is derived using the internally filtered Sin and Cos signals. It is generated by determining the zero crossing of either the Sin or Cos (whichever signal is larger, to improve phase accuracy) and evaluating the phase of the resolver reference excitation. The synthetic reference reduces the phase shift between the reference and Sin/Cos inputs to less than 10°, and will operate for phase shifts of ±45°.

SUPPLY SEQUENCING AND RESET

The AD2S1205 requires an external reset signal to hold the $\overline{RESET}$ input low until V_{DD} is within the specified operating range of 4.5 V to 5.5 V.

The $\overline{RESET}$ pin must be held low for a minimum of 10 µs after V_{DD} is within the specified range (t_{RST} in Figure 10). Applying a $\overline{RESET}$ signal to the AD2S1205 initializes the output position to a value of 0x000 (degrees output through the parallel, serial, and encoder interfaces) and causes LOS to be indicated (LOT and DOS pins pulled low) as shown in Figure 10.

Failure to apply the above (correct) power-up/reset sequence can result in an incorrect position indication.

After a rising edge on the $\overline{\text{RESET}}$ input, the device must be allowed at least 20 ms (t_{TRACK}) as shown in Figure 10 for internal circuitry to stabilize and the tracking loop to settle to the step change in input position. After t_{TRACK}, a $\overline{\text{SAMPLE}}$ pulse must be applied, releasing the LOT and DOT pins to the state determined by the fault detection circuitry and providing valid position data at the parallel and serial outputs (note that if position data is being acquired via the encoder outputs, they may be monitored during t_{TRACK}).

The $\overline{\text{RESET}}$ pin is internally pulled up.

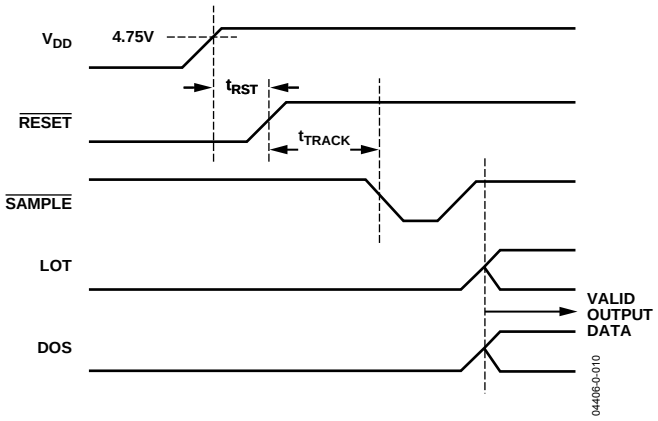

Figure 10. Power Supply Sequencing and Reset

CHARGE PUMP OUTPUT

A 204.8 kHz square wave output with 50% duty cycle is available at the CPO output pin of the AD2S1205. This square wave output can be used for negative rail voltage generation, or to create a V_{CC} rail.

CIRCUIT DYNAMICS

AD2S1205 LOOP RESPONSE MODEL

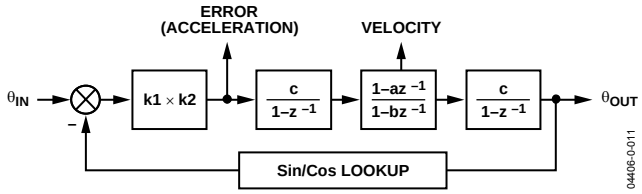

Figure 11. RDC System Response Block Diagram

The RDC is a mixed-signal device, which uses two A/D converters to digitize signals from the resolver and a Type II tracking loop to convert these to digital position and velocity words.

The first gain stage consists of the ADC gain on the Sin/Cos inputs, and the gain of the error signal into the first integrator. The first integrator generates a signal proportional to velocity. The compensation filter contains a pole and a zero, used to provide phase margin and reduce high frequency noise gain. The second integrator is the same as the first integrator and generates the output position from the velocity signal. The Sin/Cos lookup has unity gain. Values are given below for each section:

- ADC gain parameter ($k1_{nom}$ = 1.8/2.5) $$k1 = \frac{V_{IN}(V_p)}{V_{REF}(V)}$$
- Error gain parameter $$k2 = 18\,x\,10^6 \times 2\pi$$
- Compensator zero coefficient $$a = \frac{4095}{4096}$$
- Compensator pole coefficient $$b = \frac{4085}{4096}$$
- Integrator gain parameter $$c = \frac{1}{4096000}$$
- INT1 and INT2 transfer function $$I(z) = \frac{c}{1 - z^{-1}}$$
- Compensation filter transfer function $$C(z) = \frac{1 - az^{-1}}{1 - bz^{-1}}$$
- R2D open-loop transfer function $$G(z) = k1 \times k2 \times I(z)^2 \times C(z)$$
- R2D closed-loop transfer function $$H(z) = \frac{G(z)}{1 + G(z)}$$

The closed-loop magnitude and phase responses are that of a second-order low-pass filter (see Figure 12 and Figure 13).

To convert G(z) into the s-plane, we perform an inverse bilinear transformation by substituting for *z,* where *T* = the sampling period (1/4.096 MHz ≈ 244 ns).

$$z = \frac{\frac{2}{T} + s}{\frac{2}{T} - s}$$

Substitution yields the open-loop transfer function G(s).

$$G(s) = \frac{k1 \times k2(1-a)}{a-b} \times \frac{1 + sT + \frac{s^2T^2}{4}}{s^2} \times \frac{1 + s \times \frac{T(1+a)}{2(1-a)}}{1 + s \times \frac{T(1+b)}{2(1-b)}}$$

This transformation produces the best matching at low frequencies ($f << f_{SAMPLE}$). At lower frequencies (within the closed-loop bandwidth of the AD2S1205), the transfer function can be simplified to

$$G(s) \cong \frac{K_a}{s^2} \times \frac{1 + st_1}{1 + st_2}$$

where:

$$t_1 = \frac{T(1+a)}{2(1-a)}$$

$$t_2 = \frac{T(1+b)}{2(1-b)}$$

$$K_a = \frac{k1 \times k2(1-a)}{a-b}$$

Solving for each value gives t_1 = 1 ms, t_2 = 90 µs, and $K_a \approx 7.4 \times 10^6\ s^{-2}$. Note that the closed-loop response is described as

$$H(s) = \frac{G(s)}{1 + G(s)}$$

By converting to the s-domain, we are able to quantify the open-loop dc gain (K_a). This value is useful during calculation of acceleration error of the loop as discussed in the Sources of Error section.

The step response to a 10° input step is shown in Figure 14. Because the error calculation (Equation 3) is nonlinear for large values of θ − ϕ, the response time for larger step changes in position (90°–180°) will typically take three times as long as the response to a small step change in position (<20°). In response to a step change in velocity, the AD2S1205 will exhibit the same response characteristics as for a step change in position.

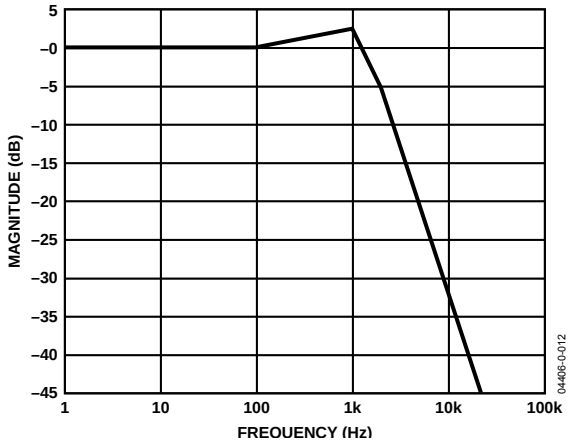

Figure 12. RDC System Magnitude Response

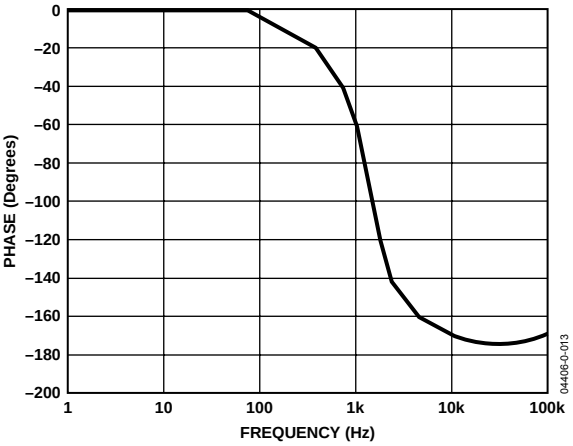

Figure 13. RDC System Phase Response

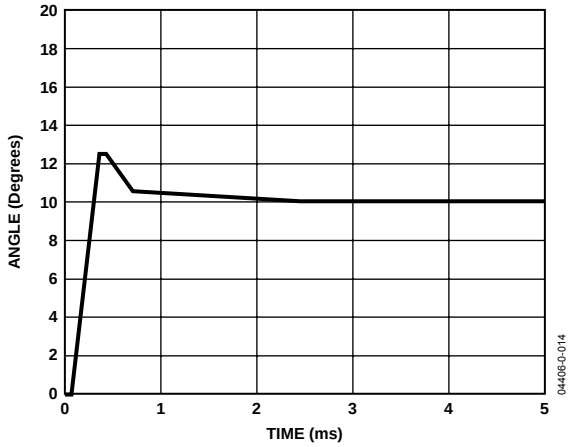

Figure 14. RDC Small Step Response

SOURCES OF ERROR

Acceleration

A tracking converter employing a Type II servo loop does not suffer any velocity lag. There is, however, an error associated with acceleration. This error can be quantified using the acceleration constant (K_a) of the converter.

$$K_a = \frac{Input\ Acceleration}{Tracking\ Error}$$

Conversely,

$$Tracking\ Error = \frac{Input\ Acceleration}{K_a}$$

Figure 15 shows tracking error versus acceleration for the AD2S1205.

The numerator and denominator's units must be consistent. The maximum acceleration of the AD2S1205 has been defined as the acceleration that creates an output position error of 5° (when LOT is indicated). The maximum acceleration can be calculated as

$$Maximum\ Acceleration = \frac{K_a(\sec^{-2}) \times 5°}{360(°/rev)} \cong 103{,}000\,rps^2$$

The AD2S1205 will be able to withstand the maximum acceleration of 103,000 rps^2 for approximately 10 ms before reaching its maximum tracking rate of 1,000 rps.

$$\frac{1{,}000(rps)}{103{,}000(rps^2)} \cong 10\,ms$$

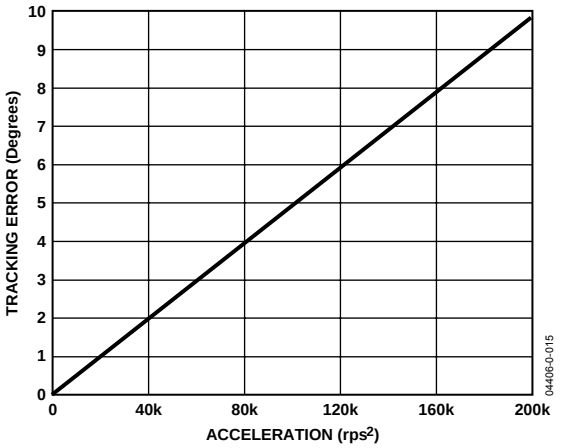

Figure 15. Tracking Error vs. Acceleration

CLOCK REQUIREMENTS

To achieve the specified dynamic performance, an external crystal is recommended at the CLKIN, XTALOUT pins. The position and velocity accuracy are guaranteed for operation with a range of input frequencies from 6.144MHz to 10.24 MHz., based around a nominal value of 8.192 MHz. The velocity outputs are scaled in proportion to the clock frequency so that if the clock is 25% higher than the nominal, the full-scale velocity will be 25% higher than nominal. The maximum tracking rate, the tracking loop bandwidth and the excitation output frequencies also vary with the clock frequency.

CONNECTING TO THE DSP

The AD2S1205 serial port is ideally suited for interfacing to DSP configured microprocessors. Figure 16 shows the AD2S1205 interfaced to ADMC401, one of the DSP based motor controllers.

The on-chip serial port of the ADMC401 is used in the following configuration:

- Alternate framing transmit mode with internal framing (internally inverted)
- Normal framing receive mode with external framing (internally inverted)
- Internal serial clock generation

In this mode, the ADMC401 uses the internal TFS signal as external RFS to fully control the timing of receiving data and it uses the same TFS as $\overline{RD}$ to the AD2S1205. The ADMC401 also provides an internal continuous serial clock to the AD2S1205.

The $\overline{SAMPLE}$ signal on the AD2S1205 could be provided either by using a PIO or by inverting the PWMSYNC signal to synchronize the position and velocity reading with the PWM switching frequency. $\overline{CS}$ and $\overline{RDVEL}$ may be obtained using two PIO outputs of the ADMC401. The 12 bits of significant data plus status bits are available on each consecutive negative edge of the clock following the low going of the $\overline{RD}$ signal. Data is clocked from the AD2S1205 into the data receive register of the ADMC401. This is internally set to 16 bits (12 bits data, 4 status bits) because 16 bits are received overall. The serial port automatically generates an internal processor interrupt. This allows the ADMC401 to read 16 bits at once and continue processing.

All ADMC401 products can interface to the AD2S1205 with similar interface circuitry.

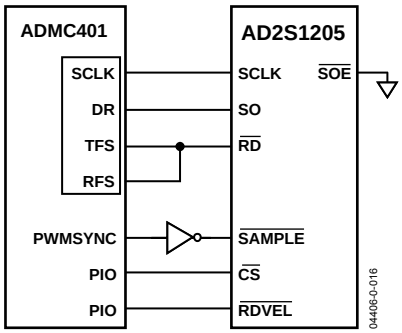

Figure 16. Connecting to the ADMC401

OUTLINE DIMENSIONS

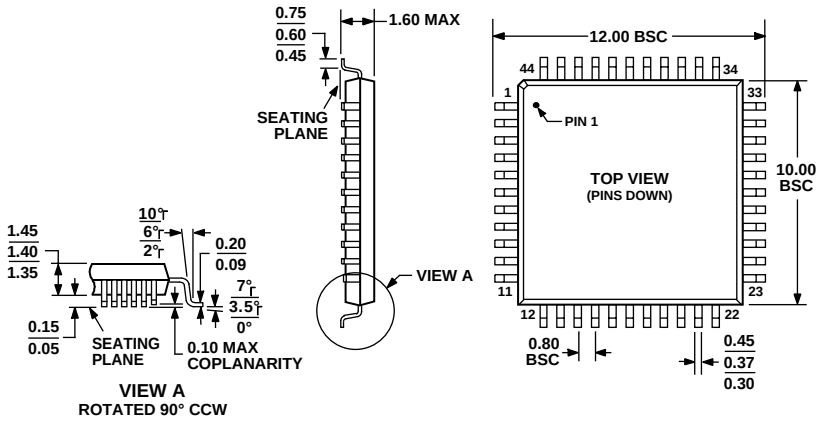

Figure 17. 44-Lead Low Profile Quad Flat Package [LQFP]
(ST-44)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Angular Accuracy	Package Description	Package Option
AD2S1205YSTZ	−40°C to +125°C	±11 arc min	44-Lead Low Profile Quad Flat Package (LQFP)	ST-44
AD2S1205WSTZ	−40°C to +125°C	±22 arc min	44-Lead Low Profile Quad Flat Package (LQFP)	ST-44

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