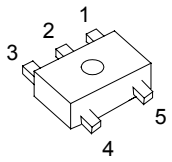
88CXX **CMOS IC**

BUILT-IN DELAY CIRCUIT HIGH-PRECISION VOLTAGE DETECTOR



SOT-25

*Pb-free plating product number: 88CXXL

■ DESCRIPTION

The UTC **88CXX** series is a high-precision voltage detector developed and foundry using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0%. The CMOS output is available. Besides, **88CXX** can easily delay a release signal by attachment of an external capacitor with built-in delay circuit.

■ FEATURES

* High-precision detection voltage: ±2.0%
* Hysteresis characteristics: 5% typ
* Ultra-low current consumption satisfied various detection voltage, 1.0 μA typ. (V_{DD}=2.0V) for ≤1.4V and 1.2 μA typ. (V_{DD}=3.5V) for ≥1.5V.
* Available detection voltage from 1.1~6.0V and step by 0.1V.
* Low operating voltage based on detection voltage, 0.8~6.0V for for ≤1.4V and 0.95~10V for ≥1.5V.
* Delay time setting by an additional external capacitor.

■ PIN CONFIGURATION

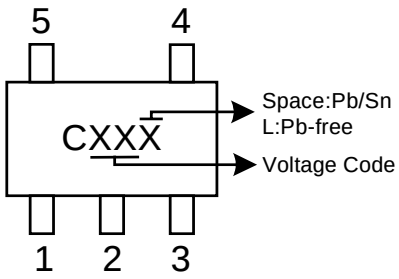
PIN NO.	PIN NAME
1	OUT
2	V_{DD}
3	V_{SS}
4	NC
5	C_D

■ ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free		
88**C**xx-AF5-R	88**C**xxL-AF5-R	SOT-25	Tape Reel

xx: Output Voltage, refer to Marking Information.

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE		MARKING
SOT-25	11:1.1V	36:3.6V	
	12:1.2V	37:3.7V	
	13:1.3V	38:3.8V	
	14:1.4V	39:3.9V	
	15:1.5V	40:4.0V	
	16:1.6V	41:4.1V	
	17:1.7V	42:4.2V	
	18:1.8V	43:4.3V	
	19:1.9V	44:4.4V	
	20:2.0V	45:4.5V	
	21:2.1V	46:4.6V	
	22:2.2V	47:4.7V	
	23:2.3V	48:4.8V	
	24:2.4V	49:4.9V	
	25:2.5V	50:5.0V	
	26:2.6V	51:5.1V	
	27:2.7V	52:5.2V	
	28:2.8V	53:5.3V	
	29:2.9V	54:5.4V	
	30:3.0V	55:5.5V	
	31:3.1V	56:5.6V	
	32:3.2V	57:5.7V	
	33:3.3V	58:5.8V	
	34:3.4V	59:5.9V	
	35:3.5V	60:6.0V	

■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃, unless otherwise specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Power Supply Voltage	≤1.4V	V_{DD}-Vss	8	V
	≥1.5V		12	
C_D terminal Input Voltage		V_{CD}	V_{SS}-0.3 ~ V_{DD} +0.3	V
Output Voltage		V_{OUT}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Output Current		I_{OUT}	50	mA
Power Dissipation		P_D	150	mW
Operating Temperature		T_{OPR}	-40 ~ +85	℃
Storage Temperature		T_{STG}	-40 ~ +150	℃

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CIRCUIT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Detection Voltage		$-V_{DET}$	1			$-V_{DET}$ ×0.98	$-V_{DET}$	$-V_{DET}$ ×1.02	V
Hysteresis Width		V_{HYS}	1			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V
Operating Voltage	≤1.4V	V_{DD}	1			0.8		6.0	V
	≥1.5V					0.95		10.0	
Current Consumption	1.1V ~ 1.4V	I_{SS}	2	V_{DD}=2.0V			1.0	2.5	μA
	1.5V ~ 2.6V			V_{DD}=3.5V			1.2	3.0	
	2.7V ~ 3.9V			V_{DD}=4.5V			1.3	3.3	
	4.0V ~ 5.4V			V_{DD}=6.0V			1.5	3.8	
	5.5V ~ 6.0V			V_{DD}=7.5V			1.6	4.2	
Output Current	1.1V ~ 1.4V	I_{OUT}	3	Nch V_{DS}=0.5V	V_{DD}=0.95V	0.03	0.25		mA
	1.5V ~ 2.6V				V_{DD}=1.20V	0.23	0.50		
	2.7V ~ 3.9V				V_{DD}=1.20V V_{DD}=2.40V	0.23 1.60	0.50 3.70		
	4.0V ~ 5.4V				V_{DD}=1.20V V_{DD}=2.40V	0.23 1.60	0.50 3.70		
	5.5V ~ 6.0V				V_{DD}=1.20V V_{DD}=2.40V	0.23 1.60	0.50 3.70		
	1.1V ~ 1.4V		4	Pch(CMOS output) V_{DS}=0.5V	V_{DD}=4.8V	0.36	0.62		
	1.5V ~ 2.6V				V_{DD}=4.8V	0.36	0.62		
	2.7V ~ 3.9V				V_{DD}=4.8V	0.36	0.62		
	4.0V ~ 5.4V				V_{DD}=6.0V	0.46	0.75		
	5.5V ~ 6.0V				V_{DD}=8.4V	0.59	0.96		
Delay Time	1.1V ~ 1.4V	td	5	V_{DD}=4.5V, C_D=4.7nF		4.95	6.6	8.25	ms
	1.5V ~ 2.6V			V_{DD}=4.5V, C_D=4.7nF		4.95	6.6	8.25	
	2.7V ~ 3.9V			V_{DD}=4.5V, C_D=4.7nF		4.95	6.6	8.25	
	4.0V ~ 5.4V			V_{DD}=7.0V, C_D=4.7nF		3	4	5	
	5.5V ~ 6.0V			V_{DD}=7.0V, C_D=4.7nF		3	4	5	

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature Characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	1	$-V_{DET}$=1.1V		±0.19	±0.57	mV/℃
			$-V_{DET}$=1.2V		±0.20	±0.60	
			$-V_{DET}$=1.3V		±0.22	±0.66	
			$-V_{DET}$=1.4V		±0.24	±0.72	
			$-V_{DET}$=1.5V		±0.18	±0.54	
			$-V_{DET}$=1.6V		±0.19	±0.57	
			$-V_{DET}$=1.7V		±0.20	±0.60	
			$-V_{DET}$=1.8V		±0.21	±0.63	
			$-V_{DET}$=1.9V		±0.22	±0.66	
			$-V_{DET}$=2.0V		±0.24	±0.72	
			$-V_{DET}$=2.1V		±0.25	±0.75	
			$-V_{DET}$=2.2V		±0.26	±0.78	
			$-V_{DET}$=2.3V		±0.27	±0.81	
			$-V_{DET}$=2.4V		±0.28	±0.84	
			$-V_{DET}$=2.5V		±0.29	±0.87	
			$-V_{DET}$=2.6V		±0.31	±0.93	
			$-V_{DET}$=2.7V		±0.32	±0.96	
			$-V_{DET}$=2.8V		±0.33	±0.99	
			$-V_{DET}$=2.9V		±0.34	±1.02	
			$-V_{DET}$=3.0V		±0.35	±1.05	
			$-V_{DET}$=3.1V		±0.36	±1.08	
			$-V_{DET}$=3.2V		±0.38	±1.14	
			$-V_{DET}$=3.3V		±0.39	±1.17	
			$-V_{DET}$=3.4V		±0.40	±1.20	
			$-V_{DET}$=3.5V		±0.41	±1.23	
			$-V_{DET}$=3.6V		±0.42	±1.26	
			$-V_{DET}$=3.7V		±0.44	±1.32	
			$-V_{DET}$=3.8V		±0.45	±1.35	
			$-V_{DET}$=3.9V		±0.46	±1.38	
			$-V_{DET}$=4.0V		±0.47	±1.41	
			$-V_{DET}$=4.1V		±0.48	±1.44	
			$-V_{DET}$=4.2V		±0.49	±1.47	
			$-V_{DET}$=4.3V		±0.51	±1.53	
			$-V_{DET}$=4.4V		±0.52	±1.56	
			$-V_{DET}$=4.5V		±0.53	±1.59	
			$-V_{DET}$=4.6V		±0.54	±1.62	
			$-V_{DET}$=4.7V		±0.55	±1.65	
			$-V_{DET}$=4.8V		±0.56	±1.68	
			$-V_{DET}$=4.9V		±0.58	±1.74	
			$-V_{DET}$=5.0V		±0.59	±1.77	
			$-V_{DET}$=5.1V		±0.60	±1.80	
			$-V_{DET}$=5.2V		±0.61	±1.83	
			$-V_{DET}$=5.3V		±0.62	±1.86	
			$-V_{DET}$=5.4V		±0.64	±1.92	
			$-V_{DET}$=5.5V		±0.65	±1.95	
			$-V_{DET}$=5.6V		±0.66	±1.98	
			$-V_{DET}$=5.7V		±0.67	±2.01	
			$-V_{DET}$=5.8V		±0.68	±2.04	
			$-V_{DET}$=5.9V		±0.69	±2.07	
			$-V_{DET}$=6.0V		±0.71	±2.13	

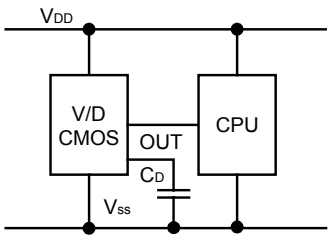
■ DECTECTION VOLTAGE RANGE vs HYSTERESIS WIDTH

DETECTION VOLTAGE RANGE (V)	HYSTERESIS WIDTH V_{HYS} TYP (V)	DETECTION VOLTAGE RANGE (V)	HYSTERESIS WIDTH V_{HYS} TYP (V)
1.1V±2.0%	0.055	3.6V±2.0%	0.180
1.2V±2.0%	0.060	3.7V±2.0%	0.185
1.3V±2.0%	0.065	3.8V±2.0%	0.190
1.4V±2.0%	0.070	3.9V±2.0%	0.195
1.5V±2.0%	0.075	4.0V±2.0%	0.200
1.6V±2.0%	0.080	4.1V±2.0%	0.205
1.7V±2.0%	0.085	4.2V±2.0%	0.210
1.8V±2.0%	0.090	4.3V±2.0%	0.215
1.9V±2.0%	0.095	4.4V±2.0%	0.220
2.0V±2.0%	0.100	4.5V±2.0%	0.225
2.1V±2.0%	0.105	4.6V±2.0%	0.230
2.2V±2.0%	0.110	4.7V±2.0%	0.235
2.3V±2.0%	0.115	4.8V±2.0%	0.240
2.4V±2.0%	0.120	4.9V±2.0%	0.245
2.5V±2.0%	0.125	5.0V±2.0%	0.250
2.6V±2.0%	0.130	5.1V±2.0%	0.255
2.7V±2.0%	0.135	5.2V±2.0%	0.260
2.8V±2.0%	0.140	5.3V±2.0%	0.265
2.9V±2.0%	0.145	5.4V±2.0%	0.270
3.0V±2.0%	0.150	5.5V±2.0%	0.275
3.1V±2.0%	0.155	5.6V±2.0%	0.280
3.2V±2.0%	0.160	5.7V±2.0%	0.285
3.3V±2.0%	0.165	5.8V±2.0%	0.290
3.4V±2.0%	0.170	5.9V±2.0%	0.295
3.5V±2.0%	0.175	6.0V±2.0%	0.300

■ OUTPUT CONFIGURATIONS

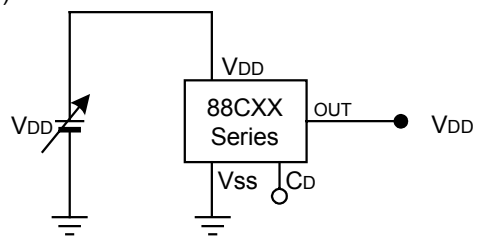
Implementation	CMOS
With different power supplies	No
With active low reset CPUs	Yes
With active high reset CPUs	No
With voltage divider variable resistors	No

Example with one power supply

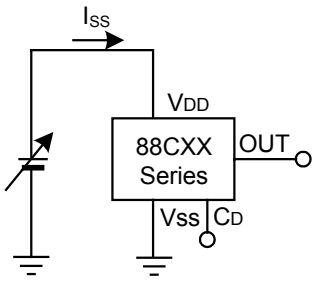


■ TEST CIRCUITS

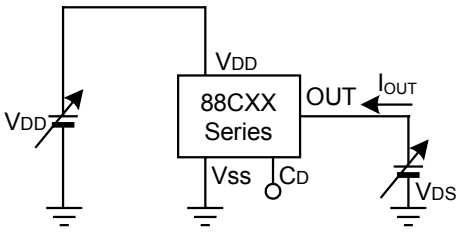
(1)



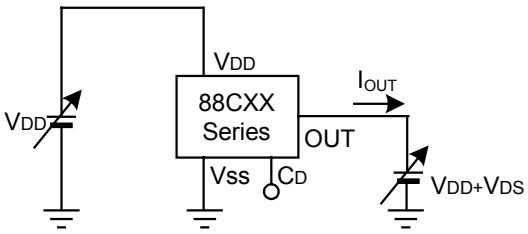
(2)



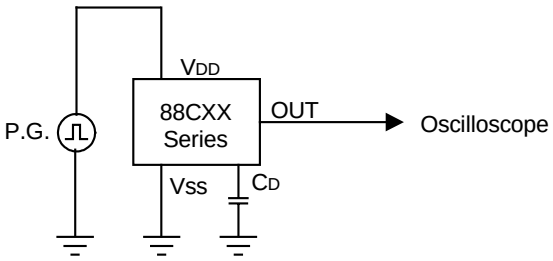
(3)

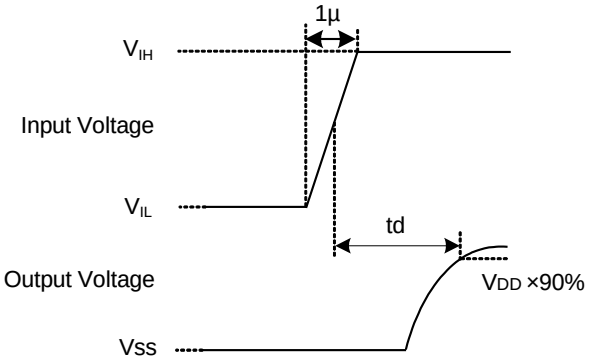


(4)



(5)





(a):V_{IH}=6V, V_{IL}=0.80V
(b):V_{IH}=10V, V_{IL}=0.95V

■ TECHNICAL TERMS

1. Detection voltage ($-V_{DET}$)

The detection voltage $-V_{DET}$ is the voltage at which the output switches to low. This detection voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [$(-V_{DET})$min.] and maximum [$(-V_{DET})$max.] values is called the detection voltage range (See Figure 1).

Example: For the $-V_{DET}$=1.5V, detection voltage lies in the range of $1.470 \leqq (-V_{DET}) \leqq 1.530$. This means that $-V_{DET}$ is 1.470 in a product while $-V_{DET}$ is 1.530 in another of the same $-V_{DET}$=1.5V.

2. Release voltage ($+V_{DET}$)

The release voltage $+V_{DET}$ is the voltage at which the output returns (is “released”) to high. This release voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [$(+V_{DET})$min.] and maximum [$(+V_{DET})$max.] values is called the release voltage range (See Figure 2).

Example: For the $-V_{DET}$=1.5V, the release voltage lies in the range of $1.514 \leqq (+V_{DET}) \leqq 1.652$. This means that $+V_{DET}$ is 1.514 in a product while $+V_{DET}$ is 1.652 in another of the same $-V_{DET}$=1.5V.

Remark: Although the detection voltage and release voltage overlap in the range of 1.514 V ~ 1.530 V, $+V_{DET}$ will always be larger than $-V_{DET}$.

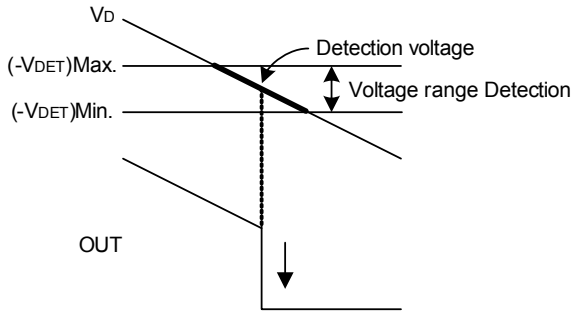


Figure 1

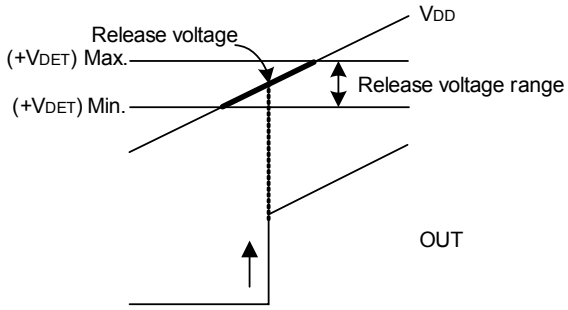


Figure 2 (C_D=0F)

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (B-A=V_{HYS} in Figure 7). By giving a device hysteresis, trouble such as noise at the input is avoided.

4. Delay time (t_d)

The delay time is a time that the input voltage to V_{DD} terminal exceeds the release voltage ($+V_{DET}$) and then the output of the OUT terminal inverts. The delay time can be changed by the additional external capacitor C_D.

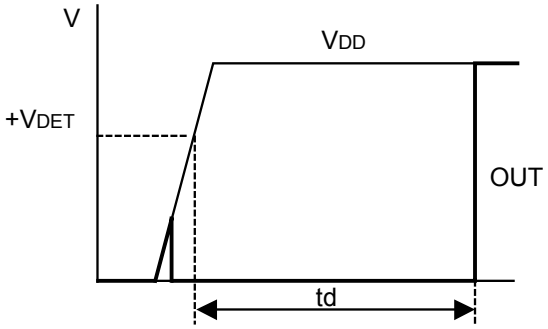


Figure 3

5. Through-type current

Through-type current refers to the current which flows instantaneously, at the time of detection and release of a voltage detector. Through-type current is large in CMOS output devices.

6. Oscillation

In applications where a resistor is connected to the voltage detector input , in the CMOS active low products for example, the through-type current generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current]×[input resistance] across the resistor. When the resultant input voltage drops below the detection voltage $-V_{DET}$, the output voltage returns to its low level. In this state, the through-type current and its resultant voltage drop have disappeared, and the output goes back from low to high. A through-type current is again generated, a voltage drop appears, and the process repeats. This unstable condition is referred to as oscillation.

■ STANDARD CIRCUIT

Connect directly the C_D capacitor for delay between C_D and Vss terminals

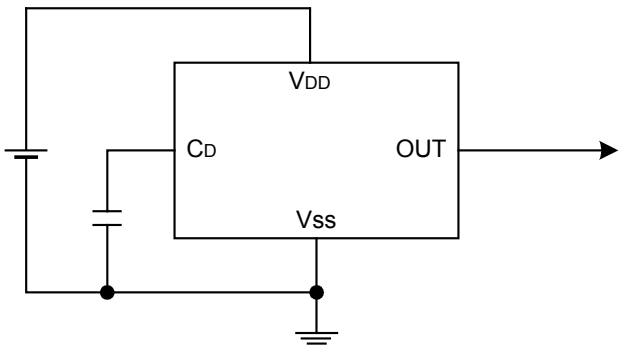


Figure 5

■ OPERATION

1. Basic operation: CMOS active low output

(1) When power supply voltage V_{DD} is greater than the release voltage $+V_{DET}$, the Nch transistor is OFF and the Pch transistor ON, causing V_{DD} (high) to appear at the output.

(2) When power supply voltage V_{DD} goes below $+V_{DET}$, the output maintains the power supply voltage level, as long as V_{DD} remains above the detection voltage $-V_{DET}$. When V_{DD} does fall below $-V_{DET}$ (A in Figure 7), the Nch transistor goes ON the Pch transistor goes OFF, and V_{SS} appears at the output.

(3) When V_{DD} falls below the minimum operating voltage, the output becomes undefined. However, output will revert to V_{DD} if a pull-up has been employed.

(4) V_{SS} will again be output when V_{DD} rises above the minimum operating voltage. V_{SS} will continue to be output even when V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When V_{DD} rises above $+V_{DET}$ (B in Figure 7), the Nch transistor goes OFF the Pch transistor goes ON, and V_{DD} appears at the output. Then V_{DD} at the OUT terminal appears with delay time (td) due to delay circuit.

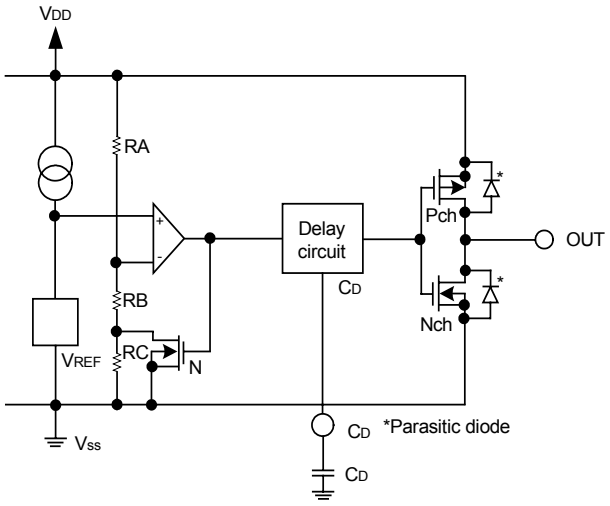


Figure 6

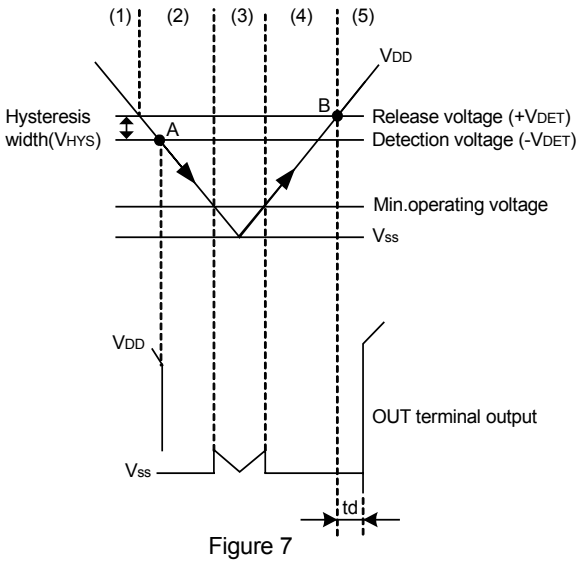


Figure 7

2. Delay circuit

The delay circuit outputs the signal delayed from the release voltage ($+V_{DET}$) point of the power voltage V_{DD} rising. The output signal is not delayed when the V_{DD} goes down the detection voltage ($-V_{DET}$) or less. (See Figure 7).

The delay time (td) is determined by the time constant of the built-in constant current (approx. 100nA in the case of products with detection voltage of 1.5V or more, approx. 570nA in the case of products with detection voltage of 1.4V or less) and the attached external capacitor (C_D), and calculated from the following formula.

td (ms) = Delay factor×C_D (nF)

Delay factor: (25℃)

Products with detection voltage of 1.4V or less: Min.0.57, Typ.0.77, Max.0.96

Products with detection voltage of 1.5V or more: Min.3.8, Typ. 5.1, Max.6.4

Cautions

*The open of C_D terminal may cause double pulses shown in Figure 8 at release. If the double pulses cause a trouble, attach 10pF or larger capacitor to the C_D terminal. Do not apply the voltage to the C_D terminal.

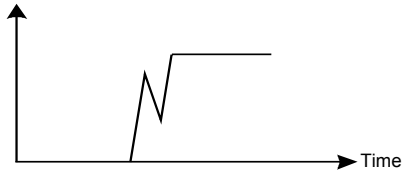


Figure 8

*Layout the print circuit board not to apply or flow out the current to/from the C_D terminal. Doing not so may cause inaccurate delay time.

*Use an external capacitor, C_D of which leakage current can be ignored for the built-in constant-current value. A leakage current may cause an error of delay time. Also, a leakage current over the built-in constant-current causes unrelease status.

3. Other characteristics

(1) Temperature characteristic of detection voltage.

The temperature characteristics of the detection voltage are expressed by the oblique line parts in Figure 9.

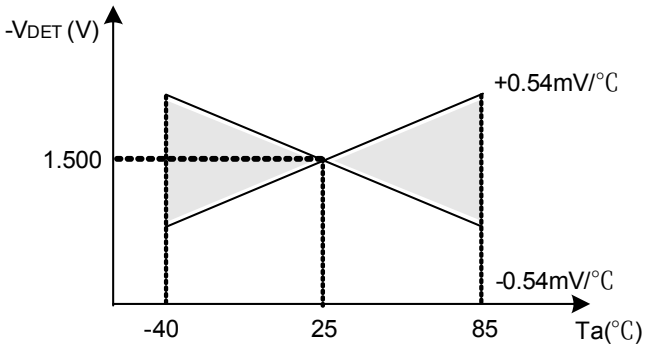


Figure 9

(2) Temperature characteristics of release voltage

The temperature factor ($\frac{\Delta +V_{DEF}}{\Delta Ta}$) of the release voltage is calculated by the temperature factor of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+ V_{DET}}{- V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature factor of the release voltage has a same sign characteristics as the temperature factor of the detection voltage.

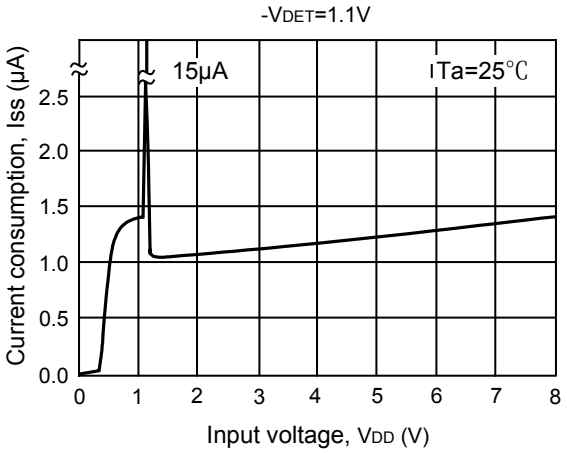
(3) Temperature characteristics of hysteresis voltage

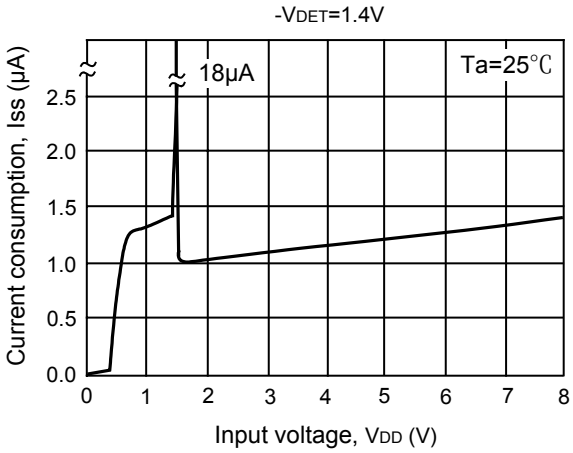
The temperature characteristics of hysteresis voltage ($\frac{\Delta +V_{DEF}}{\Delta Ta} - \frac{\Delta -V_{DEF}}{\Delta Ta}$) is calculated as follows:

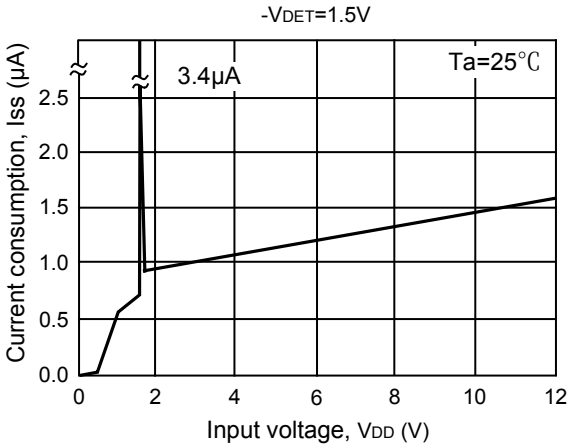
$$\frac{\Delta +V_{DET}}{\Delta Ta} - \frac{\Delta -V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta -V_{DET}}{\Delta Ta}$$

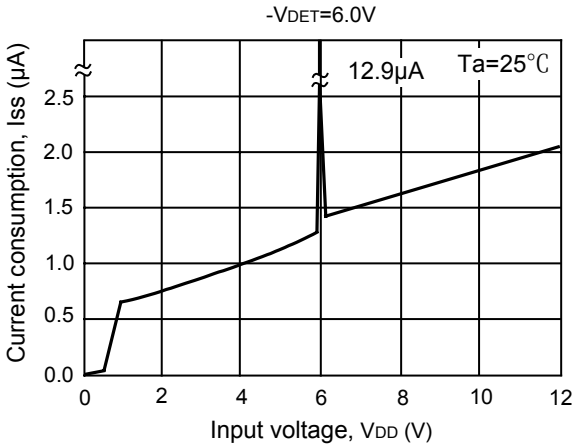
■ TYPICAL PERFORMANCE CHARACTERISTICS

(1) Current consumption – Input voltage

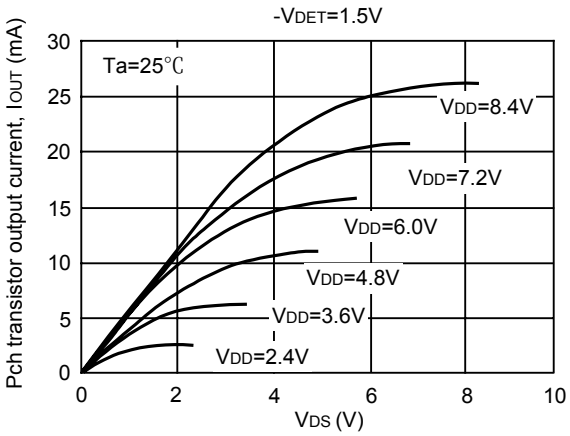






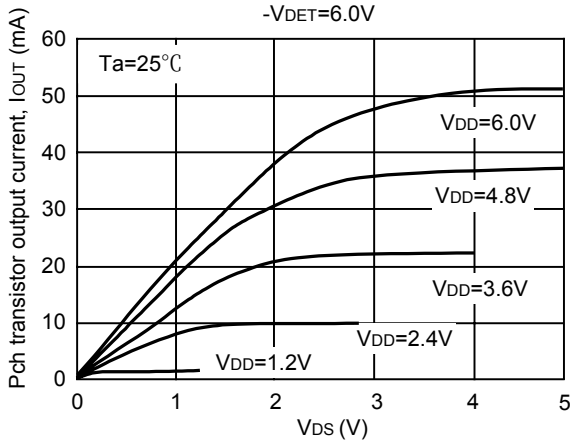


(2) Pch transistor output current - V_{DS}

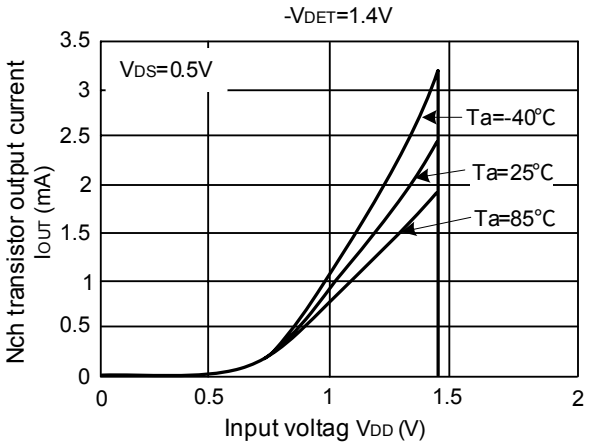


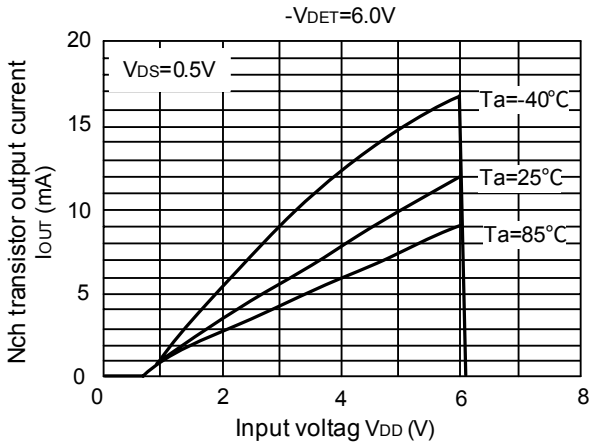
■ TYPICAL PERFORMANCE CHARACTERICS (Cont.)

(3) Nch transistor output current (I_{OUT}) – V_{DS}

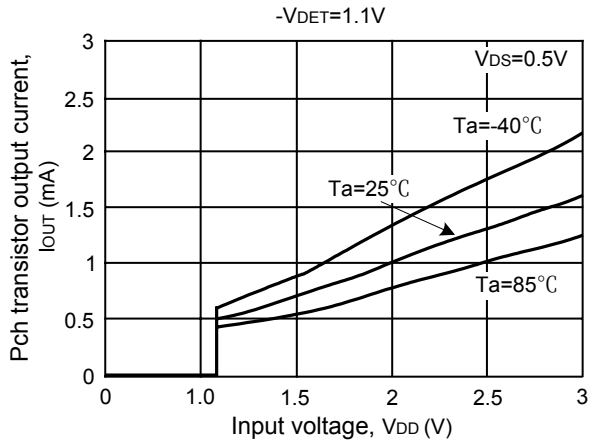


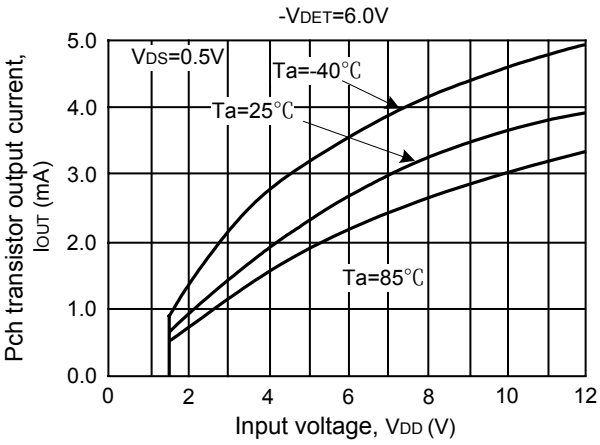
(4) Nch transistor output current – Input voltage





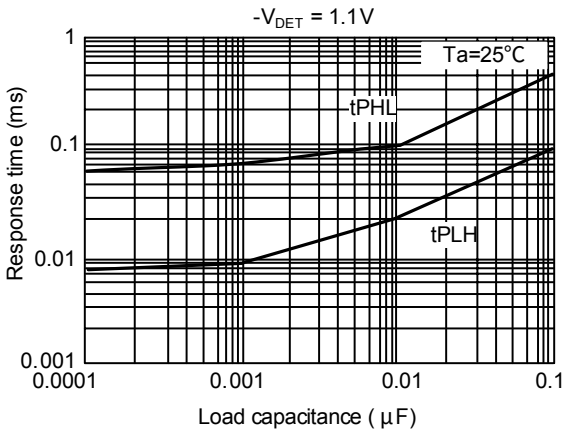
(5) Pch transistor output current– Input voltage

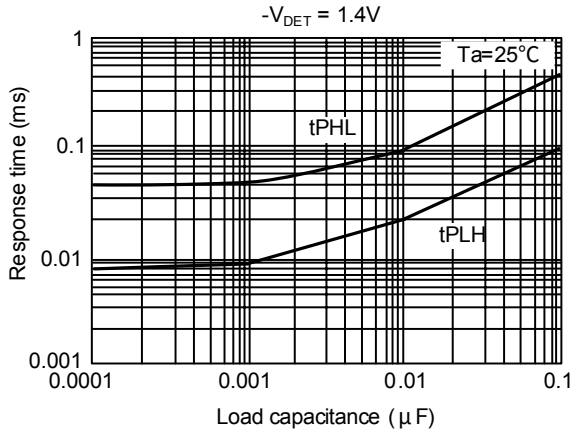


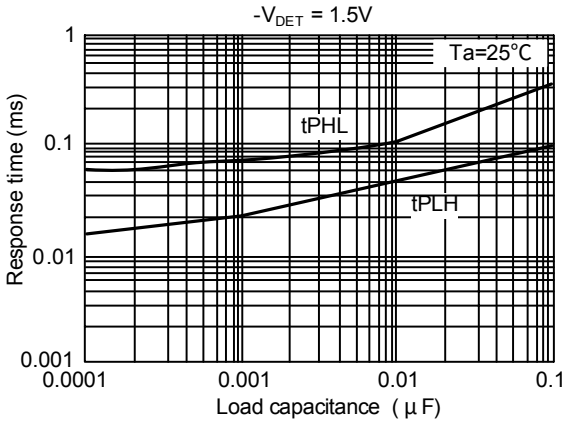


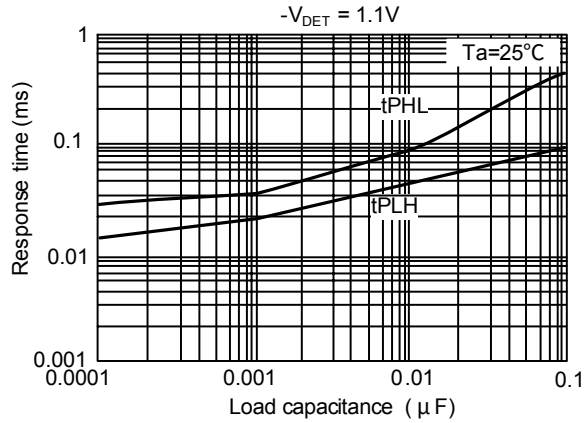
■ TYPICAL PERFORMANCE CHARACTERICS (Cont.)

(6) Dynamic response (CD : Open)









Response Time Measure Circuit