PM7381

FREEDM-32A672

REVISION C DEVICE ERRATA

ISSUE 3

December, 2001

TABLE OF CONTENTS

1.　Introduction

In this document, Section 2 lists the known functional errata for revision C of PM7381 FREEDM-32A672 and Section 3 lists errors found in Issue 6 of the FREEDM-32A672 datasheet (PMC-1990263).

1.1.　Device Identification

The information contained in Section 2 relates to Revision C of PM7381 FREEDM-32A672 only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1.1). PM7381 FREEDM-32A672 Revision C is packaged in a 329-pin Plastic Ball Grid Array (PBGA).

Figure 1.1: PM7381 FREEDM-32A672 Branding Format.

Not to Scale
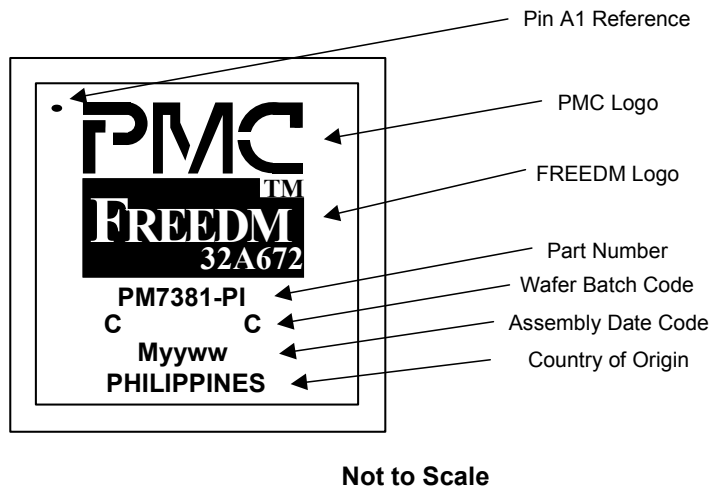
1.2.　Reference

• 　PMC-1990263, FREEDM-32A672 Long Form Data Sheet, Issue 6.

2.　FREEDM-32A672 Revision C Functional Deficiency List

This section lists the known functional deficiencies for Revision C of FREEDM-32A672 (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

2.1. Following recovery from receive FIFO overrun events, truncated data transfers may occur on the receive Any-PHY bus.

Description:

When outputting packets on the receive Any-PHY bus, the FREEDM-32A672 will normally transfer bursts of data containing ((XFER+1)*16) bytes, where XFER is a value between 0 and 15 configurable on a per-channel basis, or alternatively, bursts of data containing fewer bytes but including an end of packet. The Any-PHY interface is intended to operate in such a manner at all times, so that a downstream device may assume that any data transfer, in which REOP is not asserted is of a fixed length.

Following a receive FIFO overrun, however, the FREEDM-32A672 implements an automatic FIFO healing mechanism. As a consequence of this mechanism, the FREEDM-32A672 may output a burst of data containing (n*16) bytes of data, where n is less than (XFER+1), but which does not include an end of packet.

Workarounds:

There are 4 possible independent workarounds:

i)   Set the receive path XFER to 0. All transfers not containing an end of packet will then be 16 bytes and thus of constant length. This workaround may not be suitable in high bandwidth systems, especially if multple FREEDM-32A672s are sharing an Any-PHY bus.

ii)   Attach a pull-down resistor to the RVAL output and monitor this signal to detect truncated data transfers.

iii)   Attach a pull-up resistor to the RERR output and monitor this signal to detect truncated data transfers. RERR is always logic 0 when the FREEDM-32A672 is outputting data on the Any-PHY bus, except when REOP is asserted. If a pull-up resistor is attached to RERR, a truncated transfer will be indicated by RERR = 1 and REOP = 0. The downstream device can the take appropriate action such as discarding the packet.

iv)   Attach pull-down or pull-up resistors to the RXDATA[15:0] outputs and a pull-down resistor to the RXPRTY output. If the FREEDM-32A672 outputs a truncated burst of data and the downstream device is not monitoring RVAL and is expecting a fixed length burst of data, the downstream device will observe parity errors and can take appropriate action such as discarding the packet.

Performance with workaround:

FREEDM-32A672 operates correctly.

Performance without workaround:

The downstream device may sample invalid packet data.

3. Documentation Errors

This section lists the known documentation errors in Issue 6 of PMC-1990263 FREEDM-32A672 Datasheet (as of the publication date of this document).

Please report any documentation errors not covered in this document to PMC-Sierra.

3.1. PROV and DELIN bits in Register 0x204 are Write-Only

PROV and DELIN bits in Register 0x204 are write-only and not read/write. Changes to the register table are shown below.

Register 0x204 : RHDL Indirect Channel Data Register #1

Bit	Type	Function	Default
Bit 15	R/W **W**	PROV	0
Bit 14	R/W	STRIP	0
Bit 13	R/W **W**	DELIN	0
Bit 12	R	TAVAIL	X
Bit 11	W	Reserved	X
Bit 10	W	FPTR[10]	X
Bit 9	W	FPTR[9]	X
Bit 8	W	FPTR[8]	X
Bit 7	W	FPTR[7]	X
Bit 6	W	FPTR[6]	X
Bit 5	W	FPTR[5]	X
Bit 4	W	FPTR[4]	X
Bit 3	W	FPTR[3]	X
Bit 2	W	FPTR[2]	X
Bit 1	W	FPTR[1]	X
Bit 0	W	FPTR[0]	X

3.2. 7BIT, INVERT, CRC[1], and CRC[0] bits in Register 0x208 are Write-Only

7BIT, INVERT, CRC[1], and CRC[0] bits in Register 0x208 are write-only and not read/write. Changes to the register table are shown below.

Register 0x208 : RHDL Indirect Channel Data Register #2

Bit	Type	Function	Default
Bit 15	~~R/W~~ **W**	7BIT	0
Bit 14	R/W	PRIORITY	0
Bit 13	~~R/W~~ **W**	INVERT	0
Bit 12		Unused	X
Bit 11	~~R/W~~ **W**	CRC[1]	0
Bit 10	~~R/W~~ **W**	CRC[0]	0
Bit 9	R/W	OFFSET[1]	0
Bit 8	R/W	OFFSET[0]	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	XFER[3]	0
Bit 2	R/W	XFER[2]	0
Bit 1	R/W	XFER[1]	0
Bit 0	R/W	XFER[0]	0

4.   Contacting PMC-Sierra

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NOTES

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