



CYPRESS

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CY7C374

UltraLogic™ 128-Macrocell Flash CPLD

Features

- 128 macrocells in eight logic blocks
- 64 I/O pins
- 6 dedicated inputs including 4 clock pins
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
 - $f_{MAX} = 100$ MHz
 - $t_{PD} = 12$ ns
 - $t_S = 6$ ns
 - $t_{CO} = 7$ ns
- Electrically Alterable Flash technology
- Available in 84-pin PLCC, 84-pin CLCC, 100-pin TQFP, and 84-pin PGA packages
- Pin compatible with the CY7C373

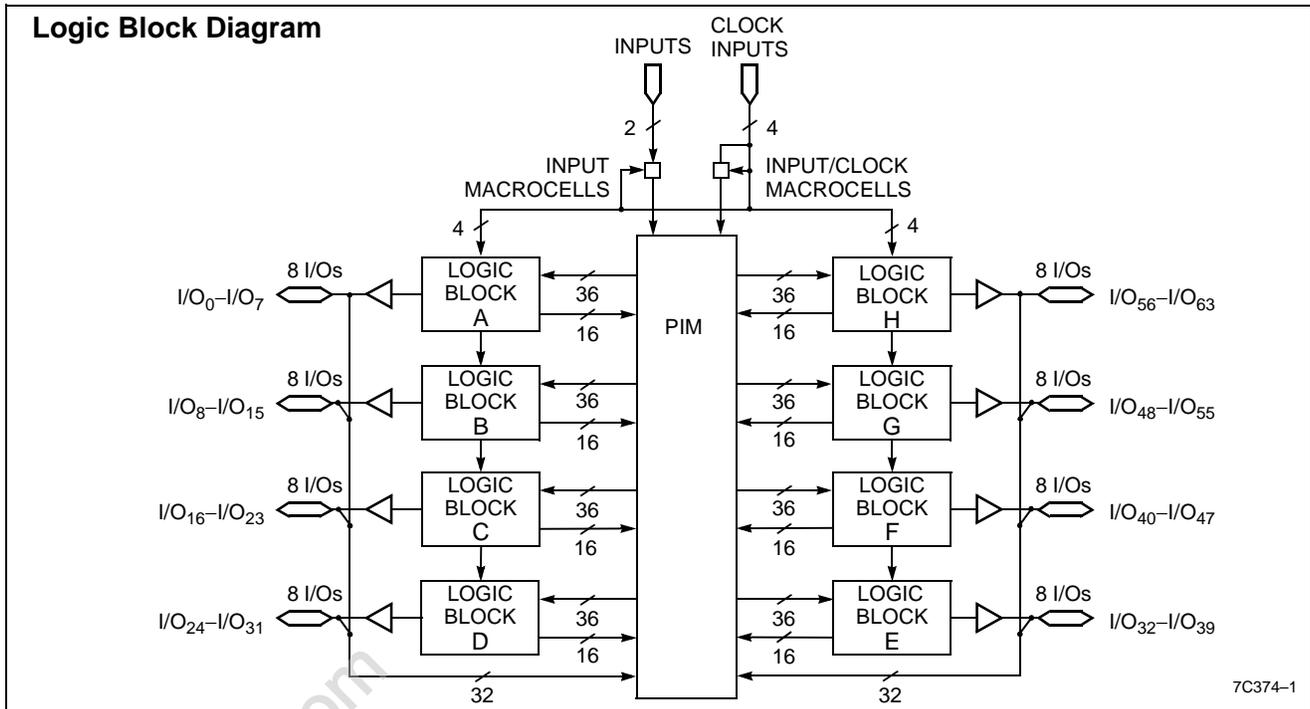
Functional Description

The CY7C374 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C374 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 128 macrocells in the CY7C374 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

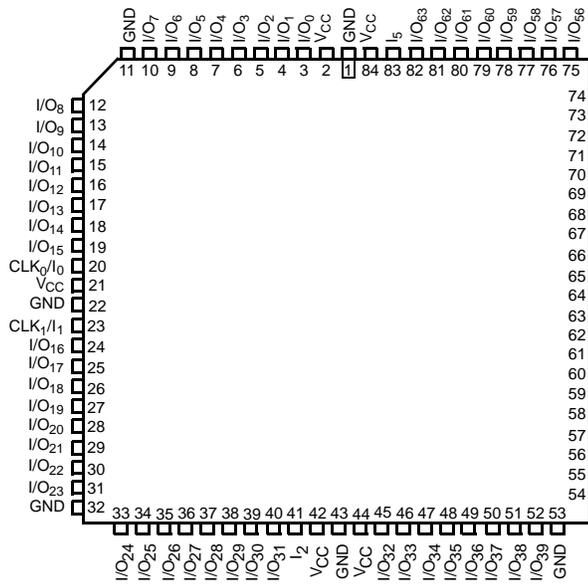
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

The CY7C374 is a register intensive 128-Macrocell CPLD. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374. In addition, there are two dedicated inputs and four input/clock pins.

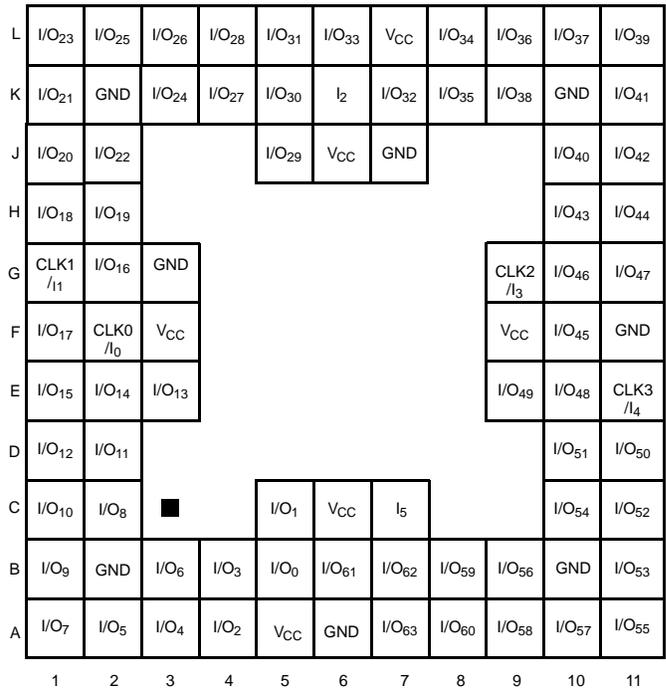


Selection Guide

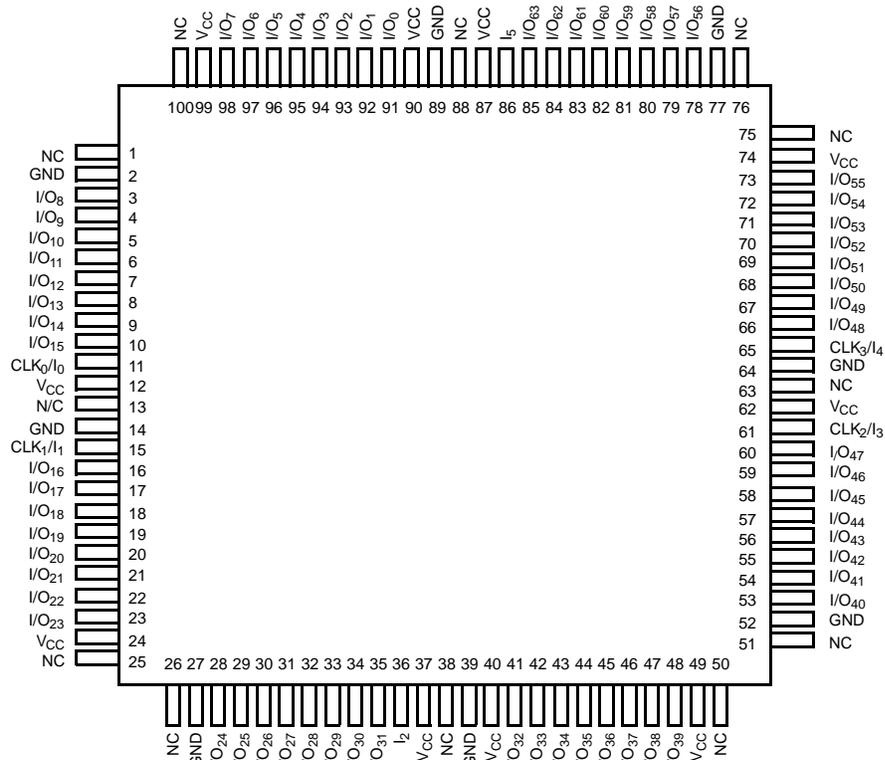
| | | 7C374-100 | 7C374-83 | 7C374-66 | 7C374L-66 |
|---|---------------------|-----------|----------|----------|-----------|
| Maximum Propagation Delay t_{PD} (ns) | | 12 | 15 | 20 | 20 |
| Minimum Set-Up, t_S (ns) | | 6 | 8 | 10 | 10 |
| Maximum Clock to Output, t_{CO} (ns) | | 7 | 8 | 10 | 10 |
| Maximum Supply Current, I_{CC} (mA) | Commercial | 300 | 300 | 300 | 150 |
| | Military/Industrial | | 370 | 370 | |

Pin Configurations
**PLCC/CLCC
Top View**


7C374-2

**PGA
Bottom View**


7C374-3

**TQFP
Top View**


7C374-4

Functional Description (continued)

Finally, the CY7C374 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374 remain the same.

Logic Block

The number and configuration of logic blocks distinguishes the members of the FLASH370 family. The CY7C374 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block receives 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374 have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two

global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is to be used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

A feature called bus-hold has been added to all FLASH370 I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Development Tools

Development software for the CY7C374 is available from Cypress's *Warp*™ software packages. Both of these products are based on IEEE standard 1076/1164 VHDL. Cypress CPLDs are also supported by a number of third-party vendors such as ABEL™, CUPL™, and LOG/iC™. Please refer to third-party tool support data sheets for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied..... | -55°C to +125°C |
| Supply Voltage to Ground Potential | -0.5V to +7.0V |
| DC Voltage Applied to Outputs in High Z State..... | -0.5V to +7.0V |
| DC Input Voltage | -0.5V to +7.0V |
| DC Program Voltage..... | 12.5V |

| | |
|-----------------------------------|---------------------------------------|
| Output Current into Outputs | 16 mA |
| Static Discharge Voltage | >2001V (per MIL-STD-883, Method 3015) |
| Latch-Up Current..... | >200 mA |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 5% |
| Industrial | -40°C to +85°C | 5V ± 5% |
| Military ^[1] | -55°C to +125°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range^[2]

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------------|--|--|---------------|------|---------------------------------|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min. I _{OH} = -3.2 mA (Com'l/Ind) | 2.4 | | V |
| | | | | | I _{OH} = -2.0 mA (Mil) |
| V _{OL} | Output LOW Voltage | V _{CC} = Min. I _{OL} = 16 mA (Com'l/Ind) | | 0.5 | V |
| | | | | | I _{OL} = 12 mA (Mil) |
| V _{IH} | Input HIGH Voltage | Guaranteed Input Logical HIGH voltage for all inputs ^[3] | 2.0 | 7.0 | V |
| V _{IL} | Input LOW Voltage | Guaranteed Input Logical LOW voltage for all inputs ^[3] | -0.5 | 0.8 | V |
| I _{Ix} | Input Load Current | V _I = Internal GND, V _I = V _{CC} | -10 | +10 | µA |
| I _{OZ} | Output Leakage Current | V _o = Internal GND, V _o = V _{CC} | -50 | +50 | µA |
| I _{OS} | Output Short Circuit Current ^[4, 5] | V _{CC} = Max., V _{OUT} = 0.5V | -30 | -160 | mA |
| I _{CC} | Power Supply Current ^[6] | V _{CC} = Max., I _{OUT} = 0 mA f = 1 MHz, V _{IN} = GND, V _{CC} | Com'l | 300 | mA |
| | | | Com'l "L" -66 | 150 | mA |
| | | | Mil./Ind. | 370 | mA |

Shaded area contains preliminary information.

Capacitance^[5]

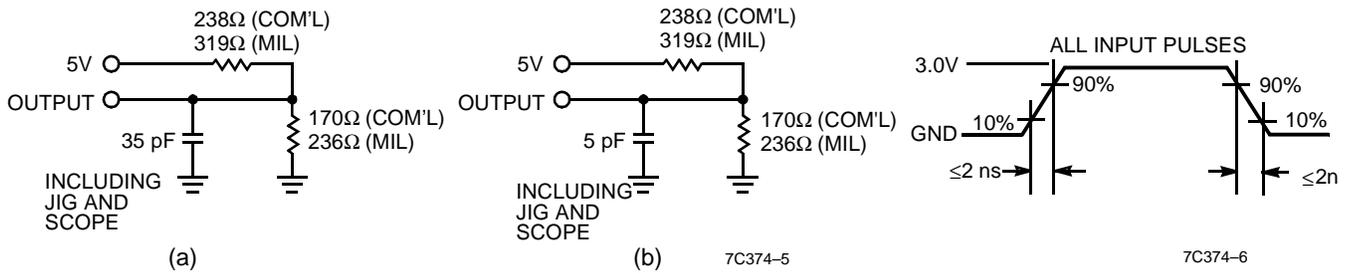
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------------------------|-------------------|-----------------------------------|------|------|
| C _{I/O} ^[7, 8] | Input Capacitance | V _{IN} = 5.0V at f=1 MHz | 10 | pF |

Endurance Characteristics^[5]

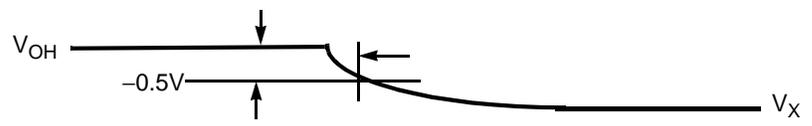
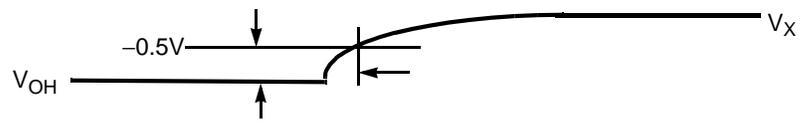
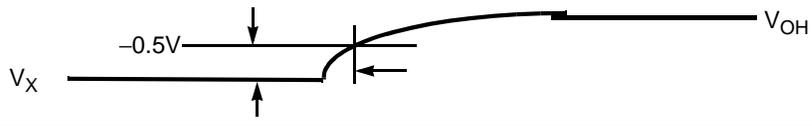
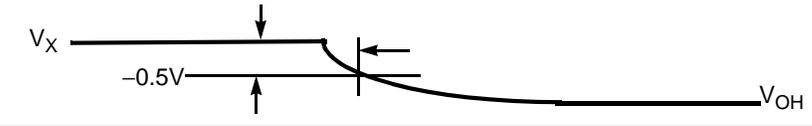
| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------|------------------------------|-------------------------------|------|------|--------|
| N | Minimum Reprogramming Cycles | Normal Programming Conditions | 100 | | Cycles |

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Measured with 16-bit counter programmed into each logic block.
7. C_{I/O} for the CLCC and CPGA packages is 15 pF max.
8. C_{I/O} for I₅ is 15 pF max

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT
 99Ω (COM'L), 136Ω (MIL) in series with 2.08V (COM'L), 2.13V (MIL) in parallel with output.

| Parameter ^[9] | V _X | Output Waveform Measurement Level |
|--------------------------|------------------|--|
| t _{ER(-)} | 1.5V |  |
| t _{ER(+)} | 2.6V |  |
| t _{EA(+)} | 1.5V |  |
| t _{EA(-)} | V _{thc} |  |

Note:

9. t_{ER} is measured with 5-pF AC Test Load and t_{EA} is measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range^[10]

| Parameter | Description | 7C374-100 | | 7C374-83 | | 7C374-66 7C374L-66 | | Unit |
|--|---|-----------|------|----------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Combinatorial Mode Parameters | | | | | | | | |
| t _{PD} | Input to Combinatorial Output | | 12 | | 15 | | 20 | ns |
| t _{PDL} | Input to Output Through Transparent Input or Output Latch | | 15 | | 18 | | 22 | ns |
| t _{PDLL} | Input to Output Through Transparent Input and Output Latches | | 16 | | 19 | | 24 | ns |
| t _{EA} | Input to Output Enable | | 16 | | 19 | | 24 | ns |
| t _{ER} | Input to Output Disable | | 16 | | 19 | | 24 | ns |
| Input Registered/Latched Mode Parameters | | | | | | | | |
| t _{WL} | Clock or Latch Enable Input LOW Time ^[5] | 3 | | 4 | | 5 | | ns |
| t _{WH} | Clock or Latch Enable Input HIGH Time ^[5] | 3 | | 4 | | 5 | | ns |
| t _{IS} | Input Register or Latch Set-Up Time | 2 | | 3 | | 4 | | ns |
| t _{IH} | Input Register or Latch Hold Time | 2 | | 3 | | 4 | | ns |
| t _{ICO} | Input Register Clock or Latch Enable to Combinatorial Output | | 16 | | 19 | | 24 | ns |
| t _{ICOL} | Input Register Clock or Latch Enable to Output Through Transparent Output Latch | | 18 | | 21 | | 26 | ns |
| Output Registered/Latched Mode Parameters | | | | | | | | |
| t _{CO} | Clock or Latch Enable to Output | | 7 | | 8 | | 10 | ns |
| t _S | Set-Up Time from Input to Clock or Latch Enable | 6 | | 8 | | 10 | | ns |
| t _H | Register or Latch Data Hold Time | 0 | | 0 | | 0 | | ns |
| t _{CO2} | Output Clock or Latch Enable to Output Delay (Through Memory Array) | | 16 | | 19 | | 24 | ns |
| t _{SCS} | Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array) | 10 | | 12 | | 15 | | ns |
| t _{SL} | Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable | 12 | | 15 | | 20 | | ns |
| t _{HL} | Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable | 0 | | 0 | | 0 | | ns |
| f _{MAX1} | Maximum Frequency with Internal Feedback (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[5] | 100 | | 83 | | 66 | | MHz |
| f _{MAX2} | Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO}) | 143 | | 125 | | 100 | | MHz |
| f _{MAX3} | Maximum Frequency with External Feedback (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH})) | 76.9 | | 67.5 | | 50 | | MHz |
| t _{OH} -t _{IH} 37x | Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x ^[5, 11] | 0 | | 0 | | 0 | | ns |
| Pipelined Mode Parameters | | | | | | | | |
| t _{ICS} | Input Register Clock to Output Register Clock | 10 | | 12 | | 15 | | ns |
| f _{MAX4} | Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _S), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{SCS}) | 100 | | 83.3 | | 66.6 | | MHz |

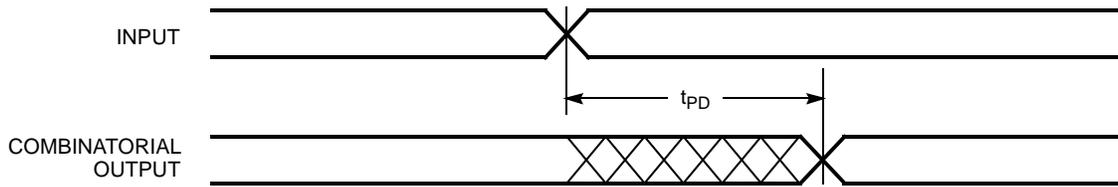
Switching Characteristics Over the Operating Range^[10] (continued)

| Parameter | Description | 7C374-100 | | 7C374-83 | | 7C374-66 7C374L-66 | | Unit |
|--------------------------------|--|-----------|------|----------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Reset/Preset Parameters | | | | | | | | |
| t _{RW} | Asynchronous Reset Width ^[5] | 12 | | 15 | | 20 | | ns |
| t _{RR} | Asynchronous Reset Recovery Time ^[5] | 14 | | 17 | | 22 | | ns |
| t _{RO} | Asynchronous Reset to Output | | 18 | | 21 | | 26 | ns |
| t _{PW} | Asynchronous Preset Width ^[5] | 12 | | 15 | | 20 | | ns |
| t _{PR} | Asynchronous Preset Recovery Time ^[5] | 14 | | 17 | | 22 | | ns |
| t _{PO} | Asynchronous Preset to Output | | 18 | | 21 | | 26 | ns |

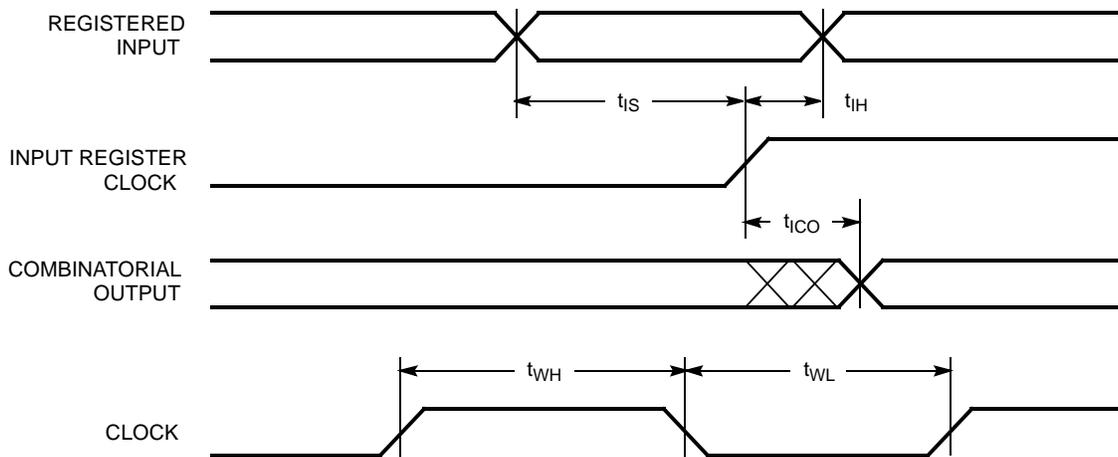
Notes:

10. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

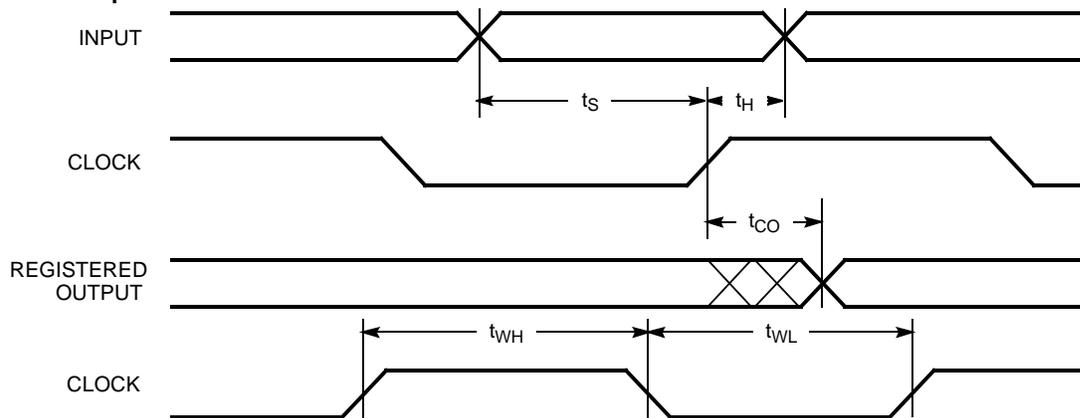
11. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C374. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Waveforms
Combinatorial Output


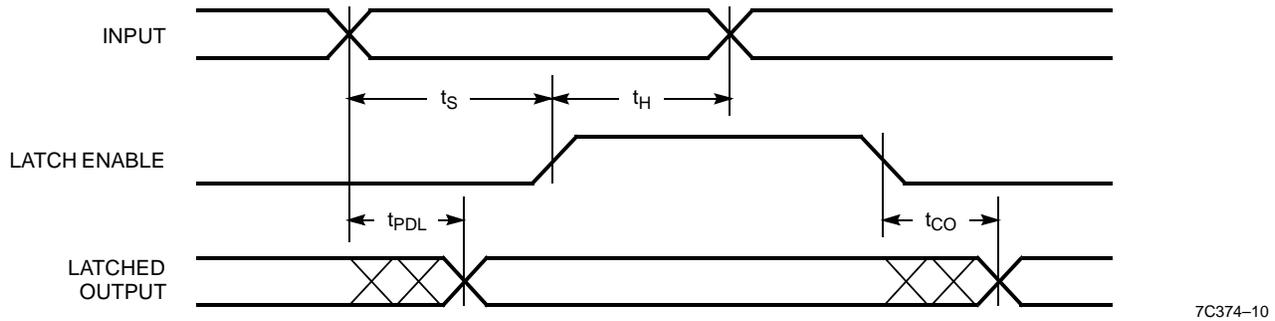
7C374-7

Registered Input


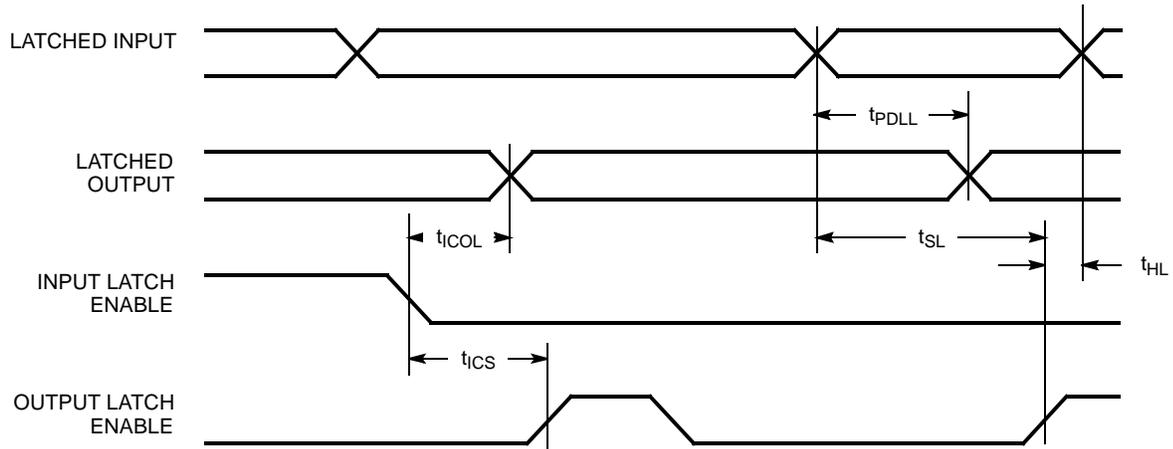
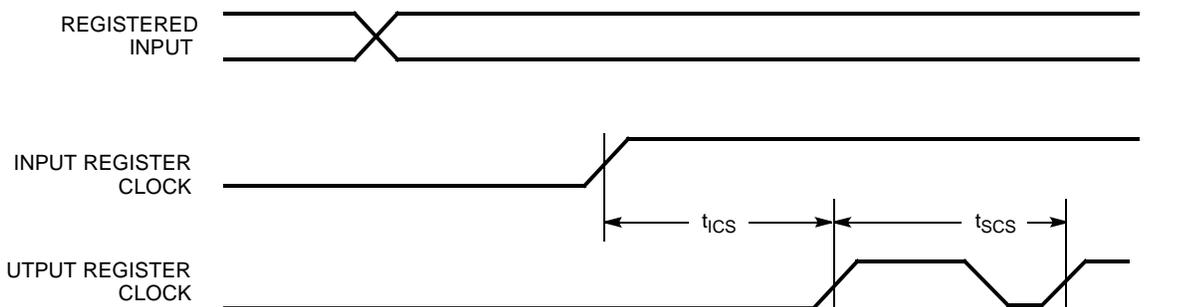
7C374-8

Registered Output


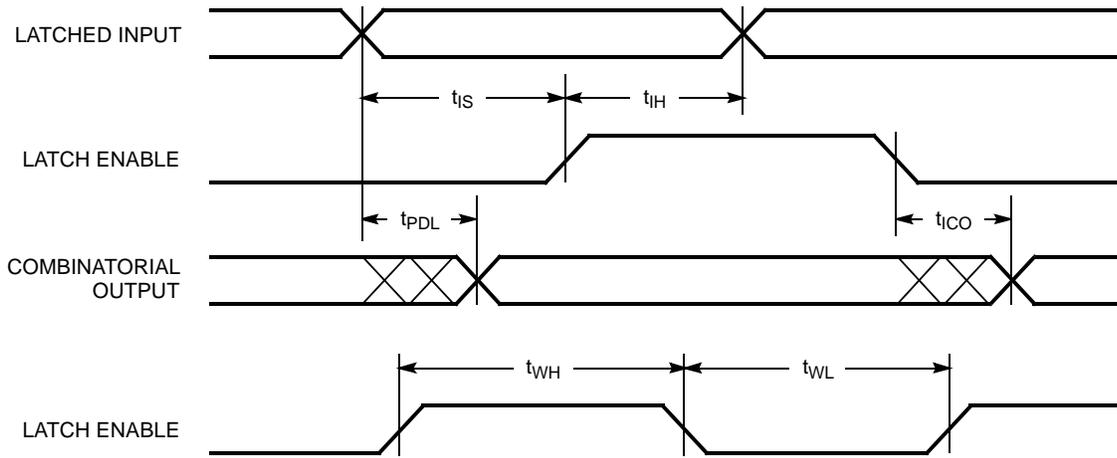
7C374-9

Switching Waveforms (continued)
Latched Output


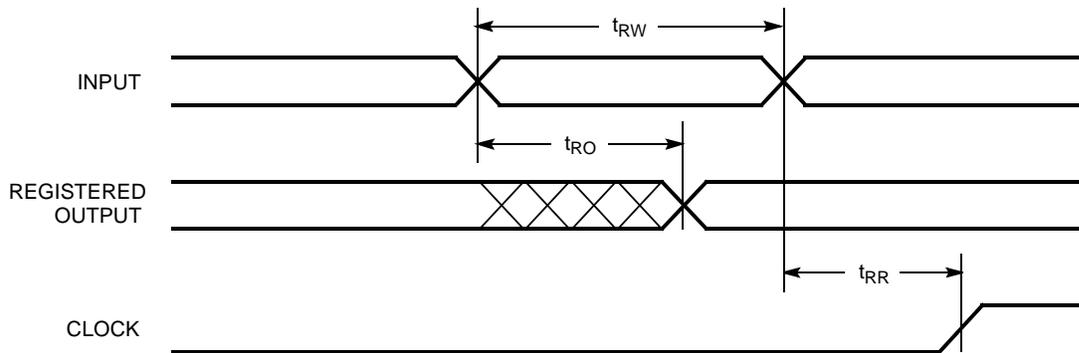
7C374-10

Latched Input and Output

Clock to Clock


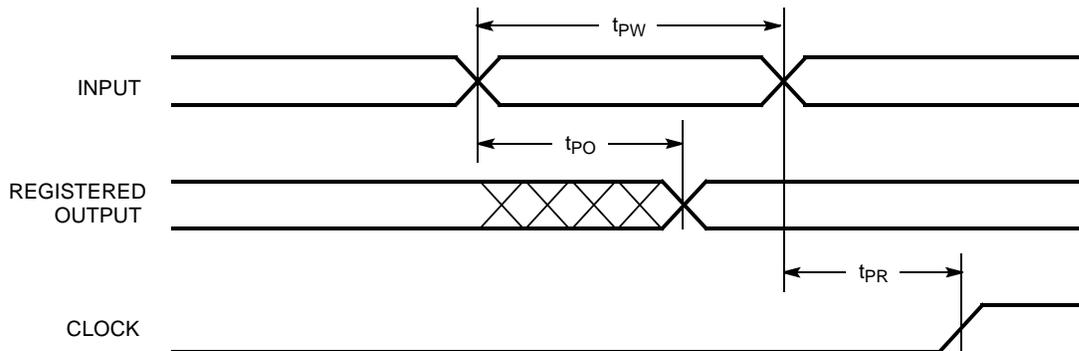
7C374-12

Switching Waveforms (continued)
Latched Input


7C374-13

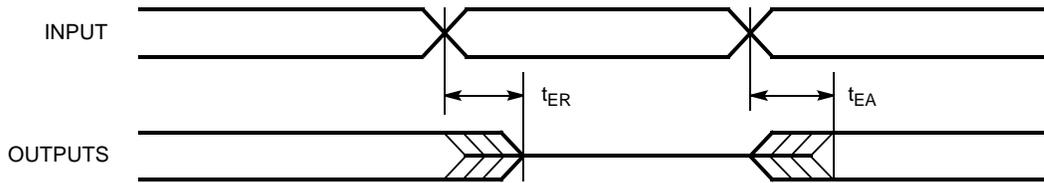
Asynchronous Reset


7C374-14

Asynchronous Preset


7C374-15

Switching Waveforms (continued)

Output Enable/Disable


7C374-17

Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------|---------------|--------------|-------------------------------------|-----------------|
| 100 | CY7C374-100AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C374-100GC | G84 | 84-Pin Grid Array (Cavity Up) | |
| | CY7C374-100JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| 83 | CY7C374-83AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C374-83GC | G84 | 84-Pin Grid Array (Cavity Up) | |
| | CY7C374-83JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C374-83AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C374-83JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C374-83GMB | G84 | 84-Pin Grid Array (Cavity Up) | Military |
| | CY7C374-83YMB | Y84 | 84-Pin Ceramic Leaded Chip Carrier | |
| 66 | CY7C374-66AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C374-66GC | G84 | 84-Pin Grid Array (Cavity Up) | |
| | CY7C374-66JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C374-66AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C374-66JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C374-66GMB | G84 | 84-Pin Grid Array (Cavity Up) | Military |
| | CY7C374-66YMB | Y84 | 84-Pin Ceramic Leaded Chip Carrier | |
| | CY7C374L-66AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C374L-66JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**
DC Characteristics

| Parameter | Subgroups |
|-----------|-----------|
| V_{OH} | 1, 2, 3 |
| V_{OL} | 1, 2, 3 |
| V_{IH} | 1, 2, 3 |
| V_{IL} | 1, 2, 3 |
| I_{IX} | 1, 2, 3 |
| I_{OZ} | 1, 2, 3 |
| I_{CC1} | 1, 2, 3 |

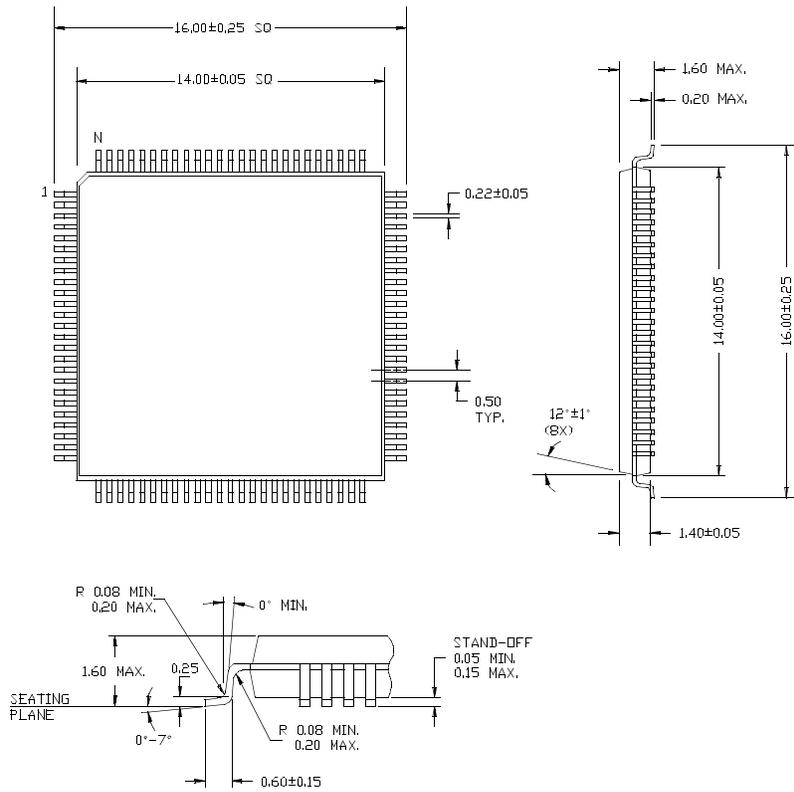
Switching Characteristics

| Parameter | Subgroups |
|------------|-----------|
| t_{PD} | 9, 10, 11 |
| t_{PDL} | 9, 10, 11 |
| t_{PDLL} | 9, 10, 11 |
| t_{CO} | 9, 10, 11 |
| t_{ICO} | 9, 10, 11 |
| t_{ICOL} | 9, 10, 11 |
| t_S | 9, 10, 11 |
| t_{SL} | 9, 10, 11 |
| t_H | 9, 10, 11 |
| t_{HL} | 9, 10, 11 |
| t_{IS} | 9, 10, 11 |
| t_{IH} | 9, 10, 11 |
| t_{ICS} | 9, 10, 11 |
| t_{EA} | 9, 10, 11 |
| t_{ER} | 9, 10, 11 |

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 CUPL is a trademark of Logical Devices Incorporated.
 LOG/iC is a trademark of Isdata Corporation.

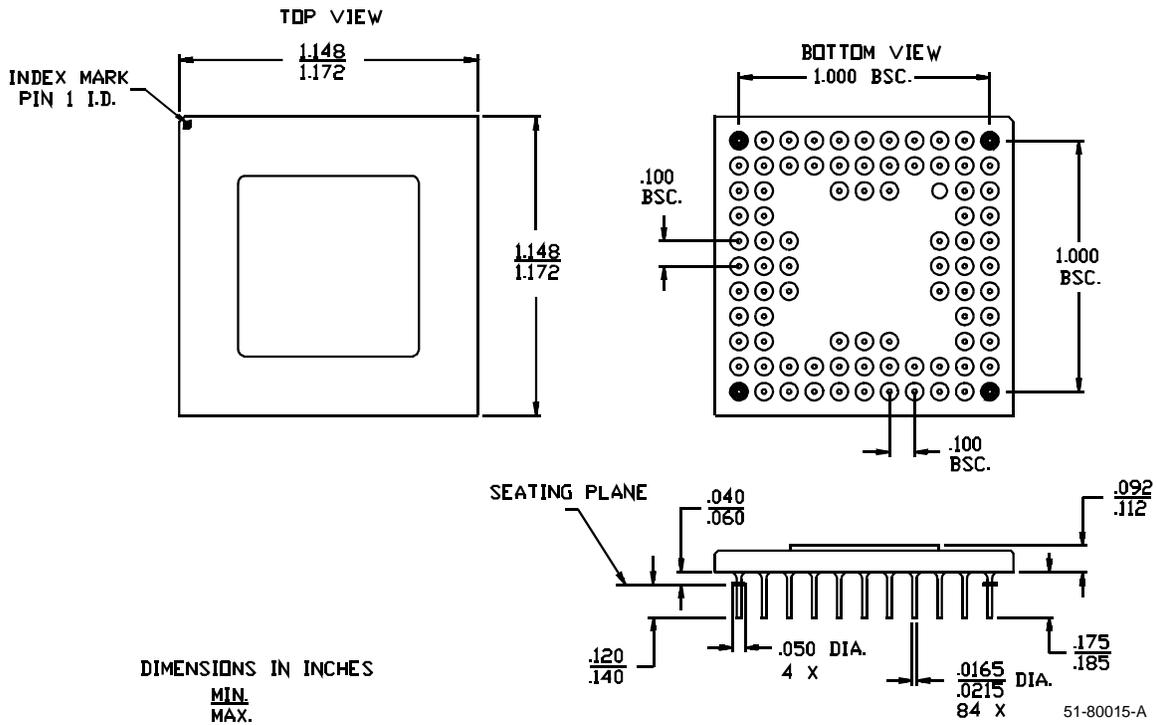
Package Diagrams

100-Pin Thin Quad Flat Pack A100

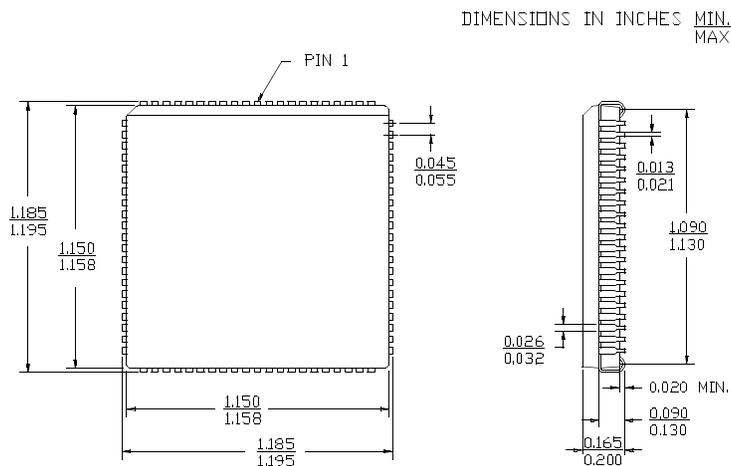


Package Diagrams (continued)

84-Pin Grid Array (Cavity Up) G84

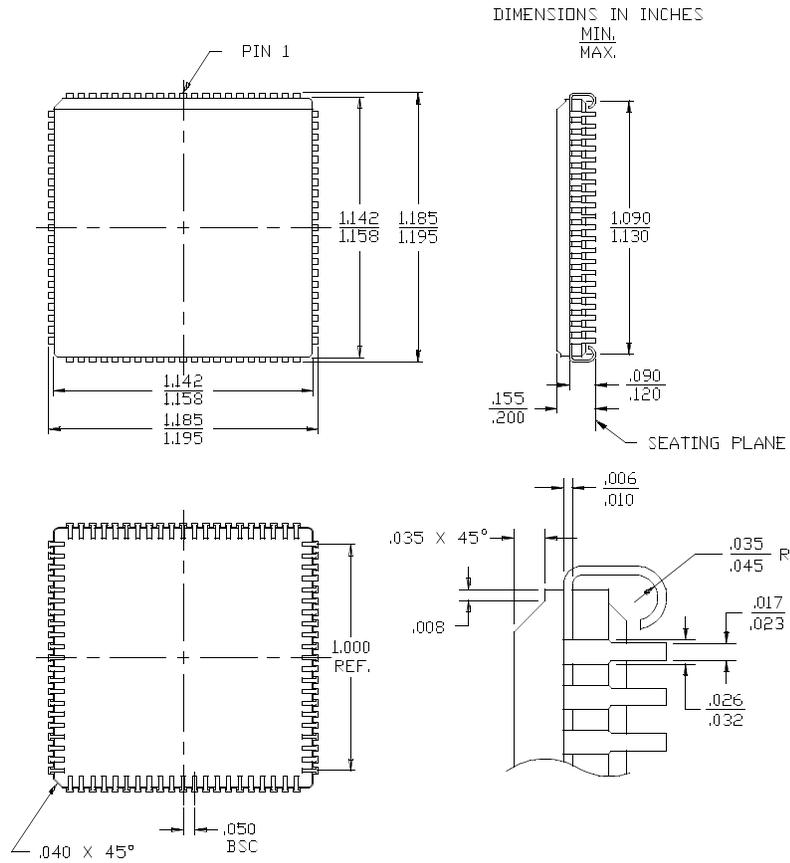


84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

84-pin Ceramic Leaded Chip Carrier Y84



Document Title: CY7C374 UltraLogic™ 128-Macrocell Flash CPLD
Document Number: 38-03021

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|------|---------|------------|-----------------|---|
| ** | 106324 | 05/08/01 | SZV | Transferred from Spec number: 38-00214 to 38-03021. |