

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

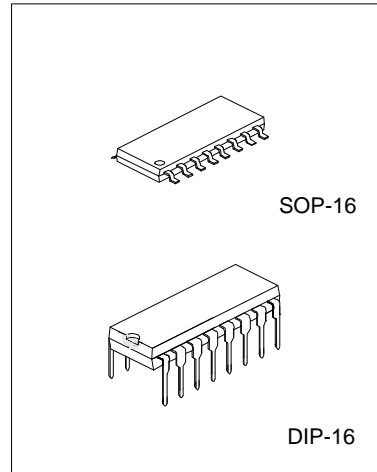
LOW VOLTAGE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

DESCRIPTION

The UTC TEA1062/1062A is a bipolar integrated circuit performing all speech and line interface function, required in the fully electronic telephone sets. It performs electronic switching between dialing speech. The circuit is able to operate down to D.C. line voltage of 1.6V (with reduced performance) to facilitate the use of more telephone sets in parallel.

FEATURES

- * Low d.c. line voltage; operates down to 1.6V (excluding polarity guard).
- *Voltage regulator with adjustment static resistance.
- *Provides supply with limited current for external circuitry.
- *Symmetrical high-impedance inputs (64k Ω)for dynamic, magnetic or piezoelectric microphones.
- *Asymmetrical high-impedance inputs (32k Ω)for electret microphones.
- *DTMF signal input with confidence tone.
- *Mute input for pulse or DTMF dialing.
- *Receiving amplifier for several types of earphones.
- *Large amplification setting range on microphone and earpiece amplifiers.
- *Line loss compensation facility, line current dependant (microphone and earpiece amplifiers).
- *Gain control adaptable to exchange supply.
- *Possibility to adjust the d.c. line voltage.



QUICK REFERENCE DATA

Line voltage at $I_{line}=15mA$	V _{LN}	typ. 3.8 V
Line current operating range[$pin1$] normal operation	I_{line}	11 to 140 mA
with reduced performance	I_{line}	1 to 11 mA
Internal supply current	I _{CC}	typ. 1mA
Supply current for peripherals at $I_{line}=15 mA$ MUTE input LOW(1062 is HIGH) V _{CC} >2.2V	I_p	typ. 1.8mA
V _{CC} >2.8V	I_p	typ. 0.7mA
Voltage amplification range microphone amplifier	AVD	44 to 52 dB
receiving amplifier	AVD	20 to 39 dB
Line loss compensation	AVD	typ. 6 dB
Amplification control range	V _{exch}	36 to 60V
Exchange supply voltage range	R _{exch}	400 to 100 Ω
Exchange feeding bridge resistance range	T _{amb}	-25 to +75°C
Operating ambient temperature range		

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

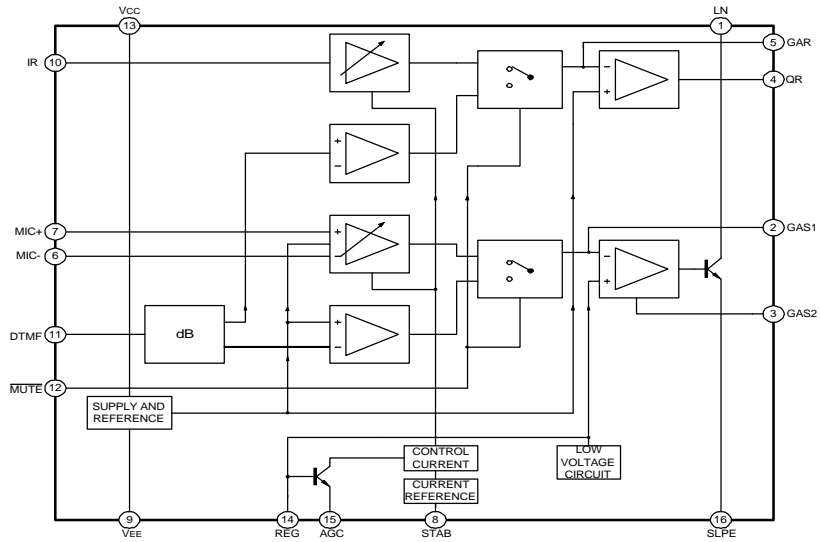


Fig.1 Block Diagram

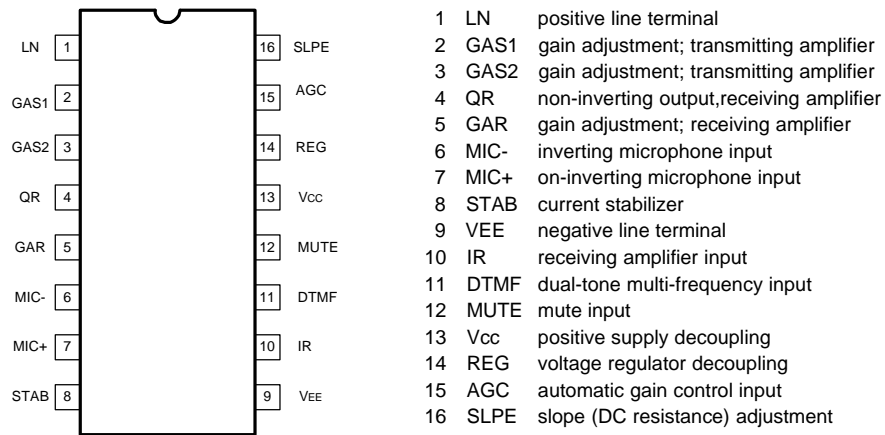


Fig.2 PIN CONFIGURATIONS

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
Positive Continuous Line Voltage		VLN		12	V
Repetitive Line Voltage During Switch-On Or Line Interruption		VLN		13.2	V
Repetitive Peak Line Voltage for a 1 ms Pulse/5s	R10=13Ω R9=20Ω (see Fig.15)	VLN		28	V
Line Current (1)	R9=20Ω	Iline		140	mA
Voltage on All Other Pins		Vi -Vi		VCC+0.7 0.7	V V
Total Power Dissipation(2)	R9=20Ω	Ptot		640	mW
Storage Temperature Range		Tstg	-40	+125	°C
Operating Ambient Temperature Range		Tamb	-25	+75	°C
Junction Temperature		Tj		+125	°C

1. Mostly dependent on the maximum required Tamb and the voltage between LN and SLPE (see Figs 6).

2. Calculated for the maximum ambient temperature specified Tamb=75°C and a maximum junction temperature of 125°C.

THERMAL RESISTANCE

From junction to ambient in free air Rth j-a = 75K/W

ELECTRICAL CHARACTERISTICS(Iline=11 to 140mA;V_{EE}=0V;f=800Hz;Tamb=25°C; unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Supply; LN and VCC(pins 1 and 13)						
Voltage Drop Over Circuit, between LN and VEE	MIC inputs open					
	Iline=1mA	VLN		1.6		V
	Iline=4mA	VLN		1.9		V
	Iline=15mA	VLN	3.55	4.0	4.25	V
	Iline=100mA	VLN	4.9	5.7	6.5	V
	Iline=140mA	VLN			7.5	V
Variation with Temperature	Iline=15mA	ΔVLN/ΔT		-0.3		mV/K
Voltage Drop Over Circuit, between LN and VEE with External Resistor RVA	Iline=15mA RVA(LN to REG) =68kΩ			3.5		V
	Iline=15mA RVA(REG to SLPE) =39kΩ			4.5		V
Supply Current	VCC=2.8V	Icc		0.9	1.35	mA
Supply Voltage Available for Peripheral Circuitry	TEA1062 Iline=15mA Ip=1.2mA;MUTE=HIGH	VCC	2.2	2.7		V
	TEA1062A Ip=0mA;MUTE=HIGH	VCC		3.4		V
	TEA1062 Ip=1.2mA;MUTE=LOW	VCC	2.2	2.7		V
	TEA1062A Ip=0mA;MUTE=LOW	VCC		3.4		V

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Microphone inputs MIC+ and MIC- (pins 6 and 7)						
Input impedance (differential) between MIC- and MIC+		Z_{in}		64		k Ω
Input impedance (single-ended) MIC- or MIC+ to VEE		Z_{in}		32		k Ω
Common Mode Rejection Ratio		KCMR		82		dB
Voltage Gain MIC+ or MIC- to LN	I _{line} =15mA R7=68k Ω	G _v	50.5	52.0	53.5	dB
Gain Variation with Frequency at f=300Hz and f=3400Hz	w.r.t.800Hz	ΔG_{vf}		+0.2		dB
Gain Variation with Temperature at -25°C and +75°C	w.r.t.25°C without R6; I _{line} =50mA	ΔG_{vT}		+0.2		dB
Dual-tone multi-frequency input DTMF (pin 11)						
Input impedance		Z_{in}		20.7		k Ω
Voltage Gain from DTMF to LN	I _{line} =15mA R7=68k Ω	G _v	24	25.5	27	dB
Gain Variation with Frequency at f=300Hz and f=3400Hz	w.r.t.800Hz	ΔG_{vf}		+0.2		dB
Gain Variation with Temperature at -25°C and +75°C	w.r.t.25°C I _{line} =50mA	ΔG_{vT}		+0.2		dB
Gain Adjustment GAS1 and GAS2 (pins 2 and 3)						
Gain Variation of the Transmitting Amplifier by Varying R7 between GAS1 and GAS2		ΔG_v	-8		0	dB
Sending Amplifier Output LN(pin 1) Output Voltage	I _{line} =15mA THD=10% I _{line} =4mA THD=10%	V _{LN(rms)}	1.7	2.3		V
Noise output voltage	I _{line} =15mA; R7=68k Ω ; 200 Ω between MIC- and MIC+; psophometrically weighted	V _{NO(rms)}				dBmp
Receiving Amplifier Input IR (pin 10)						
Input impedance		Z_{in}		21		k Ω
Receiving Amplifier Output QR (pin 4)						
Output Impedance		Z_{out}		4		Ω
Voltage gain from IR to QR	I _{line} =15mA; R _L (from pin 9 to pin 4)=300 Ω	G _v	29.5	31	32.5	dB

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Gain Variation with Frequency at f=300Hz and f=3400Hz	w.r.t.800Hz	ΔG_{vf}		±0.2		dB
Gain Variation with Temperature at -25°C and +75°C	w.r.t.25°C without R6 I _{line} =50mA	ΔG_{vT}		+0.2		dB
Output Voltage	sinwave drive; I _p =0mA; THD=2% R4=100kΩ I _{line} =15mA R _L =150Ω R _L =450Ω	V _{O(rms)} V _{O(rms)}	0.22 0.3	0.33 0.48		V V
Output Voltage	THD=10% R4=100kΩ R _L =150Ω I _{line} =4mA	V _{O(rms)}		15		mV
Noise Output Voltage	I _{line} =15mA R4=100kΩ IR open-circuit psophometrically weighted R _L =300Ω	V _{NO(rms)}		50		μV
Gain adjustment GAR (pin 5)						
Gain Variation of Receiving Amplifier Achievable by Varying R4 between GAR and QR		ΔG_v	-11		0	dB
Mute Input (pin 12)						
Input Voltage(HIGH) Input Voltage(LOW) Input Current		V _{IH} V _{IL} I _{MUTE}	1.5		V _{CC} 0.3 15	V V μA
Reduction of Gain						
MIC+ or MIC- to QR Voltage Gain from DTMF to QR	MUTE=LOW MUTE=LOW R4=100kΩ R _L =300Ω	ΔG_v G _v		70 -19		dB dB
Automatic Gain Control Input AGC (pin 15)						
Controlling the Gain from IR to QR and the Gain from MIC+/MIC- to LN; R6 between AGC and VEE Gain Control Range	R6=110kΩ I _{line} =70mA	ΔG_v		-5.8		dB
Highest Line Current for Maximum Gain		I _{line}		23		mA
Minimum Line Current for Minimum Gain		I _{line}		61		mA

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

FUNCTIONAL DESCRIPTION

Supply: VCC, LN, SLPE, REG and STAB

Power for the UTC TEA1062/1062A and its peripheral circuits is usually obtained from the telephone line. The IC supply voltage is derived from the line via a dropping resistor and regulated by the UTC TEA1062/1062A. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits. Decoupling of the supply voltage is performed by a capacitor between V_{CC} and VEE while the internal voltage regulator is decoupled by a capacitor between REG and VEE . The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance (R_{exch}) and the DC resistance of the telephone line (R_{line}). The UTC TEA1062/1062A has an internal current stabilizer operating at a level determined by a $3.6k\Omega$ resistor connected between $STAB$ and VEE (see Fig.8). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to VEE via LN . The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \cdot R_9 \text{ or; } \\ V_{LN} = V_{ref} + (I_{line} - I_{CC} - 0.5 \cdot 10^{-3} \text{ A}) \cdot I_p \cdot R_9$$

where: V_{ref} is an internally generated temperature compensated reference voltage of 3.7V and R_9 is an external resistor connected between $SLPE$ and VEE . In normal use the value of R_9 would be 20Ω . Changing the value of R_9 will also affect microphone gain, DTMF gain, gain control characteristics, side tone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages). Under normal conditions, when $I_{SLPE} \approx I_{CC} + 0.5\text{mA} + I_p$, the static behaviour of the circuit is that of a 3.7V regulator diode with an internal resistance equal to that of R_9 . In the audio frequency range the dynamic impedance is largely determined by R_1 . Fig.3 shows the equivalent impedance of the circuit.

Microphone inputs (MIC+ and MIC-) and gain pins (GAS1 and GAS2)

The UTC TEA1062/1062A has symmetrical inputs. Its input impedance is $64k\Omega$ ($2 \cdot 32k\Omega$) and its voltage gain is typically 52 dB (when $R_7 = 68k\Omega$, see Fig.13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.10. The gain of the microphone amplifier can be adjusted between 44dB

and 52dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R_7 which is connected between $GAS1$ and $GAS2$. Stability is ensured by the external capacitors, C_6 connected between $GAS1$ and $SLPE$ and C_8 connected between $GAS1$ and VEE . The value of C_6 is 100pF but this may be increased to obtain a first-order low-pass filter. The value of C_8 is 10 times the value of C_6 . The cut-off frequency corresponds to the time constant $R_7 \cdot C_6$.

Mute input (MUTE)

A LOW (UTC TEA1062 is HIGH) level at $MUTE$ enables DTMF input and inhibits the microphone inputs and the receiving amplifier inputs; a HIGH (UTC TEA1062 is LOW) level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line. In case the line current drops below 6mA (parallel operation of more sets) the circuit is always in speech condition independent of the DC level applied to the $MUTE$ input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5dB (when $R_7 = 68k\Omega$) and varies with R_7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier (IR, QR and GAR)

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.11. The IR to QR gain is typically 31dB (when $R_4 = 100k\Omega$). It can be adjusted between 20 and 31dB to match the sensitivity of the transducer in use. The gain is set with the value of R_4 which is connected between GAR and QR . The overall receive gain, between LN and QR , is calculated by subtracting the anti-sidetone network attenuation (32dB) from the amplifier gain. Two external capacitors, C_4 and C_7 , ensure stability. C_4 is normally 100pF and C_7 is 10 times the value of C_4 . The value of C_4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant $R_4 \cdot C_4$. The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

Automatic gain control input(AGC)

Automatic line loss compensation is achieved by connecting a resistor(R6) between AGC and VEE. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8dB which corresponds to a line length of 5km for a 0.5mm diameter twisted pair copper cable with a DC resistance of 176Ω/km and average attenuation of 1.2dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance(see Fig.12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifier, in this condition, will give their maximum specified gain.

Side-tone suppression

The anti-sidetone network, R1//Z_{line}, R2, R3, R8, R9 and Z_{bal},(see Fig.4) suppresses the transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

$$(a) R9 \cdot R2 = R1[R3 + (R8/Z_{bal})];$$

$$(b) [Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)];$$

If fixed values are chosen for R1, R2, R3 and R9 then condition(a) will always be fulfilled when $R8/Z_{bal} = R3/R2$. To obtain optimum side-tone suppression condition(b) has to be fulfilled which results in:

$$Z_{bal} = (R8/R1) Z_{line} = k \cdot Z_{line} \text{ where } k \text{ is a scale factor; } k = (R8/R1).$$

The scale factor (k), dependent on the value of R8, is chosen to meet following criteria:

- Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.
- $Z_{bal}/R8 \approx R3/R2$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation,
- $Z_{bal} + R8 \approx R9$ to avoid influencing the transmitter gain.

In practice Z_{line} varies considerably with the type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by: Suppose Z_{line} = 210Ω + (1265Ω//140nF) representing a 5km line of 0.5 mm diameter, copper, twisted pair cable matched

to 600Ω(176Ω/km;38nF/km). When k=0.64 then R8=390Ω, Z_{bal}=130Ω+(820Ω//220nF). At line currents below 9mA the internal reference voltage is automatically adjusted to a lower value(typically 1.6V at 1mA) This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6V. With line currents below 9mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor(R_VA). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage. Current(I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.9 shows this current for V_{CC} > 2.2V. If MUTE is LOW (1062 is HIGH)when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC(1081) in parallel with R1, as shown in Fig.16(c), or, by increasing the DC line voltage by means of an external resistor(R_VA) connected between REG and SLPE.

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

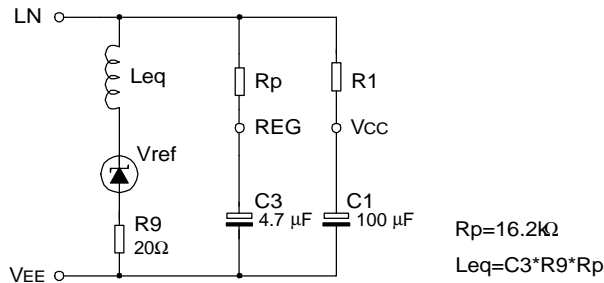


Fig.3 Equivalent impedance circuit

The anti-sidetone network for the UTC TEA1062/1062A family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig.5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

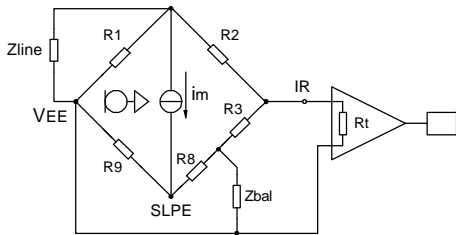


Fig 4 Equivalent circuit of UTC TEA1062/1062A anti-sidetone bridge

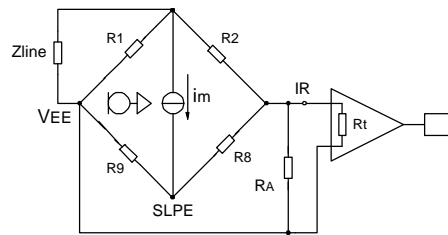


Fig 5 Equivalent circuit of an anti-sidetone network in a wheatstone bridge configuration

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

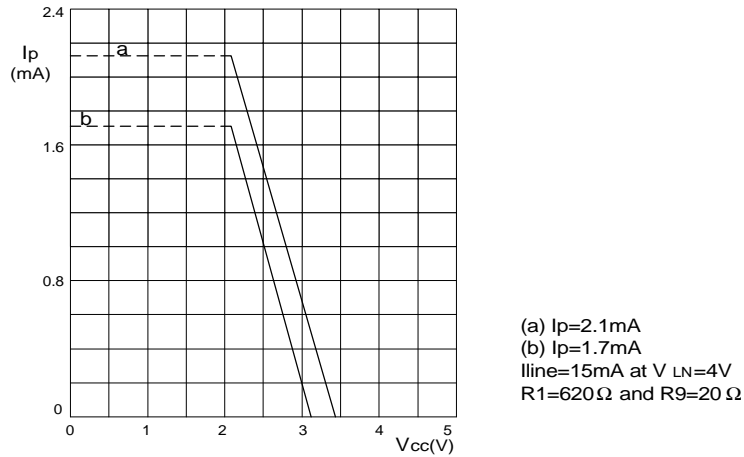


Fig.9 Typical current I_p available from V_{cc} peripheral circuitry with $V_{cc} \geq 2.2 \text{ V}$.

curve (a) is valid when the receiving amplifier is not driven or when MUTE =LOW(UTC TEA1062 is HIGH) .curve(b) is valid when MUTE=HIGH(UTC TEA1062 is LOW) and the receiving amplifier is driven; $V_o(\text{rms}) = 150 \text{ mV}$, $R_L = 150 \Omega$. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a high value by means of resistor R_{VA} connected between REG and SLPE.

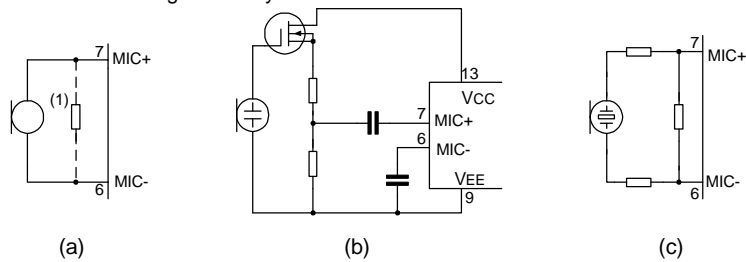


Fig. 10 Alternative microphone arrangement

- (a) Magnetic or dynamic microphone. The resistor marked(1) may be connected to decrease the terminating impedance.
- (b) Electret microphone.
- (c) Piezoelectric microphone.

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

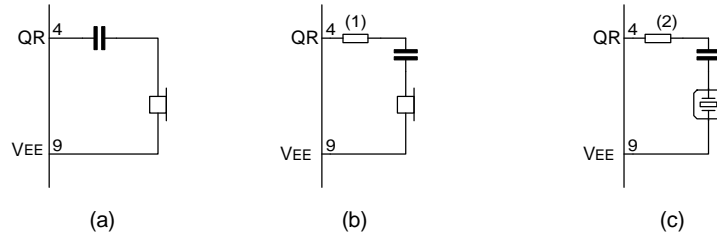
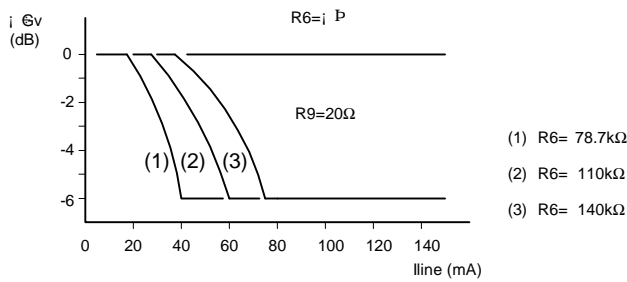


Fig.11 Alternative receiver arrangement

- (a) Dynamic earpiece.
- (b) Magnetic earpiece. The resistor marked (1) may be connected to prevent distortion (inductive load)
- (c) Piezoelectric earpiece. The earpiece marked (2) is required to increase the phase margin (capacitive load)

Fig.12 Variation of gain with line current, with R6 as a parameter.



		Rexch(Ω)			
		400	600	800	1000
		R6(kΩ)			
Vexch(V)	36	100	78.7	i Á	i Á
	48	140	110	93.1	82
	60	i Á	i Á	120	102

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (Vexch) and exchange feeding bridge resistance (Rexch); R9=20Ω.

UTC TEA1062/1062A LINEAR INTEGRATED CIRCUIT

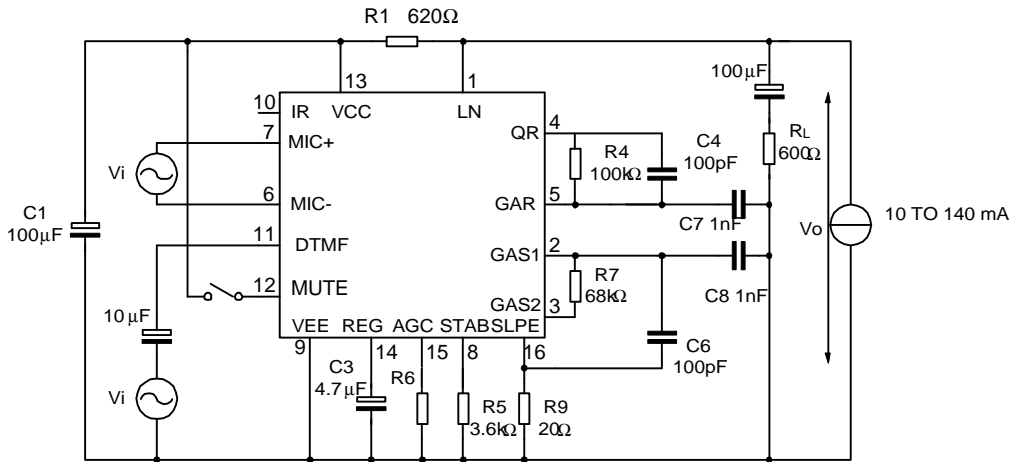


Fig.13 Test circuit defining voltage gain of MIC+,MIC- and DTMF inputs.

Voltage gain is defined as : $GV=20*\log(|VO/Vi|)$. For measuring the gain from MIC+ and MIC- the MUTE input should be HIGH(UTC TEA1062 is LOW) or open-circuit, for measuring the DTMF input MUTE should be LOW(UTC TEA1062 is HIGH) .Inputs not under test should be open-circuit.

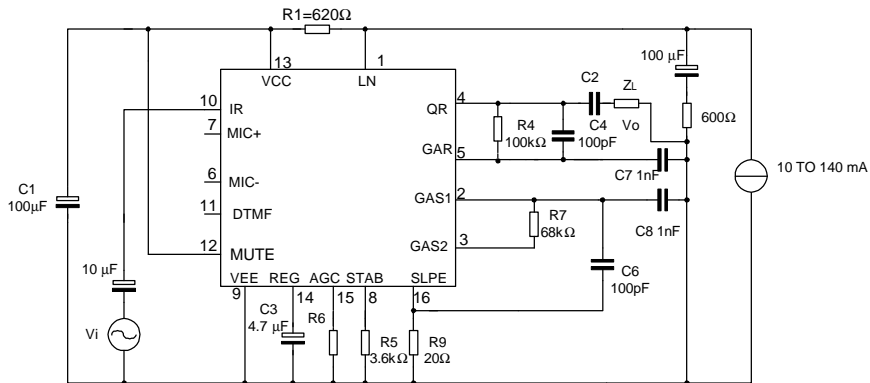


Fig.14 Test circuit for defining voltage gain of the receiving amplifier.

Voltage gain is defined as: $GV=20*\log(|VO/Vi|)$.

