



SPC08A

6.5KB Sound Controller

SEP. 19, 2001

Version 1.7

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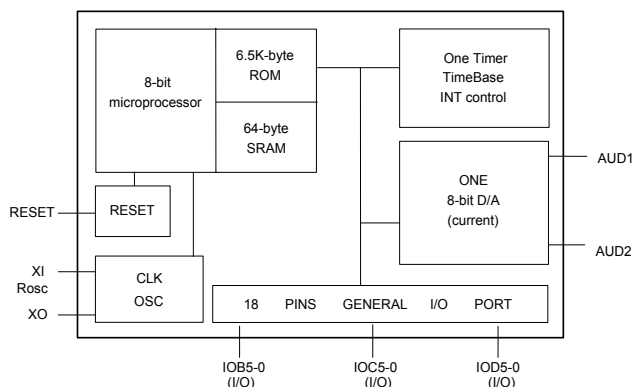
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6.5KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC08A is a CPU based one-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 6.5K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 2 sec speech duration @ 7KHz sampling rate) and 64-byte working SRAM. It includes one Timer/Counter, 18 Software Selectable I/Os and one audio current output (D/A). For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V. In addition, the SPC08A has a Clock Stop mode for power saving. The power saving mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 3.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPC08A includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Provides 6.5K-byte ROM for program and audio data
- 64-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 1.5MHz
3.6V - 5.5V @ 3.0MHz
- Supports Crystal Resonator or Rosc (with Bonding option)
- Max. CPU clock: 1.5MHz @ 3.0V, 3.0MHz @ 5.0V
- Standby mode (Clock Stop mode) for power saving.
Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- Provides 18 general I/Os
- One 12-bit timer/counter
- 4 INT sources
- Key wake-up function
- Approx. 2 sec speech
@ 7KHz sampling rate with ADPCM

4. APPLICATION FIELD

- Intelligent education toys
Ex. Pattern to voice (animal, car, color, etc.)
Spelling (English or Chinese)
Math
- Toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS*

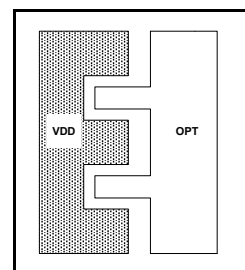
Mnemonic	PIN No.	Type	Description
VDD	8	I	POWER VDD
VSS	11	I	POWER VSS
XI	1	I	CRYSTAL OSC IN or RESISTOR
XO	40	O	CRYSTAL OSC OUT
OPT***	8A	I	Rosc OPTION connect to VDD
RESET	39	I	RESET
TEST	35	I	TEST MODE
AUD	3	O	AUDIO OUTPUT
IOA0	34	I/O	Port A is a 6-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A can be either Buffer or Open-drain NMOS types (Sink current). **See note 1 and 2 below.
IOA1	33	I/O	
IOA2	32	I/O	
IOA3	31	I/O	
IOA4	30	I/O	
IOA5	29	I/O	
IOB0	28	I/O	Port B is a 6-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current). IOC1: EXT INT IN IOC2: EXT COUNT IN **See note 1 and 2 below.
IOB1	24	I/O	
IOB2	23	I/O	
IOB3	22	I/O	
IOB4	21	I/O	
IOB5	20	I/O	
IOD0	19	I/O	Port D is a 6-bit bi-directional programmable Input/Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS type (source current). (Key change, Wake up I/O) **See note 1 and 2 below.
IOD1	18	I/O	
IOD2	13	I/O	
IOD3	12	I/O	
IOD4	10	I/O	
IOD5	9	I/O	

* Refer to SPC Programming Guide for complete information.

**Note: 1.) Three input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified, Buffer output, Open Drain PMOS output (source), or Open Drain NMOS output (sink).

***OPT is the selection pin for ROSC or X'TAL using the bonding option. The shape looks like the figure at the right. When ROSC is selected, OPT is connected to VDD. If X'TAL is selected, OPT is floating. The reason OPT is near VDD is that when ROSC is selected, it is easy to make the connection between VDD and OPT.



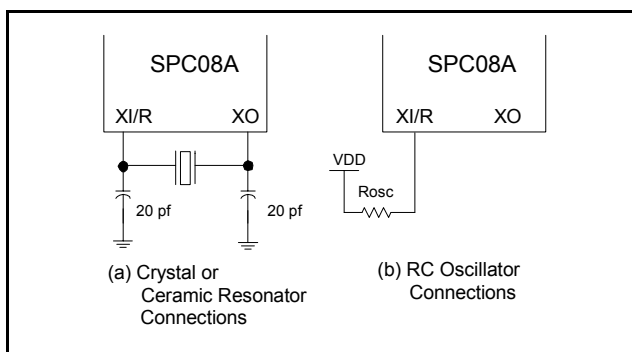
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit microprocessor in SPC08A is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure).

6.2. Oscillator

The SPC08A supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by using the bonding option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagram below is typical of X'TAL/ROSC circuits for most applications:



6.3. Bonding Option

Crystal Resonator/Rosc can be selected by bonding option.

6.4. ROM Area

The SPC08A provides a 6.5K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register.

6.5. RAM Area

There are 64-byte RAM including stack at locations from \$80 through \$FF.

6.6. Map of Memory and I/Os

*I/O PORT:

- PORT IOA \$0002
IOB \$0003
IOD \$0005

- I/O CONFIG \$0000
\$0001

*NMI SOURCE:

- INTA (from TIMER A)

*INT SOURCE:

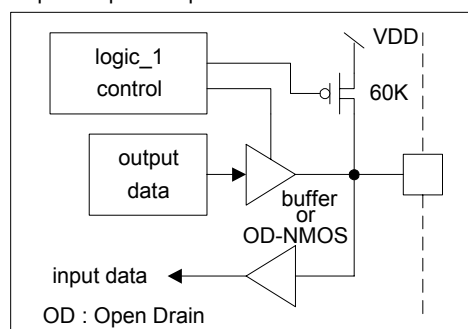
- INTA (from TIMER A)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536

*MEMORY MAP (From ROM view)

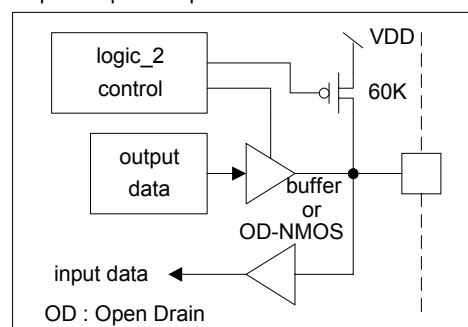
\$00000	HW register, I/Os
\$000C0	USER RAM and STACK
\$00100	UNUSED
\$00200	SUNPLUS TEST PROGRAM
\$00600	USER'S PROGRAM & DATA AREA
\$01FFF	

6.7. I/O Port Configuration*

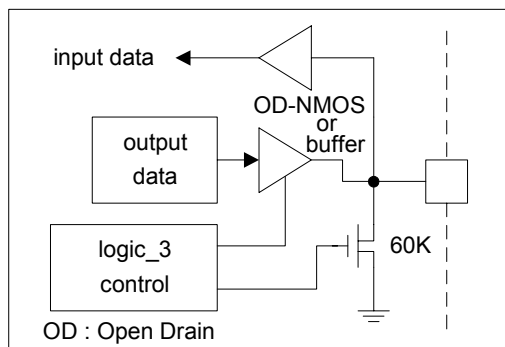
Input/Output IOA port : IOA3 - 0



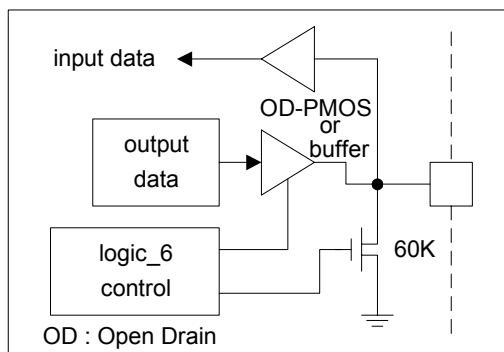
Input/Output IOA port : IOA5 - 4



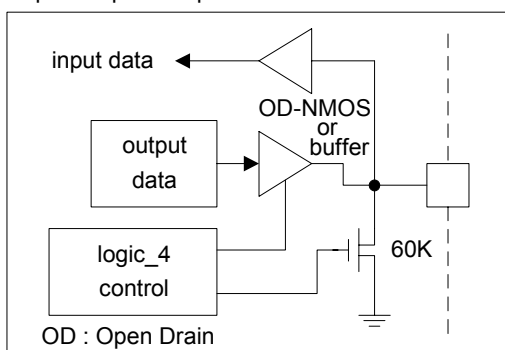
Input/Output IOB port : IOB3 - 0



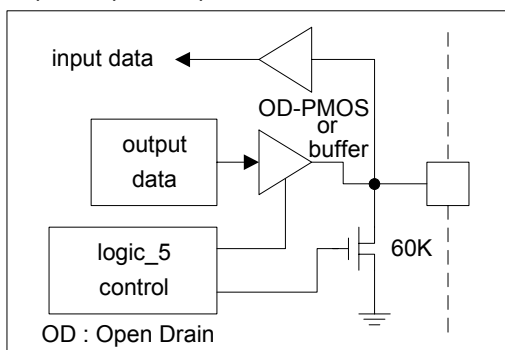
Input/Output IOD port : IOD5 - 4



Input/Output IOB port : IOB5 - 4



Input/Output IOD port : IOD3 - 0



*Values shown are for VDD = 5.0V test conditions only.

6.8. Timer/Counter

SPC08A contains one 12-bit timer/counter, TMA respectively. TMA can be specified as a timer or a counter. In the timer mode, the TMA is a re-loaded up-counter. When timer overflows, the user's pre-set value will be reloaded automatically and the timer upcounts again. At the same time, interrupt will be generated if the interrupt is enabled. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.9. Speech and Melody

Since SPC08A provides 6.5K ROM (0.5K for Sunplus test program) only, it is a suitable IC for simple speech and melody synthesis.

For speech synthesis, SPC08A can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

6.10. Power Saving Mode

The SPC08A provides a power saving mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD5 - 0 are the wake-up sources in SPC08A. After SPC08A is awakened, the internal CPU will go to the RESET State ($T_w \geq 65536 \times T_1$) and then continue processing the program. Wakeup Reset will not affect the contents of RAM and I/Os (FIG.1).

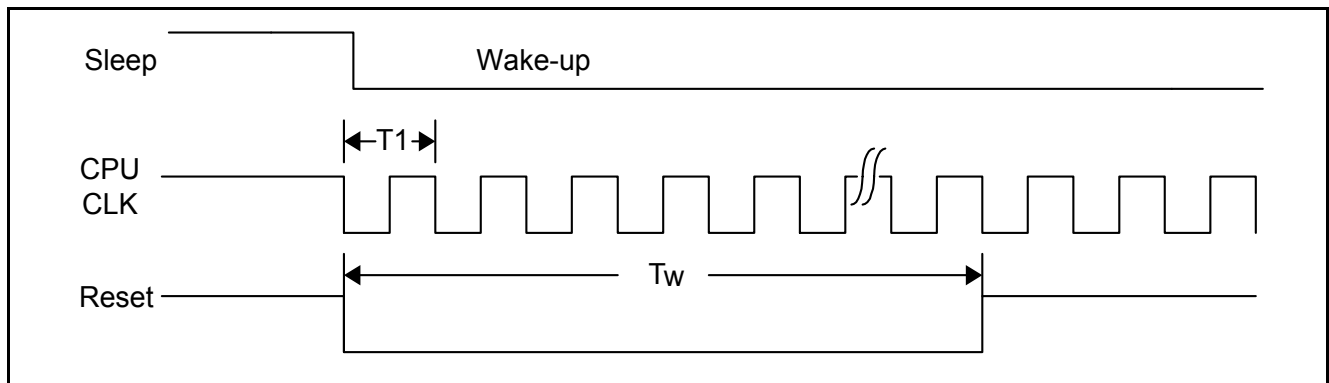


FIG. 1

$$T_1 = 1 / (F_{cpu}), T_w \geq 65536 \times T_1$$

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics ($T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	1.0	1.5	MHz	VDD = 3.0V
		-	2.0	3.0	MHz	VDD = 5.0V

7.3. DC Characteristics (VDD = 3.0V, $T_A = 25^\circ\text{C}$)

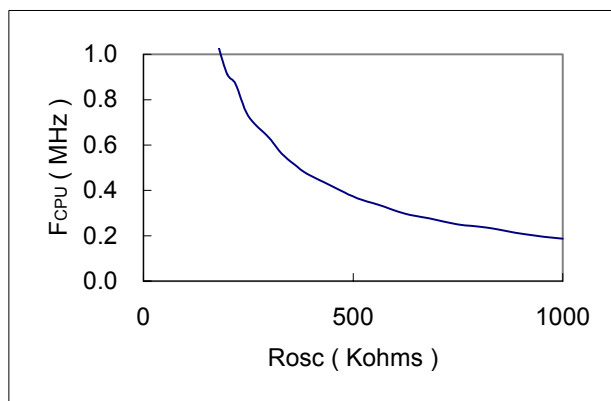
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	$F_{CPU} = 1.0\text{MHz}$ @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3.0V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (IOA, IOD)	I_{OH}	-	-6.0	-	mA	VDD = 3.0V, $V_{OH} = 2.0V$
Output Sink I (IOA, IOD)	I_{OL}	-	8.0	-	mA	VDD = 3.0V, $V_{OL} = 0.8V$
Output Sink I (IOB)	I_{OL}	-	12	-	mA	VDD = 3.0V, $V_{OL} = 0.8V$
Input Resistor (IOD)	R_{IN}	-	80	-	Kohm	Pull Low, VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, $T_A = 25^\circ\text{C}$)

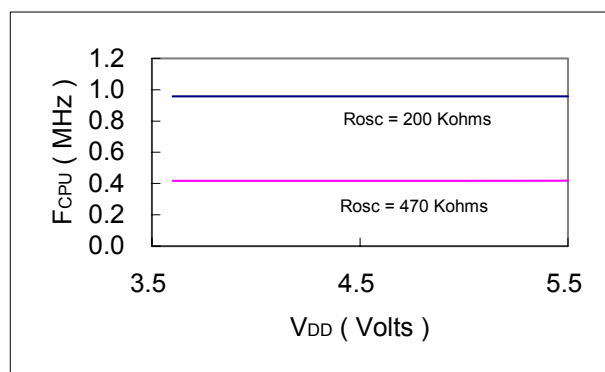
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	2.5	-	mA	$F_{CPU} = 3.0\text{MHz}$ @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I (IOA, IOD)	I_{OH}	-	-10	-	mA	VDD = 5.0V, $V_{OH} = 4.2V$
Output Sink I (IOA, IOD)	I_{OL}	-	12	-	mA	VDD = 5.0V, $V_{OL} = 0.8V$
Output Sink I (IOB)	I_{OL}	-	17	-	mA	VDD = 5.0V, $V_{OL} = 0.8V$
Input Resistor (IOD)	R_{IN}	-	60	-	Kohm	Pull Low, VDD = 5.0V

7.5. The Relationship between the R_{OSC} and the F_{CPU}

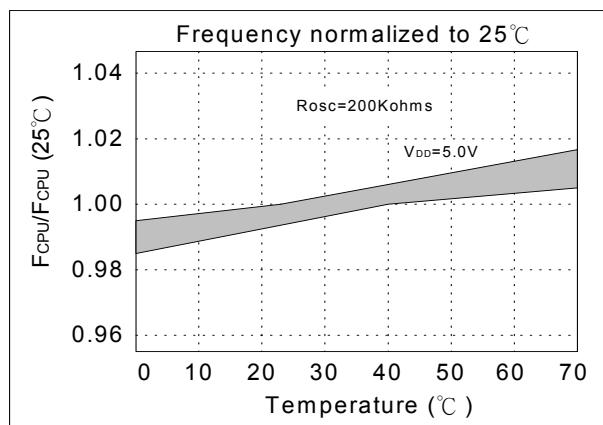
7.5.1. $V_{DD} = 5.0V$, $T_A = 25^\circ C$



7.5.3. Frequency vs. V_{DD}

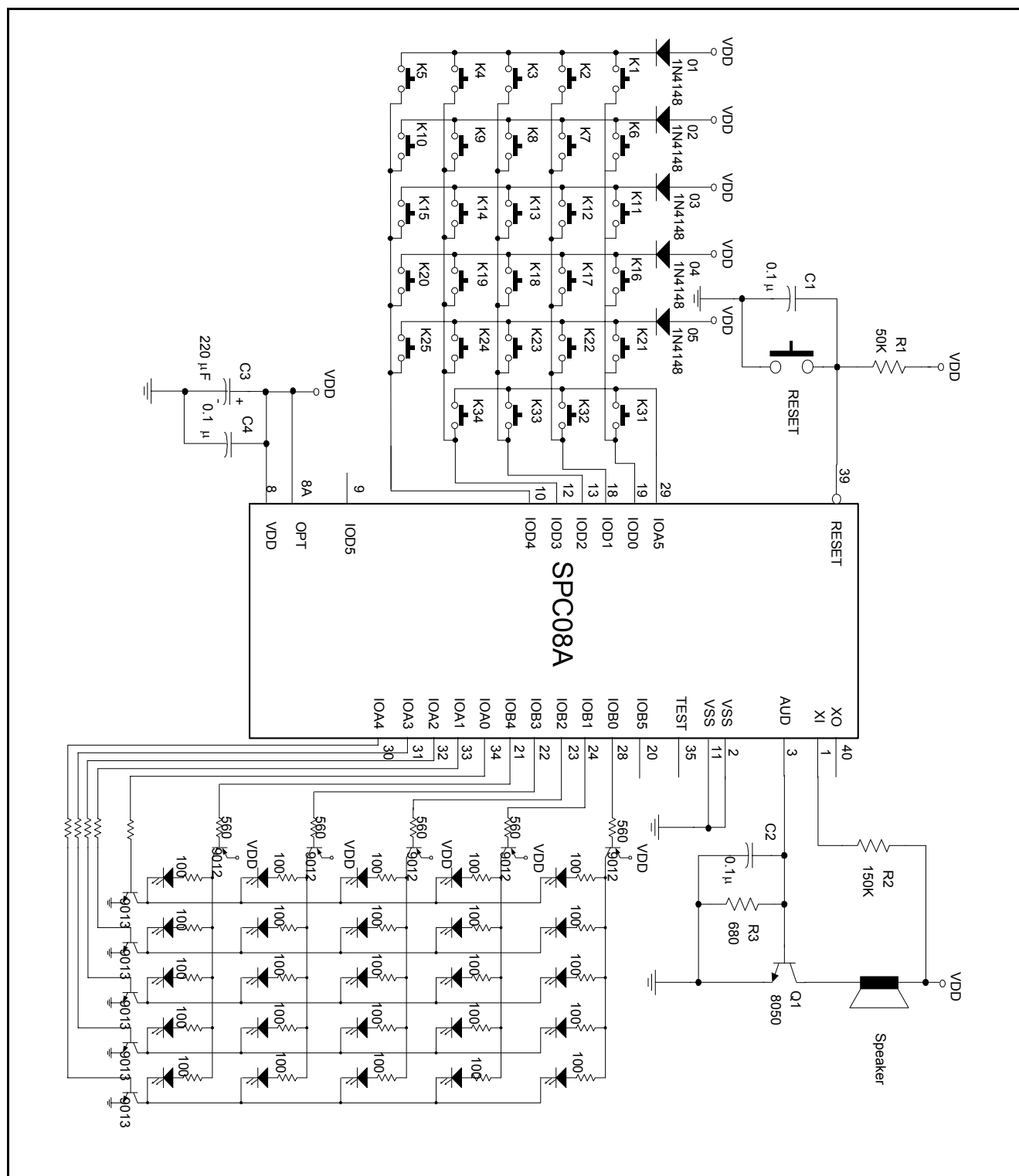


7.5.2. Frequency vs. temperature



8. APPLICATION CIRCUITS

8.1. Application Circuit



8.2. Current Mode DAC Speaker Driver

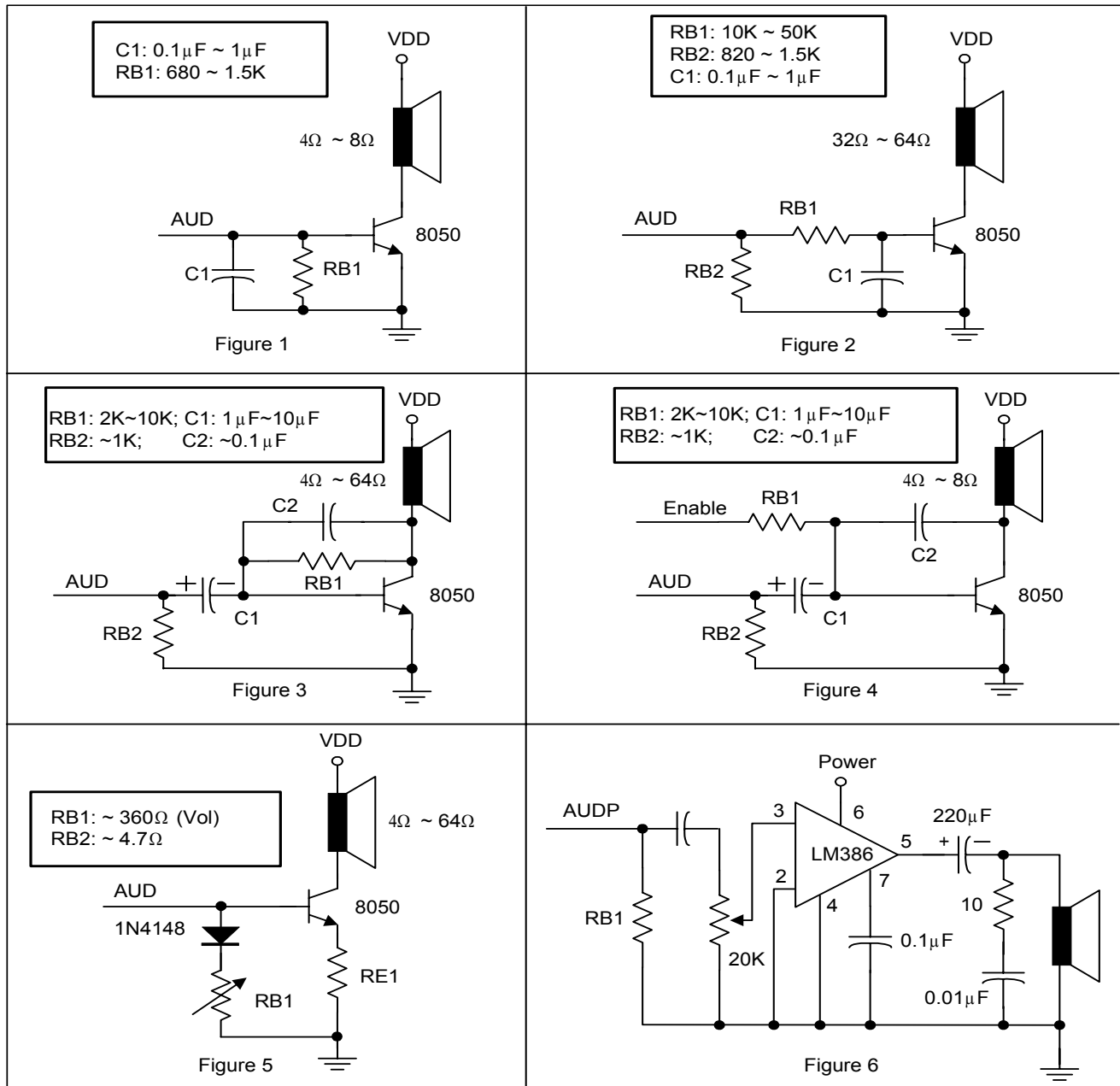


Figure 1: The simplest CKT uses a low impedance speaker. It has high operation current, but has lowest cost.

Figure 2: It is the same as Figure 1 but a high impedance speaker is used.

Figure 3: The CKT contains a low pass filter. It is capable of providing higher speech quality, but it takes higher operation current.

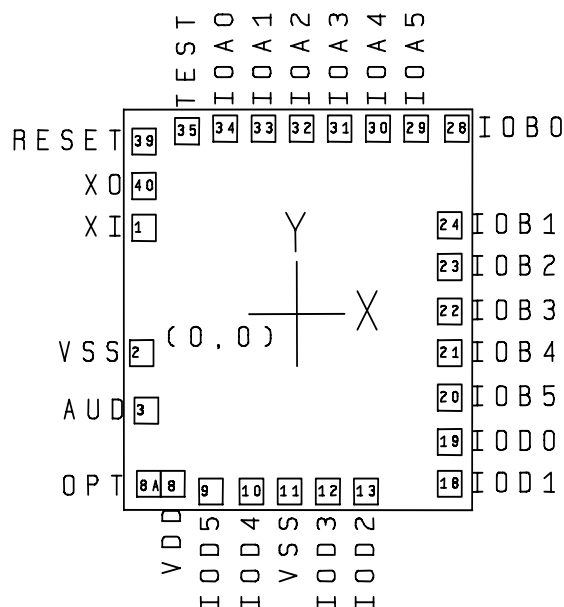
Figure 4: Improved version of Figure 3. The standby current can be controlled by the enable pin.

Figure 5: The current mirror mode. It is able to control the volume. In addition, it has more stable and lower operation current than Figure 1-3.

Figure 6: High quality, low operation current CKT, but more expensive.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 1690μm x 1840μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, bond all VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC08A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	XI	-633	318
2	VSS	-640	-164
3	AUD	-625	-384
8A	OPT	-608	-660
8	VDD	-513	-660
9	IOD5	-354	-691
10	IOD4	-187	-691
11	VSS	-27	-690
12	IOD3	132	-691
13	IOD2	299	-691
18	IOD1	643	-661
19	IOD0	643	-500
20	IOB5	643	-331
21	IOB4	643	-169
22	IOB3	643	0
23	IOB2	643	161
24	IOB1	643	330
28	IOB0	671	694
29	IOA5	507	694
30	IOA4	349	694
31	IOA3	187	694
32	IOA2	28	694
33	IOA1	-134	694
34	IOA0	-292	694
35	TEST	-452	682
39	RESET	-633	641
40	XO	-633	475

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 18, 1997	0.1	Original	
NOV. 06, 1997	0.2	Renew to a new document format	
MAR. 20, 1998	1.0	VDD operation range 2.4V - 3.0V (frequency 0.1MHz - 1.5MHz) 3.6V - 5.5V (frequency 0.1MHz - 3.0MHz)	
MAY. 13, 1998	1.1	Add "Note: To ensure that the IC functions properly, bond all VDD and VSS pins."	
JUN. 01, 1998	1.2	1. Revise the grammars and spelling in " <u>GENERAL DESCRIPTION</u> ", " <u>FEATURES</u> ", and " <u>APPLICATION CIRCUITS</u> " 2. Revise the pin naming in Pad Assignment RESB -> RESET, AUDA -> AUD	
JUN. 10, 1998	1.3	1. Add OPT pin description in the " <u>SIGNAL DESCRIPTIONS</u> " 2. Add "The Relationship between the R _{OSC} and the F _{CPU} "	
NOV. 14, 1999	1.4	1. Renew to a new document format 2. Add 3.0V description in the " <u>ELECTRICAL SPECIFICATIONS</u> " 3. Modify " <u>APPLICATION CIRCUITS</u> "	
SEP. 01, 2000	1.5	1. When VDD = 5.0V, V _{OH} = 4.2V, add typical value (I _{OH} = -10mA) 2. When VDD = 5.0V, V _{OL} = 0.8V, add typical value (I _{OL} = 12mA) for IOA, IOD 3. When VDD = 5.0V, V _{OL} = 0.8V, add typical value (I _{OL} = 17mA) for IOB 4. When VDD = 3.0V, V _{OH} = 2.0V, add typical value (I _{OH} = -6mA) 5. When VDD = 3.0V, V _{OL} = 0.8V, add typical value (I _{OL} = 8mA) for IOA, IOD 6. When VDD = 3.0V, V _{OL} = 0.8V, add typical value (I _{OL} = 12mA) for IOB	
SEP. 01, 2000	1.6	Modify: 1. F _{CPU} = 3.0MHz @ 3.0V -> F _{CPU} = 1.0MHz @ 3.0V	7
		2. F _{CPU} = 1.0MHz @ 5.0V -> F _{CPU} = 3.0MHz @ 5.0V	8
SEP. 19, 2001	1.7	1. Modify wide operating voltage: 2.4V - 3.4V -> 2.4V - 3.6V	3, 8
		2. Correct chip size	12
		3. Add Note1 and Note3 in the " <u>9.1 PAD Assignment</u> "	12
		4. Renew to a new document format	