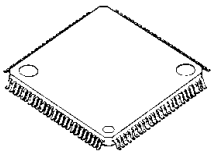
15-CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER with OUTPUT PORT

■GENERAL DESCRIPTION

The NJU6623A is a Dot Matrix LCD controller driver for 15-character 1-line with icon display in single chip.
It contains bleeder resistance, general output port, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers.
The character generator ROM consists of 7,840 bits stores 224 kinds of character Font. Each 1,120 bits CG RAM and Icon display RAM can stores 32 kinds of special character displayed on the dot matrix display area or 75 kind of Icon on the Icon display area.
The 8-common (7 for character, 1 for icon) and 75-segment drivers operated 15-character 1-line with 75 Icon LCD display and LED driver drives 4 LED which can use like as indicator.
The 16th gray scale contrast control function is incorporated for its adjustment. Therefore, simple power supply circuit and easy contrast adjustment are available.
The complete CR oscillator is incorporated, therefore no external components for oscillation circuit are required.
The microprocessor interface circuits which operate by 1MHz, can be selected serial interface.

■PACKAGE OUTLINE



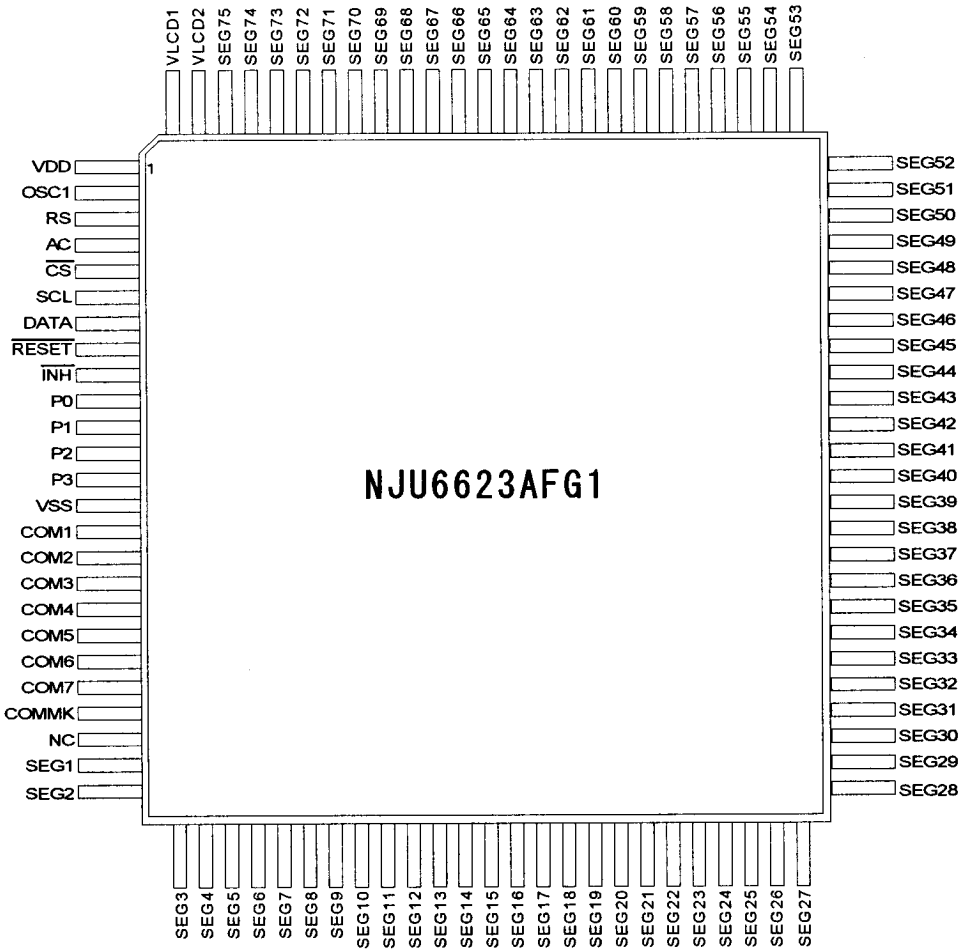
NJU6623AFG1

■FEATURES

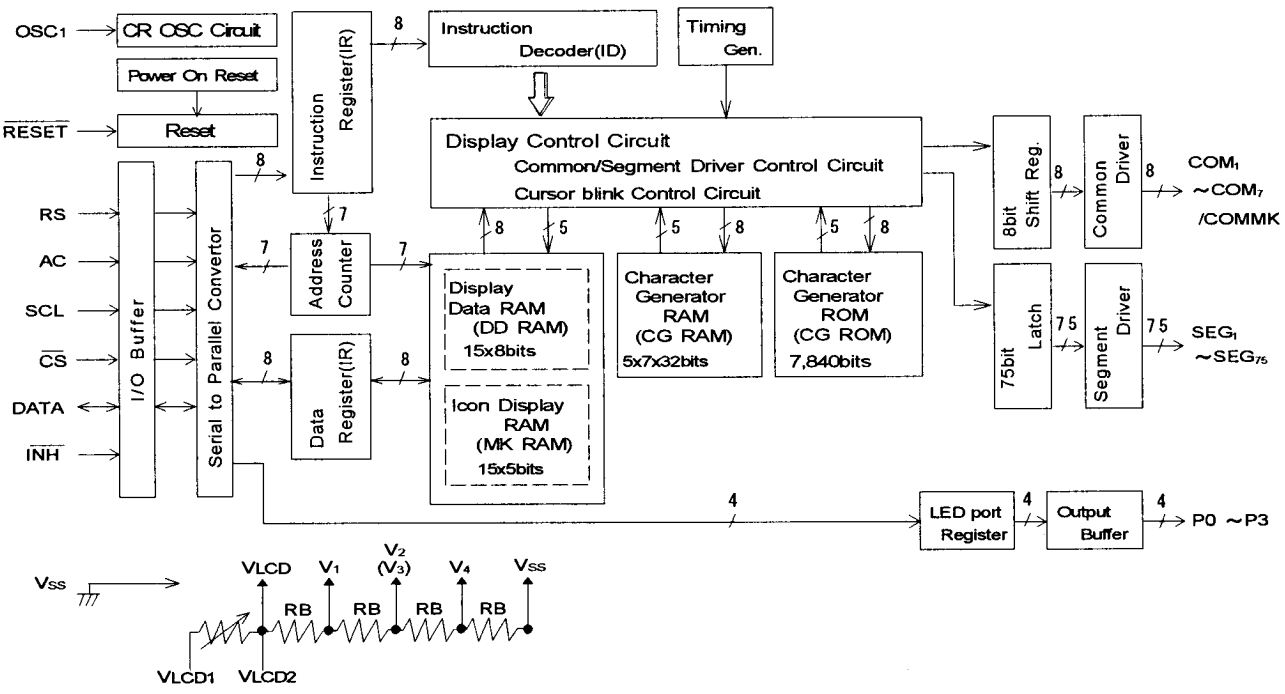
- 15-character 1-line Dot Matrix LCD Controller Driver
- Maximum 75 Icon Display
- Serial Direct Interface with Microprocessor
- Display Data RAM - 15 x 8 bits : Maximum 15-character 1-line Display
- Character Generator ROM - 7,840 bits : 224 Characters for 5 x 7 Dots
- Character Generator RAM - 1,120 bits : 32 Patterns(5 x 7 Dots)
- Icon Display RAM - 15 x 5 bits : Maximum 75 Icons
- High Voltage LCD Driver : 8-common / 75-segment
- Duty and Bias Ratio : 1/8 duty, 1/4 bias
- Useful Instruction Set : Clear Display, Address Home, Display ON/OFF Cont, Display Blink, Address Shift, Character Shift
- General output port (4 ports)
- Power On Initialization / Hardware Reset
- Bleeder Resistance on-chip
- Software contrast control(16 step)
- Oscillation Circuit on-chip
- Low Power Consumption
- Operating Voltage --- 2.4 to 5.5 V
- Package Outline --- QFP 100
- C-MOS Technology

Jul.2002
Ver.4

■PIN CONFIGURATION



■BLOCK DIAGRAM



■TERMINAL DESCRIPTION

No.	SYMBOL	I/O	F U N C T I O N
1,14	VDD,VSS	-	Power Source:VDD=+5V,GND:VSS=0V
100	VLCD1	I	LCD driving voltage input terminal
99	VLCD2	I	LCD driving voltage stabilize capacitor terminal connect the capacitor between VLCD2 and VSS typ. : 0.1uF
2	OSC1	I	System clock input terminal This terminal should be open for internal clock operation.
3	RS	I	Register selection signal input terminal "0":Instruction register "1":Data register
4	AC	I	Set CG RAM address selection signal input terminal "0":other Instruction "1":Set CG RAM Address
5	$\overline{CS}$	I	Chip select signal input in serial mode
6	SCL	I	Sift clock input in serial mode
7	DATA	I	Serial Data Input terminal
8	$\overline{RESET}$	I	Reset Terminal. When the "L" level input over than 1.2ms to this terminal, the system will be reset (at fosc 153KHz).
9	$\overline{INH}$	I	Stand-by mode terminal When the "L" level input to this terminal, the system will be low power mode(stand-by mode).
10-13	P0-P3	O	General output port LED driver drives LED which can use like as indicator.
15-21	COM1-COM7	O	LCD common driving signal output terminals
22	COMMK	O	Icon common driving signal output terminals
24-98	SEG1-SEG75	O	LCD segment driving signal output terminals
23	NC	-	These terminals are electrically open.

■FUNCTIONAL DESCRIPTION

(1-1)Register

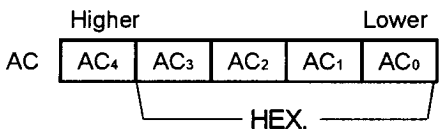
The NJU6623A incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift" or address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM (MK RAM).
The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM, CG RAM or MK RAM.
The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation.
These two registers are selected by the selection signal RS as shown below.

(1-2)Address Counter (AC)

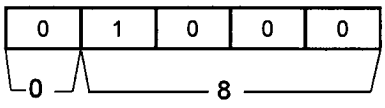
The address counter(AC) addresses the DD RAM, CG RAM or MK RAM.
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter(AC) increments (or decrements) automatically.

(1-3)Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 15 x 8 bits stores up to 15-character display data represented in 8-bit code.
The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



(Example) DD RAM address " 08 "



The relation between DD RAM address and display position on the LCD is shown below.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	-Display Position
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	-DD RAM Address (Hex.)

When the display shift is performed,the DD RAM address changes as follows:

(Left Shift Display)

(00)<=	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	00

(Right Shift Display)

0E	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	=>(0E)

(1-4)Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character code.
The storage capacity is up to 224 kinds of 5 x 7 dots character pattern(available address is $(20)_H$ through $(FF)_H$).
The correspondence between character code and standard character pattern of NJU6623 is shown in Table 2.
User-defined character patterns (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version -02)

Lower 4bit(HEX.) \ Upper 4bit(HEX.)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)	(17)														
1	(02)	(18)														
2	(03)	(19)														
3	(04)	(20)														
4	(05)	(21)														
5	(06)	(22)														
6	(07)	(23)														
7	(08)	(24)														
8	(09)	(25)														
9	(10)	(26)														
A	(11)	(27)														
B	(12)	(28)														
C	(13)	(29)														
D	(14)	(30)														
E	(15)	(31)														
F	(16)	(32)														

(1-5)Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 32 kind of character in 5 x 7 dots mode.
To display user's original character pattern stored in the CG RAM, the address data $(00)_H$-$(1F)_H$ should be written to the DD RAM as shown in Table 2.
Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots)

Character Code (DD RAM Data)	CG RAM Address			Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ← → Upperbit Lower bit	7 6 5 4 3 2 1 0 ← → Upperbit Lower bit			← 4 3 2 1 0 → Upper bit Lower bit	
0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * * *	Character Pattern Example(1) <= Cursor Position
0 0 0 0 0 0 0 1	0 0 0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * * *	Character Pattern Example(2) <= Cursor Position
		0 0 0 0 0 1			
. . . . .	. . . . .	. . . . .		. . . . .	
0 0 0 1 1 1 1 1	1 1 1 1 1	1 0 0 1 0 1 1 1 0 1 1 1			*=Don't care

Notes :

1. Character code bit 0 to 4 correspond to the CG RAM address bit 3 to 7(5bits:32 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is Don't care line. In case of input CG RAM data continuously, invalid address are Cursor position automatically.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code of DD RAM bits 5 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-6)Icon Display RAM (MK RAM)

The NJU6623A can display maximum 75 Icons.
The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.
The relation between MK RAM address and Icon Display position is shown below:

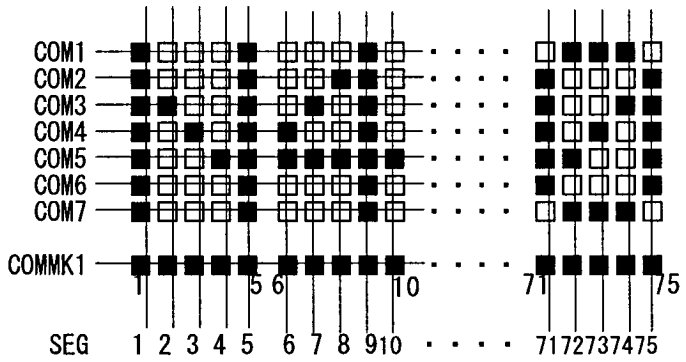


Table 4. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address (10H-1EH)		Bits for Icon Display Position							
		D7	D6	D5	D4	D3	D2	D1	D0
1 0000	10H	0	0	0	"1"	"2"	"3"	"4"	"5"
1 0001	11H	0	0	0	"5"	"7"	"8"	"9"	"10"
1 0010	12H	0	0	0	"11"	"12"	"13"	"14"	"15"
1 0011	13H	0	0	0	"16"	"17"	"18"	"19"	"20"
:	:	:							
1 1110	1EH	0	0	0	"71"	"72"	"73"	"74"	"75"

Notes : When the Icon display function using by the software initialization because the MK RAM is not initialized by the power turning on and hardware reset.

(1-7)Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.
RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.
Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

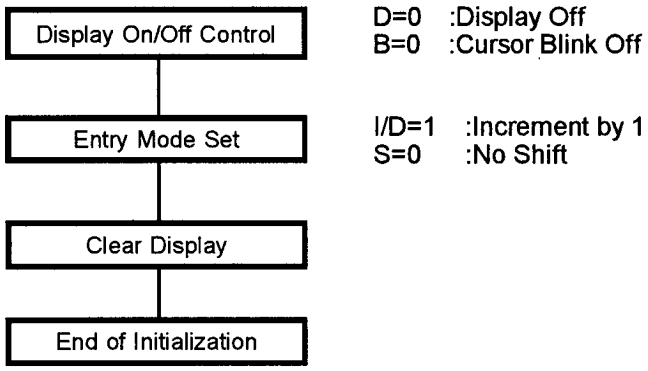
(1-8)LCD Driver

LCD Driver consists of 8-common driver and 75-segment driver.
The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

(2)Power on Initialization by internal circuits

(2-1)Initialization By Internal Reset Circuits

The NJU6623A is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 1.5ms (fosc=153kHz) after V_{DD} rises to 2.4V. Initialization flow is shown below:

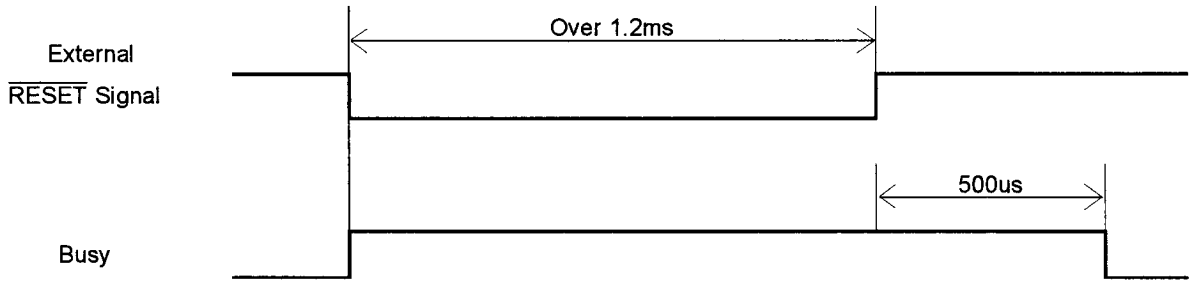


Note : If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed. In this case the initialization by MPU software is required.

(2-2)Initialization By Hardware

The NJU6623A incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 500us (fosc=153kHz) after $\overline{\text{RESET}}$ terminal goes to "H". During this 500us period, any other instruction must not be input to the NJU6623A.

-Timing Chart



(3)Stand by Mode

The NJU6623A equipped stand by mode for reducing power consumption.
Setting of stand by mode are INH terminal = "L", return to stand by mode are INH terminal = "H".
The internal circuit of stand by mode shown below,

-All character, mark off.
-The contents of written data for DD/CG/MK RAM will be hold.
-Osc circuit will be stop, COM,SEG output terminal VLCD level.

Note) In case of stand by mode, it should not be input a instruction, it will be come error factor.

(4)Instructions

The NJU6623A incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6623 and MPU or peripheral ICs operating different cycles. The operation of NJU6623A is determined by this control signal from MPU. The control information includes register selection signals (RS), Set CG RAM address signals (AC) and data bus signals (DATA).

Table 4. Table of Instructions

INSTRUCTION	CODE										DESCRIPTION	Execute Time (f_{osc}=153kHz)
	RS	AC	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	-
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets RAM address $(00)_H$ in AC.	427.59us
Return Home	0	0	0	0	0	0	0	0	1	0	Sets RAM address $(00)_H$ in AC and returns display being shifted original position. RAM contents remain unchanged.	0us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets address move direction and specifies shift of display are performed in data write. I/D=1:Increment,I/D=0:Decremen S=1:Accompanies display shift	0us
Display ON/OFF Control	0	0	0	0	0	0	1	D	0	B	Sets of display On/Off(D) and blink of cursor position character(B).	0us
Address or Display Shift	0	0	0	0	0	1	S/A	R/L	0	0	Moves address & shifts display without changing RAM contents S/C=1 : Display shift S/C=0 : address shift R/L=1 : Shift to the right R/L=0 : Shift to the left	0us
Set Static Port	0	0	0	0	1	0	P3	P2	P1	P0	Sets Static port data.	0us
Contrast control	0	0	0	1	0	0	E.V.R. value				Sets data to Contrast Control Register.	0us
Set DD/MKRAM Address	0	0	1	0	0	address					Sets DD/MK RAM address. After this instruction, the data is transferred to RAM.	0us
Set CG RAM Address	0	1	address								Sets CG RAM address. After this instruction, the data is transferred to RAM.	0us
Write Data to CG or DD or MK RAM	1	0	Write Data(DD RAM)								Writes data into RAM.	41.38us
			0	0	0	(CG RAM)						
						(MK RAM)						
*=Don't care	DD RAM : Display data RAM,CG RAM : Character generator RAM, MK RAM : Icon display RAM If the oscillation frequency is changed, the execution time is also changed.											

(4-1)Description of each instructions

(a)Maker Testing

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	0	0	0	0	0	0

All "0" code is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please check the output condition of Enable signal when the power turns on.)

(b)Clear Display

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0.
When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set to increment.The S of entry mode does not change.
Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern (Custom font).

(c)Return Home

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	0	0	0	0	1	0

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned its original position if shifted. The DD RAM contents do not change.

(d)Entry Mode Set

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the address moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the whole display shift in the DD RAM writing.

I/D	F u n c t i o n
1	Address increment: The address of the DD RAM or MK RAM or CG RAM increment (+1) when the write.
0	Address decrement: The address of the DD RAM or MK RAM or CG RAM decrement:(-1) when the write.

S	F u n c\ t i o n
1	Whole display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The display does not shift when writing into CG, MK RAM.
0	The display does not shift.

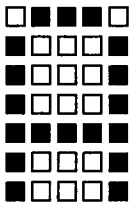
(e)Display ON/OFF Control

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	0	0	1	D	0	B

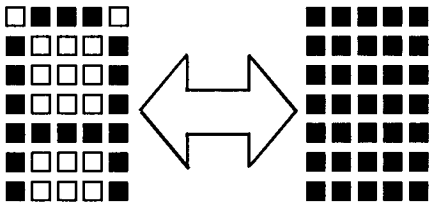
Display On/Off control instruction which controls the whole display On/Off and the addressed position character blink, is executed when the code "1" is written into DB_3 and the codes of (D) and (B) are written into DB_2(D) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off.I n this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

B	Function
1	The addressed position character is blinking. Blinking rate is 500ms at f_{osc}=153kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots
(1)Cursor display example



Alternating display
(2)Blink display example

(f)Address/Display Shift

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	0	1	S/A	R/L	0	0

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display.
The contents of address counter(AC) does not change by operation of the display shift only.
This instruction is executed when the code "1" is written into DB_4 and the codes of (S/A)and (R/L) are written into DB_3(S/A) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the address position to the left ((AC) is decremented by 1)
0	1	Shifts the address position to the right ((AC) is incremented by 1)
1	0	Shifts the whole display to the left and the cursor follows it.
1	1	Shifts the whole display to the right and the cursor follows it.

(g)Set Static Port

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	0	1	0	P3	P2	P1	P0

It sets Static Output Port signal which can drive LED directly like as indicator. Initial status is "L".

(h)Contrast Control

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	0	1	0	0	C_3	C_2	C_1	C_0

Contrast Control instruction which adjusts the contrast of the LCD,is executed when the code "1" is written into DB_6 and the codes of C_3 to C_0 are written into DB_3 to DB_0 as shown below.
The contrast of LCD can be adjusted one of 16 voltage-stages by setting this 4-bit register.
See (5-1) "how to adjust the Contrast of LCD".
Set the binary code "0000" when contrast adjustment is unused.

C_3	C_2	C_1	C_0	V_{LCD}
0	0	0	0	low
		:		
1	1	1	1	high

$V_{LCD} = V_{LCD2} - V_{SS}$

(i)Set DD/MK RAM Address

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	0	0	1	0	0	A	A	A	A	A

The DD/MK RAM address set instruction is executed when the code "1" is written into DB_7 and the address is written into DB_4 to DB_0 as shown above.
The address data (DB_4 to DB_0) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed DD/MK RAM.
The RAM includes DD RAM and MK RAM, and these RAMs are shared by address as shown below.

		RAM address
DD RAM	:	$(00)_H$ - $(0E)_H$
MK RAM	:	$(10)_H$ - $(1E)_H$

(j)Set CG RAM Address

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
コード	0	1	A	A	A	A	A	A	A	A

The CG RAM address set instruction is executed when the "H" level input to the AC terminal and the address is written into DB_7 to DB_0 as shown above.
The address data (DB_7 to DB_0) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed RAM.
The RAM includes CG RAM address as shown below.

		RAM address
CG RAM	:	$(00)_H$ - $(1F)_H$

(k)Write Data to CG, DD or MK RAM

Write Data to RAM instruction is executed when the "H" level input to the RS terminal.
By the execution of this instruction, the binary 8-bit data (A_7 to A_0) are written into the DD RAM, and the binary 5-bit data (A_4 to A_0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

-Write Data to DD RAM

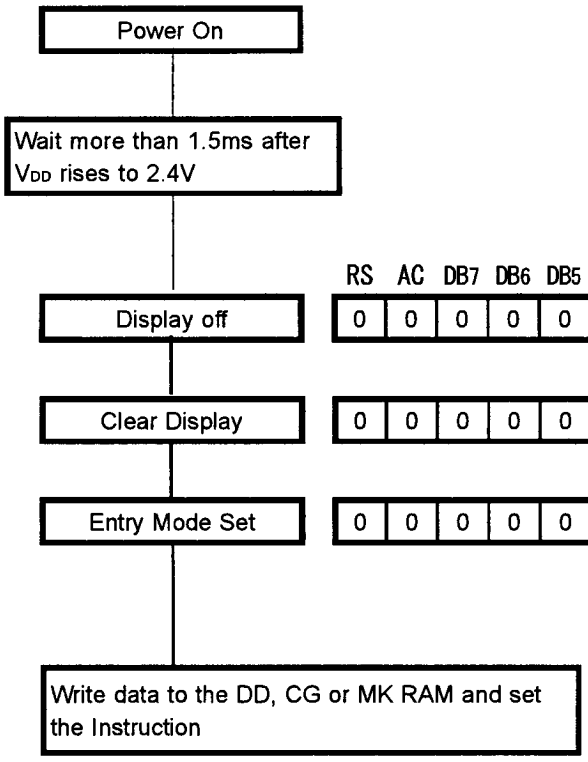
	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	1	0	D	D	D	D	D	D	D	D

-Write Data to CG or MK RAM

	RS	AC	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
code	1	0	0	0	0	D	D	D	D	D

(4-2)Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not satisfied, the NJU6623A must be initialized by the instruction.



Initialized.
No display appears.

Example for set address increment and cursor right shift when the data write to the DD, CG or MK RAM.

Note : When the Icon display function using, the system should be initialized by software initialization.

(5)LCD display

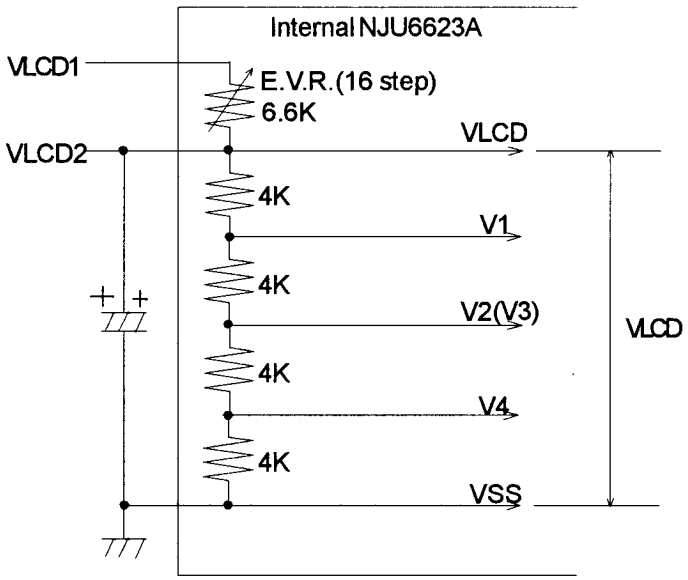
(5-1)Bleeder Resistance

Each LCD driving voltage (V_1, V_2, V_3, V_4) is LCD driving high voltage input to the VLCD1 terminal, generated by the E.V.R. and high impedance bleeder resistance.
The bleeder resistance is set 1/4 bias suitable for 1/8 duty ratio.
The capacitor connected between VLCD2 and V_{SS} is needed for stabilizing VLCD. The determination of the each capacitance requires to operate with the LCD panel actually.

LCD Driving Voltage vs Duty Ratio

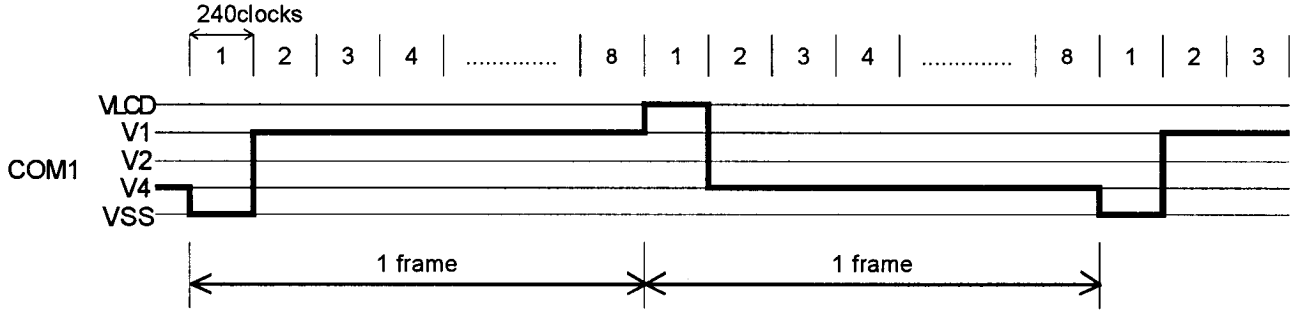
Power supply	Duty Ratio	1/8
	Bias	1/4
V_{LCD}		VLCD2- VSS

V_{LCD} is the maximum amplitude for LCD driving voltage.



(5-2)Relation between oscillation frequency and LCD frame frequency

As the NJU6623A incorporate oscillation capacitor and resistor for CR oscillation, 153kHz oscillation is available without any external components.
The LCD frame frequency example mentioned below is based on 153kHz oscillation.(1clock =6.54us)

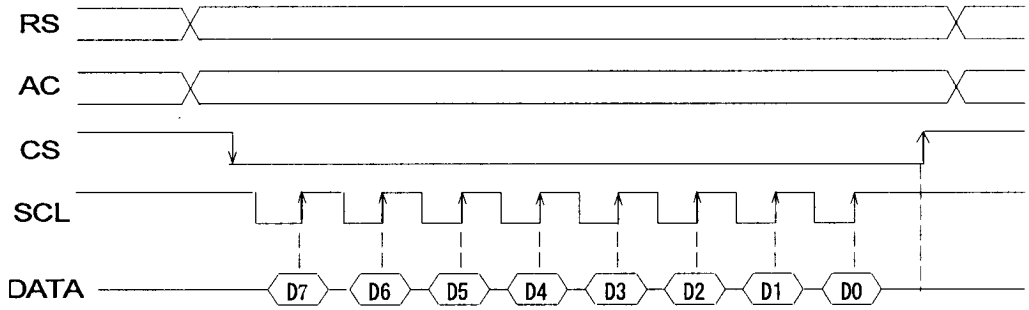


1 frame = 6.54(us) x 240 x 8 = 12.55(ms)
Frame frequency = 1 / 12.55(ms) = 79.68(Hz)

(6)Interface with MPU

Serial interface circuit is activated when the chip select terminal (CS) goes to "L" level. The data input is MSB first like as the order of DB_7, DB_6 ····· DB_0.
The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The latest 8-bit data in the shift register converts to parallel data at the CS rise edge input.
In case of entering over than 8-bit data, valid data is last 8-bit data.
The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



■ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage(1)	VDD	-0.3 to +7.0	V	
Supply Voltage(2)	VLCD1	VSS+10.5 to VSS+0.3	V	VLCD1 Terminal
Input Voltage	V_{IN}	-0.3 to VDD+0.3	V	
Operating Temperature	Topr	-30 to +80	°C	
Storage Temperature	Tstg	-55 to +125	°C	

Note 1 : If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause mal function and poor reliability.
Note 2 : Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the Voltage converter.
Note 3 : All voltage values are specified as V_{SS} = 0V
Note 4 : The relation : $V_{DD} > V_{SS}$, $V_{DD} > V_{SS} \geq V_{SOUT}$, V_{SS}=0V must be maintained.

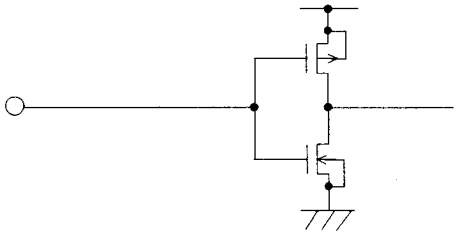
■ELECTRICAL CHARACTERISTICS

(VDD=4.5V to 5.5V, Ta=-40°C to +80°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage		VIH		0.8VDD	-	VDD	V	5
		VIL		VSS	-	0.2VDD	V	5
Output Voltage		VOH	-IOH=2mA,VDD=5V	4.0	-	-	V	6
		VOL	IOL=2mA,VDD=5V	-	-	0.5	V	6
Driver On-resist.(COM)		RCOM	±Id=1uA(COM Terminal) Vo=VLCD,VSS,V1,V4	-	-	40	KΩ	8
Driver On-resist.(SEG)		RSEG	±Id=1uA(SEG Terminal) Vo=VLCD,VSS,V2	-	-	40	KΩ	8
Input Leakage Current		ILI	VIN=0 to VDD	-1.0	-	1.0	uA	10
Operating Current		IDD1	VDD=5V fosc=153KHz Ta=25°C, display	-	T.B.D.	-	uA	7
		IDD2	VDD=5V, Ta=25°C stand-by mode	-	T.B.D.	-	uA	7
Bleeder resistance circuit	LCD Driving Voltage	V1	VLCD1-VSS=8V,Ta=25°C E.V.R. value "1111" COM/SEG terminal	5.8	6.0	6.2	V	
		V2		3.8	4.0	4.2	V	
		V4		1.8	2.0	2.2	V	
	Bleeder resistance	RB	VLCD1-VSS=8V,Ta=25°C E.V.R. value "1111"	11.2	16.0	20.8	KΩ	
Oscillation Frequency		fosc	VDD=5V,Ta=25°C	77	153	229	KHz	
LCD Display Voltage		VLCD1	VLCD1 Terminal,VSS=0V	VDD	-	10.0	V	9
VCD1 Current		ILCD1	VLCD1-VSS=8V			1	mA	

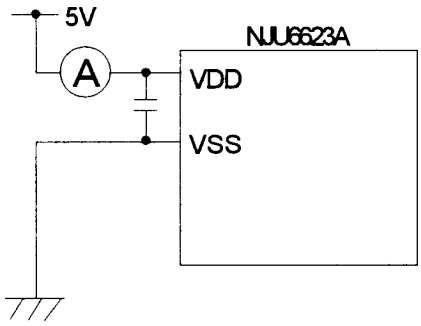
Note 5 : Input structure except LCD driver are shown below:

Input Terminal Structure
RS,AC,SCL,DATA,$\overline{CS}$,$\overline{RESET}$,$\overline{INH}$ Terminals



Note 6 : Apply to the Output and Input/Output Terminals.
Note 7 : Except Input/output current. If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

-Operating Current Measurement Circuit



Note 8 : R_{COM} and R_{COM} are the resistance values between power supply terminals (V_{SS}, VLCD2 or V_1,V_2,V_4) and each common terminal (COM_1 to COM_7/COMMK) and supply voltage (V_{SS}, VLCD2 or V_1,V_2,V_4) and each segment terminal (SEG_1 to SEG_{75}) respectively, and measured when the current I_d is flown on every common and segment terminals at a same time.
Note 9 : Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD}, V_{SOUT}) at no load condition.
Note 10: Apply to the RS,AC,SCL,DATA,$\overline{CS}$,$\overline{RESET}$,$\overline{INH}$.

■ Bus timing characteristics

-Serial Interface Sequence

(V_{DD}=4.5V～5.5V, VLCD1=V_{SS}+8.0V, Ta=25°C)

PARAMETER	SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial clock cycle time	t_{CYCE}	1	-	fig.1	us
Serial clock width	t_{SC}	300	-		ns
Chip select pulse width	PW_{CS}	100	-		us
Chip select set up time	t_{CSU}	300	-		ns
Chip select hold time	t_{CH}	300	-		ns
Serial input data set up time	t_{SISU}	300	-		ns
Serial input data hold time	t_{SIH}	300	-		ns
Register select set up time	t_{RS}	300	-		ns
Register select hold time	t_{RH}	300	-		ns
Address change set up time	t_{AS}	300	-		ns
Address change hold time	t_{AH}	300	-		ns

Serial Interface

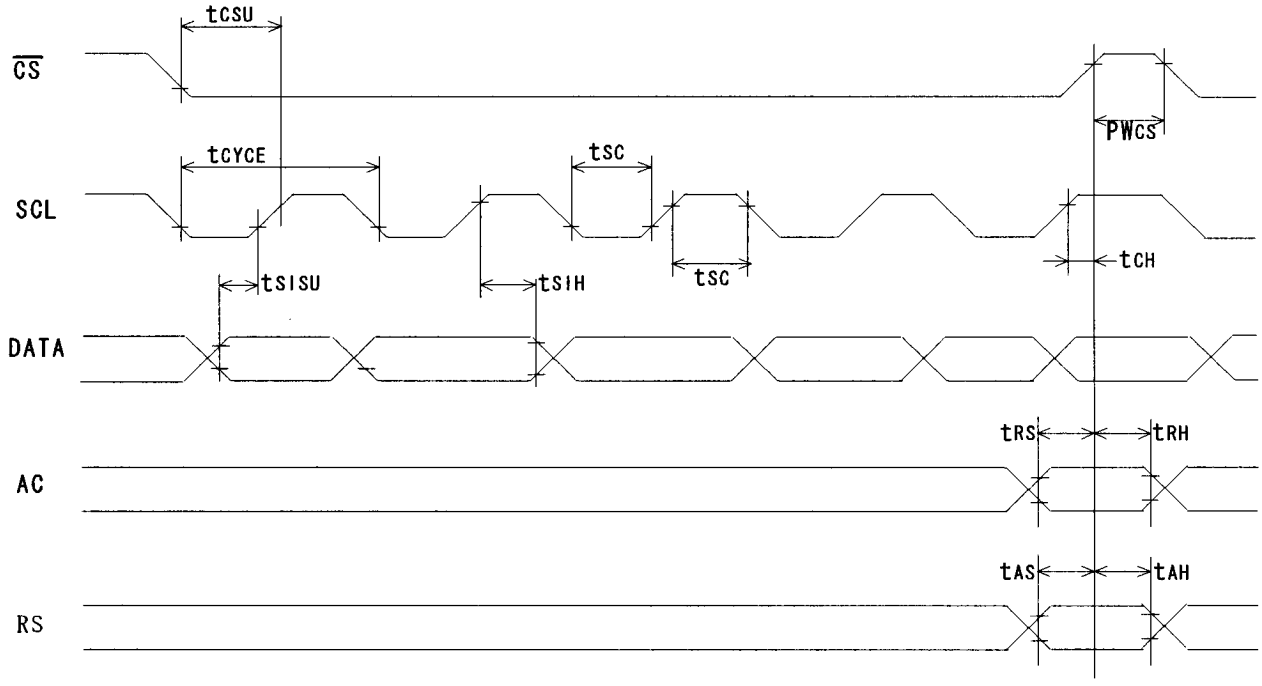
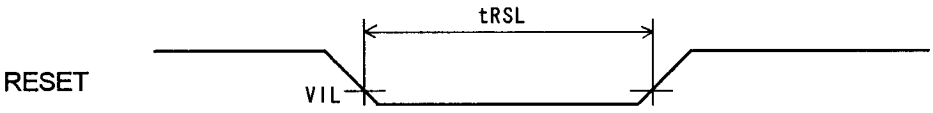


fig.1

-The Input Condition when using the Hardware Reset Circuit

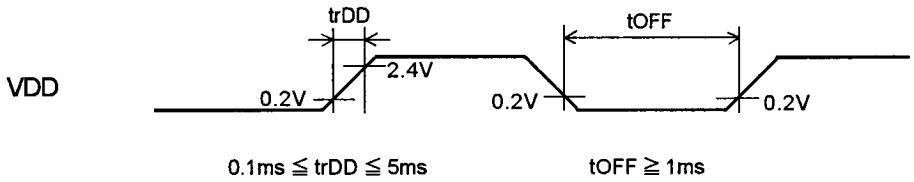


PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Reset input "0" level width	t_{RSL}	f_{OSC}=153kHz	1.2	-	ms

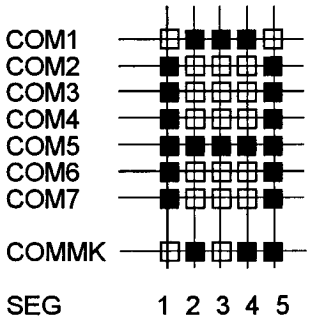
-Power Supply Condition when using the internal initialization circuit (Ta=25°C)

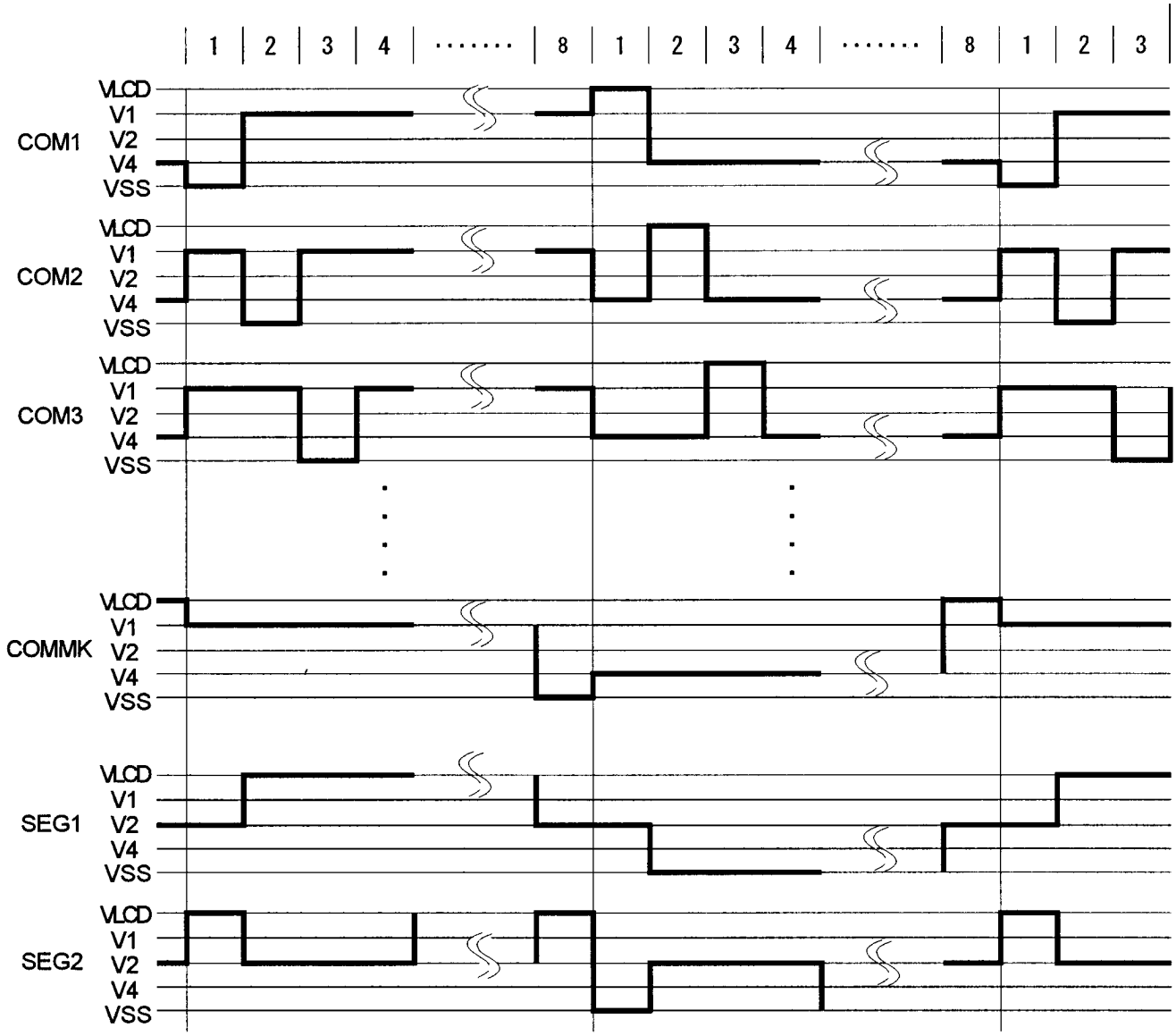
PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Power supply rise time	t_{rDD}	-	0.1	5	ms
Power supply OFF time	t_{OFF}	-	1	-	ms

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction. (Refer to initialization by the instruction)



■LCD DRIVING WAVE FORM





■APPLICATION CIRCUITS

15-character 1-line Display Example