

M33281GS-20

CMOS FLOATING-POINT PROCESSING UNIT (M32/FPU)

T-49-12-05

DESCRIPTION

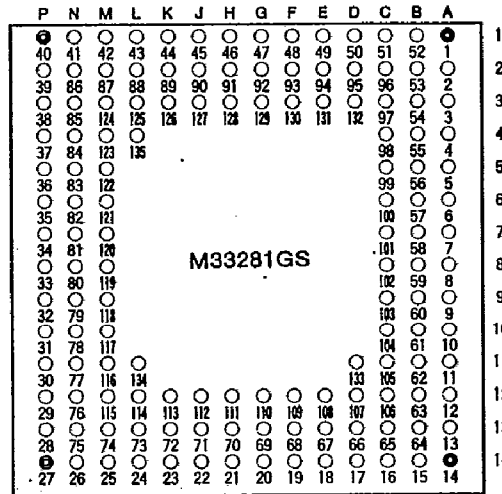
M33281GS-20 is a high-speed floating-point arithmetic LSI unit, and support the extended precision data format of IEEE standard.

The M33281GS-20 is designed to give maximum performance as a coprocessor for M32 family microprocessors (M33220GS-20, M33230GS-20). In addition to arithmetic operations and square roots, it has elementary function instructions, inner product instructions for fast matrix and vector calculations, area discrimination instructions for clipping discrimination, graphics oriented instructions and many more.

FEATURES

- Performance (20MHz operation with M33220GS-20)
 - Addition or subtraction 0.5 μ s
 - Multiplication 0.45 μ s
 - Division 1.5 μ s
- Elementary function calculation
- Graphics support
- Conforms to IEEE754
- Fast coprocessor interface
- Comprehensive system functions
- Software and system support
- Variety of instruction types
 - 31 arithmetic related
 - 21 control related
- 16 floating point operation registers (80-bit)

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8X-A

- Peripheral device mode specifiable (for use when MPU lacks coprocessor interface)
- Package 135 pin PGA

APPLICATION

Scientific and technical calculations, engineering diagram processing

PIN ASSIGN

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	V _{SS}	B10	61	CPDC	D12	107	D ₁₆	H3	128	D ₁₀	L14	24	V _{CC}	N9	79	V _{SS}
A2	2	A ₂₉	B11	62	BERR	D13	66	D ₁₉	H12	111	V _{CC}	M1	42	V _{SS}	N10	78	V _{CC}
A3	3	HACK	B12	63	CPST ₂	D14	17	V _{CC}	H13	70	V _{SS}	M2	87	FCPST ₁	N11	77	V _{CC}
A4	4	BC ₂	B13	64	V _{SS}	E1	49	V _{CC}	H14	21	V _{CC}	M3	124	LD	N12	76	V _{CC}
A5	5	R/W	B14	15	V _{CC}	E2	94	D ₃	J1	45	D ₉	M4	123	CPID ₁	N13	75	V _{SS}
A6	6	BAT ₀	C1	51	V _{CC}	E3	131	D ₀	J2	90	D ₁₁	M5	122	IRL	N14	26	V _{SS}
A7	7	V _{SS}	C2	96	V _{CC}	E12	108	D ₁₈	J3	127	D ₁₃	M6	121	V _{SS}	P1	40	V _{CC}
A8	8	NC	C3	97	A ₂₈	E13	67	D ₂₁	J12	112	D ₂₉	M7	120	V _{SS}	P2	39	RESET
A9	9	V _{SS}	C4	98	BC ₀	E14	18	D ₂₃	J13	71	D ₂₇	M8	119	V _{CC}	P3	38	CPID ₀
A10	10	V _{SS}	C5	99	BC ₃	F1	48	D ₆	J14	22	D ₂₈	M9	118	V _{CC}	P4	37	V _{SS}
A11	11	V _{CC}	C6	100	V _{SS}	F2	93	D ₄	K1	44	V _{SS}	M10	117	V _{CC}	P5	36	SI216
A12	12	V _{SS}	C7	101	BAT ₂	F3	130	D ₂	K2	89	D ₁₂	M11	116	V _{CC}	P6	35	NC
A13	13	CPST ₀	C8	102	V _{CC}	F12	109	D ₂₀	K3	126	D ₁₅	M12	115	V _{CC}	P7	34	V _{CC}
A14	14	V _{CC}	C9	103	V _{CC}	F13	68	V _{CC}	K12	113	D ₃₀	M13	74	V _{CC}	P8	33	CLKI
B1	52	V _{SS}	C10	104	RETRY	F14	19	V _{SS}	K13	72	D ₂₈	M14	25	D ₃₁	P9	32	V _{SS}
B2	53	V _{CC}	C11	105	DC	G1	47	V _{SS}	K14	23	V _{SS}	N1	41	FCPST ₂	P10	31	FCPDC
B3	54	A ₂₇	C12	106	CPST ₁	G2	92	D ₇	L1	43	V _{CC}	N2	86	V _{SS}	P11	30	V _{CC}
B4	55	BC ₁	C13	65	D ₁₇	G3	129	D ₅	L2	88	D ₁₄	N3	85	UD	P12	29	V _{CC}
B5	56	BS	C14	16	V _{SS}	G12	110	D ₂₂	L3	125	V _{SS}	N4	84	CPID ₂	P13	28	NC
B6	57	V _{CC}	D1	50	V _{SS}	G13	69	D ₂₄	L4	135	V _{CC}	N5	83	V _{CC}	P14	27	V _{CC}
B7	58	BAT ₁	D2	95	D ₁	G14	20	D ₂₅	L11	134	FCPST ₀	N6	82	V _{CC}			
B8	59	V _{SS}	D3	132	V _{SS}	H1	46	D ₈	L12	114	V _{SS}	N7	81	V _{SS}			
B9	60	CDE	D11	133	V _{SS}	H2	91	D ₁₀	L13	73	V _{SS}	N8	80	CLKI			

Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

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BLOCK DIAGRAM

