Quad HOTLinkII™ SERDES

Features

- **Second generation HOTLink® technology**
- **Fibre-Channel and Gigabit-Ethernet-compliant**
- **10-bit unencoded data transport**
  - **Aggregate throughput of 12 GB/s**
- **Selectable parity check/generate**
- **Four independently controlled 10-bit channels**
- **Selectable input clocking options**
- **User selectable framing character**
  - **+Comma, ±comma, or full K28.5 detect**
  - **Single or multicharacter framer for character alignment**
  - **Low-latency option**
- **Synchronous parallel input interface**
  - **User-configurable threshold level**
  - **Compatible with LVTTL, LVCMOS, LVTTL**
- **Synchronous parallel output interface**
  - **Compatible with LVTTL, LVCMOS, LVTTL**
- **200-to-1500 MBaud serial signaling rate**
- **Internal PLLs with no external PLL components**
  - **Separate clock and data-recovery PLL per channel**
  - **Common transmit clock multiplier PLL**
- **Differential PECL-compatible serial inputs**
- **Differential PECL-compatible serial outputs**
  - **Source matched for 50Ω transmission lines**
  - **No external resistors required**
  - **Adjustable amplitude for 100Ω or 150Ω balanced loads**
- **Compatible with fiber-optic modules and copper cables**
- **JTAG boundary scan**
- **Built-in self-test (BIST) for at-speed link testing**
- **Per-channel Link Quality Indicator**
  - **Analog signal detect**
  - **Digital signal detect**
- **Low-power 3W typical**
- **256-ball BGA**
- **0.25µ BiCMOS technology**

Functional Description

The CYP15G0402DX Quad HOTLinkII™ SERDES is a point-to-point communications building block allowing the transfer of pre-encoded data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at speeds ranging from 200 to 1500 MBaud per serial link.

Each transmit channel accepts pre-encoded 10-bit transmission characters in an input register, serializes each character, and drives it out a PECL-compatible differential line driver. Each receive channel accepts a serial data stream at a differential line receiver, deserializes the stream into 10-bit characters, frames these characters to the proper 10-bit character boundaries, and this data becomes register outputs with a recovered character clock. *Figure 1* illustrates typical connections between independent systems and a CYP15G0402DX.

As a second-generation HOTLink device, the CYP15G0402DX extends the HOTLink family to faster data rates, while maintaining serial link compatibility with other HOTLink devices.

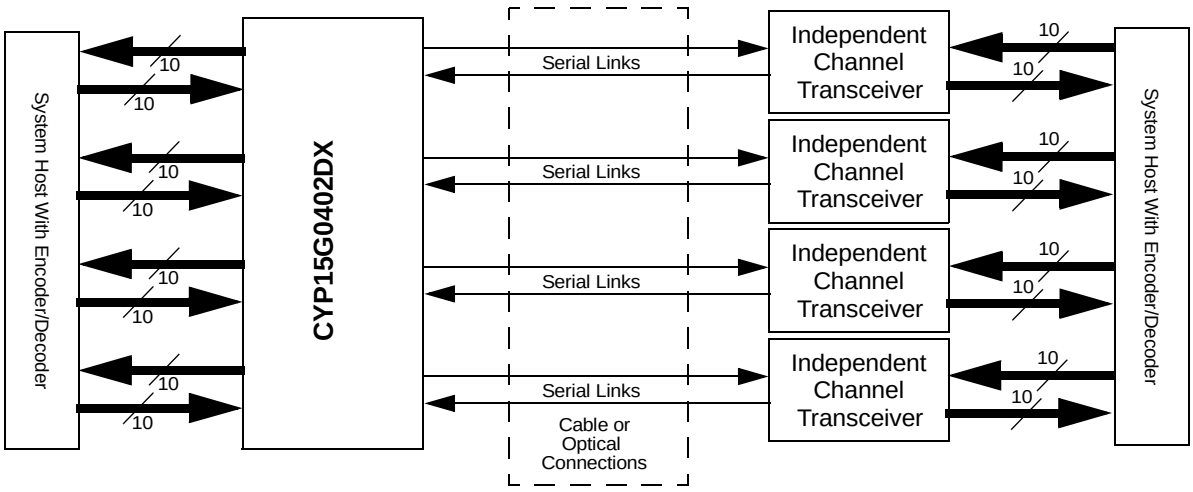


Figure 1. CYP15G0402DX HOTLink II™ System Connections

The transmit section of the CYP15G0402DX Quad HOTLinkII SERDES consists of four byte wide channels that accept a pre-encoded character on every clock cycle. Transmission characters are passed from the Transmit Input Register to a Serializer. The serialized characters are output from a differential transmission line driver at a bit-rate of 10 or 20 times the input reference clock.

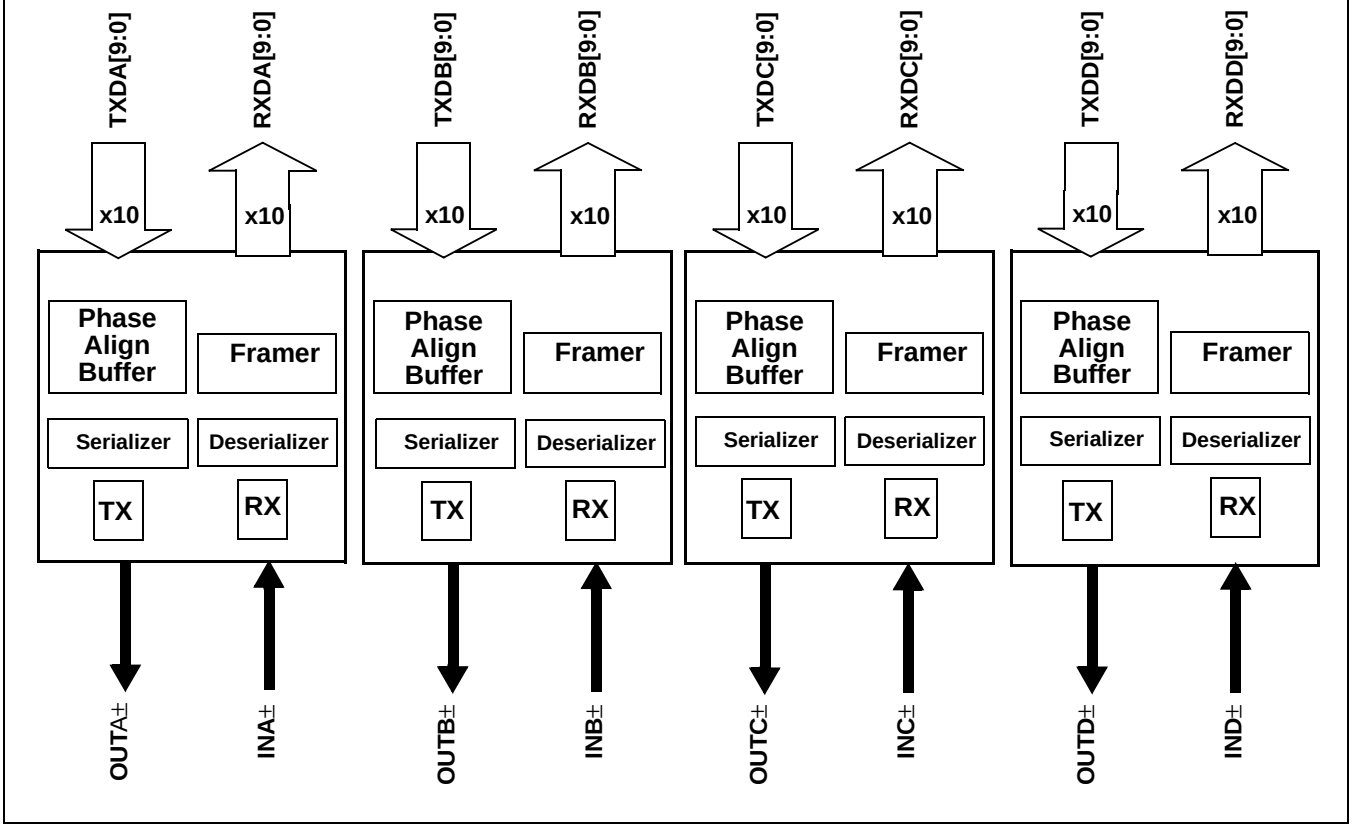
The receive section of the CYP15G0402DX Quad HOTLink II SERDES consists of four byte wide channels. Each channel accepts a serial bit-stream from a PECL-compatible differential line receiver and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters. Recovered characters are then passed to the receiver output register, along with a recovered character clock.

The LVTTL parallel input interface use different clocking sources to provide flexibility in system architecture. The receive output interface may be configured to output the data with a character-rate or half character-rate clock. Both true and complement recovered-clock outputs are available.

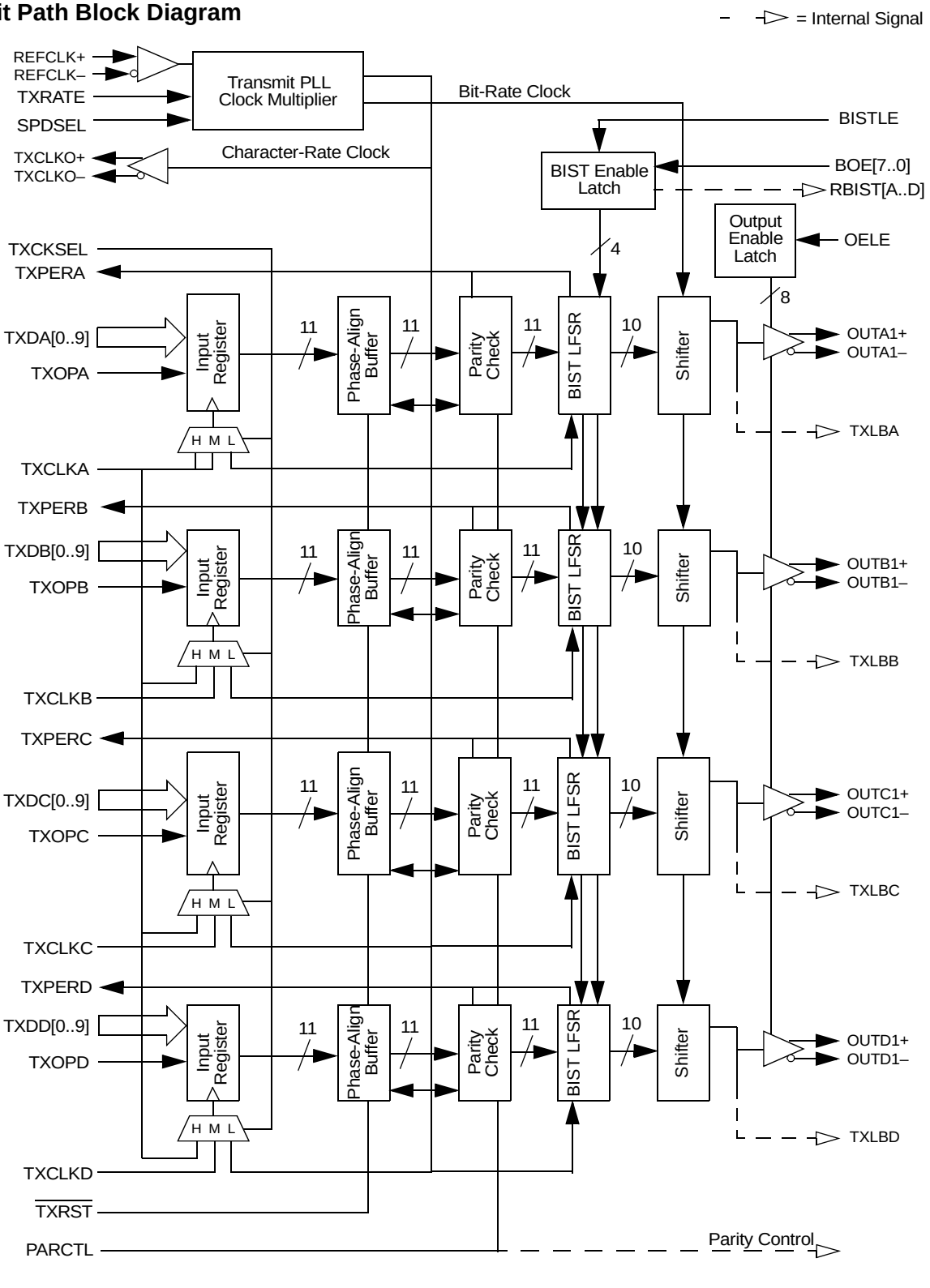
Each transmit and receive channel contains independent Built-In Self-Test (BIST) pattern generators and checkers. This BIST hardware allows at-speed testing of the interface data path.

HOTLink II devices are ideal for a variety of applications to replace parallel interfaces with high-speed, point-to-point serial links.Some applications include interconnecting backplanes on switches, routers, servers and video transmission systems

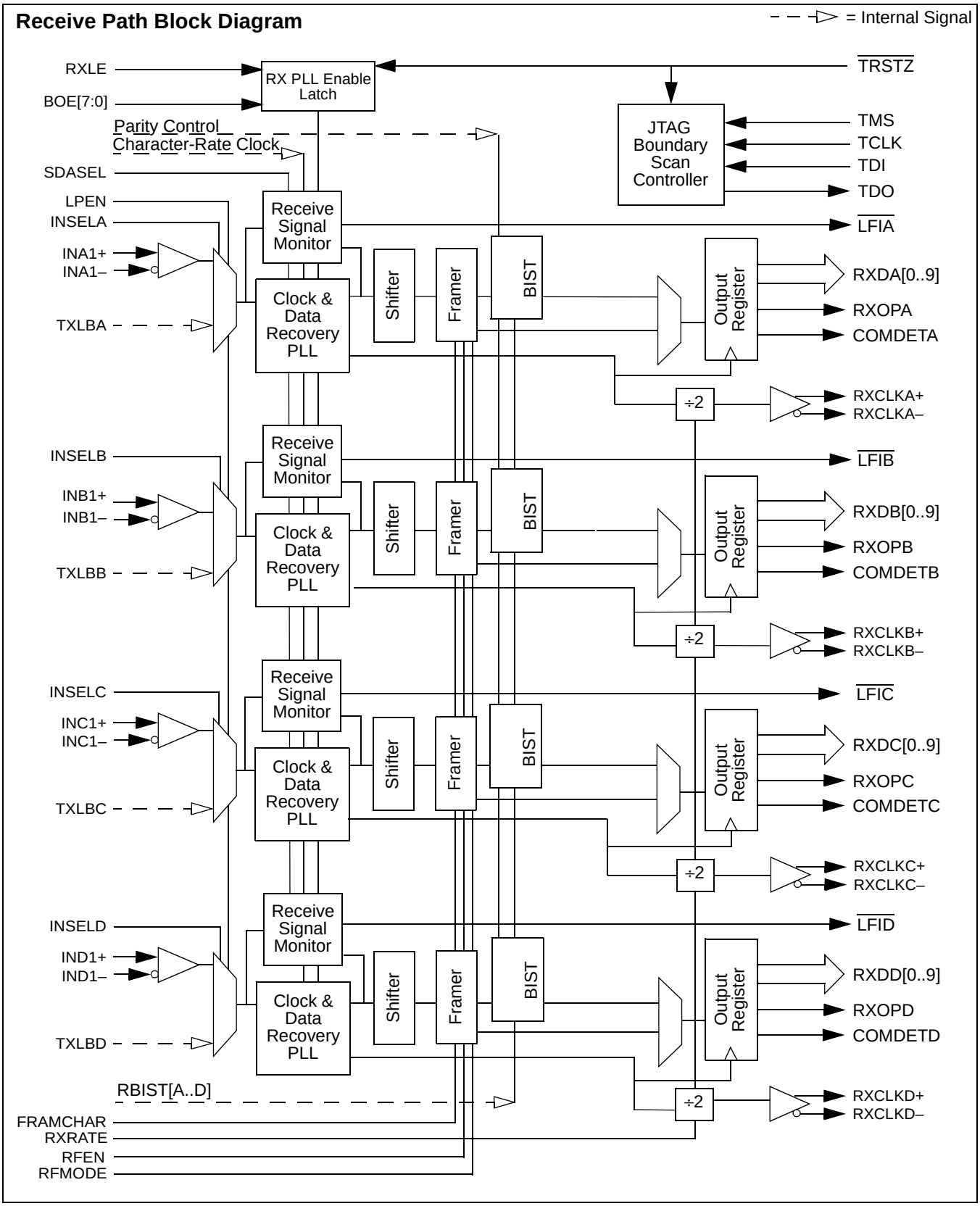
Transceiver Logic Block Diagram



Transmit Path Block Diagram



Receive Path Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	INC-	OUTC -	N/C	N/C	V_{CC}	IND-	OUTD -	GND	N/C	N/C	INA-	OUTA -	GND	N/C	N/C	V_{CC}	INB-	OUTB -	N/C	N/C
B	INC+	OUTC +	N/C	N/C	V_{CC}	IND+	OUTD +	GND	N/C	N/C	INA+	OUTA +	GND	N/C	N/C	V_{CC}	INB+	OUTB +	N/C	N/C
C	TDI	TMS	LP ENC	LP ENB	V_{CC}	PAR CTL	SDAS EL	GND	BOE[7]	BOE[5]	BOE [3]	BOE [1	GND	GND	GND	V_{CC}	TX RATE	RX RATE	N/C	TDO
D	TCLK	$\overline{\text{TRSTZ}}$	LP END	LP ENA	V_{CC}	RF MODE	SPD SEL	GND	BOE[6]	BOE[4]	BOE [2]	BOE [0]	GND	GND	GND	V_{CC}	N/C	RXLE	N/C	N/C
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	TX PERC	TX OPC	TXDC [0]	RXCK SEL													BISTL E	RXDB [0]	RXOP B	RXDB [1]
G	TXDC [7]	TXCK SEL	TXDC [4]	TXDC [1]													GND	OELE	FRAM CHAR]	RXDB [3]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	TXDC [9]	TXDC [5]	TXDC [2}	TXDC [3]													COMD ETB	RXDB [2]	RXDB [7]	RXDB [4]
K	RXDC [4]	RX CLKC -	TXDC [8]	$\overline{\text{LFIC}}$													RXDB [5]	RX DB[6]	RXDB [9]	RX CLK B+
L	RXDC [5]	RX CLKC +	TXCLK C	TXDC [6]													RXDB [8]	LFIB	RXCL K B-	TXDB [6]
M	RXDC [6]	RXDC [7]	RXDC [9]	RXDC [8]													TXDB [9]	TXDB [8]	TX DB[7]	TX CLKB
N	GND	GND	GND	GND													GND	GND	GND	GND
P	RXDC [3]	RXDC [2]	RXDC [1]	RXDC [0]													TXDB [5]	TXDB [4]	TX DB[3]	TX DB[2]
R	COM DETC	RX OPC	TX PERD	TX OPD													TXDB [1]	TXDB [0]	TX OPB	TX PERB
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	TXDD [0]	TXDD [1]	TXDD [2]	TXDD [9]	V_{CC}	RXDD [4]	RXDD [3]	GND	RX OPD	RF ENC	REFC LK -	TXDA [1]	GND	TXDA [4]	TXDA [8]	V_{CC}	RXDA [4]	RX OPA	COM DETA	RX DA[0]
V	TXDD [3]	TXDD [4]	TXDD [8]	RX DD[8]	V_{CC}	RXDD [5]	RXDD [1]	GND	COM DETD	RF END	REFC LK +	RFEN B	GND	TXDA [3]	TXDA [7]	V_{CC}	RXDA [9]	RX DA[5]	RX DA[2]	RX DA[1]
W	TXDD [5]	TXDD [7]	$\overline{\text{LFID}}$	RX CLK D–	V_{CC}	RXDD [6]	RXDD [0]	GND	TX CLK O–	$\overline{\text{TX}}$ RST	TX OPA	RFEN A	GND	TXDA [2]	TXDA [6]	V_{CC}	$\overline{\text{LFIA}}$	RX CLK A–	RX DA[6]	RX DA[3]
Y	TX DD[6]	TX CLKD	RXDD [9]	RX CLK D+	V_{CC}	RXDD [7]	RXDD [2]	GND	TX CLK O+	N/C	TX CLKA	TX PERA	GND	TXDA [0]	TXDA [5]	V_{CC}	TXDA [9]	RX CLK A+	RX DA[8]	RX DA[7]

Pin Configuration (Bottom View)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	N/C	N/C	OUTB-	INB-	**V_{CC}**	N/C	N/C	**GND**	OUTA-	INA-	N/C	N/C	**GND**	OUTD-	IND-	**V_{CC}**	N/C	N/C	OUTC-	INC-
B	N/C	N/C	OUTB+	INB+	**V_{CC}**	N/C	N/C	**GND**	OUTA+	INA+	N/C	N/C	**GND**	OUTD+	IND+	**V_{CC}**	N/C	N/C	OUTC+	INC+
C	TDO	N/C	RX RATE	TX RATE	**V_{CC}**	**GND**	**GND**	**GND**	BOE[1	BOE[3]	BOE[5]	BOE[7]	**GND**	SDASEL	PAR CTL	**V_{CC}**	LP ENB	LP ENC	TMS	TDI
D	N/C	N/C	RXLE	N/C	**V_{CC}**	**GND**	**GND**	**GND**	BOE[0]	BOE[2]	BOE[4]	BOE[6]	**GND**	SPD SEL	RF MODE	**V_{CC}**	LP ENA	LP END	$\overline{TRSTZ}$	TCLK
E	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
F	RXDB[1]	RXOPB	RXDB[0]	BISTLE													RXCKSEL	TXDC[0]	TX OPC	TX PERC
G	RXDB[3]	FRAM CHAR]	OELE	**GND**													TXDC[1]	TXDC[4]	TXCK SEL	TXDC[7]
H	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
J	RXDB[4]	RXDB[7]	RXDB[2]	COMDETB													TXDC[3]	TXDC{2}	TXDC[5]	TXDC[9]
K	RX CLKB+	RXDB[9]	RX DB[6]	RXDB[5]													$\overline{LFIC}$	TXDC[8]	RX CLKC-	RXDC[4]
L	TXDB[6]	RXCLKB-	$\overline{LFIB}$	RXDB[8]													TXDC[6]	TXCLKC	RX CLKC+	RXDC[5]
M	TX CLKB	TX DB[7]	TXDB[8]	TXDB[9]													RXDC[8]	RXDC[9]	RXDC[7]	RXDC[6]
N	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
P	TX DB[2]	TX DB[3]	TXDB[4]	TXDB[5]													RXDC[0]	RXDC[1]	RXDC[2]	RXDC[3]
R	TX PERB	TX OPB	TXDB[0]	TXDB[1]													TX OPD	TX PERD	RX OPC	COM DETC
T	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
U	RX DA[0]	COM DETA	RX OPA	RXDA[4]	**V_{CC}**	TXDA[8]	TXDA[4]	**GND**	TXDA[1]	REFCLK-	RF ENC	RX OPD	**GND**	RXDD[3]	RXDD[4]	**V_{CC}**	TXDD[9]	TXDD[2]	TXDD[1]	TXDD[0]
V	RX DA[1]	RX DA[2]	RX DA[5]	RXDA[9]	**V_{CC}**	TXDA[7]	TXDA[3]	**GND**	RFEN B	REFCLK+	RF END	COM DETD	**GND**	RXDD[1]	RXDD[5]	**V_{CC}**	RX DD[8]	TXDD[8]	TXDD[4]	TXDD[3]
W	RX DA[3]	RX DA[6]	RX CLKA–	$\overline{LFIA}$	**V_{CC}**	TXDA[6]	TXDA[2]	**GND**	RFEN A	TX OPA	$\overline{TX}$ RST	TX CLKO–	**GND**	RXDD[0]	RXDD[6]	**V_{CC}**	RX CLKD–	$\overline{LFID}$	TXDD[7]	TXDD[5]
Y	RX DA[7]	RX DA[8]	RX CLKA+	TXDA[9]	**V_{CC}**	TXDA[5]	TXDA[0]	**GND**	TX PERA	TX CLKA	N/C	TX CLKO+	**GND**	RXDD[2]	RXDD[7]	**V_{CC}**	RX CLKD+	RXDD[9]	TX CLKD	TX DD[6]

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPERA TXPERB TXPERC TXPERD	LVTTL output, changes following TXCLKO↑	**Transmit Path Parity Error**. Active HIGH parity checking must be enabled and a parity error will be detected. This output is HIGH for one TXCLKO± clock period to indicate detection of a parity error in the character presented to the shifter. When parity error is detected, the character in error is replaced with a +C0.7 character to force a corresponding bad character detection at the remote end of the link. This replacement takes place only when parity checking is enabled (PARCTL ≠ LOW). When BIST is enabled for a transmit channel, BIST progress is presented on the associated TXPERx output. Once every 511 character times, TXPERx pulses HIGH for one TXCLKO± period to indicate a complete pass through the BIST sequence. When the transmit Phase Align Buffers are enabled (TXCKSEL ≠ LOW), if an underflow or overflow condition is detected, TXPERx for that channel is asserted and remains asserted until reset by $\overline{\text{TXRST}}$.
TXDA[9:0] TXDB[9:0] TXDC[9:0] TXDD[9:0]	LVTTL input, synchronous, sampled by the respective TXCLKx↑ or TXCLKO↑	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock and passed to the transmit shifter. TXDx[9:0] specify the specific transmission character to be sent.
TXOPA TXOPB TXOPC TXOPD	LVTTL input, synchronous, sampled by the respective TXCLKx↑ or TXCLKO↑	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the ODD parity captured at these inputs is XORed with the bits on the associated TXDx bus to verify the integrity of the captured character.
Transmit Path Clock and Control		
TXCLKO±	LVTTL output	**Transmit Clock Output**. This true and complement clock is synthesized by the transmit PLL and is synchronous to the internal transmit character clock. It operates at either the same frequency as REFCLK, or at twice the frequency of REFCLK. TXCLKO± is always equal to the VCO bit-clock frequency ÷10. The TXCLKO+ output rising edges and TXCLKO– falling edges are phase aligned to the rising edges of the REFCLK input.
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous	**Transmit Clock Phase Reset, active LOW**. When LOW, the transmit Phase Align Buffers are allowed to adjust their data transfer timing to allow clean transfer of data from the Input Register to the transmit shifter. When $\overline{\text{TXRST}}$ is HIGH, the internal phase relationship between the selected TXCLKx and the internal character-rate clock is fixed. During this reset alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit elasticity buffers are adjusted.
TXCKSEL	3-Level Select[1] Static Control Input	**Transmit Clock Select**. Selects the clock source used to write data into the transmit Input Register. When LOW, all four input registers are clocked by the internal TXCLKO↑ derivative of REFCLK. When TXCKSEL is MID, TXCLKx↑ is used as the input register clock for the associated TXDx[9:0] and TXOPx. When HIGH, TXCLKA↑ is used to clock data into the input register for all channels.
TXRATE	LVTTL Input, asynchronous, internal pull-up	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiples REFCLK by 10 to generate the serial bit-rate clock. See *Table 3* for a list of operating serial rates. When REFCLK is selected for clocking of the receive parallel interfaces, the TXRATE input also determines if the clock on the RXCLKA± and RXCLKC± outputs is a full or half-rate clock. When TXRATE = HIGH, these clocks are half-rate clocks. When TXRATE = LOW, these output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLK input.
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input asynchronous, internal pull-up	**Transmit Path Input Clocks**. These inputs are only used when TXCKSEL ≠ LOW. These clocks are frequency coherent to TXCLKO±, but may be offset in phase. Operating phase is adjusted when $\overline{\text{TXRST}}$ is LOW; and phase locked when $\overline{\text{TXRST}}$ is HIGH.

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
Receive Path Data Signals		
RXDA[9:0] RXDB[9:0] RXDC[9:0] RXDD[9:0]	LVTTL Output, synchronous	**Receive Data Output**. These outputs change following the rising edge of the associated RXCLKx± clock.
COMDETA COMDETB COMDETC COMDETD	LVTTL Output, synchronous	**Frame Character Detected**. The character in the output register matches that of the selected framing character.
RXOPA RXOPB RXOPC RXOPD	Three-state, LVTTL Output	**Receive Path Odd Parity**. When PARCTL isn't low parity generation is enabled, the parity output at these pins is valid for the data on the associated RXDx bus bits. When PARCTL=LOW parity generation is disabled, these output drivers are High-Z.
RXRATE	LVTTL Input Static Control Input	**Receive Clock Rate Select**. When LOW, the RXCLKx± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–. When HIGH, the RXCLKx± recovered clock outputs are complementary clocks operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When operating with REFCLK clocking of the received parallel data outputs both RXCKSEL and RXRATE must be LOW.
REFCLK±	Differential LVPECL or single-ended LVCMOS input clock	**Reference Clock**. This clock input is used as the timing reference for the transmit and receive PLLs. This input clock may also be selected to clock the transmit and receive parallel interfaces. For an LVCMOS or LVTTL input clock connect clock source to REFCLK to the input pin and float the other REFCLK–. For an LVPECL input level input clock has to be a differential clock, using both inputs. For an LVPECL differential clock, both inputs must have a phase difference of 180 degrees. When TXCKSEL is LOW, a character-rate derivative of REFCLK is used as the clock for the parallel transmit data input interface.
SPDSEL	3-Level Select[1], Static Control Input	**Serial Rate Select**. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 200–400 MBaud, MID = 400–800 MBaud, HIGH = 800–1500 MBaud.
Analog I/O and Control		
OUTA± OUTB± OUTC± OUTD±	CML Differential Output	**Differential Serial Data Outputs**. These CML outputs are capable of driving terminated transmission lines or standard fiber-optic transmitter modules.
INA± INB± INC± IND±	LVPECL Differential Input	**Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx± serial stream is fed to the receiver to extract the data and clock content when LPENx is LOW.
SDASEL	3-Level Select[1], static configuration input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 4*.
LPENA LPENB LPENC LPEND	LVTTL Input, asynchronous, internal pull-down	**Loop-Back-Enable**. When HIGH, the transmit serial data from the associated channel is internally routed to its respective receiver clock and data recovery (CDR) circuit. The serial output for the channel where LPENx is active is forced to differential logic-1, and serial data inputs for that channel are ignored.

Pin Descriptions

Quad HOTLink II SERDES

Name	I/O Characteristics	Signal Description
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. When OELE = HIGH, the signals on the BOE[7:0] inputs directly control the OUTx± differential drivers. When the BOE[x] input is HIGH, the associated OUTx± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTx± differential driver is powered down. When OELE returns LOW, the last values BOE[7:0] are captured. The specific mapping of BOE[7:0] signals to transmit output enables is listed in *Table 2*. If the device is reset, the latch is reset to enable all outputs.
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit and Receive BIST Latch Enable**. When BISTLE = HIGH, the signals on the BOE[7:0] inputs directly control the transmit and receive BIST enables. When BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data mode. When BISTLE returns LOW, value present on BOE[7:0] is captured. The specific mapping of BOE[7:0] signals to transmit and receive BIST enables is listed in *Table 2*. If the device is reset, this enable latch is reset to disable BIST on all transmit and receive channels.
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-Control Latch Enable**. When RXLE = HIGH, the signals on the BOE[7:0] directly control the power enables for the receive PLLs and analog logic. When the BOE[7:0] input is HIGH, the all receive channels PLL's and analog logic are active. When the BOE[7:0] input is LOW, all the receive channels are in a power down mode. When RXLE returns LOW, BOE[7:0] values are captured. The specific mapping of BOE[7:0] signals to the associated receive channel enables is listed in *Table 2*. If the device is reset, the latch is reset to enable all receive channels.
BOE[7:0]	LVTTL Input, asynchronous, internal pull-up	**BIST, Serial Output, and Receive Channel Enables**. These inputs are passed through the output enable latch when OELE is HIGH, and captured in this latch when OELE returns LOW. These inputs are passed through the BIST enable latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed through the Receive Channel enable latch when RXLE is HIGH, and captured in this latch when RXLE returns LOW.
$\overline{\text{LFIA}}$ $\overline{\text{LFIB}}$ $\overline{\text{LFIC}}$ $\overline{\text{LFID}}$	LVTTL Output, changes following RXCLKx↑	**Link Fault Indication Output**. Active LOW. LFI* is the logical OR of three internal conditions on the associated channel: 1. received serial data frequency outside expected range; 2. analog amplitude below expected levels; and 3. transition density lower than expected.
JTAG Interface		
TMS	LVCMOS Input, internal pull-up	Test Mode Select. Enables JTAG Test Mode
TCLK	LVCMOS Input, internal pull-down	JTAG Test Clock
TDO	Three-state LVCMOS Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVCMOS Input, internal pull-up	**Test Data In**. JTAG data input port.
$\overline{\text{TRSTZ}}$	LVCMOS Input, internal pull-up	**Test Reset**. JTAG and full chip reset. Active LOW. Initializes the JTAG controller and all other state machines.
Power		
V_{CC}		+3.3V power
GND		Signal and power ground for all internal circuits

Name	I/O Characteristics	Signal Description
FRAMCHAR	3-Level Select[1] Static Control Input	Framing Character Select. Used to control the type of character used for framing the received data streams. When LOW, the framer looks for an 8-bit positive COMMA character in the data stream. When MID, the framer looks for both positive and negative disparity versions of the 8-bit COMMA character. When HIGH, the framer looks for both positive and negative disparity versions of the K28.5 character.
RFMODE	3-Level Select[1] Static Control Input	Reframe Mode Select. Used to control the type of character framing system. This signal operates in conjunction with the presently enabled channel bonding mode, and the type of framing character selected. When LOW, the low-latency framer is selected. This will frame on the first occurrence of the selected framing character in the received data stream. This framing mode stretches the recovered clock for multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode multi-byte parallel framer is selected. This requires a pair of the selected framing character, on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phasing regardless of character offset. When HIGH, the alternate mode multi-byte parallel framer is selected. This requires detection of the selected framing character of the allowed disparities in the received data stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phasing regardless of character offset.
Receive Path Clock and Clock Control		
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	Three-state, LVTTL Output clock Static control input	**Receive Character Clock**. These true and complement clocks are the Receive interface clocks which are used to control timing of data output transfers. These clocks are output continuously at either character rate of 1/20th or 1/10th the serial bit-rate of the input data.
RFENA RFENB RFENC RFEND	LVTTL Input, asynchronous, internal pull-down	**Reframe Enable**. Active HIGH. When HIGH the framer for the associated channel is enabled to frame as per the framing mode and selected framing character.
RXCKSEL	3-Level Select[1] Static Control Input	**Receive Clock Mode**. Selects the receive clock-source used to transfer data to the output registers. When LOW, all four output registers are clocked by REFCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and RXCLKA± and RXCLKC± present buffered and delayed forms of REFCLK. This clocking mode is required for channel bonding across multiple devices. When MID, each RXCLKx± output follows the recovered clock for the respective channel, as selected by RXRATE. When HIGH, and channel bonding is enabled in dual-channel mode (RX modes 3 and 5), RXCLKA± outputs the recovered clock from either receive channel A or receive channel B as selected by RXCLKB+, and RXCLKC± outputs the recovered clock from either receive channel C or receive channel D as selected by RXCLKD+. These output clocks may operate at the character-rate or half the character-rate as selected by RXRATE. When HIGH and channel bonding is enabled in quad channel mode (RX modes 6 and 8), or if the receive channels are operated in independent mode (RX modes 0 and 2), RXCLKA± and RXCLKC± output the recovered clock from receive channel A, B, C, or D, as selected by RXCLKB+ and RXCLKD+. This output clock may operate at the character-rate or half the character-rate as selected by RXRATE.
Device Control Signals		
PARCTL	3-Level Select[1], Static Control Input	**Parity Check/Generate Control**. Used to control the different parity checks. When LOW, parity checking and generation are disabled, and the RXOPx output drivers are disabled. When MID, the TXDx[9:0] inputs are checked, along with TXOPx, for valid ODD parity, and valid ODD parity is generated for the RXDx[9:0] outputs and presented on RXOPx. When HIGH, the TXDx[9:0] inputs are checked, along with TXOPx, for valid ODD parity. Valid ODD parity is generated for the RXDx[9:0] and COMDETx outputs and presented on RXOPx.

Note:

1. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

CYP15G0402DX HOTLink II SERDES Operation

The CYP15G0402DX is designed to support transfer of large quantities of data, using high-speed serial links. This device contains four byte wide channels.

CYP15G0402DX Transmit Data Path

Data Path
The transmit path of the CYP15G0402DX supports four character-wide data paths. These four data paths are internally unencoded and require input data that is encoded for reliable transport.

Input Register
The bits in the Input Register for each channel have fixed bit assignments, as listed in *Table 1*.

Table 1. Input Register Bit Mapping

Signal Name	Bus Weight	10B Name
TXDx[0] (LSB)	2^0	a[2]
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXDx[8]	2^8	h
TXDx[9] (MSB)	2^9	j
TXOPx[3]		

Each input register captures 10 bits on each input clock cycle. When parity checking is enabled, the TXOPx parity input is also captured in the associated input register.

Input Register Clocking
The transmit Input Registers can be configured to accept data relative to different clock sources. The selection of the clock source is controlled by TXCKSEL.
When TXCKSEL is LOW, the transmit Input Registers capture data synchronous to the TXCLKO a derivative of REFCLK. When TXCKSEL is MID, the rising edge of TXCLK is used to capture the data at the associated TXDx[9:0] and TXOPx inputs. When TXCKSEL is HIGH, the rising edge of TXCLKA is used to capture the data at the associated TXDx[9:0] and TXOPx inputs on all four channels.

Phase-Align Buffer
Data from the Input Registers is normally routed to the associated Phase-Align Buffer. If the transmit Input Registers are configured to capture data synchronous to REFCLK (TXCKSEL = LOW), the Phase-Align Buffers are bypassed and data is passed directly to the parity check and serializer blocks.
When the Input Registers are clocked with REFCLK and TXCKSEL ≠ LOW, the Phase-Align Buffers are enabled. These buffers will absorb clock phase differences between the presently selected input clock and the internal character clock. $\overline{\text{TXRST}}$ when low will Initialize the Phase-Align Buffers. When $\overline{\text{TXRST}}$ is returned HIGH, the present input clock phase relative to REFCLK is set.
Once set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK. This time-shift allows the delay paths of the character clocks to change due to operating voltage and temperature, while not affecting operation.

Parity Support

In addition to the ten data and control bits that are captured at each channel, a TXOPx input is also available on each channel. This allows the CYP15G0402DX to support ODD parity checking for each channel. When PARCTL is LOW, parity checking is disabled. When PARCTL is MID or HIGH, parity is checked on the TXDx[9:0] and TXOPx bits.
If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character in error is replaced with the 1001111000 pattern an invalid character.

Transmit BIST

The transmitter interfaces contains an internal BIST pattern generators that can be used to validate both device and link operation. This generator is enabled by the associated BOE[x] signals listed in *Table 2* and when BISTLE latch enable input is HIGH. When enabled, a register in the associated transmit channel becomes a pattern generator. This 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical receiver.
When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in that associated transmit channel or the BIST checker in the associated receive channel. When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. BIST is disabled following a device reset by $\overline{\text{TRSTZ}}$.
All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel. If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and reset of clock phase.

Notes:
2. LSB is shifted out first.
3. The TXOPx inputs are also captured in the associated input register, but their interpretation is under the separate control of PARCTL.

Serial Output Drivers

The serial interface Output Drivers make use of differential Current Mode Logic to provide a source-matched driver for the transmission lines. These drivers accept data from the Transmit Shifters. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

When configured for internal local loopback test, LPEN = HIGH, the output drivers for all enabled ports are configured to drive a static differential logic-1.

Each output can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Serial Output Enable latch to control the serial output drivers. The BOE[7:0] input associated with a specific OUTx± driver is listed in *Table 2*.

When OELE is HIGH and BOE[x] is HIGH, the associated serial driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated driver is disabled and in a power down mode. If both outputs for a channel are disabled, the associated internal logic for that channel is also configured for low power operation. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to opened the latch again. **Note**. When a disabled transmit channel is re-enabled, the data on the serial outputs may not meet all timing specifications for up to 10 ms.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiplies that clock by 10 or 20 to generate a bit-rate clock for use by the transmit Shifter.

The clock multiplier PLL can accept a REFCLK input between 10 MHz and 150 MHz, however, this clock range of the PLL is controlled by the TXRATE and SPDSEL input signals of the CYP15G0402DX.

SPDSEL is a 3-level select[1] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signalling rate and allowable range of REFCLK frequencies is listed in *Table 3*.

Table 2. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[7]	X	Transmit D	X
BOE[6]	OUTD±	Receive D	Receive D
BOE[5]	X	Transmit C	X
BOE[4]	OUTC±	Receive C	Receive C
BOE[3]	X	Transmit B	X
BOE[2]	OUTB±	Receive B	Receive B
BOE[1]	X	Transmit A	X
BOE[0]	OUTA±	Receive A	Receive A

Table 3. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	20	200–400
	0	20–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.5V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when the clock signal passes through the internal biased point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a LVPECL clock, or a differential LVTTL or LVCMOS clock.

CYP15G0402DX Receive Data Path

Serial Line Receivers

A differential line receiver, INx±, is on each channel for accepting a serial bit stream. The serial line receiver inputs are differential needing only 100mv pp AC differential input. The input can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules with a ECL/PECL output level. The input could be AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of input signals.

The local loopback input (LPENx) for each channel allows the serial transmit data for the associated channel to be routed internally back to the clock and data recovery circuit associated with that channel. When a channel is configured for local loopback, the associated transmit serial driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers or optical drivers.

Receive Channel Enabled

The CYP15G0402DX contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Receive Channel Enable latch to control the PLLs and logic of the associated receive channel. The BOE[7:0] input associated with a specific receive channel is listed in *Table 2*.

When RXLE and BOE[x] are HIGH, the associated receive channel is enabled to receive a serial stream from the selected line receiver. When RXLE is HIGH and BOE[x] is LOW, the associated receive channel is disabled and powered down.

Signal Detect

Each Line Receiver is simultaneously monitored for:

- analog amplitude
- transition density
- received data stream outside normal frequency range (±200 ppm).

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIx (Link Fault Indicator) output associated with each receive channel. These LFIx outputs change synchronous to the receive interface recovered clock.

While the majority of these signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with attenuated signals. This adjustment is made through the SDASEL signal, a 3-level select[1] input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 4*. SDASEL input controls the analog monitors for all receive channels.

Table 4. Analog Amplitude Detect Valid Signal Levels

SDASEL	Typical Signal with Peak Amplitudes Above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each channel. The clock extraction function is performed by embedded phase-locked loops that track the frequency and phase of transitions of the incoming bit streams.

Each CDR accepts a character-rate or half-character-rate reference clock on the REFCLK± input. This REFCLK± input is used to ensure that the VCO is operating at the correct frequency. The use of the REFCLK improves PLL acquisition time, and limits the unlocked frequency excursions of the VCO when there is no input data.

Regardless of the type of input signal, the CDR will attempt to recover a data stream. If the frequency of the recovered data stream is outside the limits set by the integrated range controls, the PLL reference will switch to REFCLK. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ±200 ppm of the frequency of the clock that drives the REFCLK signal of the *remote* transmitter to ensure a lock to the incoming data stream.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more COMMA or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the frame of the characters that follow.

Framing Character

The CYP15G0402DX allows selection of one of three combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

FRAMCHAR is a 3-level select [1] input that allows selection of one of three different characters or character combinations. These combinations are listed in *Table 5*.

Table 5. Framing Character Selector

FRAMCHAR	Bits Detected in Framer	
	Character Name	Bits Detected
LOW	+COMMA	00111110XX
MID (Open)	+COMMA –COMMA	00111110XX or 11000001XX
HIGH	+K28.5 –K28.5	0011111010 or 1100000101

Framer

The framer on each channel operates in one of three different modes, as selected by the RFMODE input. When RFMODE is LOW, the low-latency framer is selected. This framer operates by stretching the recovered character clock until it aligns with the character boundaries. In this mode the framer aligns on the first detection of the selected framing character.

When RFMODE is MID the Cypress-mode multi-character framer is selected. The detection of multiple framing

characters makes the associated link much more robust to incorrect framing. In this mode the framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock will not contain any significant phase changes or hops during normal operation. This allows the recovered clock to be distributed to other external circuits. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE is HIGH, the alternate-mode multi-character framer is enabled. Like Cypress-mode multi-character framing, multiple framing characters must be detected to adjust the character boundaries. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, before character framing is adjusted.

In systems that use 8B/10B coding running disparity rules prohibit the presence of multiple +COMMA characters as consecutive characters, except for the K28.7 comma character. Because of this, the combination of FRAMCHAR LOW and RFMODE HIGH is not recommended. While framing can still take place while following all 8B/10B coding rules, this configuration prevents framing to the normal K28.5 character. Framing is enabled for a channel when the associated RFENx input is HIGH. When RFENx is LOW, the framer for the associated channel is disabled. When a framer is disabled, no changes are made to the recovered character boundaries on that channel, regardless of the presence of framing characters in the data stream.

BIST LFSR

The output register of each Framer is normally used to pass received characters to the associated output register. When configured for BIST mode, this register becomes a signature pattern generator. When in the BIST mode, a 511-character sequence is generated that includes all Data and Special Character codes, including the explicit violation symbols.This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated receiver checks each character received with each character generated by the LFSR and indicates compare errors and BIST status at the RXDx[2:0] bits of the output register.

These generators are enabled by the associated BOE[x] signals listed in *Table 2* (when the BISTLE latch enable input is HIGH).When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator/checker in the associated receive channel. When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch.These values remain in the BIST Enable Latch until BISTLE is returned high to resample the input again. All captured signals in the BIST Enable Latch are set HIGH and BIST is disabled following a device reset by $\overline{\text{TRSTZ}}$.

The LFSR is initialized by the BIST hardware once the external enable ($\overline{\text{RXBISTEN}}$x) is recognized. The enable resets the BIST LFSR to the BIST-loop start-code of D0.0. D0.0 is sent only at the beginning of the BIST loop. The status of the BIST progress and any character mismatches is appears as an output on the RXDx[2:0] outputs.

Code rule violations or running disparity errors the BIST loop will not cause an error indication. RXDx[2:0] indicates 01X for one RXCLK cycle per BIST loop to indicate loop completion. This can be used to check test pattern progress.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-Test.” The sequence compared by the CYP15G0402DX is identical to that in the CY7B933 and CY7C924, allowing interoperable systems to be built when used at compatible serial signalling rates.

If a large number of errors are detected, the receive BIST state machine aborts the compare operations and resets the LFSR to look for the start of the BIST sequence again.

Table 6. BIST Status Bits

Status			Priority	Description
COMDETx	RXDx[0]	RXDx[1]		BIST Mode ($\overline{\text{RXBISTEN}}$ is LOW)
0	0	0	7	**BIST Data Compare.** Data Character compared correctly.
0	0	1	7	**BIST Command Compare.** Command Character compared correctly.
0	1	0	2	**BIST Last Good.** Last Character of BIST sequence detected and valid.
0	1	1	5	Reserved
1	0	0	4	**BIST Last Bad.** Last Character of BIST sequence was detected invalid.
1	0	1	1	**BIST Start.** RXBISTEN recognized on this channel, but character compares have not yet commenced. Also presented when the receive PLL is tracking REFCLK instead of the selected data stream.
1	1	0	6	**BIST Error.** While comparing characters, a mismatch was found in one or more of the decoded character bits.
1	1	1	3	**BIST Wait.** The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

Power Control

The chip can be powered down one channel at a time. The channel to be selected is controlled by BOE[7:0] latch. Both the transmit and the receive channels are controlled by a receive channel power latch and the transmit channel is controlled by an output enable control system. Powering down

channels will save considerable power and will reduce system heat generation. Controlling system power dissipation will improve the system reliability.

Receive Channel Power-Control Latch Enable. Active HIGH.
When RXLE is HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the receive PLLs and analog circuits. When the BOE[7:0] input is HIGH, the associated receive channel [A.D] PLLs and analog logic are active. When the BOE[7:0] input is LOW, the associated receive channel [A.D] PLL's and analog circuits are in a power down mode. When RXLE returns LOW, the last values present on BOE[7:0] are captured. The channels controlled by BOE[7:0] signals are listed in *Table 2*.
When RXLE is HIGH and BOE[x] is HIGH, the associated receive channel is enabled to receive a serial stream from the selected line receiver. When RXLE is HIGH and BOE[x] is LOW, the associated receive channel is disabled and powered down.

Any disabled channel will indicate a constant /LFIx output.
When a disabled receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms. After powering the chip, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character
When OELE is HIGH and BOE[x] is HIGH, the associated serial driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated driver is disabled and powered down. If both outputs for a channel are disabled, the internal logic for that channel is powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch.

Output Bus

Each receive channel presents a 12-signal output bus consisting of:

- a 10-bit data bus
- a COMMA detect indicator
- a parity bit.

The receive decoder assigns the bit values per *Table 7*.
The externally encoded data, the RXDx[0] corresponds to the MSB of the 10 bit data. The signals present on this output bus are shown in *Table 8*.
The framed 10-bit value is presented to the associated Output Register, along with a status output indicating if the character in the output register matches the selected framing characters.
The COMDETx status outputs operate the same regardless of the bit combination selected for character framing by the FRAMCHAR input. Characters in *Table 5* will cause COMDET assertion, all others characters are mapped to invalid characters. COMDETx is HIGH when the character in the output register of the associated channel contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.
When the low-latency framer and half-rate receive port clocking are enabled, RFMODE and RXRATE are both LOW, the framer will stretch the recovered clock to the next 20-bit boundary such that the rising edge of RXCLKx+ occurs when COMDET is present on the associated output bus.

Table 7. Output Register Bit Assignments [4]

Signal Name	
RXSTx[2] (LSB)	COMDETx
RXSTx[1]	DOUTx[0]
RXSTx[0]	DOUTx[1]
RXDx[0]	DOUTx[2]
RXDx[1]	DOUTx[3]
RXDx[2]	DOUTx[4]
RXDx[3]	DOUTx[5]
RXDx[4]	DOUTx[6]
RXDx[5]	DOUTx[7]
RXDx[6]	DOUTx[8]
RXDx[7] (MSB)	DOUTx[9]

Note:
4. The RXOPx outputs are also driven from the associated output register, but their interpretation is under the separate control of PARCTL.

Table 8. Output Register Bit Assignments

Signal Name	Bus Weight	10B Name
RXOPx[5]		
COMDET[5]		
RXDx[0] (LSB)	2^0	a[6]
RXDx[1]	2^1	b
RXDx[2]	2^2	c
RXDx[3]	2^3	d
RXDx[4]	2^4	e
RXDx[5]	2^5	i
RXDx[6]	2^6	f
RXDx[7]	2^7	g
RXDx[8]	2^8	h
RXDx[9] (MSB)	2^9	j

5. The RXOPx and COMDETx outputs are also driven from the associated output register, but their generation and interpretation are separate from the data bus.
6. LSB will be shifted in first.

When the standard framer is enabled and half-rate receive port clocking are enabled, RFMODE is not low and RXRATE is LOW, the output clock is not modified, but a single pipeline stage may be added or subtracted from the data stream by the framer logic such that the rising edge of RXCLKx+ occurs when COMDET is present on the associated output bus.
This adjustment only occurs when the framer for that channel is enabled (RFENx is HIGH). When the framer is disabled, the

clock boundaries are not adjusted, and COMDETx may be active during the rising edge of RXCLKx–.

Parity Generation

In addition to the ten data and COMDETx status bits that are output on each channel, an RXOPx output is also available on that channel. The CYP15G0402DX to supports ODD parity generation for each channel. To handle a wide range of system environments, the CYP15G0402DX supports two forms of parity and no parity.

- parity on the RXDx[9:0] character
- parity on the RXDx[9:0] character and COMDETx status.

These modes differ in the number bits which are included in the parity calculation. Only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 9*.

Parity generation is enabled through the 3-level select PARCTL input. When PARCTL is LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z).

When PARCTL is MID, ODD parity is generated for the RXDx[9:0] bits.

When PARCTL is HIGH, ODD parity is generated for both the RXDx[9:0] bits and the associated COMDETx signal.

JTAG Support

The CYP15G0402DX contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs and outputs and REFCLK. The high-speed serial signals are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP15G0402DX is ‘0C801069’hex.

Table 9. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)		
	LOW[7]	MID	HIGH
COMDETx			X[8]
RXDx[0]		X	X
RXDx[1]		X	X
RXDx[2]		X	X
RXDx[3]		X	X
RXDx[4]		X	X
RXDx[5]		X	X
RXDx[6]		X	X
RXDx[7]		X	X
RXDx[8]		X	X
RXDx[9]		X	X

Notes:

7. Receive path parity output drivers are disabled when PARCTL is LOW.
8. When BIST is not enabled,COMDETx is usually driven to a logic 0, but will be driven HIGH when the character in the output buffer is the selected framing character.

3-Level Select Inputs

Each 3-Level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11, respectively.

Maximum Ratings

Above which the useful life may be impaired.
For user guidelines, not tested.
Storage Temperature –65°C to +150°C
Ambient Temperature with
Power Applied–55°C to +125°C
Supply Voltage to Ground Potential–0.5V to +3.8V
Output Current into LVTTL Outputs (LOW)30 mA
DC Input Voltage-–0.5V to V_{CC}+0.5V

Static Discharge Voltage> 2000 V
(per MIL-STD-883, Method 3015)
Latch-Up Current> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	–40°C to +85°C	3.3V ± 5%

CYP15G0402DX DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL Compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, Vcc = Min.	2.4	VCC	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, Vcc = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[9]	–15	–35	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL Compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	Vcc+0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK Input, $V_{IN} = V_{CC}$		+1.5	mA
		Other Inputs, $V_{IN} = V_{CC}$		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	$V_{IN} = V_{CC}$		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF}	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.0	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		GND	$V_{CC}/2$	V
V_{COM}	Common Mode Range		0.8	V_{CC}–1.2V	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
V_{IHH}	Input High Current	Vin = Vcc		200	µA
V_{IMM}	Input MID Current	Vin = Vcc/2	–50	50	µA
V_{ILL}	Input LOW Current	Vin = GND		–200	µA

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

Note:
9. Outputs tested one output at a time, output shorted for less than one second, much less than 10% duty cycle.

Differential CML Serial Outputs: OUTA±, OUTB±, OUTC±, OUTD±			Typical	Max	Unit
V_{OHC}	Output HIGH Voltage	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
V_{OLC}	Output LOW Voltage	100Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load	450	800	mV
		150Ω differential load	560	1000	mV

Differential Serial Line Receiver Inputs: INA±, INB±, INC±, IND±					
$VI_{DIFF]}$	Input Differential Voltage |(IN+) – (IN–)|		100	1200	mV
V_{IHE}	Highest Input HIGH Voltage			V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage		V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHH}$ Max.		1000	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILL}$ Min.	–700		µA
Iv_{com}[10]	Input common mode range	((Vcc-2.0)+.05)min., ((Vcc-.05)max.	1.25	3.25	V
Miscellaneous			**Typical**	**Max.**	**Unit**
I_{CC}[11]	Power Supply Current	Commercial	860	1100	mA
		Industrial	TBD	TBD	mA

CYP15G0402DX Transmitter LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{TS}	TXCLKx Clock Cycle Frequency	20	150	MHz
t_{TXCLK}	TXCLKx Period	6.66	50	ns
t_{TXCLKH}	TXCLKx HIGH Time	2.2		ns
t_{TXCLKL}	TXCLKx LOW Time	2.2		ns
t_{TXCLKR} [12]	TXCLKx Rise Time	0.3	1.7	ns
t_{TXCLKF}[12]	TXCLKx Fall Time	0.3	1.7	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLKx↑ (TXCKSEL ≠ LOW)	2		ns
t_{TXDH}	Transmit Data Hold Time from TXCLKx↑ (TXCKSEL ≠ LOW)	1		ns
f_{TOS}	TXCLKO Clock Cycle Frequency equals 1x or 2x REFCLK Frequency	20	150	MHz
t_{TXCLKO}	TXCLKO Period	6.66	50	ns
$t_{TXCLKOD}$	TXCLKOP Duty Cycle Centered with 60 per cent high time	-0.7	+0.7	ns
$t_{TXCLKOD}$	TXCLKON Duty Cycle Centered with 40 per cent high time	-0.0	1.5	ns
t_{TXODS}	Transmit Data Set-Up Time to TXCLKO↑ (TXCKSEL = LOW)	1.5		ns
t_{TXODH}	Transmit Data Hold Time from TXCLKO↑ (TXCKSEL = LOW)	1.5		ns
t_{TXRSS}	$\overline{\text{TXRST}}$ Set-Up Time to TXCLKO↑	3		ns
t_{TXRSH}	$\overline{\text{TXRST}}$ Hold Time from TXCLKO↑	1		ns

Notes:

10. This is the minimum difference in voltage between the true and the complement input required to ensure detection of a logic 1 or logic 0. A logic true occurs when the input + is above the -input. A logic zero is true when the +input is below the voltage of - input.
11. Maximum current is measured with V_{CC} = MAX, RFEN = LOW, with all serial channels sending a constant alternations 01 pattern, and the output unloaded. Typical is measured under same conditions, except that power is 3.3V.
12. Paralleled data output specifications are only valid if all outputs are loaded with similar DC and AC loads.

CYP15G0402DX Transmit Serial Outputs and TX PLL Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		5000	660	ps
t_{RISE}	CML Output Rise Time 20–80% (CML Test Load)[13]	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	200	1000	ps
t_{FALL}	CML Output Fall Time 80–20% (CML Test Load)[13]	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	200	1000	ps
t_{DJ}	Deterministic Jitter (peak-peak)[14, 17]			0.1	UI
t_{TJ}	Total Jitter (σ)[15, 17]	0.2-1.0Gbps		0.2	UI
		1.0-1.5Gbps		192	ps
t_{TXLOCK}	Transmit PLL lock to REFCLK		TBD	TBD	ns

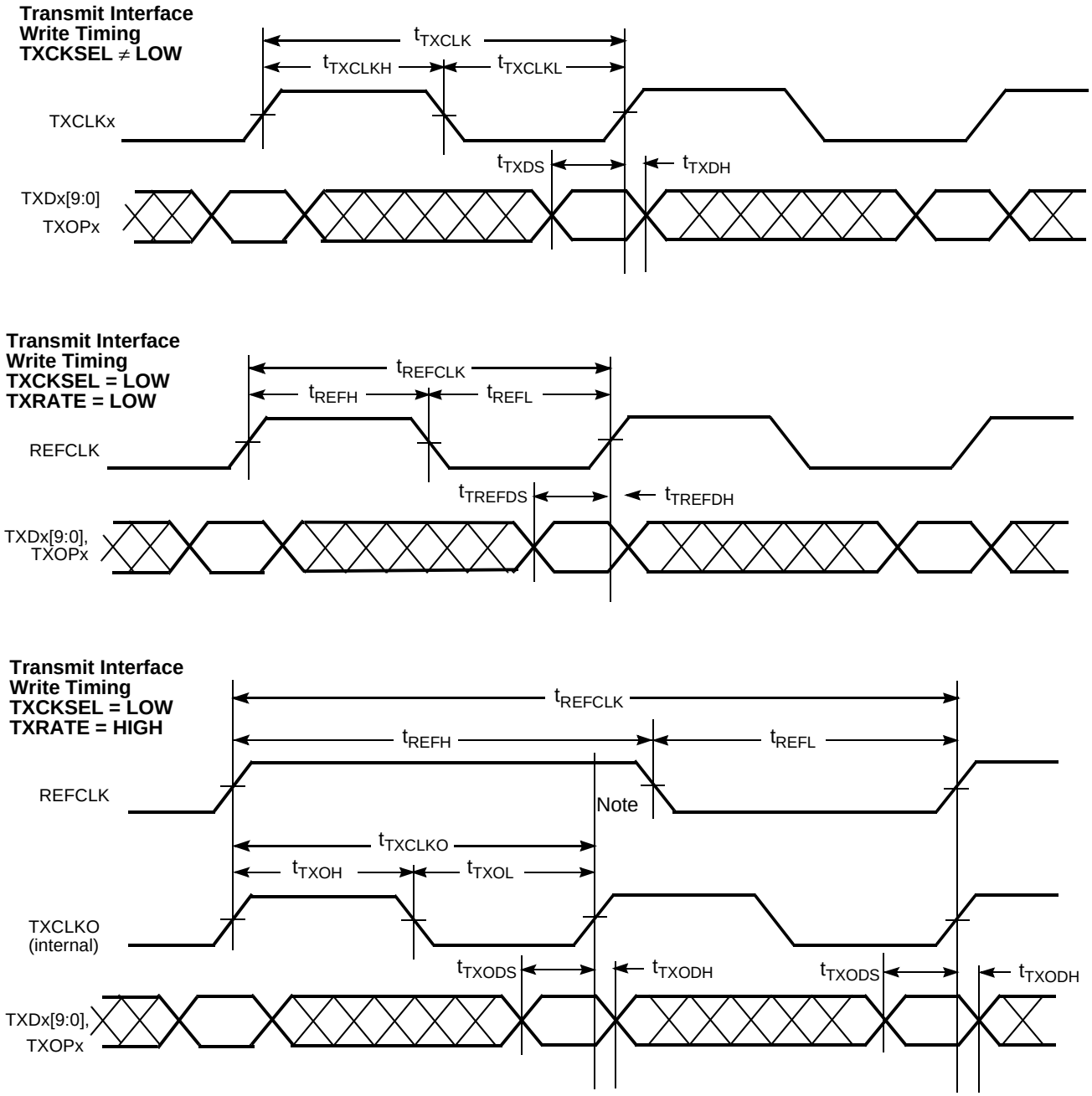
Receive Serial Inputs and CDR PLL Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_{RXLOCK}	Receive PLL Lock to Input Data Stream		10	ms
	Receive PLL Lock to Input Data Stream		2500	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate	TBD	TBD	ns
t_{SA}	Static Alignment[16]			ps
t_{EFW}	Error-free Window [14, 17, 18]	0.75		UI

Notes:

13. REFCLK has no phase or frequency relationship with RXCLK and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±200- ppm (±0.02%) of the transmitter PLL reference (REFCLK) frequency, necessitating a ±100-ppm crystal.
14. While sending continuous K28.5s, outputs loaded to a balanced 100Ω load, over the operating range.
15. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.
16. Static alignments is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a character error occurs.
17. Receiver UI is calculated as 1/Fref*10 when RXRATE = LOW if no data is being received of the remote transmitter. If data is being received it is equal to 1/transmit serial bit rate.
18. Error Free Window is a measure of the time window between the bit centers where a transition may occur without causing a sampling error. It is measured over the operational range.

HOTLink II Transmitter Switching Waveforms



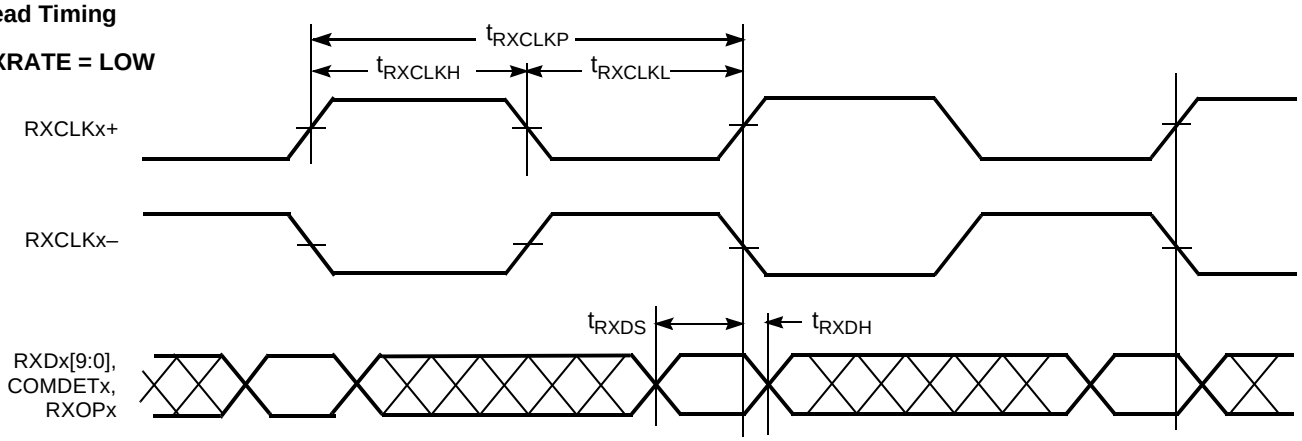
Note:

19. When REFCLK is configured for half-rate operation (TXRATE = LOW) and data is captured using REFCLK instead of a TXCLKx clock (TXCKSEL = LOW), data is captured using the rising edges of the internally synthesized character rate clock. While the rising edge of this clock (TXCLKO) is aligned to the rising edge of REFLCK, it is not aligned to the falling edge of REFCLK.

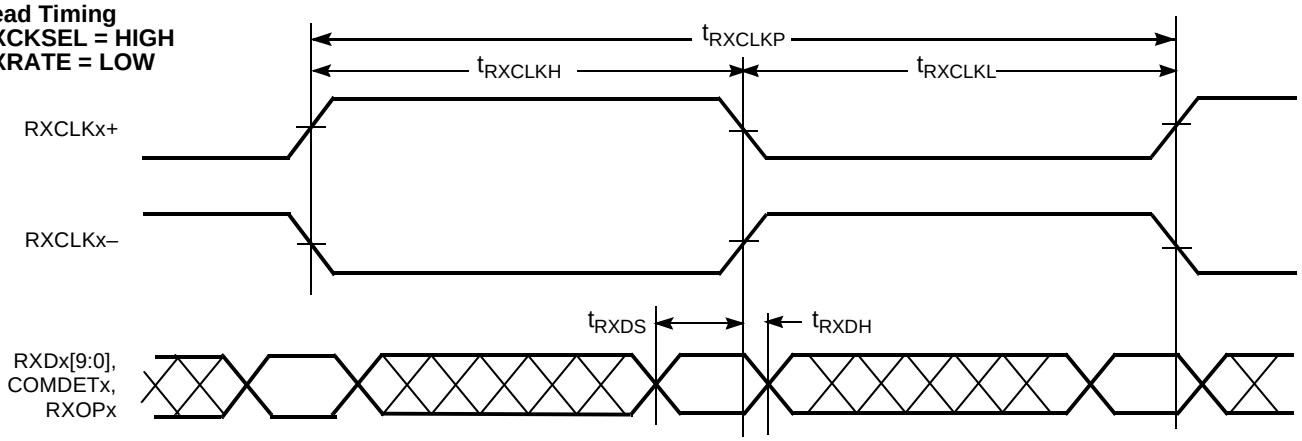
HOTLink II Receiver Switching Waveforms

Receive Interface Read Timing

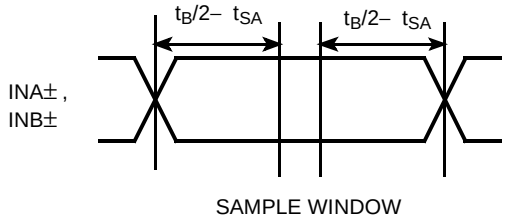
RXRATE = LOW



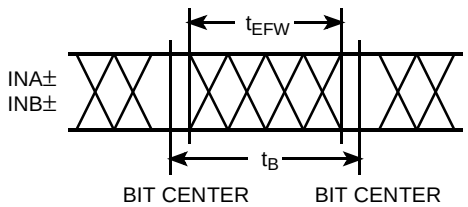
Receive Interface Read Timing RXCKSEL = HIGH RXRATE = LOW



Static Alignment



Error-Free Window



CYP15G0402DX Receiver LVTTL Switching Characteristics Over the Operation Range

Parameter	Description	Min.	Max.	Unit
f_{RS}	RXCLKx Clock Output Frequency	20	150	MHz
t_{RXCLKP}	RXCLKx Period	6.66	50	ns
t_{RXCLKH}	RXCLKx HIGH Time (RXRATE = HIGH)	1.5	24	ns
	RXCLKx HIGH Time (RXRATE = LOW)	5	25	ns
t_{RXCLKL}	RXCLKx LOW Time (RXRATE = HIGH)	1.5	24	ns
	RXCLKx LOW Time (RXRATE = LOW)	5	25	ns
t_{RXCLKD}	RXCLKx Duty Cycle centered with a 50% HIGH Time	–1.0	+1.0	ns
t_{RXCLKR}[20]	RXCLKx Rise Time	0.3	1.2	ns
t_{RXCLKF}[20]	RXCLKx Fall Time	0.3	1.2	ns
t_{RXDV-}[21]	Status and Data Valid Time From RXCLKx (RXCKSEL HIGH or MID)	5UI–1.5		ns
t_{RXDV+}[21]	Status and Data Valid Time From RXCLKx (RXCKSEL HIGH or MID)	5UI–1.8		ns
t_{RXDV-}[21]	Status and Data Invalid Time From RXCLKx (half-rate clock)	5UI–1.0		ns
t_{RXDV+}[21]	Status and Data Invalid Time From RXCLKx (half-rate clock)	5UI–2.3		ns

CYP15G0402DXA REFCLK Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{REF}	REFCLK Clock Output Frequency	20	150	MHz
t_{REFCLK}	REFCLK Period	6.6	100	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = HIGH)	5.9	24	ns
	REFCLK HIGH Time (TXRATE = LOW)	2.9	35	ns
t_{REFL}	REFCLK LOW Time (TXRATE = HIGH)	5.9	24	ns
	REFCLK LOW Time (TXRATE = LOW)	2.9	35	ns
t_{REFD}	REFCLK Duty Cycle	30	7 0	%
t_{REF}	RXCLKx Rise Time		2	ns
t_{REFF}	RXCLKx Fall Time		2	ns
t_{REFDS}[21]	Transmit Data Hold Time to REFCLK (TXCKSEL = LOW)	2		ns
t_{REFDH}[21]	Transmit Data Hold Time to REFCLK (TXCKSEL = LOW	1		ns
t_{RREFDA}[21]	Receive Data Access Time from REFCLK (RXCKSEL = LOW)		9.5	ns
t_{RREFDV}	Receive Data Valid Time from REFCLK (RXCKSEL = LOW)	4.0		ns
$t_{RREFDV-}$	Receive Data Valid Time from RXCLKA (RXCKSEL = LOW)	1.5		ns
$t_{RREFDV+}$	Receive Data Valid Time from RXCLKA (RXCKSEL = LOW)	1.5		ns
$t_{RREFCDV-}$	Receive Data Valid Time from RXCLKC (RXCKSEL = LOW)	3.0		ns
$t_{RREFCDV+}$	Receive Data Valid Time from RXCLKC (RXCKSEL = LOW)	0.5		ns
t_{REFRX}	REFCLK Frequency Referenced to Received Clock Period	-0.02	+0.02	%

Notes:

20. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
21. Parallel data output or input specifications are only valid if all signals are loaded with similar DC and AC loads.

Chip Pin Numbers

Pin	Name	Type
A01	INC-	CMLIN
A02	OUTC-	CMLOUT
A03	NC	
A04	NC	
A05	VCC	POWER
A06	IND-	CMLIN
A07	OUTD-	CMLOUT
A08	GND	GND
A09	NC	
A10	NC	
A11	INA-	CMLIN
A12	OUTA-	CMLOUT
A13	GND	GND
A14	NC	
A15	NC	
A16	VCC	POWER
A17	INB-	CMLIN
A18	OUTB-	CMLOUT
A19	NC	
A20	NC	
B01	INC+	CMLIN
B02	OUTC+	CMLOUT
B03	NC	
B04		NC
B05	VCC	POWER
B06	IND+	CMLIN
B07	OUTD+	CMLOUT
B08	GND	GND
B09		NC
B10		NC
B11	INA+	CMLIN
B12	OUTA+	CMLOUT
B13		GND
B14		NC
B15		NC
B16	VCC	POWER
B17	INB+	CMLIN
B18	OUTB+	CMLOUT
B19		NC
B20		NC
C01	TDI	LVTTLINU
C02	TMS	LVTTLINU
C03	LPENC	LVTTLIN
C04	LPENB	LVTTLIN
C05	VCC	POWER
C06	PARCTL	LVLSEL
C07	SDASEL	LVLSEL
C08	GND	GND
C09	BOE<7>	LVTTLINU
C10	BOE<5>	LVTTLINU
C11	BOE<3>	LVTTLINU
C12	BOE<1>	LVTTLINU
C13	GND	GND
C14	GND	GND
C15	GND	GND
C16	VCC	POWER
C17	TXRATE	LVTTLIND
C18	RXRATE	LVTTLIND
C19		NC
C20	TDO	LTOUT3ST

Pin	Name	Type
D01	TCLK	LVTTLIND
D02	/TRSTZ	LVTTLINU
D03	LPEND	LVTTLIN
D04	LPENA	LVTTLIN
D05	VCC	POWER
D06	RFMODE	LVLSEL
D07	SPDSEL	LVLSEL
D08	GND	GND
D09	BOE<6>	LVTTLINU
D10	BOE<4>	LVTTLINU
D11	BOE<2>	LVTTLINU
D12	BOE<0>	LVTTLINU
D13	GND	GND
D14	GND	GND
D15	GND	GND
D16	VCC	POWER
D17	NC	
D18	RXLE	LVTTLINU
D19	NC	
D20	NC	
E01	VCC	POWER
E02	VCC	POWER
E03	VCC	POWER
E04	VCC	POWER
E17	VCC	POWER
E18	VCC	POWER
E19	VCC	POWER
E20	VCC	POWER
F01	TXPERC	LVTTLOUT
F02	TXOPC	LVTTLINU
F03	TXDC[0]	LVTTLIN
F04	RXCKSEL	LVLSEL
F17	BISTLE	LVTTLINU
F18	RXDB[0]	LVTTLOUT
F19	RXOPB	LTOUT3ST
F20	RXDB[1]	LVTTLOUT
G01	TXDC[7]	LVTTLIN
G02	XCKSEL	LVLSEL
G03	TXDC[4]	LVTTLIN
G04	TXDC[1]	LVTTLIN
G17	GND	GND
G18	OELE	LVTTLINU
G19	FRAMCHAR	LVLSEL
G20	RXDB[3]	LVTTLOUT
H01	GND	GND
H02	GND	GND
H03	GND	GND
H04	GND	GND
PIN	NAME	TYPE
H17	GND	GND
H18	GND	GND
H19	GND	GND
H20	GND	GND
J01	TXDC[9]	LVTTLIN
J02	TXDC[5]	LVTTLIN
J03	TXDC[2]	LVTTLIN
J04	TXDC[3]	LVTTLIN
J17	COMDETB	LVTTLOUT
J18	RXDB[2]	LVTTLOUT
J19	RXDB[7]	LVTTLOUT

Pin	Name	Type
J20	RXDB[4]	LVTTLOUT
K01	RXDC[4]	LVTTLOUT
K02	RXCLKC-	LVTTLOUT
K03	TXDC[8]	LVTTLIN
K04	/LFIC	LVTTLOUT
K17	RXDB[5]	LVTTLOUT
K18	RXDB[6]	LVTTLOUT
K19	RXDB[9]	LVTTLOUT
K20	RXCLKB+	LVTTLIOD
L01	RXDC[5]	LVTTLOUT
L02	RXCLKC+	LVTTLIOD
L03	TXCLKC	LVTTLIND
L04	TXDC[6]	LVTTLIN
L17	RXDB[8]	LVTTLOUT
L18	/LFIB	LVTTLOUT
L19	RXCLKB-	LVTTLOUT
L20	TXDB[6]	LVTTLIN
M01	RXDC[6]	LVTTLOUT
M02	RXDC[7]	LVTTLOUT
M03	RXDC[9]	LVTTLOUT
M04	RXDC[8]	LVTTLOUT
M17	TXDB[9]	LVTTLIN
M18	TDDB[8]	LVTTLIN
M19	TXDB[7]	LVTTLIN
M20	TXCLKB	LVTTLIN
N01	GND	GND
N02	GND	GND
N03	GND	GND
N04	GND	GND
N17	GND	GND
N18	GND	GND
N19	GND	GND
N20	GND	GND
P01	RXDC[3]	LVTTLOUT
P02	RXDC[2]	LVTTLOUT
P03	RXDC[1]	LVTTLOUT
P04	RXDC[0]	LVTTLOUT
P17	TXDB[5]	LVTTLIN
P18	TXDB[4]	LVTTLIN
P19	TXDB[3]	LVTTLIN
P20	TXDB[2]	LVTTLIN
R01	COMDETC	LVTTLOUT
R02	RXOPC	LTTTLOUT
R03	TXPERD	LVTTLOUT
PIN	NAME	TYPE
R04	TXOPD	LVTTLINU
R17	TXDB[1]	LVTTLIN
R18	TXDB[0]	LVTTLIN
R19	TXOPB	LVTTLINU
R20	TXPERB	LVTTLOUT
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	TXDD[0]	LVTTLIN
U02	TXDD[1]	LVTTLIN

Pin	Name	Type
U03	TXDD[2]	LVTTLIN
U04	TXDD[9]	LVTTLIN
U05	VCC	POWER
U06	RXDD[4]	LVTTLOUT
U07	RXDD[3]	LVTTLOUT
U08	GND	GND
U09	RXOPD	LTOUT3ST
U10	RFENC	LVTTLIND
U11	REFCLK-	PECLIN
U12	TXDA[1]	LVTTLIN
U13	GND	GND
U14	TXDA[4]	LVTTLIN
U15	TXDA[8]	LVTTLIN
U16	VCC	POWER
U17	RXDA[4]	LVTTLOUT
U18	RXOPA	LVTTLOUT
U19	COMDETA	LVTTLOUT
U20	RXDA[0]	LVTTLOUT
V01	TXDD[3]	LVTTLIN
V02	TXDD[4]	LVTTLIN
V03	TDDD[8]	LVTTLIN
V04	RXDD[8]	LVTTLOUT
V05	VCC	POWER
V06	RXDD[5]	LVTTLOUT
V07	RXDD[1]	LVTTLOUT
V08	GND	GND
V09	COMDETD	LVTTLOUT
V10	RFEND	LVTTLOD3
V11	REFCLK+	PECLIN
V12	RFENB	LVTTLOD3
V13	GND	GND
V14	TXDA[3]	LVTTLIN
V15	TXDA[7]	LVTTLIN
V16	VCC	POWER
V17	RXDA[9]	LVTTLOUT
V18	RXDA[5]	LVTTLOUT
V19	RXDA[2]	LVTTLOUT
V20	RXDA[1]	LVTTLOUT
W01	TXDD[5]	LVTTLIN
W02	TXDD[7]	LVTTLIN
PIN	NAME	TYPE
W03	/LFID	LVTTLOUT
W04	RXCLKD-	LVTTLOUT
W05	VCC	POWER
W06	RXDD[6]	LVTTLOUT
W07	RXDD[0]	LVTTLOUT
W08	GND	GND
W09	TXCLKO-	LVTTLOUT
W10	/TXRST	LVTTLINU
W11	TXOPA	LVTTLINU
W12	RFENA	LVTTLIN
W13	GND	GND
W14	TXDA[2]	LVTTLIN
W15	TXDA[6]	LVTTLIN
W16	VCC	POWER
W17	/LFIA	LVTTLOUT
W18	RXCLKA-	LVTTLOUT
W19	RXDA[6]	LVTTLOUT
W20	RXDA[3]	LVTTLOUT
Y01	TXDD[6]	LVTTLIN

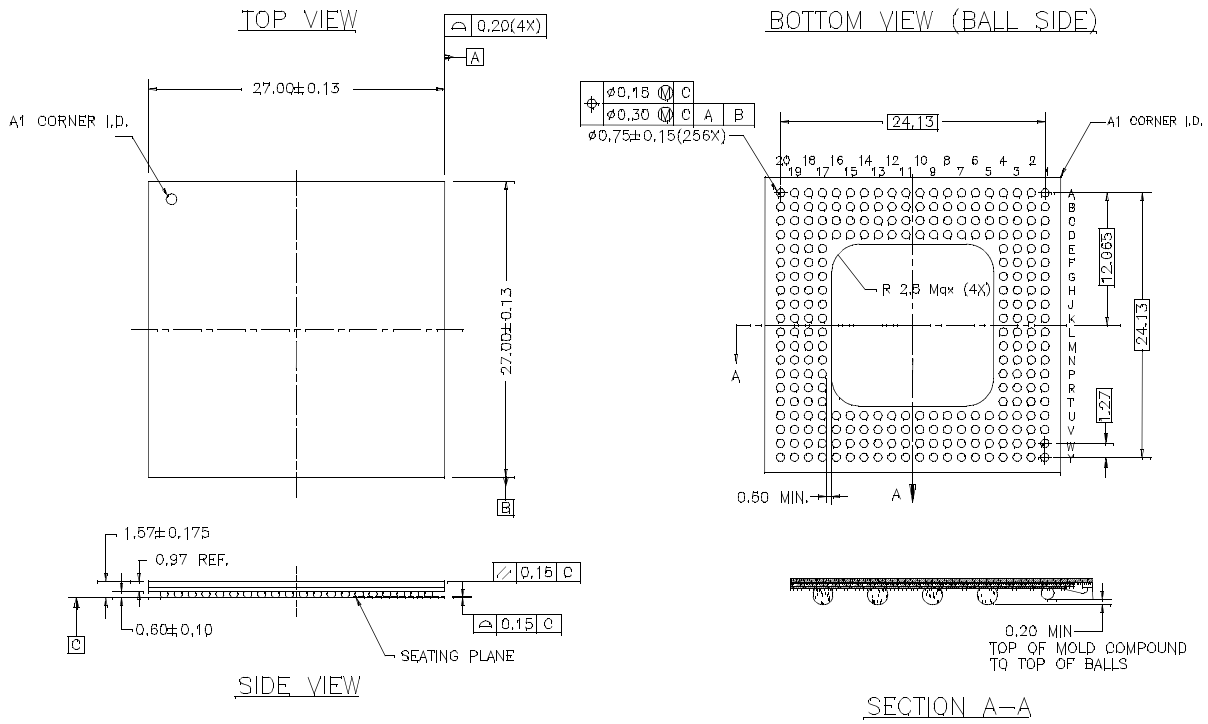
Pin	Name	Type
Y02	TXCLKD	LVTTLIND
Y03	RXDD[9]	LVTTLOUT
Y04	RXCLKD+	LVTTLIOD
Y05	VCC	POWER
Y06	RXDD[7]	LVTTLOUT
Y07	RXDD[2]	LVTTLOUT
Y08	GND	GND
Y09	TXCLKO+	LVTTLOUT
Y10	NC	GND
Y11	TXCLKA	LVTTLIND
Y12	TXPERA	LVTTLOUT
Y13	GND	GND
Y14	TXDA[0]	LVTTLIN
Y15	TXDA[5]	LVTTLIN
Y16	VCC	POWER
Y17	TXDA[9]	LVTTLIN
Y18	RXCLKA+	LVTTLIOD
Y19	RXDA[8]	LVTTLOUT
Y20	RXDA[7]	LVTTLOUT

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP15G0402DX-BGC	BL256	256-ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYP15G0402DX-BGI	BL256	256-ball Thermally Enhanced Ball Grid Array	Industrial

Package Diagram

256-lead Thermally Enhanced L2BGA (27 x 27 x 1.52 mm) BL256



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Document Title: CYP15G0402DX Quad HOTLinkII™ SERDES Document Number: 38-02023				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	108363	07/11/01	TME	New Data Sheet
*A	108915	07/31/01	AMV	Changed name of part from PHY to SERDES
*B	112986	03/01/02	TPS	Changed common mode input specs to match 401D part pp. 17, 18 Added engineering changes to half-rate timing. p. 22 Updated the spec as per meeting with engineering pp. 20–23 Changed the Refclock input to VLTTL both inputs p. 9 Addition of TXCLKO N and the TXCLKO P specs p. 22 Changed the TXCLKO clock output to reflect the new timing p. 22 Changed the Half Clock drawing so that the valid time was at clock edges Changed the input power input p. 21, p. 22 max. power Changed the spec for serial output levels at the different terminations. Changed the common mode input range of serial input Increased the serial input current under the conditions of V_{CC} and min. Added to the duty cycle of transmit and receiver clock signals Changed rise time of the serial inputs and receiver Changed half-rate timing drawing from not valid at clock edges to valid at clock edges Max. voltage reduced from 4.2 to 3.8 Matched the common specs with the family of parts pp. 21–24 Changed max output current to 35 Ma p. 20 Corrected period timing of min. clock from 100 ns to 50 ns p. 19 Added “Preliminary” Added pin RXCKSEL to the pin layout p. 6, 7 to pin layout and pin descriptions Change min. clock frequency Change the front pages Remove decoder command from p. 16, as it is no longer used.