Features

- **ARM7TDMI® ARM® Thumb® Processor Core**
  - **In-Circuit Emulator, 40 MHz operation**
- **16-bit Fixed-point OakDSPCore®**
  - **Up to 60 MHz operations**
  - **104K bytes of Integrated Fast RAM, Codec Interface**
- **Ethernet Bridge**
  - **Dual Ethernet 10/100 Mbps MAC Interface**
  - **16-Kbyte Frame Buffer**
- **1 K-Byte Boot ROM, Embedding a Boot Program**
  - **Enable Application Download from DataFlash®**
- **External Bus Interface**
  - **On-chip 32-bit SDRAM Controller**
  - **4 Chip Select Static Memory Controller**
- **Multi-level Priority, Individually Maskable, Vectored Interrupt Controller**
- **Three 16-bit Timer/Counters**
- **Two UARTs with Modem Control Lines**
- **Serial Peripheral Interface (SPI)**
- **Two PIO Controllers, Managing up to 48 General-purpose I/O Pins**
- **Supported by a Wide Range of Ready-to-use Application Software**
  - **Multi-tasking Operating System, Networking**
  - **Voice-processing Functions**
- **Available in a 208-lead PQFP Package and 256-ball BGA Package**
- **Power Supplies**
  - **VDDIO 3.3V nominal**
  - **VDDCORE and VDDOSC 1.8V nominal**
- **0°C to + 70°C Operating Temperature Range**

Smart Internet Appliance Processor (SIAP™)

AT75C221

Summary

Description

The AT75C221, Atmel's latest device in the family of smart internet appliance processors (SIAP™), is a high-performance processor designed for professional internet appliance applications such as the Ethernet IP phone. The AT75C221 is built around an ARM7TDMI microcontroller core running at 40 MHz with an OakDSPCore coprocessor running at 60 MHz and a dual Ethernet 10/100 Mbits/sec MAC interface.

In a typical standalone IP phone, the DSP handles the voice processing functions (voice compression, acoustic echo cancellation, etc.) while the dual-port Ethernet 10/100 Mbits/sec MAC interface establishes the connection to the Ethernet physical layer (PHY) that links the network and the PC. In such an application, the power of the ARM7TDMI allows it to run a VoIP protocol stack as well as all the system control tasks.

Atmel provides the AT75C221 with several software modules, including:

- A set of drivers for a Linux® kernel capable of driving the embedded peripherals.

- A comprehensive set of tunable DSP algorithms for voice processing, tailored to be run by the DSP subsystem.

Pinout

The AT75C221 ships in two alternative packages:

- 208-lead PQFP
- 256-ball BGA

The product features of the 256-ball BGA package are increased compared to the 208-lead PQFP package.

The features available only with the BGA package are:

- The 32-bit wide data bus (In PQFP, only a 16-bit wide data bus is supported.)
- The Parallel I/O lines PA13 to PA18 and PA20 to PA31
- The Parallel I/O lines PB10 to PB16

208-lead PQFP Package Pinout

Table 1. Pinout for 208-lead PQFP Package

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	GND	37	MB_TXD0	73	A15	109	RAS
2	SCLKA	38	MB_TXD1	74	A16	110	CAS
3	VDDIO	39	MB_TXD2	75	A17	111	NC[1]
4	FSA	40	GND	76	A18	112	WE
5	STXA	41	MB_TXD3	77	A19B/A0	113	DQM0
6	SRXA	42	MB_TXEN	78	A20/BA1	114	DQM1
7	NTRST	43	MB_TXCLK	79	A21	115	NC[1]
8	MA_COL	44	MB_RXD0	80	D0	116	GND
9	MA_CRS	45	MB_RXD1	81	D1	117	NC[1]
10	MA_TXER	46	MB_RXD2	82	D2	118	VDDCORE
11	MA_TXD0	47	MB_RXD3	83	D3	119	GND
12	MA_TXD1	48	MB_RXER	84	GND	120	VDDOSC
13	MA_TXD2	49	MB_RXCLK	85	D4	121	PLLRC
14	MA_TXD3	50	MB_RXDV	86	VDDIO	122	GND
15	MA_TXEN	51	MB_MDC	87	D5	123	GND
16	VDDIO	52	VDDIO	88	D6	124	XTALOUT
17	MA_TXCLK	53	GND	89	D7	125	XTALIN
18	GND	54	MB_MDIO	90	D8	126	VDDCORE
19	MA_RXD0	55	MB_LINK	91	D9	127	NCE0
20	MA_RXD1	56	A0	92	D10	128	NCE1
21	MA_RXD2	57	A1	93	D11	129	NCE2
22	MA_RXD3	58	A2	94	D12	130	VDDIO
23	MA_RXER	59	A3	95	D13	131	NCE3
24	MA_RXCLK	60	A4	96	D14	132	NWE0
25	GND	61	A5	97	VDDCORE	133	NWE1
26	VDDCORE	62	A6	98	GND	134	NC[1]
27	MA_RXDV	63	A7	99	D15	135	VDDIO
28	MA_MDC	64	A8	100	VDDIO	136	GND
29	MA_MDIO	65	A9	101	GND	137	NC[1]
30	MA_LINK	66	A10	102	VDDIO	138	NWR
31	MB_COL	67	A11	103	NC[1]	139	NSOE
32	MB_CRS	68	A12	104	VDDIO	140	GND
33	GND	69	VDDIO	105	GND	141	VDDCORE
34	VDDCORE	70	GND	106	SDCK	142	VDDIO
35	VDDIO	71	A13	107	SDCS	143	MISO
36	MB_TXER	72	A14	108	SDA10	144	MOSI

Table 1. Pinout for 208-lead PQFP Package (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
145	SPCK	161	TMS	177	PA5	193	GND
146	PA22	162	TCK	178	PA4	194	PB0
147	VDDIO	163	PA19	179	PA3	195	PB1
148	GND	164	VDDCORE	180	PA2	196	PB2
149	NRST	165	GND	181	PA1	197	PB3
150	FIQ	166	PA12	182	PA0	198	PB4
151	IRQ0	167	GND	183	GND	199	PB5
152	TST	168	VDDIO	184	RXDA	200	PB6
153	GND	169	PA11	185	TXDA	201	PB7
154	VDDCORE	170	PA10	186	NRSTA	202	PB8
155	NC[1]	171	PA9	187	NCTSA	203	PB9
156	VDDIO	172	PA8	188	NDTRA	204	VDDIO
157	GND	173	PA7	189	NDSRA	205	DBW32
158	VDDIO	174	PA6	190	NDCDA	206	GND
159	TDO	175	VDDIO	191	RXDB	207	BO256
160	TDI	176	NC[1]	192	TXDB	208	VDDIO

Note: 1. NC pins should be left unconnected.

Figure 1.   208-lead PQFP Package Orientation (Top View)
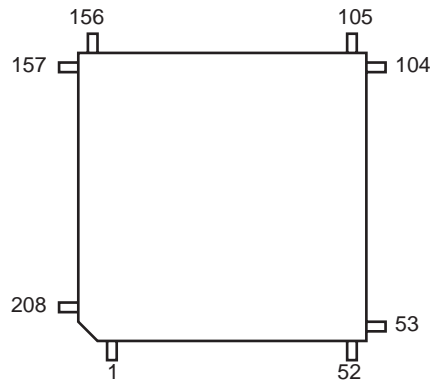
256-ball BGA Package Pinout

Table 1. Pinout for 256-ball BGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	GND	B18	TDI	D15	VDDIO	H20	NSOE
A2	PB9	B19	NC[1]	D16	PA24	J1	MA_TXEN
A3	PB4	B20	NC[1]	D17	GND	J2	MA_TXD3
A4	PB1	C1	PB10	D18	PA29	J3	MA_TXD2
A5	NDSRB	C2	PA28	D19	VDDCORE	J4	MA_TXD1
A6	NRSTB	C3	DBW32	D20	IRQ1	J17	NWR
A7	RXDB	C4	PB6	E1	STXA	J18	NWE3
A8	NDSRA	C5	PB2	E2	FSA	J19	NC[1]
A9	TXDA	C6	NRIB	E3	SCLKA	J20	NWE2
A10	PA2	C7	NCTSB	E4	PA25	K1	MA_RXD0
A11	PA3	C8	NRIA	E17	PA30	K2	MA_TXCLK
A12	PA6	C9	NCTSA	E18	TST	K3	NC[1]
A13	PA10	C10	PA0	E19	IRQ0	K4	VDDIO
A14	PA13	C11	PA4	E20	NC[1]	K17	NWE1
A15	PA15	C12	PA8	F1	PB13	K18	NWE0
A16	PA19	C13	PA12	F2	PB12	K19	NCE3
A17	NC[1]	C14	PA14	F3	SRXA	K20	NCE2
A18	PA23	C15	PA18	F4	VDDIO	L1	MA_RXD1
A19	TDO	C16	PA21	F17	VDDIO	L2	MA_RXD2
A20	NC[1]	C17	TCK	F18	FIQ	L3	MA_RXD3
B1	BO256	C18	NC[1]	F19	NC[1]	L4	MA_RXER
B2	PB8	C19	NC[1]	F20	SPCK	L17	VDDIO
B3	PB7	C20	PA31	G1	MA_COL	L18	NCE0
B4	PB3	D1	PB11	G2	PB15	L19	NC[1]
B5	PB0	D2	PA27	G3	PB14	L20	NCE1
B6	NDTRB	D3	PA26	G4	NTRST	M1	MA_RXCLK
B7	TXDB	D4	GND	G17	NRST	M2	VDDCORE
B8	NDCDA	D5	PB5	G18	PA22	M3	MA_RXDV
B9	NRSTA	D6	VDDIO	G19	MOSI	M4	MA_MDC
B10	PA1	D7	NDCDB	G20	MISO	M17	PLLRC
B11	PA5	D8	GND	H1	MA_TXD0	M18	NC[1]
B12	PA7	D9	NDTRA	H2	MA_TXER	M19	XTALOUT
B13	PA11	D10	RXDA	H3	MA_CRS	M20	XTALIN
B14	VDDCORE	D11	VDDIO	H4	GND	N1	MA_MDIO
B15	PA16	D12	PA9	H17	GND	N2	MA_LINK
B16	PA20	D13	GND	H18	VDDIO	N3	MB_COL
B17	TMS	D14	PA17	H19	VDDCORE	N4	GND

Table 1. Pinout for 256-ball BGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
N17	GND	T20	SDCS	V7	A11	W14	D12
N18	DQM3	U1	MB_RXD0	V8	A14	W15	VDDCORE
N19	VDDCORE	U2	MB_RXD2	V9	A18	W16	D17
N20	VDDOSC	U3	MB_RXCLK	V10	A22	W17	D20
P1	MB_CRS	U4	GND	V11	D2	W18	D24
P2	VDDCORE	U5	A1	V12	D6	W19	VDDIO
P3	MB_TXD0	U6	VDDIO	V13	D10	W20	NC[1]
P4	MB_TXD3	U7	A8	V14	D14	Y1	NC[1]
P17	RAS	U8	GND	V15	NC[1]	Y2	MB_MDIO
P18	DQM0	U9	A17	V16	D19	Y3	A2
P19	DQM1	U10	VDDIO	V17	D23	Y4	A3
P20	DQM2	U11	D3	V18	D26	Y5	A6
R1	MB_TXER	U12	D7	V19	NC[1]	Y6	A10
R2	MB_TXD1	U13	GND	V20	D29	Y7	A13
R3	MB_TXEN	U14	D16	W1	MB_MDC	Y8	A16
R4	VDDIO	U15	VDDIO	W2	NC[1]	Y9	A20/BA1
R17	VDDIO	U16	D22	W3	NC[1]	Y10	A23
R18	SDA10	U17	GND	W4	MB_LINK	Y11	D0
R19	CAS	U18	D27	W5	A5	Y12	D4
R20	WE	U19	NC[1]	W6	A9	Y13	D8
T1	MB_TXD2	U20	D30	W7	A12	Y14	D11
T2	MB_TXCLK	V1	MB_RXD3	W8	A15	Y15	D13
T3	MB_RXD1	V2	MB_RXDV	W9	A19/BA0	Y16	D15
T4	MB_RXER	V3	NC[1]	W10	A21	Y17	D18
T17	D28	V4	A0	W11	D1	Y18	D21
T18	D31	V5	A4	W12	D5	Y19	D25
T19	SDCK	V6	A7	W13	D9	Y20	NC[1]

Note: 1. NC Balls should be left unconnected.

6   **AT75C221 Summary**

Figure 2. 256-ball Package Orientation (Top View)
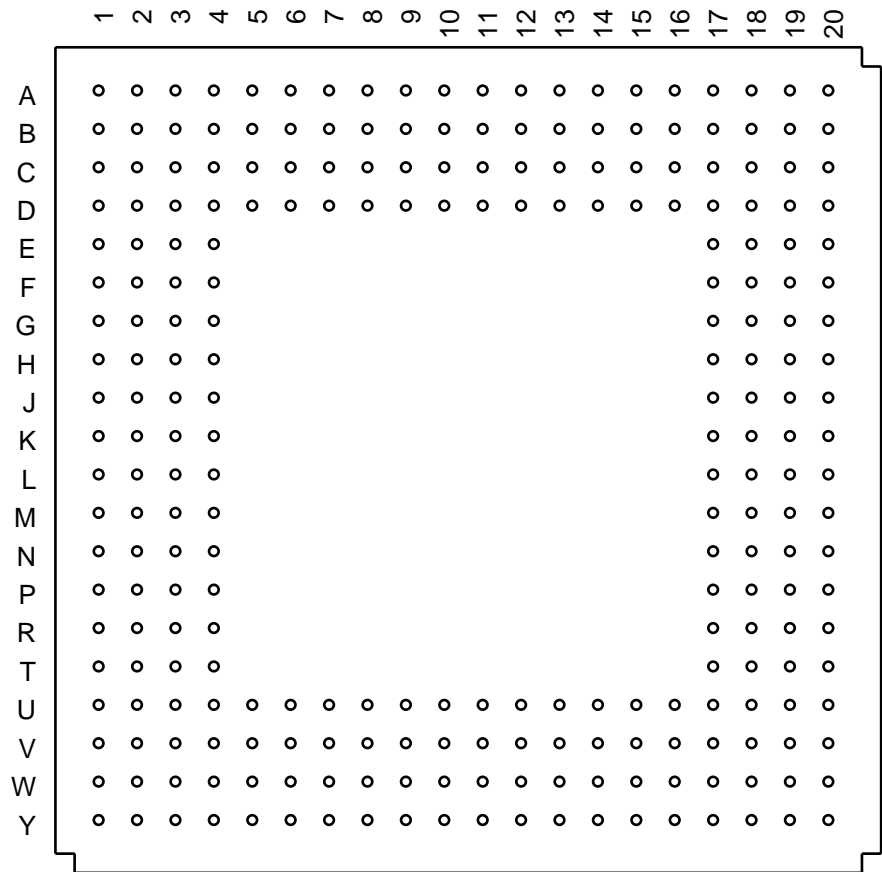
Signal Description

Table 1. Signal Description

Block	Signal Name	Function	Type
Power Supplies	VDDIO	I/O Lines Power Supply	
	VDDCORE	Device Core Power Supply	
	VDDOSC	PLL and Oscillator Power Supply	
	GND	Ground	
External Bus Interface	A0-A23	Address Bus	Output
	D0-D31	Data Bus	Input/Output
Synchronous Dynamic Memory Controller	SDCK	SDRAM Clock	Output
	DQM0-DQM3	SDRAM Byte Masks	Output
	SDCS	SDRAM Chip Select	Output
	SDA10	SDRAM Address Line 10	Output
	RAS	Row Address Strobes	Output
	CAS	Column Address Strobes	Output
	WE	Write Enable	Output
	BA0-BA1	Bank Address Line	Output
Static Memory Controller	NCE0-NCE3	Chip Selects	Output
	NWE0-NWE3	Byte Select/Write Enable	Output
	NSOE	Output Enable	Output
	NWR	Memory Block Write Enable	Output
PIO Controller A	PA0-PA31	PIO Controller A I/O Lines	Input/Output
PIO Controller B	PB0-PB15	PIO Controller B I/O Lines	Input/Output
Timer Counter	TCLK0-TCLK2	Timer Counter Clock 0 to 2	Input
	TIOA0-TIOA2	Timer Counter I/O Line A 0 to 2	Input/Output
	TIOB0-TIOA2	Timer Counter I/O Line B 0 to 2	Input/Output
Serial Peripheral Interface	MISO	Master In/Slave Out	Input/Output
	MOSI	Master Out/Slave In	Input/Output
	SPCK	Serial Clock	Input/Output
	NPCS0/NSS	Peripheral Chip Select 0/Slave Select	Input/Output
	NPCS1-NPCS3	Peripheral Chip Select 1 to 3	Output

Table 1. Signal Description (Continued)

Block	Signal Name	Function	Type
UART A and UART B	RXDA-RXDB	Receive Data	Input
	TXDA-TXDB	Transmit Data	Output
	NRTSA-NRSTB	Ready to Send	Output
	NCTSA-NCTSB	Clear to Send	Input
	NDTRA-NDTRB	Data Terminal Ready	Output
	NDSRA-NDSRB	Data Set Ready	Input
	NDCDA-NDCDB	Data Carrier Detect	Input
	NRIA-NRIB	Ring Indicator	Input
MAC A Interface	MA_COL	MAC A Collision Detect	Input
	MA_CRS	MAC A Carrier Sense	Input
	MA_TXER	MAC A Transmit Error	Output
	MA_TXD0-MA_TXD3	MAC A Transmit Data Bus	Output
	MA_TXEN	MAC A Transmit Enable	Output
	MA_TXCLK	MAC A Transmit Clock	Input
	MA_RXD0-MA_RXD3	MAC A Receive Data Bus	Input
	MA_RXER	MAC A Receive Error	Input
	MA_RXCLK	MAC A Receive Clock	Input
	MA_RXDV	MAC A Receive Data Valid	Output
	MA_MDC	MAC A Management Data Clock	Output
	MA_MDIO	MAC A Management Data Bus	Input/Output
	MA_LINK	MAC A Link Interrupt	Input
MAC B Interface	MB_COL	MAC B Collision Detect	Input
	MB_CRS	MAC B Carrier Sense	Input
	MB_TXER	MAC B Transmit Error	Output
	MB_TXD0-MB_TXD3	MAC B Transmit Data Bus	Output
	MB_TXEN	MAC B Transmit Enable	Output
	MB_TXCLK	MAC B Transmit Clock	Input
	MB_RXD0-MB_RXD3	MAC B Receive Data Bus	Input
	MB_RXER	MAC B Receive Error	Input
	MB_RXCLK	MAC B Receive Clock	Input
	MB_RXDV	MAC B Receive Data Valid	Output
	MB_MDC	MAC B Management Data Clock	Output
	MB_MDIO	MAC B Management Data Bus	Input/Output
	MB_LINK	MAC B Link Interrupt	Input

Table 1. Signal Description (Continued)

Block	Signal Name	Function	Type
In-Circuit Emulator	NTRST	Test Reset	Input
	TCK	Test Clock	Input
	TMS	Test Mode Select	Input
	TDI	Test Data Input	Input
	TDO	Test Data Output	Output
Codec Interface	SCLKA	Serial Clock	Input/Output
	FSA	Frame Pulse	Input/Output
	STXA	Transmit Data to Codec	Output
	SRXA	Receive Data to Codec	Input
DSP Subsystem	OAKAIN0-OAKAIN1	OakDSPCore User Input	Input
	OAKAOUT0-OAKAOUT1	OakDSPCore User Output	Output
Miscellaneous	NRST	Reset	Input
	FIQ	Fast Interrupt	Input
	IRQ0-IRQ1	Interrupt Lines	Input
	PLLRC	PLL RC Filter	Analog
	XTALIN	Crystal Input	Analog
	XTALOUT	External Crystal	Analog
	TST	Test Mode	Input
	B0256	Package Size Option (1 = 256 pins)	Input
	DBW32	External Data Bus Width for CS0 (1 = 32 bits)	Input
	ACLKO	ARM Clock Output	Output

Block Diagram

Figure 3. AT75C221 Block Diagram
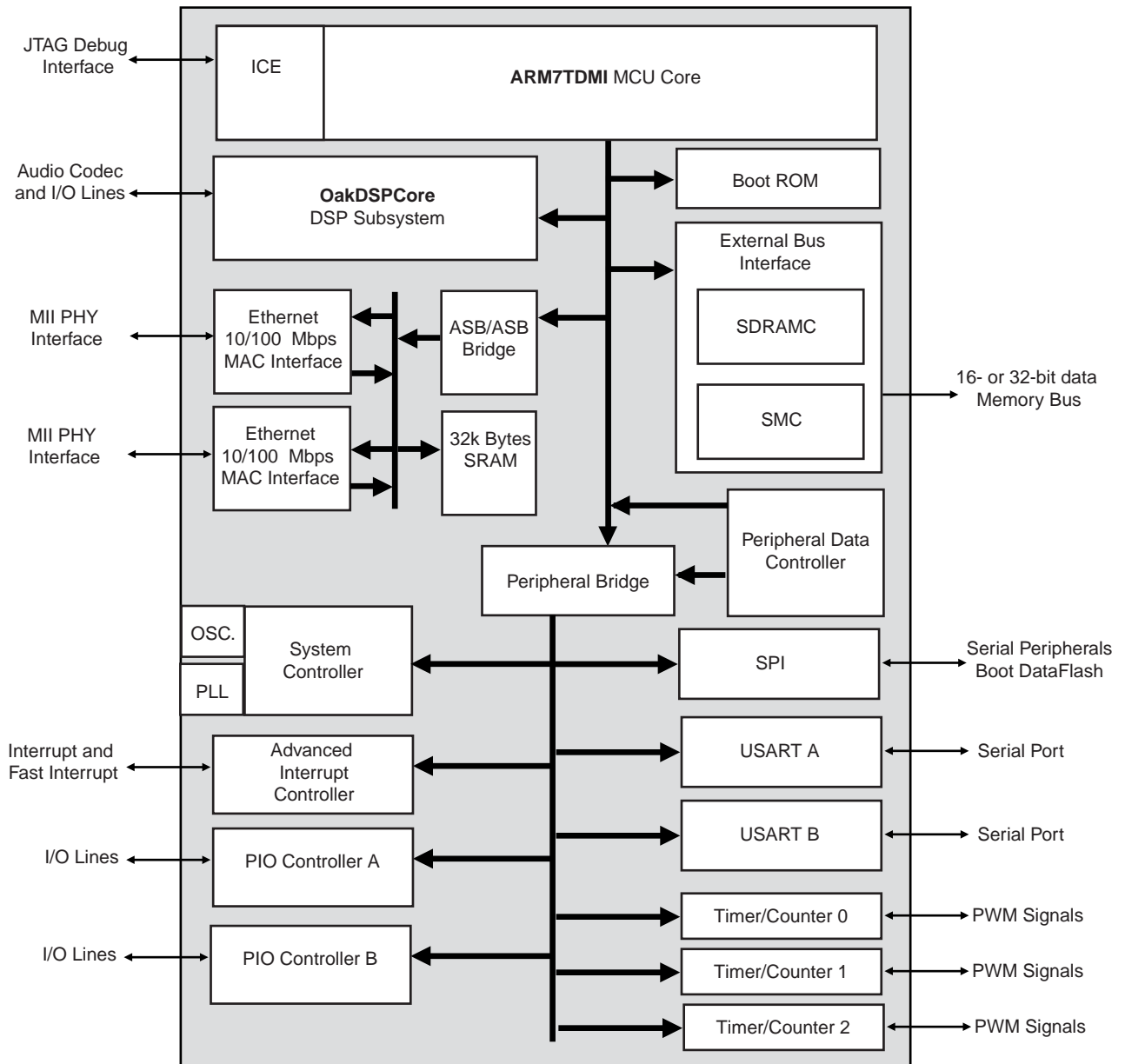
Application Example

Figure 4. DSP Subsystem
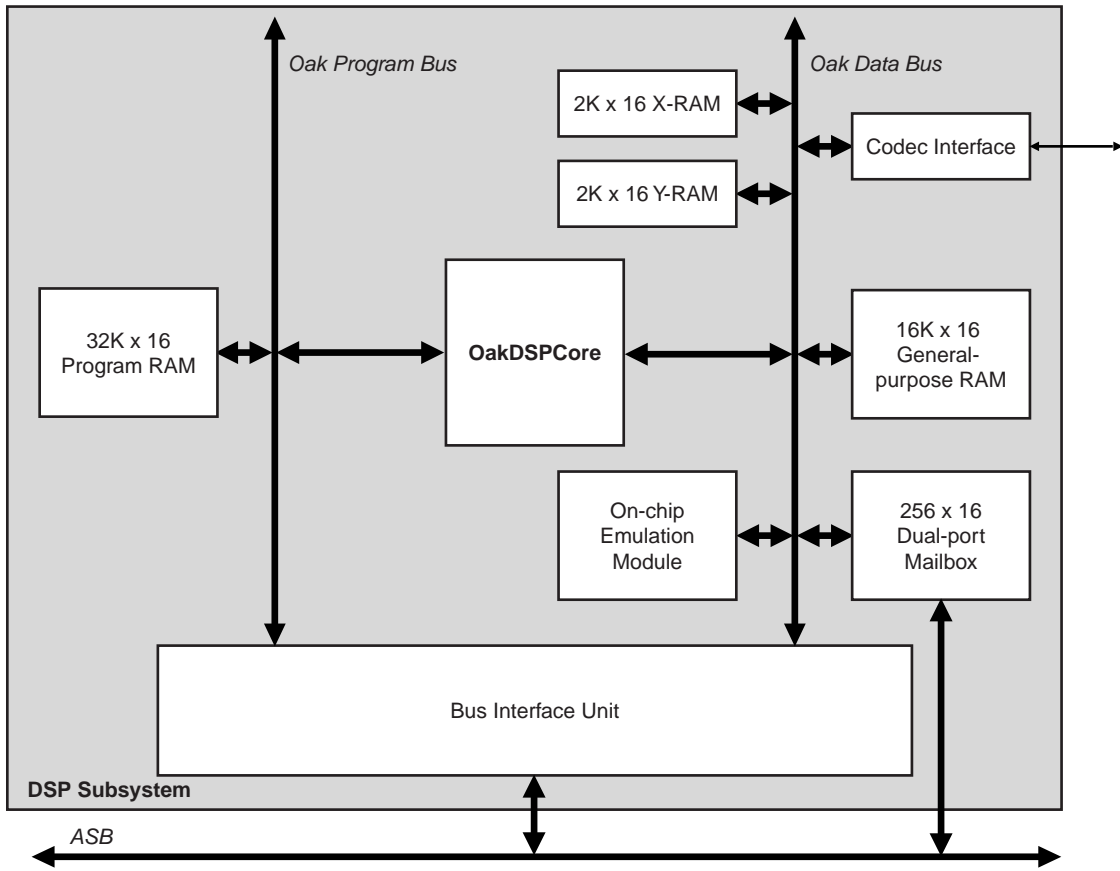
Figure 5. Application Example Overview: Standalone Ethernet Telephone
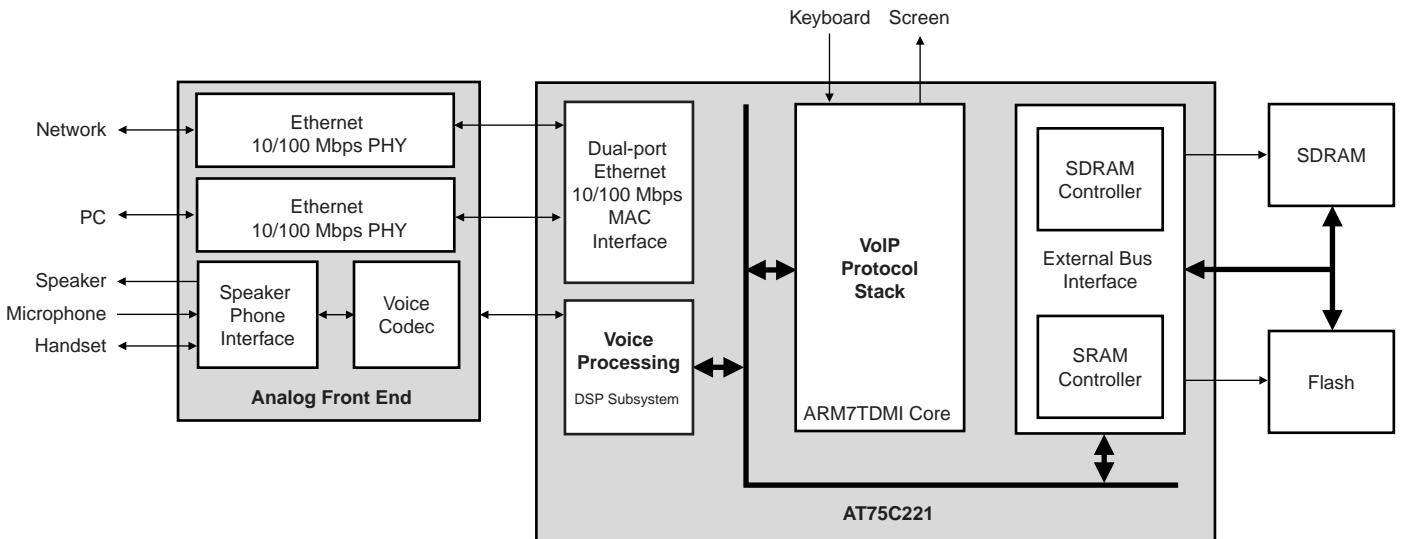
Functional Description

ARM7TDMI Core

The ARM7TDMI is a three-stage pipeline, 32-bit RISC processor. The processor architecture is Von Neumann load/store architecture, characterized by a single data and address bus for instructions and data. The CPU has two instruction sets: the ARM and the Thumb instruction set. The ARM instruction set has 32-bit wide instructions and provides maximum performance. Thumb instructions are 16-bit wide and give maximum code density.

Instructions operate on 8-bit, 16-bit and 32-bit data types.

The CPU has seven operating modes. Each operating mode has dedicated banked registers for fast exception handling. The processor has a total of 37 32-bit registers, including six status registers.

DSP Subsystem

The AT75C221 DSP subsystem is composed of:

- An OakDSPCore running at 60 MIPS
- 2K x 16 of X-RAM
- 2K x 16 of Y-RAM
- 16K x 16 of General Purpose Data RAM
- 32K x 16 of Loadable Program RAM
- One 256 x 16 Dual-port Mailbox
- One Codec Interface

The DSP subsystem is fully autonomous. The local X- and Y-RAM allows it to reach its maximum processing rate, and a local large data RAM enables complex DSP algorithms to be implemented. The large size of the loadable program RAM permits the use of functions as complex as a low bit-rate vocoder.

During boot time, the ARM7TDMI core has the ability to maintain the OakDSPCore in reset state and to upload DSP code. When the OakDSPCore reverts to an active state, this code is executed.

When the OakDSPCore is running the dual-port mailbox is used as the communication channel between the ARM7TDMI and the OakDSPCore.

A programmable codec interface is directly connected to the OakDSPCore. It allows the connection of most industrial voice, multimedia or data codecs.

Ethernet MAC

The AT75C221 features two identical Ethernet MACs with the same attributes as follows:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbits per Second Data Throughput Capability
- Full- and Half-duplex Operation
- Media Independent Interface to the Physical Layer
- Register Interface to Address, Status and Control Registers
- DMA Interface
- Interrupt Generation to Signal Receive and Transmit Completion
- 28-byte Transmit and 28-byte Receive FIFOs
- Automatic Pad and CRC Generation on Transmitted Frames

- Address Checking Logic to Recognize Four 48-bit Addresses
- Supports Promiscuous Mode Where All Valid Frames are Copied to Memory
- Supports Physical Layer Management through MDIO Interface

The Ethernet MAC is the hardware implementation of the MAC sub-layer OSI reference model between the physical layer (PHY) and the logical link layer (LLC). It controls the data exchange between a host and a PHY layer according to Ethernet IEEE 802.3u data frame format. The Ethernet MAC contains the required logic and transmit and receive FIFOs for DMA management. In addition, it is interfaced through MDIO/MDC pins for PHY layer management. The Ethernet MAC transfers data in media-independent interface (MII).

Peripheral Multiplexing on PIO Lines

The AT75C221 features two PIO Controllers, PIOA and PIOB, multiplexing I/O lines of the peripheral set.

The PIO Controller A manages 32 I/O lines, PA0 to PA31, but only the I/O lines PA0 to PA12 PA19 and PA22 are available in the 208-lead package.

The PIO Controller B manages only 16 I/O lines, PB0 to PB15, but only the I/O lines PB0 to PB9 are available in the 208-lead package.

Each I/O line of a PIO Controller can be multiplexed with a peripheral I/O.

Power Supplies

The AT75C221 has three types of power supply pins:
- VDDCORE pins power the core, including the ARM7TDMI processor, the DSP subsystem, the memories and the peripherals; voltage is between 1.65V and 1.95V, 1.8V nominal.
- VDDIO pins power the I/O lines, including those of the External Bus Interface and those of the peripherals; voltage is between 3.0V and 3.6V, 3.3V nominal.
- VDDOSC pins power the PLL and oscillator cells; voltage is between 1.65V and 1.95V, 1.8V nominal.

Ground pins are common to all power supplies.

System Controller

The AT75C221 features a System Controller, which takes care of and controls:
- The Test Mode
- The Reset
- The Clocks of the System
- The Chip Identifier

The System Controller manages the reset of the entire system and integrates a clock generator made up of an oscillator and a PLL.

Memory Controller

The AT75C221 architecture is made up of two Advanced System Buses, the ARM ASB and the MAC ASB. Both handle a single memory space.

The ARM ASB handles the access requests of the ARM7TDMI and the PDC. It handles also the access requests coming from the MAC ASB. It connects with the External Bus Interface, the Peripheral Bridge and the Internal Memories, including the mailbox with the DSP Subsystem. It also connects with the MAC ASB.

The MAC ASB handles the access requests of the DMAs of both Ethernet MACs. It also handles the access requests coming from the the ARM ASB. It connects essentially with the Frame Buffer, but also connects with the ARM ASB.

The major advantage of this double-ASB architecture is that the Ethernet traffic does not occupy the main ASB bandwidth, ensuring that the ARM7TDMI can perform at its maximum speed while the Ethernet traffic goes through the Frame Buffer.

Boot Program

The AT75C221 can boot in several ways; including from internal boot software and a hardware connection of DataFlash. When the ARM7TDMI processor is released from reset, it basically attempts a fetch from address 0x00000000. Depending on the hardware configuration, the memory mapping can be altered and thus modify how the system boots.

Peripherals

The Peripheral Bridge allows access to the embedded peripheral user interfaces. It is optimized for low power consumption, as it is built without usage of any clock. However, any access on the peripheral is performed in two cycles.

The AT75C221 peripherals are designed to be programmed with a minimum number of instructions. Each peripheral has 16K bytes of address space allocated in the upper part of the address space.

PDC: Peripheral Data Controller

The AT75C221 features a six-channel Peripheral Data Controller (PDC) dedicated to the two on-chip UARTs and the SPI. One PDC channel is connected to the receiving channel and one to the transmitting channel of each UART and of the SPI.

Each PDC channel operates as DMA (Direct Memory Access).

The User Interface of a PDC channel is integrated in the memory space of each peripheral. It contains a 32-bit address pointer register and a 16-bit count register. When the programmed number of bytes is transferred, an end-of-transfer signal is sent to the peripheral and is visible in the peripheral status register. This status bit might trigger an interrupt.

EBI: External Bus Interface

The External Bus Interface generates the signals which control access to external memories or peripheral devices. It contains two controllers: the SDRAM Controller and the Static Memory Controller and manages the sharing of data and address buses between both controllers.

SDRAMC: SDRAM Controller

The SDRAM Controller extends the memory capabilities of a chip by providing the interface to an external 16- or 32-bit SDRAM device. The page size supports ranges from 2048 to 8192 and the number of columns from 256 to 2048. It supports byte (8-bit), half-word (16-bit) and word (32-bit) accesses. The maximum addressable SDRAM size is 256M bytes.

The SDRAM Controller supports a read or write burst length of one location. It keeps track of the active row in each bank, thus maximizing SDRAM performance, e.g., the application may be placed in one bank and data in the other banks. So as to optimize performance, it is advisable to avoid accessing different rows in the same bank.

The SDRAM Controller's function is to make the SDRAM device access protocol transparent to the user.

SMC: Static Memory Controller

The AT75C221 features a Static Memory Controller that enables interfacing with a wide range of external static memory on peripheral devices, including Flash, ROM, static RAM, and parallel peripherals.

The SMC provides a glueless memory interface to external memory using common address, data bus and dedicated control signals. The SMC is highly programmable and

has up to 24 bits of address bus, a 32- or 16-bit data bus and up to four chip select lines. The SMC supports different access protocols allowing single clock-cycle accesses. The SMC is programmed as an internal peripheral that has a standard APB bus interface and a set of memory-mapped registers. It shares the external address and data buses with the SDMC.

AIC: Advanced Interrupt Controller

The AT75C221 integrates an Advanced Interrupt Controller (AIC) which is connected to the fast interrupt request (nFIQ) and the standard interrupt request (nIRQ) inputs of the ARM7TDMI processor. The processor's nFIQ line can only be asserted by the external fast interrupt request input (FIQ). The nIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the two external interrupt request lines, IRQ0 to IRQ1.

An 8-level priority encoder allows the user to define the priority between the different interrupt sources. Internal sources are programmed to be level-sensitive or edge-triggered. External sources can be programmed to be positive- or negative-edge triggered or high- or low-level sensitive.

PIO: Programmable I/O Controller

The AT75C221 integrates 24 programmable I/O pins. Each pin can be programmed as an input or an output. Each pin can also generate an interrupt. The programmable I/O is implemented as two blocks, called PIO A and PIO B, 32 and 16 pins each, respectively.

These pins are used for several functions:

- External I/O for internal peripherals
- Keypad controller function
- General-purpose I/O

UART: Universal Asynchronous Receiver Transmitter

The AT75C221 provides two identical full-duplex, Universal Asynchronous Receiver Transmitters as UART A and UART B. These peripherals sit on the APB bus but are also connected to the ASB bus (and hence external memory) via a dedicated DMA.

The main features of the UART are:

- Programmable Baud Rate Generator
- Parity, Framing and Overrun Error Detection
- Line Break Generation and Detection
- Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Interrupt Generation
- Two Dedicated Peripheral Data Controller Channels
- 6-, 7- and 8-bit Character Length
- Modem Control Signals

TC: Timer/Counter

The AT75C221 features a timer/counter block which includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

Each timer/counter channel has three external clock inputs, five internal clock inputs, and two multi-purpose input/output signals that can be configured by the user. Each channel drives an internal interrupt signal that can be programmed to generate processor interrupts via the AIC.

The timer/counter block has two global registers which act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with

the same instruction. The Block Mode Register defines the external clock inputs for each timer/counter channel, allowing them to be chained.

SPI: Serial Peripheral Interface

The Serial Peripheral Interface circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also allows communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPI's. During a data transfer, one SPI system acts as the "master"' which controls the data flow, while the other system acts as the "slave'' which has data shifted into and out of it by the master. Different CPU's can take turn being masters (Multiple Master Protocol opposite to Single Master Protocol where one CPU is always the master while all of the others are always slaves), and one master may simultaneously shift data into multiple slaves. However, only one slave may drive its output to write data back to the master at any given time.

The main features of the SPI are:

- Four Chip Selects with External Decoder Support Allow Communication with Up to 15 Peripherals
- Serial Memories, such as DataFlash and 3-wire EEPROMs
- Serial Peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
- External Coprocessors
- Master or Serial Peripheral Bus Interface
- 8- to 16-bit Programmable Data Length Per Chip Select
- Programmable Phase and Polarity Per Chip Select
- Programmable Transfer Delays Between Consecutive Transfers and Between Clock and Data Per Chip Select
- Programmable Delay Between Consecutive Transfers
- Selectable Mode Fault Detection
- Connection to PDC Channel Capabilities Optimizes Data Transfers
- One Channel for the Receiver, One Channel for the Transmitter

Ordering Information

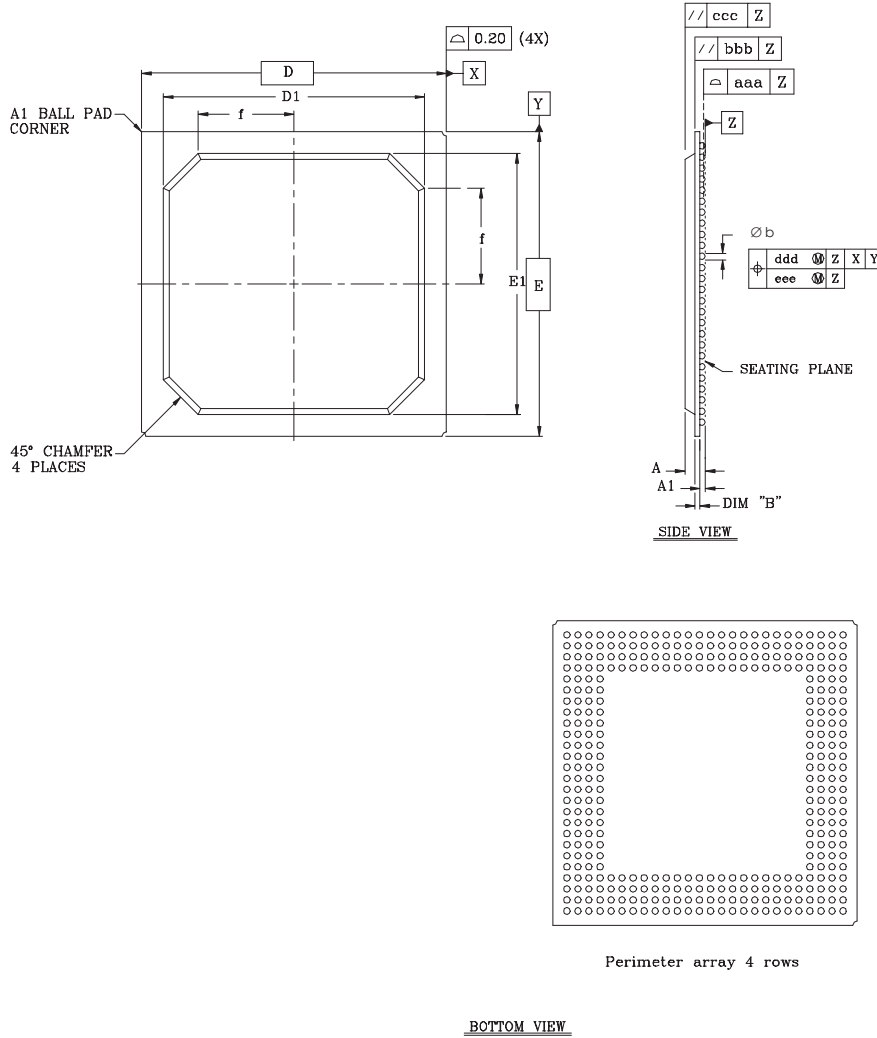Table 2 below provides package ordering information for the AT75C221.

Table 2. Ordering Information

Ordering Code	Package	Operating Temperature Range
AT75C221-Q208	PQFP208	0° to 70° C
AT75C221-C256	BGA256	0° to 70° C

Mechanical Characteristics and Packaging Information

BGA Packaging Information

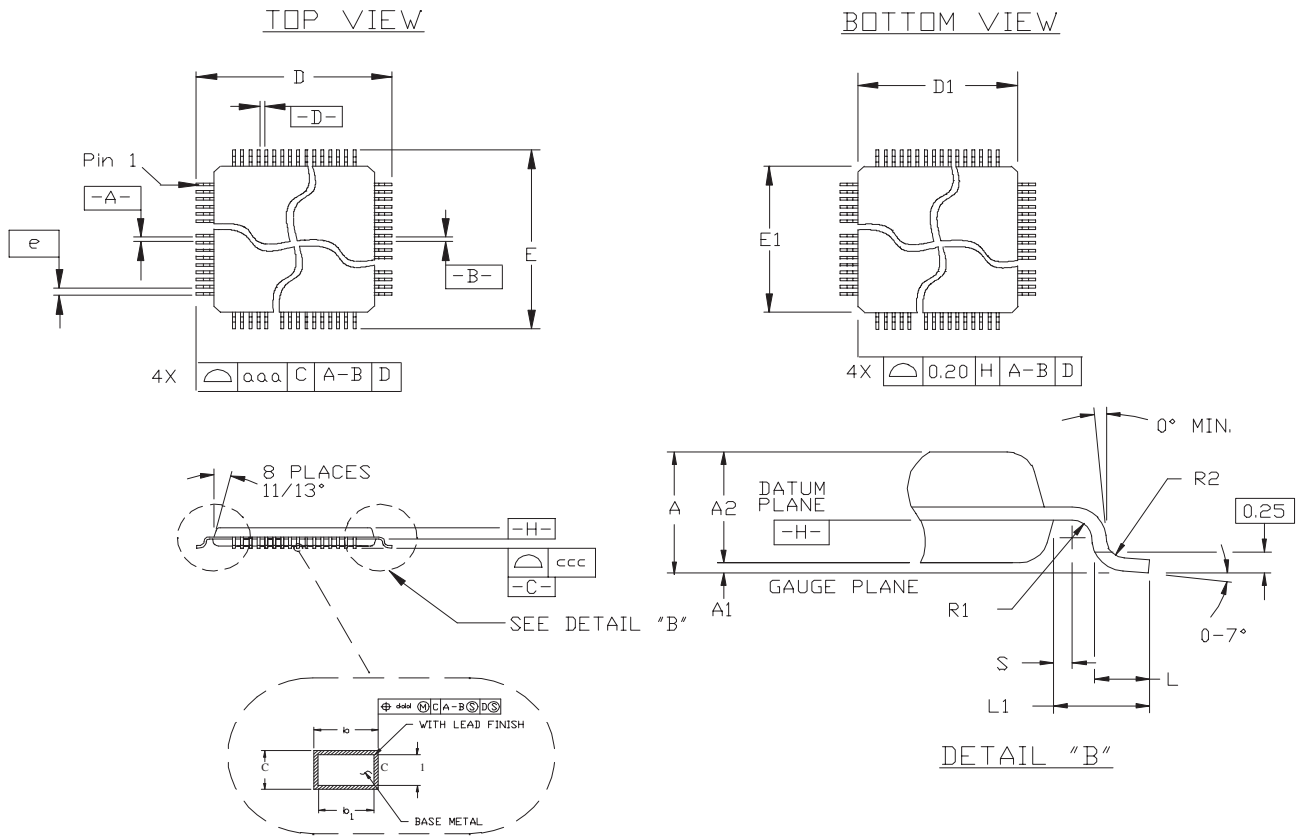**Figure 6.** AT75C221 BGA Package

For BGA package data, see Table 3 on page 20,

BGA Package Data

Table 3. Dimensions (mm)

Symbol	Min	Nom	Max
A1	0.50	0.60	0.70
$\varnothing$b	0.60	0.75	0.90
aaa		0.30	
bbb		0.25	
ccc		0.35	
ddd		0.30	
eee		0.15	
A	1.92	2.13	2.34
B	0.28	0.32	0.38
D/E	26.8	27.0	27.2
D1/E1		24.0	24.7
e		1.27	
f		8.05	

PQFP Packaging Information

Figure 7. PQFP Package Drawing

For package data, see Table 4, Table 5 and Table 6 on page 22.

PQFP Package Data

Table 4. Dimensions (mm)

Symbol	Min	Nom	Max
c	0.11		0.23
c1	0.11	0.15	0.19
L	0.65	0.88	1.03
L1	1.60 REF		
R2	0.13		0.3
R1	0.13		
S	0.4		
Tolerances of Form and Position			
aaa		0.25	
ccc			0.10

Table 5. Dimensions specific to PQFP Package (mm)

A	A1	A2			b		b1			D	D1	E	E1	e	ddd
Max	Min	Min	Nom	Max	Min	Max	Min	Nom	Max	BSC	BSC	BSC	BSC	BSC	BSC
4.10	0.25	3.20	3.40	3.60	0.17	0.27	0.17	0.20	0.23	31.20	28.00	31.20	28.00	0.50	0.10

Table 6. 208-lead PQFP Package Electrical Characteristics

Body Size	R (mΩ)		C_s (pF)		C_m (pF)		L_s (nH)		L_m (nH)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
28 x 28	53	71	1.4	1.7	0.56	0.73	6.7	8.4	3.9	5.1

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