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AN124

Application Note

FREQUENTLY ASKED QUESTIONS: VIDEO & IMAGING

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CCD ISSUES

Q. What is a CCD Imager?

A. A CCD (Charge-Coupled Device) is an integrated circuit with a two dimensional array of light sensitive Silicon photodiodes. Light from the scene is brought into focus at the imaging plane of the CCD by a lens. A CFA (Color-Filter-Array) that overlays the photo-sites ensures that each photo-site responds only to a particular color (in the case of a complementary-mosaic CFA, these colors are Cyan-Magenta-Green-Yellow).

The following functions take place within the CCD:

Integration: During the integration period, charge is integrated in the active photosites of the Imaging Area. A photosite consists of two potential wells, an active well and a storage well. The active well is a precharged photo-diode that integrates the charge from photo-transduction. The amount of charge that is integrated is proportional to (1) the illumination received at each photosite and (2) the integration time (typically 1/60sec).

Charge Transfer: Each light sensitive photo-site has a storage site that corresponds to it. After integration, the collected charge is transferred to the storage sites which are shielded from light.

Readout: After charge transfer, a new integration period begins; the stored charge is loaded one line-at-a-time into a shift register and then sequentially to a detection node where they are made available as signal voltages. Note: While one charge matrix is being read out from the storage sites, the next charge matrix is being integrated in the photosites of the CCD.

Q. What imager sizes are available?

A. CCD imager sizes vary from the small QCIF (180H x 120V) to mega-pixel imagers with 1 million, 2 million and 4 million pixels.

CS7615 & CS7665 ISSUES

Q. What is the CS7615?

A. The CS7615 is a low-power Analog front-end processor for standard four-color interline transfer CCD imagers. The architecture includes a correlated double sampler, AGC amplifier, black-level clamp, 10-Bit A/D converter, and a complete multi-sync CCD timing generator. The analog CCD imager output can be directly connected to the CS7615 input, which does not require an external buffer amplifier. The pixel data is double sampled for improved noise performance, and gain adjusted prior to being digitized by the A/D converter. Feedback from the A/D converter holds the image black level at code-16 (assumes 8-bit data path), easing ITU-601 compliance issues. The multi-sync CCD timing generator is programmed via the I^2C bus, and can be used with a wide range of interline transfer CCD imagers up to 1024 pixels wide. The CS7615 supports full ITU-601 compliance for images up to 720 pixels wide, and is compatible with both NTSC and PAL timing. The CS7615 is designed to be used along with the CS7665 Digital Color-Space Processor for CCD Cameras, which generates a 4:2:2 component digital video output.

Q. The CS7615 provides all of the timing for the camera, but how do I program it?

A. The CS7615-CS7665 has a two-wire I^2C serial I/O port which allows the user to read and write all the necessary registers within the chipset. This is usually done after power-up, since the chipset registers come up in the default mode. There are two commonly used methods of programming the CS7615-CS7665 registers:

1) EEPROM method: the CS7665 supports several commercially available EEPROMs; on power-up, the CS7665 automatically comes out of reset and queries the I^2C bus, looking for the presence of an EEPROM. If an EEPROM is detected, then register values are read from the EEPROM and written to all the targeted

devices on the I^2C bus. This mode is particularly useful for stand-alone cameras, which are not tethered to a PC.

2) HOST-CONTROLLER method: the host PC or micro-controller, under software control, can read and write registers within the CS7615-CS7665 chipset as well as registers in any other I^2C devices on the bus. Since I^2C is a relatively slow protocol (about 100 KHz clock rate, typical) it is possible to use the parallel port of a PC to "bit-bang" the I^2C bus. In other applications, the I^2C bus (2-pins) is brought out along with the digital video bus and is controlled by software that runs on the host PC.

Q. How can I determine what timing values should be programmed into the CS7615?

A. The CS7615 has several timing registers; functionally they can be broken down into the following:

1) CCD timing control: these register values are determined by the type of CCD that is in the camera. The three CCD clock groups are the frame-transfer, the vertical transfer, and the horizontal transfer clocks. The frame transfer clocks will cycle at the image frame or field rate depending on whether the imager is progressive or interlace transfer. For common consumer CCD imagers the frame transfer clocks are often designated as VH1 and VH3. The vertical transfer clocks will cycle at the horizontal line rate of around 15kHz; the vertical transfer clocks are often designated as V1, V2, V3, and V4. All three of the horizontal clocks cycle at the pixel rate, which ranges from 1MHz to 13.5MHz. The horizontal transfer clocks include the actual horizontal clocks, H1 and H2, as well as the CCD imager output amplifier reset clock.

2) CDS/AGC timing control: some of these values are determined by the type of CCD that is in the camera; others are determined by user preference. The processing group of clocks includes the feedthrough clock, the T/H clock for the CDS, the ADC convert clock, and the black level clamping clock. The first three clocks operate at the pixel rate, and move the CCD imager output through to the ADC. The black clamp clock operates at the horizontal line rate, and is only used if the black level offset is added before the ADC.

3) System timing: most of these register values are determined by the camera designer based on system choices.

Q. With all of the AGC specific control registers, how can I determine the right values?

A. The AGC uses values in several registers to provide a wide range of programmability. In order to alleviate confusion, follow these steps: First, choose which type of data upon which the AGC operates, mosaic or luminance (Reg24h bit 3). We have found that there is not much difference in performance between the two but the luminance does settle to a slightly lower gain. Most of the time it is left to its default value (luminance).

Next, choose what portion of the image to use for the AGC (reg24h bits 5,6). The choices are: entire screen, center 1/4, or center 1/16. Entire screen or center 1/4 provide the best results. We have found that center 1/16 settles to too large a gain value for most cases. For less sensitivity to surrounding lights use center 1/4.

Next, set the target value (Reg 29h). This will determine the gain value to which the AGC will settle and the sensitivity of the AGC to small bright lights. We have found that a value of 3 to 6 provides good results. If the image is still too light or dark use digital gain in the CS7665 chip. Set the maximum gain (reg 2Ah) to limit the most the CS7615 will gain up a dark image (see below). Set the minimum gain (reg 2Ch) to match the CCD output range (see below). The Maximum shutter exposure register (reg 30h) can be left at its default unless you need to limit the maximum exposure of the CCD.

The last step is to adjust the speed of the AGC. This is set with the speed and slew registers (reg 2Bh). The speed is a multiplier to control both rising and falling gain settling times. The slew is the rate at which the AGC responds to

changes in the brightness of the scene (from very dark to very bright). If the scene brightness changes abruptly from very dark to very bright, it is necessary to respond rapidly since the CCD is saturated and there is no histogram information available. It is important to keep the product of the *speed* × *slew* from exceeding -32. This will cause big negative jumps in the gain and will show up as a flash when lighting conditions change. We have found that a speed of x4 and a slew of -8 will provide good results but this is very subjective and you should tweak to your satisfaction. The flickerless setting can be chosen (reg 24h bit 1) in order to provide an extra 6 dB of gain range that is free of fluorescent light flickering.

Q. The CS7615 AGC unit is affected by numerous registers, do all of these registers need to be adjusted for the camera to work?

A. Some of the registers are more important to adjust than others. At the very minimum the target value (reg 29h) and the minimum gain (reg 2Ch) should be set. The target value's default is 0 which produces an AGC response that is very sensitive to small bright lights. We suggest a setting from 3 to 6. The minimum gain value should be set according to the maximum output range of the CCD (see below). If minimum gain is not set it can cause CCD to saturate before going into shutter mode. Next in importance would be the speed and slew (Reg 2Bh) to adjust the settling time. To customize the AGC further the AGC window = center 1/4 (reg 24h bits 5,4=0,1) can be used to reduce the sensitivity to surrounding lights and the flickerless setting (reg 24h bit 1) can increase the flicker free gain range by 6 dB. The remaining AGC settings (AGC algorithm, max gain, maximum shutter exposure) can be used for advanced fine tuning.

Q. What purpose does the Minimum Gain Register perform?

A. The minimum gain register is used when the CCD saturation voltage is less than 1.6V. In order to insure that the CCD output is not saturated by the time shutter gain becomes active, the user must set the minimum gain so that $min\_gain \times CCD\_sat\_voltage = 1.6V$. If the CCD saturates, the shutter gain will never be engaged (or will respond very slowly), causing bright scenes to be lost.

Q. What purpose does the Maximum Gain Register perform?

A. Maximum gain is used if the user wants a scene to go dark at a certain low light level as opposed to gaining up a noisy image.

Q. What is the CS7665?

A. The CS7665 is a low-power Digital Color-Space Processor for CCD cameras. It provides all necessary digital image processing for standard four-color interline transfer CCD imagers. The CS7665 processes the Magenta-Yellow-Cyan-Green CCD imager data into YCrCb formatted component digital video. Internal processing includes color separation, automatic white balance, user-programmable gamma correction curves, square pixel interpolation, and output formatting. The CS7665 employs an advanced color anti-aliasing filter which prevents both incorrect color and "color noise" that can undermine compression-based systems. The CS7665 digital output is ITU-601 compliant and supports both ITU-656 and SMPTE-125/ M transport. Additionally, HREF and VREF (or VSYNC) output pins are provided to synchronize with older analog video encoders and the current ZV-Port definition. The CS7665 can support horizontal line widths of up to 1024 pixels. It has no limitations on the number of lines it can support in the vertical direction. The CS7665 is designed to work directly with the CS7615 CCD Imager Analog Processor.

Q. What is White Balance, and why is it needed?

A. The white balance control calibrates a camera's relative sensitivity to different colors in order to match the overall color cast of the light source.

White light is a combination of all the visible frequencies, or colors, of light. Though “white” light contains all visible frequencies, the relative amounts of the frequencies present in it are not fixed. Color temperature is the quantitative measure that expresses a white light's composition in terms of degrees Kelvin.

Candle light has a color temperature of around 1600-1800K and not much of this light comes from the blue end of the spectrum. Studio photoflood light (incandescent light) is at 3200 or 3400K. The sunlight outdoors can range from 4000K to 7000K. Light of color temperature beyond 7000K has very little red component in it.

The wild card in this system is fluorescent light. Unlike natural or incandescent light, fluorescent light does not include all frequencies in the visible spectrum. Because fluorescent light is not created by heating an object (like a light bulb filament) but rather by ionizing gases to make them glow. Each gas present in the mixture emits light of a certain frequency; the manufacturers mix gases so that the combined result appears as cool white light. Typical color temperatures of fluorescent light used in household or office are 3500K, 4100K.

Since a camera sees an object by the light it reflects, different lights can cause an object to have different colors. In order to get the object's “true color”, the camera has to know what kind of light source is being used and then compensates for it. This is why white balance is needed.

To use the white balance feature, first the camera has to be pointed at a pure white object. Then the user activates the white balance function, telling the camera, “this is white.” The white balance circuit then adjusts the gains on the red, green and blue signals (computed from the Cyan-Magenta-Yellow-Green signals that come from the CCD) so that the object appears white on the output end. At this point the camera is white-balanced for the light in use and needs no more white balance unless the light source changes.

Q. What is the color separation matrix?

A. For cameras that use Cyan-Magenta-Yellow-Green mosaic CCDs, certain color conversion has to be done to generate RGB or YCbCr outputs. The arithmetic required is, in general, a linear operation and can be carried out as a matrix multiplication.

CYMG mosaic CCDs send out summed data such as CY (meaning C + Y), CM, MG, YG on alternate pixels / lines. These data do not follow normal video signal standard and therefore can not be used directly. The primary job of the CS7665 is to separate the raw CCD data and to extract the RGB values of each pixel for video output. This has been implemented as a 3x3 matrix which has nine independent coefficients. One set of fixed coefficients is sufficient for a given CCD model. Since the CS7615/7665 can support many different CYMG CCDs, we have made the 3x3 matrix fully programmable to accommodate all CCDs with ease.

Q. How do the saturation controls work?

A. The saturation controls in CS7665 are quite straightforward. The data being adjusted by the “blue saturation control” is Cb (as in YCbCr), while Cr is adjusted by the “red saturation control.” The data controls digital gain in a linear manner; a larger number represents more saturated (or rich) color.

Q. What methods are available for programming the camera settings?

A. Camera settings can be loaded in one of two ways: from a Serial EEPROM or an external controller.

When the CS7665 is RESET, it looks for a Serial EPROM on the I^2C bus and loads configuration information using the I^2C protocol.

If no Serial EPROM is present, configuration information can be loaded into the camera chip by an external controller using I^2C.

Q. What software does Crystal provide?

A. Crystal provides a program called CSCam16 to provide access to all the CS7615 and CS7665 registers. This program is designed to work with our reference designs, but can also work on other designs that provide access to the chips via I^2C.

Crystal also provides with its digital camera reference designs a video capture application called TVTap (if using the CL-GD5465 based digital camera interface) or Microsoft's Vidcap32 and drivers for the Bt848-based PCI video capture board. These are included to allow the user to evaluate our digital camera performance.

SYSTEM ISSUES

Q. What kind of imagers can be used with the CS7615 and the CS7665?

A. The CS7615-CS7665 chipset has been designed to work with imagers that meet the following criteria:

1) The number of pixels/line has to be less than 1024

2) The number of lines/field has to be less than l023

3) The imager has to generate interlaced video—progressive scan imagers are not supported by the current chipset.

4) The pixel rate has to be less than (or equal to) 15 MSPS. This can be computed from the field rate, the number of lines/field and the number of pixels per line.

5) The CFA (color-filter-array) has to be of the complementary mosaic variety—RGB stripe filters or Bayer filters are not supported by the CS7665 color processor.

Q. What specific imagers are compatible with the Crystal chips?

A. CCD Compatibility List:

The following is a partial list of imagers that meet the above criteria; in some cases, the imager part numbers have the letter (U) against them, signifying that it should work, but has not yet been tested. This list shows color imagers only, although the CS7615 can be used with monochrome imagers as well. Also, most of the imagers on this list have PAL versions which will also work with this chipset.

Manufacturer	Part Number	Description	
Sharp	LZ2313H5	1/3"; 512 (H) x 492 (V)	NTSC
Sharp	LZ2413A	1/4"; 512 (H) x 492 (V)	NTSC
Sharp	LZ2453A	1/4"; 768(H) x 494 (V)	NTSC
		pin compatible with PAL LZ2463A	
Panasonic	MN37110FP	1/4"; 512 (H) x 492 (V)	NTSC
Panasonic	MN37112FP	1/4"; 512 (H) x 492 (V)	NTSC
		** recommended for new designs (better sensitivity),	
		pin compatible with MN37110FP **	
Panasonic	MN3718MFE	1/3"; 768 (H) x 492 (V)	NTSC
Sony	ICX044BKA (U)	1/3"; 510 (H) x 492 (V)	NTSC
Sony	ICX054BKA (U)	1/3"; 510 (H) x 492 (V)	NTSC
Sony	ICX058AK	1/3"; 768 (H) x 494 (V)	NTSC
Sony	ICX058AKB (U)	1/3"; 510 (H) x 492 (V)	NTSC
Sony	ICX056AK	1/4"; 510 (H) x 492 (V)	NTSC
Sony	ICX056AKB (U)	1/4"; 510 (H) x 492 (V)	NTSC
Sony	ICX068AK (U)	1/4"; 768(H) x 492 (V)	NTSC
PAL CCDs			
Sharp	LZ2463A	1/4"; 752(H) x 582(V)	PAL

Q. What are supply voltage requirements for CCDs?

A. In addition to the +5 V that is required for most of the timing and logic circuits (including the horizontal shift register signals), most CCDs of commercial interest require +15 V (for the reset drain and the output drain) as well as -8 V (for the protecting p-well). The substrate is usually held at a bias voltage anywhere from 10 V to about 25 V (this is batch-dependent and is usually stamped on each CCD) and is pulsed higher only during electronic shutter operation. The vertical shift register clock pulses (V1,V2,V3,V4) usually swing between -8 V and +15V; V2 and V4 are bi-level signals (+15V, -8V) while V1 and V3 are tri-level signals (+15V, 0V, -8V). Note: the levels mentioned here are nominal values and care must be taken to match a particular imager's requirements.

Q. How are these voltages generated?

A. Since most camera designers prefer to work with +5V, it is necessary to generate the +15 V and -8 V from the +5V. In most cases a charge pump is used to generate the +15 V and -8 V supplies from the +5 V source. The CS7615 supplies a signal at the video horizontal line rate that can be used to drive a charge pump. It is necessary to restrict all the charge pump action to the horizontal blanking interval, in order to minimize the injection of noise during the active video period. The reference designs for the CS7615-CS7665 chipset include schematics of typical charge pump circuits using discrete components. In addition, some vertical drivers also include the charge pump function on-chip, making for a simplified camera design.

Q. Can I use a standard dc-dc converter chip?

A. Most dc-dc converter chips have an on-chip oscillator that runs at a fairly high frequency (typically a few hundred kilo-hertz). This is required in order to limit the magnetics in the dc-dc converter circuit to a reasonable size. Unfortunately, this high frequency can couple in the video signal as interference - resulting in unacceptable image quality. If it is possible to switch the dc-dc converter circuit only in the horizontal blanking interval of the video, then such a dc-dc converter circuit can be used without adversely affecting image quality.

Q. Besides the Crystal chips, what else is needed to build a camera?

A. Optics: (1) Lens (2) Lens-mount (3) Optical anti-aliasing filter (4) IR filter

Electronics: (1) CCD imager (2) Vertical driver (3) Charge pump circuit (4) Analog video encoder (required for analog output cameras only)

Miscellaneous: (1) Camera enclosure (2) Input and output connectors (3) Cables

Q. What is the V-Drive chip?

A. The V-drive (or vertical driver) chip is used to convert the TTL level vertical timing signals (V1, V2, V3, V4) to the bi-level or tri-level signals that are required by the CCD. Most V-drive chips also level shift the Vsub (or substrate drive) signal to the appropriate level that is required for normal substrate biasing as well as to a higher level for electronic shuttering.

Q. What is Electronic Shutter?

A. Electronic shuttering is the process of controlling the exposure period of the CCD by electronic methods (compared to conventional shuttering, which involves an electro-mechanical shutter system that opens, allowing light to fall momentarily on the CCD, and then closes). In most interline transfer CCDs the process of electronic shuttering involves "dumping" accumulated charge from the imaging photosites to the substrate for a predetermined amount of time and then stopping the "dumping" process for the actual exposure period. This is followed by the normal charge transfer during vertical blanking and then readout during the next field.

Q. Why is code 16 important?

A. Code 16 refers to the lowest nominal value for a digitized luminance level (black). Some excursions below this level are allowed (also referred as blacker-than-black values), but Code 0 is not is not permitted. It is reserved for timing information.

Q. What is the Black Level?

A. The "black level" in a video system establishes a datum or a reference level that corresponds to a completely black pixel. Since a video signal (digital or analog) is a method of conveying spatial and temporal information about an image, it is necessary to establish a reference "black level." All signal levels that are higher than this "black level" have a non-zero brightness. In the CCIR601 video specification, the digital 8-bit code Hex10 (or decimal 16)is used to designate the black level. This is analogous to the "pedestal" or "setup" in an analog video signal.

Every row of a CCD has some covered "optically black" pixels which are identical to the imaging photo-sites but are covered by opaque material. The signal generated when these "optical black" pixels are read out is used as a reference "black level" while that horizontal line is being processed.

In a conventional analog camera, the CCD output is clamped (once every horizontal line) to a known reference during the optical black period. In a digital system, such as the CS7615-CS7665 chipset, it is more efficient to accumulate the optical black pixel values and then force the black level to a target value (such as Hex 10) within a closed loop system. This is accomplished with the CS7615 Analog Front End chip.

Q. How many bits of resolution do I need?

A. In an ideal world, the answer to this would be "as many as you can get." In the real world, however, there are some practical limits.

a) Most commercially available CCDs have a signal-to-noise ratio of about 50 dB (max). This translates to about 8 effective bits, when the CCD video signal is digitized. If the CCD video is digitized using an A/D converter that has more than 8 bits, the extra bits usually represent random noise. While it is useful to use 10-bit (or greater) data during processing (as in the case of the CS7615-CS7665), the final result can be truncated to 8 bits without any significant loss of information.

b) Most commercially available video encoders (digital-to-analog video converters) accept 8 bit data. Therefore, the processed digital video output from the camera chipset may be limited to 8 bits if the output is to be converted into analog video data.

Q. What is the difference between the 8-Bit and 10-Bit Standards?

A. In terms of timing (via the End-active-video and Start-active-video) the 8 bit and 10 bit standards are the same except that for the 10 bit standard the EAV and SAV codes are aligned with the MSB and the bottom two bits are set to 00.

Q. What is CDS and what purpose does it serve?

A. Correlated Double Sampling (CDS) is based on using two successive track-and-holds (T/H) to reduce the low frequency noise inherent in standard CCD imager outputs. The individual pixel output level is defined relative to the CCD feedthrough level. The feedthrough level is roughly equivalent to a standard pixel output level with no light incident on the pixel itself. Although the amount of accumulated charge on a dark pixel is almost zero, several leakage and noise sources contribute a finite charge accumulation even under dark conditions. Theoretically the feedthrough or dark level is the same for all pixels, but in practice there is a statistically significant level of variation in the feedthrough level across a CCD imager. Additionally, low frequency noise sources affect pixel levels and feedthrough levels

equivalently by introducing very small voltage offsets in the CCD output. By storing the feedthrough level in a track-and-hold, the pixel level can be subtracted from the held feedthrough level for a very accurate measurement of the pixel. The feedthrough level minus the pixel level difference is typically held in a second track-and-hold, which is the basis of the double sampling in the CDS. Some ADC topologies do not require the second T/H to maintain the difference signal over an extended period, and will simply eliminate the second T/H to allow the ADC to perform this function directly.

Q. Can I use the CS4952/CS4953/CS4954 to generate an analog output?

A. The CS4952/CS4953/CS4954 family of encoders are a terrific way to generate analog composite video, S-Video and component RGB video (NTSC/PAL format) from a digital video stream. However, they are intended for use with CCIR-601 digital video (720H x 480 V x 13.5 MHz). Since there are no 720(H) CCDs available commercially, the CS7615-CS7665 camera chipset is somewhat limited in its ability to interface to the CS4952/CS4953/CS4954 family of encoders. However, the CS7615-CS7665 chipset can operate in the "interpolation" mode and can take the video output from a 512(H) CCD and create a 640(H) x 480(V) x 12.2727 MHz digital video signal which is compatible with many commercially available video encoders that are specifically designed for that format.

The CS7666 (next generation version of the CS7665, release expected by Summer, 1998) has a built-in scaler which allows a seamless interface to the CS4952/CS4953/CS4954 family of encoders.

Q. Will Crystal have a camera using the CS4952/CS4953/CS4954?

A. Yes, a reference design (involving the CS7615, CS7666 and the CS4954) is in progress. By Summer, 1998 a camera reference design will be available showcasing an "all Crystal" camera solution. Several commercial CCDs of different formats will be supported by this reference design, which will have digital as well as analog (composite and S-Video) video outputs.

Q. Why do I need an IR filter?

A. An optical IR block filters out the IR (Infra-Red) component of the light. This is required because the CCD follows the photo-response curve of Silicon and exhibits a higher sensitivity in the NIR (near-infra-red) part of the spectrum. If the IR component of a scene is allowed to fall on the CCD, it would distort the colors in the image.

For example, green leaves reflect the green part of the visible spectrum; the leaves also exhibit a high reflectance in the NIR region. If a scene that included green leaves illuminated by sunlight was imaged by a CCD camera without an IR filter, the leaves would appear to be almost white! This is because all the photo-sites would respond to the IR reflected by the leaves - instead of just the "green" sites responding.

Q. How fast is USB?

A. The maximum theoretical peak data rate over a Universal Serial Bus (USB) is 12 Mbps.

However, due to protocol and operating system overhead, you should expect a maximum sustained data rate of about 6 Mbps (or less if other devices share the bus). Your actual throughput will depend on the system's configuration.

Q. How fast is the parallel port of a PC?

A. It is difficult to quote performance for a typical PC parallel port. It is very dependent upon the PC's configuration, operating system, and the applications that are running. The speeds for transmitting and receiving data may be different. In addition, there are three different types of parallel ports that may be found in PCs today: the original Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP), and the Extended Capability Parallel Port (ECP).

The typical SPP will transmit data between 10 KB and 50 KB per second. The newer EPP and ECP parallel ports are much faster with OEMs claiming burst data transfer rates as high as 2 MB per second. More information on parallel ports, including the EPP, ECP and the IEEE 1284 PC Parallel Port Standard can be found at: http://www.lvr.com/parport.htm.

VIDEO ISSUES

Q. What is composite video?

A. Composite video is an analog representation of video; it conveys luminance (brightness), chroma (color) and sync (timing) information, carried over one wire (with respect to a ground), to a display device. Sync (short for synchronization) is timing information in the form of a series of pulses at horizontal rate (horizontal sync) and vertical rate (vertical sync). Luminance is a time-varying voltage signal that represents the brightness of each individual location of the image - referenced to a "back porch" which is the part of the signal immediately after the horizontal sync signal but before the beginning of active video. The chrominance signal is in the form of a carrier signal which is phase modulated to encode the hue (color) and amplitude modulated to encode the saturation (depth of the color) of each individual location of the image. The chrominance signal is superimposed on top of the luminance signal. A sinusoidal color burst is added at the beginning of each line; this color burst provides a zero phase reference for the display device.

Q. How many frames per second does television deliver?

A. It depends on what region of the world you are located. For example, in the United States the broadcasting system is NTSC; in the NTSC system, a television will deliver 30 frames per second. An NTSC frame is made up of two interlaced fields; therefore, there are 60 fields per second. Each frame displays one odd and one even field in an interlaced fashion. The field frequency, (60 Hz) matches that of the AC outlets in the US. In Europe, the PAL system is used. There, a television set will deliver 25 frames per second. This equals 50 fields per second. This frequency (50 Hz) matches that of the AC outlets in that region.

Q. What is a video encoder?

A. A video encoder is an integrated circuit device that is used to convert a digital video data stream into an analog signal that can be displayed on a video monitor. Most encoders have several analog outputs, including composite video, S-Video and component video (R-G-B format). Some encoders can take digital video data with embedded EAV (end-active-video) and SAV (start-active-video) codes and generate Horizontal and Vertical sync timing from those codes. Other encoders have input pins which allow the user to feed Horizontal and Vertical sync signals to the encoder. In addition to the digital video data and the sync signals, an encoder should also be supplied with a pixel clock signal. In some applications, the video encoder can act as a "master" source of sync and/or pixel clock, but in most camera applications, the video encoder is a "slave" and needs to receive sync and pixel clock signals along with digital video data. An example of a video encoder is the CS4954 encoder that is available from Cirrus Logic - Crystal Semiconductor Products Division.

Q. What are SAV and EAV?

A. EAV refers to End of Active Video

SAV refers to Start of Active Video

These are reserved data codes that are embedded in an H.656 digital video stream and occur once per video line. Each code has four bytes (Hex"FF" Hex"00" Hex"00" Hex"XY") where "XY" contains horizontal, vertical and field timing information.

Q. What are H.320 and H.324?

A. ITU-T H.320 is a family of standards developed for video teleconferencing systems using ISDN lines. It uses the ITU-T H.261 standard to define its video compression and decompression.

ITU-T H.324 standard was developed for multimedia communication systems using conventional phone lines. It uses the ITU-T H.263 standard to define its video compression and decompression.

Q. What are H.261 and H.263?

A. These two standards use Discrete-Cosine-Transform (DCT) type of compression algorithms.

ITU-T H.261 standard is used for video compression and decompression over ISDN lines. It has a data rate of p X 64 kbps (1 =< p =< 30).

ITU-T H.263 standard is used for video compression and decompression over standard telephone lines. The data rate is defined by ITU-T V.34 (28.8 kbps modem spec.).

Q. What is "magic" about 13.5 MHz?

A. In order to digitize video it needs to be sampled at a certain sampling rate. Generally the video bandwidth is about 6 Mhz, therefore the lowest sampling rate (based on the Nyquist criterion) is about 12 Mhz.

Currently there are 3 major video broadcast systems in use worldwide, which are NTSC, PAL and SECAM. NTSC uses 525 lines per frame and is based on a 59.94 Hz field frequency (resulting in a 63.55uSec line period) whereas PAL and SECAM use 625 lines per frame and are based on 50 Hz field frequencies (resulting in a 64uSec line period).

With a sampling frequency of 13.5MHz, the NTSC system has 858 pixel clock periods in each horizontal line and the PAL/SECAM systems have 864 pixel clock periods in each horizontal line. This allows all three systems (NTSC, PAL and SECAM) to have an integer number of pixel clocks in each horizontal line - easing the design of timing circuits for all three systems.

By selecting the same number (720) of active pixels per line at the same pixel clock frequency (13.5MHz) for all three systems, digitized video material at 720(H) x 13.5MHz in all three systems (NTSC, PAL & SECAM) can be viewed without aspect ratio distortion.

The digital video standard for these systems was chosen in such a way, that one sampling frequency can accommodate all these different standards. The 13.5 Mhz sampling frequency is the lowest possible frequency (above 12MHz) to achieve this goal.

Q. What is ITU-R BT.601

A. The ITU-R BT.601 is a standard of the International Telecommunication Union which defines the encoding of digital television video data. This standard was originally created by the CCIR committee, where it was called CCIR-601.

The standard defines the line and pixel numbers in digital video, it defines the color space conversion parameters (RGB <-> YCbCr) and it also defines the video signal filter specs.

Q. What is ITU-R BT.656

A. The ITU-R BT.656 was originally created by the CCIR committee, where it was called CCIR-656.

The standard defines the interfaces for digital component video signals for 525 and 625 line systems.

In particular it describes the signal format (which is based on the ITU-R BT.601 format), the characteristics of the bit-parallel and bit-serial interface signals and the mechanical characteristics of the connector.

Digital video interfaces nowadays conform to this specification, since it allows for a very straight forward implementation. One nice

feature of this specification is that the synchronization signals are already encoded into the datastream, which saves pins on ICs and wires on hardware boards.

Q. Do florescent lights really flicker?

A. Yes, they usually have a component that is at twice the power line frequency rate (i.e. 2 x 60 Hz = 120 Hz in the US). This can create a problem in a camera when the electronic shutter is used due to the fact that the exposure period in the electronic shutter mode is small (relative to the 60 Hz AC line frequency). A "breathing" effect is observed; the camera signal amplitude goes up and down over time. This occurs because the amplitude of the camera signal depends upon the amount of light that is incident on the CCD during each exposure and that changes slightly from one exposure to the next if the field rate is not locked to the power supply of the lighting system.