

FEATURES

- 1.8 V analog supply operation**
- 1.8 V to 3.3 V output supply**
- SNR = 71.8 dBc (72.3dBFS) to 70MHz input**
- SFDR = 85 dBc to 70MHz input**
- Low power: 395 mW**
- Differential input with 650 MHz bandwidth**
- On-chip reference and sample-and-hold**
- DNL = ± 0.5 LSB**
- Flexible analog input: 1 V p-p to 2 V p-p range**
- Offset binary or twos complement data format**
- Clock duty cycle stabilizer**

APPLICATIONS

- Ultrasound equipment**
- IF sampling in communications receivers:**
 - IS-95, CDMA-One, IMT-2000
- Battery-powered instruments**
- Hand-held scopemeters**
- Low cost digital oscilloscopes**

GENERAL DESCRIPTION

The AD9246 is a monolithic, single 1.8 V analog supply, 14-bit, 125 MSPS analog-to-digital converter (ADC), featuring a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9246 uses a multistage differential pipelined architecture with output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9246 is suitable for applications in communications, imaging, and medical ultrasound. A differential clock input is used to control all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. A differential data output clock (DCO) is provided to ensure proper latch timing with receiving logic.

Rev. PrH

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FUNCTIONAL BLOCK DIAGRAM

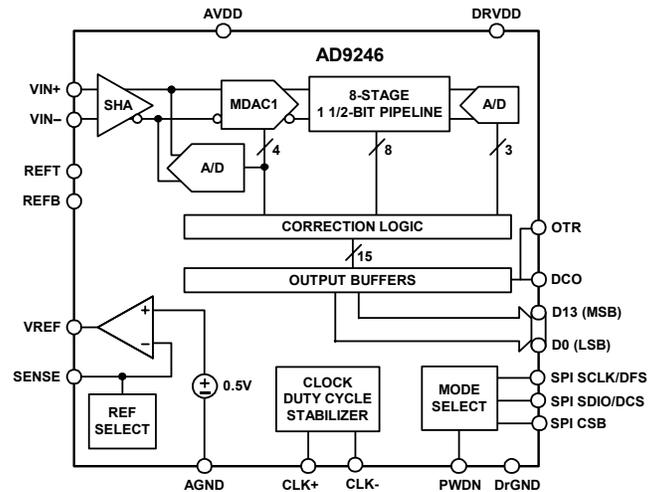


Figure 1.

Fabricated on an advanced CMOS process, the AD9246 is available in a 48-lead LFCSP and is specified over the industrial temperature range (-40°C to $+85^{\circ}\text{C}$).

PRODUCT DESCRIPTIONS

1. The AD9246 operates from a single analog 1.8 V power supply and features a separate digital output driver supply to accommodate 1.6 - 3.3 V logic families.
2. The patented SHA input maintains excellent performance for input frequencies up to 180 MHz and can be configured for single-ended or differential operation.
3. The clock DCS maintains overall ADC performance over a wide range of clock pulse widths.
4. Standard serial port interface supports various product features and functions, such as data formatting (offset binary, 2's complement, or Gray coding), enabling a clock duty cycle stabilizer, power-down, and voltage reference mode.

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REVISION HISTORY

6/05—Revision PrG: Preliminary Version

9/05 – Revision PrH: corrected SNR on page 1

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 3.3 V, sample rate = 125 MSPS, 2 V p-p differential input, 1.0 V internal reference, unless otherwise noted.

Table 1.

Parameter	Temp	AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.25	±		±0.25	±	% FSR
Gain Error (External 1.0 V Reference)	25°C		±0.2			±0.2		% FSR
Gain Error	Full		±0.3			±0.3		% FSR
Differential Nonlinearity (DNL) ¹	Full			±TBD			±TBD	LSB
	25°C		±0.5			±0.5		LSB
Integral Nonlinearity (INL) ¹	Full			±			±	LSB
	25°C		±2			±2		LSB
TEMPERATURE DRIFT								
Offset Error	Full		TBD			TBD		ppm/°C
Gain Error	Full		TBD			TBD		ppm/°C
Gain Error (External 1.0 V Reference)	Full		TBD			TBD		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		TBD			TBD		mV
Load Regulation @ 1.0 mA	Full		TBD			TBD		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		TBD			TBD		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance ²	Full		8			8		pF
REFERENCE INPUT RESISTANCE	Full		TBD			TBD		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.6	3.3	3.6	1.6	3.3	3.6	V
Supply Current								
IAVDD ¹	Full		219			219		mA
IDRVDD ¹ (3.3V)	Full		19			19		mA
IDRVDD ¹ (1.8V)	Full		10			10		mA
PSRR	Full		±0.01			±0.01		% FSR
POWER CONSUMPTION								
DC Input	Full		395			395		mW
Sine Wave Input ³ (DrVDD=1.8V)	Full		412			412		mW
Sine Wave Input ⁴ (DrVDD=3.3V)	Full		457			457		mW
Standby Power	Full		40			40		mW
Powerdown Power ⁵	Full		1.8			1.8		mW

¹ Measured at the maximum clock rate, $f_{IN} = 2.4$ MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.

² Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 2 for the equivalent analog input structure.

³ Measured at ac specification conditions with approximately 5 pF loading on each output bit.

⁴ Measured at ac specification conditions with approximately 5 pF loading on each output bit.

⁵ Standby power is measured with a dc input, the CLK pin inactive (that is, set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 3.3 V, sample rate = 125 MSPS, 2 V p-p differential input, 1.0 V internal reference, AIN = -0.5 dBFS, DCS on, unless otherwise noted.

Table 2.

Parameter	Temp	AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	
SIGNAL-TO-NOISE-RATIO (SNR)								
$f_{IN} = 2.4$ MHz	25°C		72.0			72.0		dB
	Full		70.8			70.8		dB
$f_{IN} = 70$ MHz	25°C		71.8			71.8		dB
	Full		70.5			70.5		dB
$f_{IN} = 100$ MHz	25°C		71.5			71.5		dB
$f_{IN} = 180$ MHz	25°C		69.0			69.0		dB
SIGNAL-TO-NOISE-AND DISTORTION (SINAD)								
$f_{IN} = 2.4$ MHz	25°C		71.2			71.2		dB
	Full		70.5			70.5		dB
$f_{IN} = 70$ MHz	25°C		70.7			70.7		dB
	Full		70.0			70.0		dB
$f_{IN} = 100$ MHz	25°C		70.5			70.5		dB
$f_{IN} = 180$ MHz	25°C		68.0			68.0		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
$f_{IN} = 2.4$ MHz	25°C		11.6			11.6		Bits
$f_{IN} = 70$ MHz	25°C		11.5			11.5		Bits
$f_{IN} = 100$ MHz	25°C		11.4			11.4		Bits
$f_{IN} = 180$ MHz	25°C		11.0			11.0		Bits
WORST SECOND OR THIRD HARMONIC								
$f_{IN} = 2.4$ MHz	25°C		88			88		dBc
	Full		82			82		dBc
$f_{IN} = 70$ MHz	25°C		85			85		dBc
	Full		82			82		dBc
$f_{IN} = 100$ MHz	25°C		83			83		dBc
$f_{IN} = 180$ MHz	25°C		80			80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
$f_{IN} = 2.4$ MHz	25°C		88			88		dBc
	Full		82			82		dBc
$f_{IN} = 70$ MHz	25°C		85			85		dBc
	Full		82			82		dBc
$f_{IN} = 100$ MHz	25°C		83			83		dBc
$f_{IN} = 180$ MHz	25°C		80			80		dBc
TWO TONE SFDR								
$f_{IN} = 70$ MHz, 71 MHz (-7 dBFS Each Tone)	25°C							dBFS
$f_{IN} = 70$ MHz, 71 MHz (-7 dBFS Each Tone)	Full							dBFS
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

DIGITAL SPECIFICATIONS

AVDD1 = 1.8V V, DRVDD = 3.3 V Unless otherwise noted

Table 3.

Parameter	Temp	AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	
CMOS LOGIC INPUTS (SPI CSB , SPI SDIO / DFS, SPI SCLK / DCS, CLKIN+, PWDN)								
High Level Input Voltage	Full	2.0			2.0			V
Low Level Input Voltage	Full			0.8			0.8	V
High Level Input Current	Full	-10		+10	-10		+10	μA
Low Level Input Current	Full	-10		+10	-10		+10	μA
Input Capacitance	Full		2			2		pF
DIFFERENTIAL CLOCK INPUTS								
Internal Common-Mode Bias	Full		1.2			1.2		V
Differential Input (CLKIN+ - CLKIN-)	Full	0.2		6	0.2		6	V _{p-p}
Input Voltage Range	Full	AVDD-0.3		AVDD+1.5	AVDD-0.3		AVDD+1.5	V
Input Common-Mode Range	Full	1.1V		AVDD	1.1V		AVDD	V
Input Capacitance	Full							pF
Input Resistance	Full	8	10	12	8	10	12	KΩ
DIGITAL OUTPUTS								
DRVDD = 3.3 V								
High Level Output Voltage (IOH = 50 μA)	Full	3.29			3.29			V
High Level Output Voltage (IOH = 0.5 mA)	Full	3.25			3.25			V
Low Level Output Voltage (IOH = 1.6 mA)	Full			0.2			0.2	V
Low Level Output Voltage (IOH = 50 μA)	Full			0.05			0.05	V
DRVDD = 1.8 V								
High Level Output Voltage (IOH = 50 μA)	Full	1.79			1.79			V
High Level Output Voltage (IOH = 0.5 mA)	Full	1.75			1.75			V
Low Level Output Voltage (IOH = 1.6 mA)	Full			0.2			0.2	V
Low Level Output Voltage (IOH = 50 μA)	Full			0.05			0.05	V

SWITCHING SPECIFICATIONS AVDD = 3 V, DRVDD = 2.5 V, UNLESS OTHERWISE NOTED.

Table 4.

Parameter	Temp	AD9246BCPZ-105			AD9246BCPZ-125			Unit
		Min	Typ	Max	Min	Typ	Max	
CLOCK INPUT PARAMETERS								
Maximum Conversion Rate	Full	105			125			MSPS
Minimum Conversion Rate	Full			10			10	MSPS
CLK Period	Full	9.5			8			ns
CLK Pulse Width High ¹	Full	TBD			TBD			ns
CLK Pulse Width Low ¹	Full	TBD			TBD			ns
DATA OUTPUT PARAMETERS								
Output Propagation Delay (t _{PD}) ²	Full		3.6		3.6			ns
Pipeline Delay (Latency)	Full		12		12			Cycles
Aperture Delay (t _A)	Full		TBD		TBD			ns
Aperture Uncertainty (Jitter, t _J)	Full		0.1		0.1			ps rms
Wake-Up Time ³	Full		TBD		TBD			ms
OUT-OF-RANGE RECOVERY TIME	Full		TBD		TBD			Cycles

¹ With duty cycle stabilizer (DCS) enabled.

² Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.

³ Wake-up time is dependant on the value of the decoupling capacitors, typical values shown with 0.1 μF and 10 μF capacitors on REFT and REFB.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Re- spect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND			V
DRVDD	DGND			V
AGND	DGND			V
AVDD	DRVDD			V
D0 to D13	DGND			V
CLK	AGND			V
VIN+, VIN-	AGND			V
VREF	AGND			V
SENSE	AGND			V
REFT, REFB	AGND			V
PDWN, SPI CSB, SPI SDIO, SPI SCLK	AGND			V
ENVIRONMENTAL				
Storage Temperature		-65	+125	°C
Operating Temperature Range		-40	+85	°C
Lead Temperature Range (Soldering 10 sec)			+300	°C
Junction Temperature			+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

θ_{JA} is specified for the worst-case conditions on a 4-layer board in still air, in accordance with EIA/JESD51-1.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-48	32.5	TBD	°C/W

Airflow increases heat dissipation effectively reducing θ_{JA} . Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA} . It is recommended that the exposed paddle be soldered to the ground plane for the LFCSP package. There is an increased reliability of the solder joints, and maximum thermal capability of the package is achieved with the exposed paddle soldered to the customer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TERMINOLOGY

Analog Bandwidth (Full Power Bandwidth)

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)

The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter, t_j)

The sample-to-sample variation in aperture delay.

Integral Nonlinearity (INL)

The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs $\frac{1}{2}$ LSB before the first code transition. Positive full scale is defined as a level $1\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16,384 codes must be present over all operating ranges.

Offset Error

The major carry transition should occur for an analog value $\frac{1}{2}$ LSB below $V_{IN+} = V_{IN-}$. Offset error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value $\frac{1}{2}$ LSB above negative full scale. The last transition should occur at an analog value $1\frac{1}{2}$ LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX} .

Power Supply Rejection Ratio

The change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Signal to Noise and Distortion (SINAD)^{Error! Bookmark not defined.}

The ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD by

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

Signal to Noise Ratio (SNR)^{Error! Bookmark not defined.}

The ratio of the rms input signal amplitude to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

Spurious-Free Dynamic Range (SFDR)^{Error! Bookmark not defined.}

The difference in dB between the rms input signal amplitude and the peak spurious signal. The peak spurious component may or may not be a harmonic.

Two Tone SFDR^{Error! Bookmark not defined.}

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Clock Pulse Width and Duty Cycle

Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Minimum Conversion Rate

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The clock rate at which parametric testing is performed.

Output Propagation Delay (t_{PD})

The delay between the clock rising edge and the time when all bits are within valid logic levels.

Out-of-Range Recovery Time

The time it takes for the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

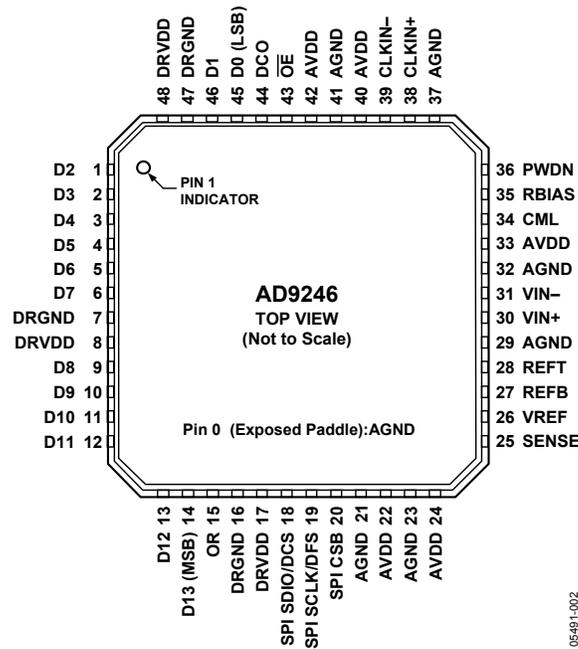


Figure 2. 48-Lead LFCSP

Note that the pin configuration is subject to change. Contact applications engineering for more information.

Table 7. Pin Function Description—48-Lead LFCSP

Pin No.	Mnemonic	Description
1 to 6, 9 to 14, 45, 46	D0 (LSB) to D13 (MSB)	Data Output Bits.
7, 16, 47	DRGND	Digital Output Ground.
8, 17, 48	DRVDD	Digital Output Driver Supply (1.8 V to 3.3 V).
15	OR	Out-of-Range Indicator.
18	SPI SDIO/DCS	Serial Port Interface Data Input/Output in Serial Port Mode; Duty Cycle Stabilizer Select Pin in External Pin Mode.
19	SPI SCLK/DFS	Serial Port Interface Clock in Serial Port Mode; Data Format Select Pin in External Pin Mode.
20	SPI CSB	Serial Port Interface Chip Select (Active Low).
0, 21, 23, 29, 32, 37, 41	AGND	Analog Ground. (Pin 0 is the exposed thermal pad on bottom of package.)
22, 24, 33, 40, 42	AVDD	Analog Power Supply (Nominally 1.8 V).
25	SENSE	Reference Mode Selection (See Table 9).
26	VREF	Voltage Reference Input/Output.
27	REFB	Differential Reference (-).
28	REFT	Differential Reference (+).
30	VIN+	Analog Input Pin (+).
31	VIN-	Analog Input Pin (-).
34	CML	Common-Mode Level Bias Output for Analog Inputs.
35	RBIAS	External Bias Resistor Connection. A TBD k Ω resistor should be connected between this pin and analog ground (GND).
36	PDWN	Power-Down Function Select.
38	CLKIN+	Clock Input—True.
39	CLKIN-	Clock Input—Complement.
43	OE	Output Enable (Active Low).
44	DCO	Data Clock Output.

THEORY OF OPERATION

The AD9246 architecture consists of a front-end sample and hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT AND REFERENCE OVERVIEW

The analog input to the AD9246 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. An on-board common-mode voltage reference is included in the design and is available from the CML pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the CML pin voltage ($\sim 0.55 \times AVDD$).

In Figure 3, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependant upon the application. In IF undersampling applications, any shunt capacitors should be reduced or removed. In combination with the driving source impedance, they would limit the input bandwidth.

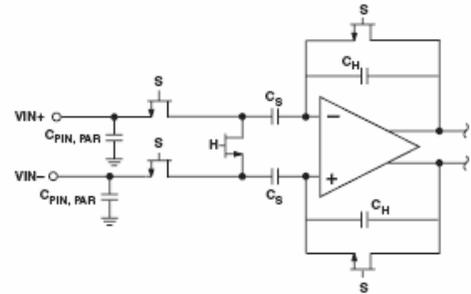


Figure 3. Switched-Capacitor SHA Input

For best dynamic performance, the source impedances driving VIN+ and VIN- should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, that define the span of the ADC core. The output common mode of the reference buffer is set to VCMREF ($\sim 1.6V$), and the REFT and REFB voltages and span are defined as:

$$REFT = VCMREF + \frac{1}{2} VREF$$

$$REFB = VCMREF - \frac{1}{2} VREF$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the VCMREF voltage and, by definition, the input span is twice the value of the VREF voltage.

Differential Input Configurations

Optimum performance is achieved while driving the AD9246 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

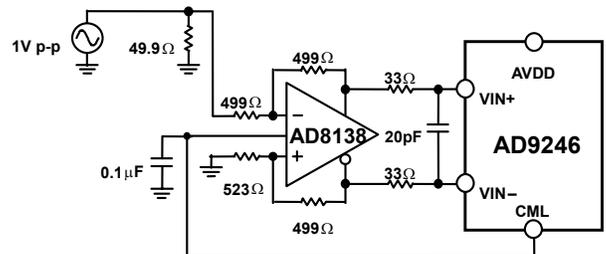


Figure 4. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9246. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The value of the shunt capacitor is dependent on the input frequency and source impedance and should be reduced or removed. The CML voltage is connected to the center tap of the transformer's secondary winding to bias the analog input. An example is shown in Figure 5.

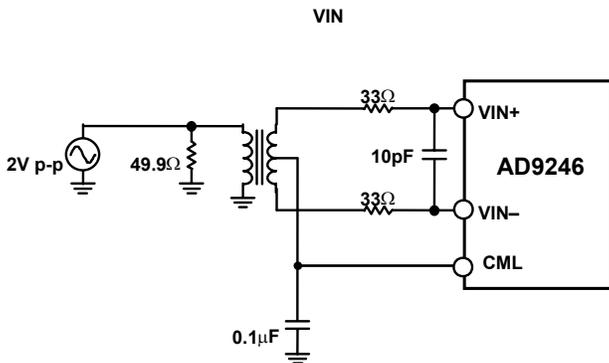


Figure 5. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9246 the sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. This signal is typically ac ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally and require no additional bias (See Figure X).

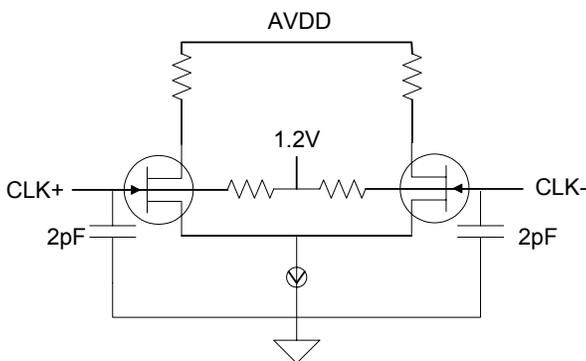


Figure. Equivalent Clock Input Circuit

Figure X shows one preferred method for clocking the AD9246. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky

diodes across the transformer secondary limit clock excursions into the AD9246 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9246 while preserving the fast rise and fall times of the signal, which are critical to a low jitter performance.

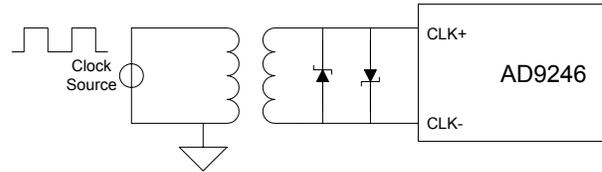


Figure X. Transformer Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure X. The AD9512 (or same family) from offers excellent jitter performance.

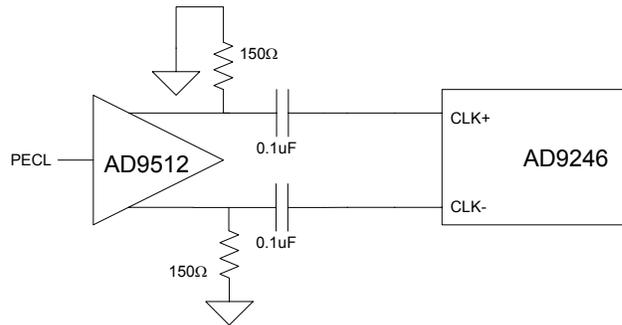


Figure X. Differential PECL Sample Clock

In some applications it may acceptable to drive the sample clock inputs with a single ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, while the CLK- pin should be bypassed to ground with a 0.1uF capacitor (see figure X). CLK+ may be directly driven from a CMOS gate. While the CLK+ input circuit supply is AVDD (1.8V), this input is designed to withstand input voltages up to 3.6V, making the selection of the drive logic voltage very flexible.

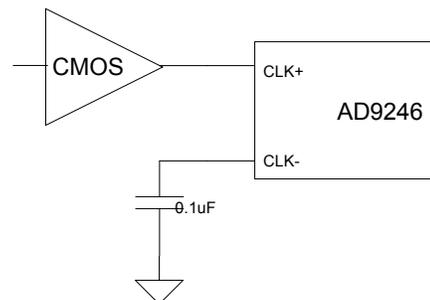


Figure X. Differential PECL Sample Clock

Clock Input Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9246 contains a DCS (duty cycle stabilizer) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9246. Noise and distortion performance are nearly flat for a wide range duty cycles with the DCS on. The DCS

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately TBD clock cycles to allow the DLL to acquire and lock to the new rate.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) due only to aperture jitter (t_j) can be calculated by

$$SNR = 20 \log \left[\frac{\pi}{2} f_{INPUT} \times t_j \right]$$

In the equation, the rms aperture jitter represents the root-mean square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. IF under-sampling applications are particularly sensitive to jitter, see Figure 6.

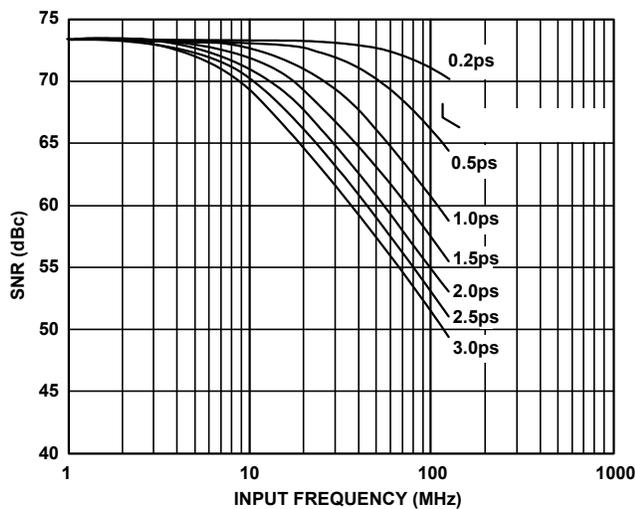


Figure 6. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the

AD9246. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 7, the power dissipated by the AD9246 is proportional to its sample rate. The digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current (I_{DRVDD}) can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits, 14 in the case of the AD9246. This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal. Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 7 was taken with the same operating conditions as the Typical Performance Characteristics and a 5 pF load on each output driver.

By asserting the PDWN pin high, the AD9246 is placed in standby mode. In this state, the ADC typically dissipates 1 mW if the CLK and analog inputs are static. During standby, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9246 into its normal operational mode.

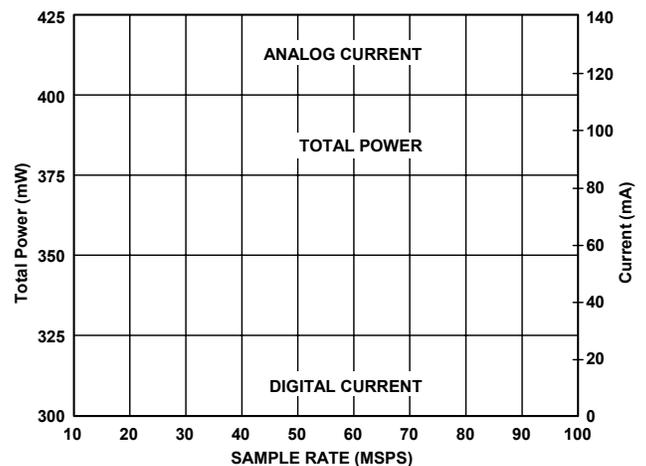


Figure 7. Power and Current vs. Sample Rate @ 2.5 MHz

Low power dissipation in standby mode is achieved by shutting down the reference, reference buffer, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode and shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 μ F and 10 μ F decoupling capacitors on REFT and REFB, it takes approximately 1 sec to fully discharge the reference buffer decoupling capacitors and 3 ms to restore full operation.

DIGITAL OUTPUTS

The AD9246 output drivers can be configured to interface with 1.8 V to 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

As detailed in *Interfacing to ADC SPI Error! Reference source not found.*, the data format can be selected for either offset binary or twos complement, or Gray code (SPI access only).

Out-of-Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OTR is a digital output

Table 8. Table III. Output Data Format

Input (V)	Condition (V)	Binary Output Mode	Twos Complement Mode	OTR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	1

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage	Internal Switch Position	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	N/A	2 \times External Reference
Internal Fixed Reference	VREF	SENSE	0.5	1.0
Programmable Reference	0.2 V to VREF	SENSE	$0.5 \times \left(1 + \frac{R2}{R1}\right)$ (See Figure 10)	2 \times VREF
Internal Fixed Reference	AGND to 0.2 V	Internal Divider	1.0	2.0

that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OTR has the same pipeline latency as the digital data. OTR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range as shown in Figure 8. OTR will remain high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OTR with the MSB and its complement, over-range high or underrange low conditions can be detected.

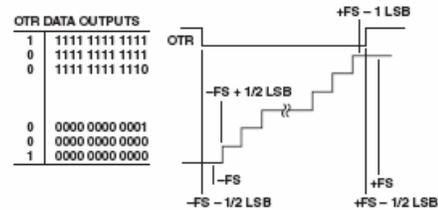


Figure 12. OTR Relation to Input Voltage and Output Data

Figure 8. OTR Relation to Input Voltage and Output Data

TIMING

The AD9246 provides latched data outputs with a pipeline delay of twelve clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9246. These transients can degrade the converter's dynamic performance. The AD9246 also provides data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO.

The lowest typical conversion rate of the AD9246 is 10 MSPS. At clock rates below 1 MSPS, dynamic performance can degrade.

Digital Output Enable Function (OEB)

The AD9246 has three-state ability. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. It is not intended for rapid access to the data bus. Note that OEB is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9246. The input range can be adjusted by varying the reference voltage applied to the AD9246, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in in the next few sections.

Internal Reference Connection

A comparator within the AD9246 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table X. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 9), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected as shown in Figure 10, the switch again sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$V_{REF} = 0.5 \times \left(1 + \frac{R2}{R1} \right)$$

The VREF pin should be externally decoupled to ground with a low ESR 1.0uF capacitor in parallel with a 0.1uF cap. In all reference configurations, REFT and REF B drive the A/D converter core and establish its input span. AN external 0.1uF capacitor should be placed across REFT / REF B to stabilize this reference. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

If the internal reference of the AD9246 is used to drive multiple converters to improve gain matching, the loading of the refer-

ence by the other converters must be considered. Figure 11 depicts how the internal reference voltage is affected by loading.

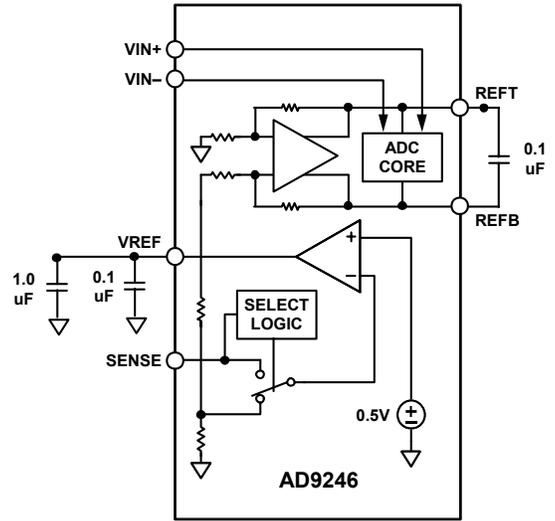


Figure 9. Internal Reference Configuration

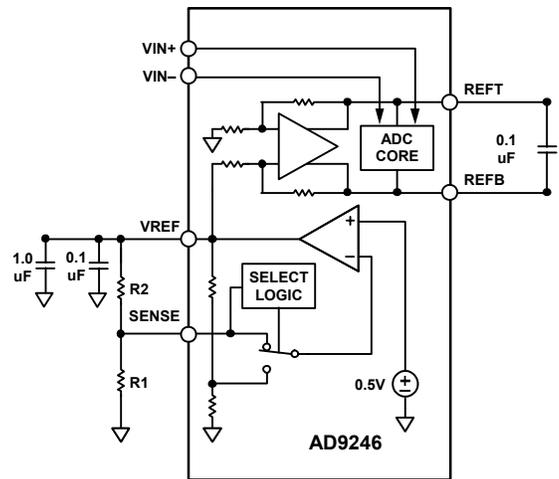


Figure 10. Programmable Reference Configuration

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. Figure 12 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent TBD kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REF B, for the ADC core. The input span is always twice the value of the reference

voltage; therefore, the external reference must be limited to a maximum of 1 V.

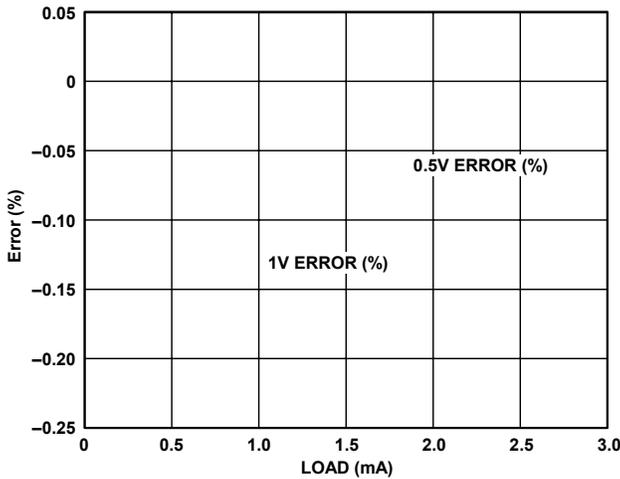


Figure 11. VREF Accuracy vs. Load

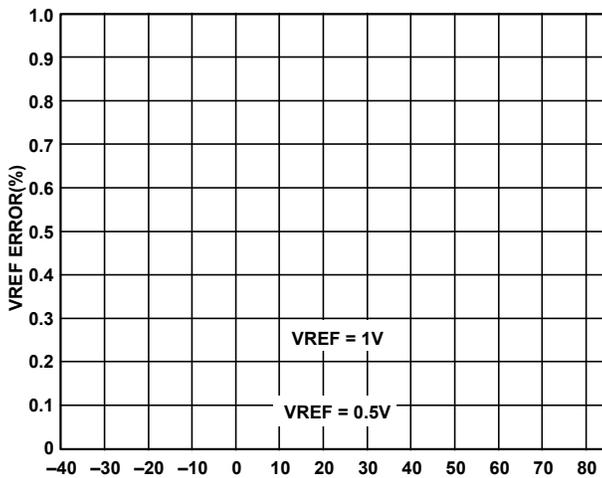


Figure 12. Typical VREF Drift

RBIAS

The AD9246 requires the user to place a 10KΩ resistor between the RBIAS pin and ground. This resistor should have a 1% tolerance, and is used to set the master current reference of the ADC core.

AD9246 CONFIGURATION USING THE SPI

The AD9246 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space inside the ADC. This gives the user added flexibility to customize device operation depending on the application. Addresses are accessed (programmed or read back) serially in one-byte words. Each byte may be further divided down into fields which are documented in the Memory Map Section below.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SPI SCLK / DFS, SPI SDIO / DCS, and CSB pins. The SCLK/DFS (serial clock) is used to synchronize the read and write data presented the ADC.. The SDIO / DCS (serial data input/output) is a dual purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB or chip select bar is an active low control that enables or disables the read and write cycles. See Table X.

Table X. Serial Port Pins

Pin	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is active low controls that gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing. An example of the serial timing and its definitions can be found in Figure X and Table X. Table X. SPI Timing Diagram specifications

Spec Name	Meaning
t _{DS}	Setup time between data and rising edge of SCLK
t _{DH}	Hold time between data and rising edge of SCLK
t _{CLK}	Period of the clock
t _S	Setup time between CSB and SCLK
t _H	Hold time between CSB and SCLK
t _{HI}	Minimum period that SCLK should be in a logic high state
t _{LO}	Minimum period that SCLK should be in a logic low state

During an instruction phase a 16bit instruction is transmitted. Data then follows the instruction phase and is determined by the W0 and W1 bits which is 1 or more bytes of data. All data is composed of 8bit words. The first bit of each individual byte of serial data indicates whether this is a read or write command. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

Data may be sent in MSB or in LSB first mode. MSB first is default on power up and may be changed by changing the configuration register. For more information about this feature and others see SPI Doc at www.analog.com.

HARDWARE INTERFACE

The pins described in Table X comprise the physical interface between the user’s programming device and the serial port of the AD9246. All serial pins are inputs, which is an open-drain output and should be tied to an external pull-up or pull-down resistor (suggested value 10 kΩ).

This interface is flexible enough to be controlled by either PROMS or PIC microcontrollers as well. This provides the user to use an alternate method to program the ADC other than a SPI controller.

If the user chooses to not use the SPI interface, some pins serve a dual function and are associated with a specific function when strapped externally to AVDD or ground during device power on. The section below describes the strappable functions supported on the AD9246. AD9246

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SPI SDIO / DCS and SPI SCLK / DFS pins can alternately serve as stand alone CMOS compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer. In this mode the SPI CSB chip select should be connected to ground, which will disable the serial port interface.

Table 10. Mode Selection

Pin	External Voltage	Configuration
SPI SDIO / DCS	AVDD	Duty Cycle Stabilizer Enabled
	AGND	Duty Cycle Stabilizer Disabled
SPI SCLK / DFS	AVDD	2’s Complement Enabled
	AGND	Offset Binary Enabled

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into four sections: chip

configuration register map (Address 0x00 to Address 0x02), device index and transfer register map (Address 0x04 to Address 0x05, and Address 0xFF), global ADC function register map (Address 0x08 to Address 0x09), and flexible ADC functions register map (Address 0x0B to Address 0x25). The flexible ADC functions register map is product specific.

Starting from the right hand column, the memory map register in Table X documents the default hex value for each hex address shown. The column with the heading Byte 7 (MSB) is the start of the default hex value giving. For example, hex address 0x14, flex_output_phase has a hex default value of 00h. This means Bit 3 = 0, Bit 2 = 0, Bit 1 = 1, and Bit 0 = 1 or 0011 in binary. This setting is the default output clock or DCO phase adjust option. The default value adjusts the DCO phase 90deg relative to the Nominal DCO edge and 180deg relative to the data edge. For more information on this function and others consult the SPI Doc at www.analog.com.

OPEN LOCATIONS

All locations marked as “open” are currently not supported for this particular device. When required, these locations should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x14). If the whole address location is open (for example, Address 0x13), then this address location does not need to be written.

DEFAULT VALUES

Coming out of reset, some of the address locations (but not all) are loaded with default values. The default values for the registers are given in the Table X.

LOGIC LEVELS

An explanation of various registers, “bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

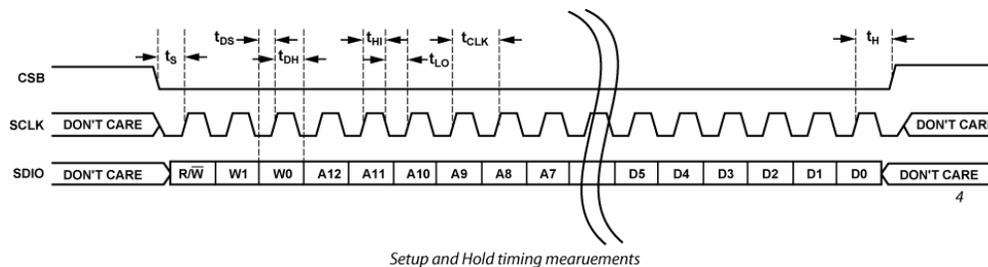


Figure X. Serial Port Interface Timing Diagram

Table X. AD9246 Device Configuration Register Memory Map

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Default Notes and comments
Chip Configuration Registers											
00	chip_port_config	OPEN	LSB First	Soft Reset	OPEN	OPEN	Soft Reset	LSB First	OPEN	18h	The nibbles should be mirrored by the user so that LSB or MSB first mode will register correctly regardless of shift mode.
01	chip_id	8-bit Chip ID bits 7:0 AD9246 – 00h								Read only	Unique chip ID
02	chip_grade	OPEN	Child ID 125MS -00h 105MS – 08h				OPEN			Read only	Read only. Child ID used to differentiate speed grades.
Device Index and Transfer Registers											
FF	device_update	OPEN							SW Transfer	00h	Synchronously transfers data from the master shift register to the slave
Global ADC Functions											
08	global_modes	OPEN	PWDN Function 0 – Full Power Down 1 - Standb y	OPEN	Internal Power Down Mode 0 – normal (power up) 1 – full power down 2 – standby 3 – normal (power up) Note: External PWDN pin overrides internal power down mode setting				00h	Determines various generic modes of chip operation.	
09	global_clock	OPEN							Duty Cycle Stabi- lizer 0- disabled 1- Enabled	01h	
Flexible ADC Functions											

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Default Notes and comments	
10				Digital Offset Adjust 10h<5:0> Offset in LSBs 011111 +31 011110 +30 011101 +29 . . . 000010 +2 000001 +1 000000 0 111111 1 111110 -2 111101 -3 . . . 100001 -31 100000 -32							00h	
0D	flex_test_io			PN23 0= normal 1=reset	PN9 0= normal 1=reset		Global Output Test Options 0 - off 1 - midscale short 2 - +FS short 3 - -FS short 4 - checker board output 5 - PN 23 sequence 6 - PN 9 7 - one/zero word toggle			00h	When set, the test data is placed on the output pins in place of normal data	
14	flex_output_mode	OPEN			Output Disable 1- Outputs disabled 0 - Outputs Enabled Note External OE/ pin over must be HIGH	OPEN	Output Data Invert 1=invert	Data Format Select 0 - offset binary 1 - 2's complement 3 - Gray 4 - offset binary		00h	Configures the outputs and the format of the data.	
16	flex_output_phase	Output Clock Polarity 1=inverted 0=Normal	OPEN							00h		
17	flex_output_drive	RESERVED 0	Output Driver Configuration 1000 for DrVDD =3.3V 1000 for DrVDD = V 1110 for DrVDD=1.8V				Reserved 000			70h		

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Default Notes and comments
18	flex_vref	Internal Reference Resistor Divider 00 – VREF=1.25V 01 – VREF=1.5V 10 – VREF=1.75V 11 – VREF=2.00V			Open					0Ch	

Power and Ground Recommendations

When connecting power to the AD9246, it is recommended that two separate supplies be used: one for analog (AVDD, 1.8V nominal) and one for digital (DRVDD, 1.8-3.3V nominal). If only a single 1.8V supply is available, then it should be routed to the AVDD first and tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors proceeding its connection to DrVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PC board ground plane should be sufficient when using the AD9246. With proper decoupling and smart partitioning of the PC board’s analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9228. A continuous exposed (no solder mask) copper plane on the PCB should mate to the AD9246 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible

resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the ADC and PCB. See Figure for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, go to www.analog.com.

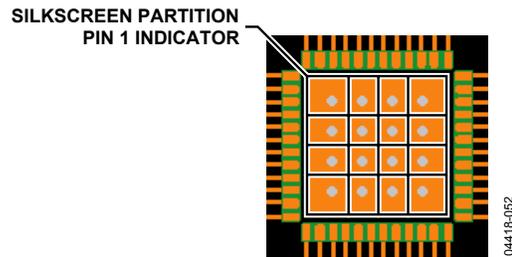
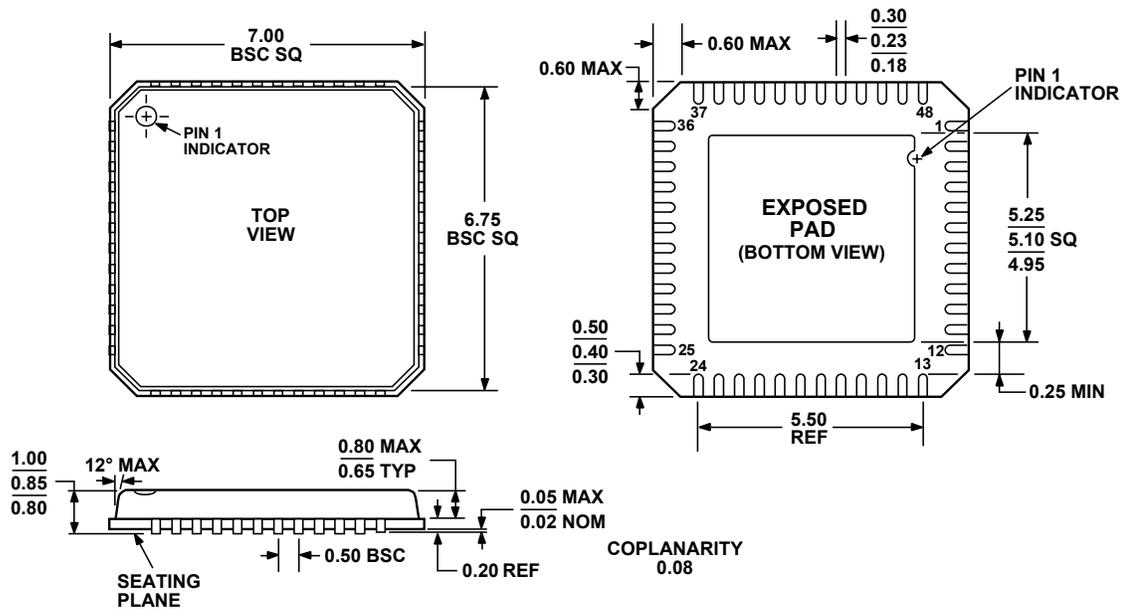


Figure 6. Typical PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

Figure 13. 48-Lead Frame Chip Scale Package [LFCSP_VQ]
 7 mm × 7 mm Body, Very Thin Quad (CP-48-1)
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline
AD9246BCPZ-125 ¹	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package	CP-48-1
AD9246BCPZRL7-125 ¹	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package	CP-48-1
AD9246BCPZ-105 ¹	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package	CP-48-1
AD9246BCPZRL7-105 ¹	-40°C to +85°C	48-Lead Lead Frame Chip Scale Package	CP-48-1
AD9246BCPZ-125EB ¹		Evaluation Board	

¹ It is recommended that the exposed paddle be soldered to the ground plane for the LFCSP package. There is an increased reliability of the solder joints, and the maximum thermal capability of the package is achieved with the exposed paddle soldered to the customer board.