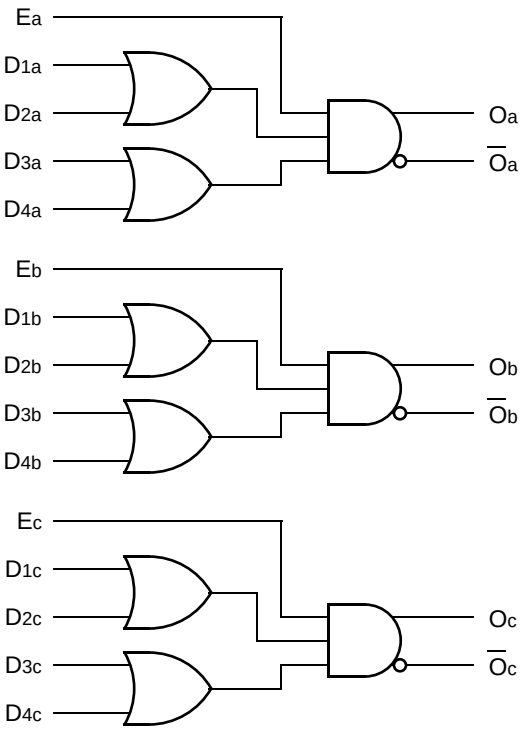
FEATURES

- **Max. propagation delay of 900ps**
- **I_{EE} min. of –48mA**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **Approximately 40% lower power than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

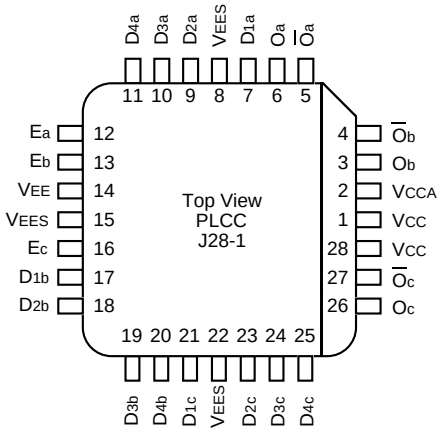
BLOCK DIAGRAM

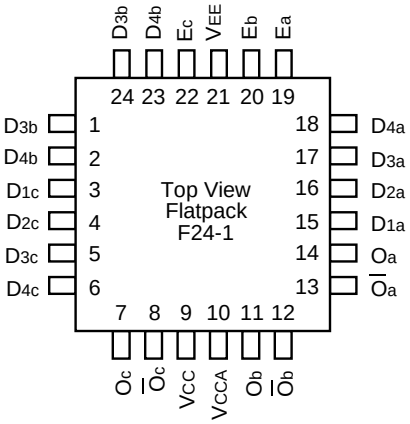


DESCRIPTION

The SY100S317 is a set of ultra-fast, triple 2-wide OR/AND gates designed for use in high-performance ECL systems. This device offers both true and complement outputs. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D_{na} – D_{nc}	Data Inputs (n = 1...4)
E_a – E_c	Enable Inputs
O_a – O_c	Data Outputs
$\overline{O}_a$ – $\overline{O}_c$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–48	–32	–22	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

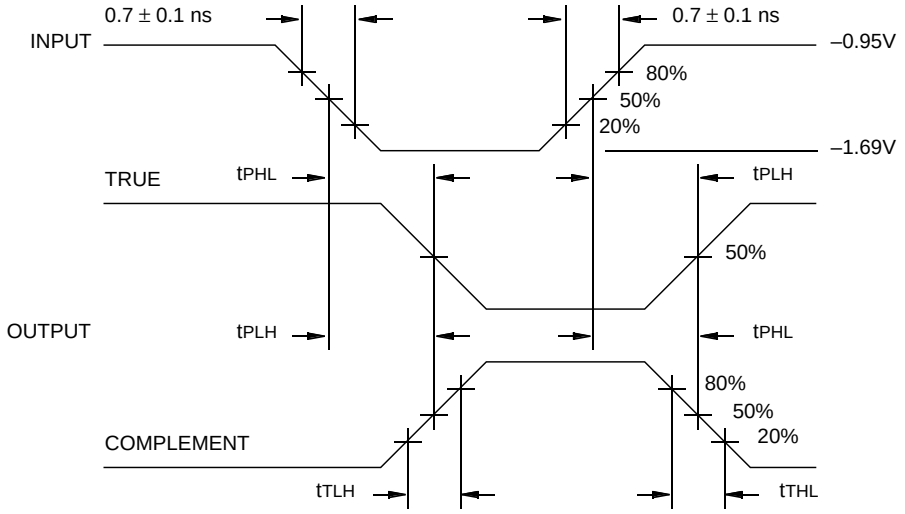
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	800	300	800	300	800	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	700	300	700	300	700	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



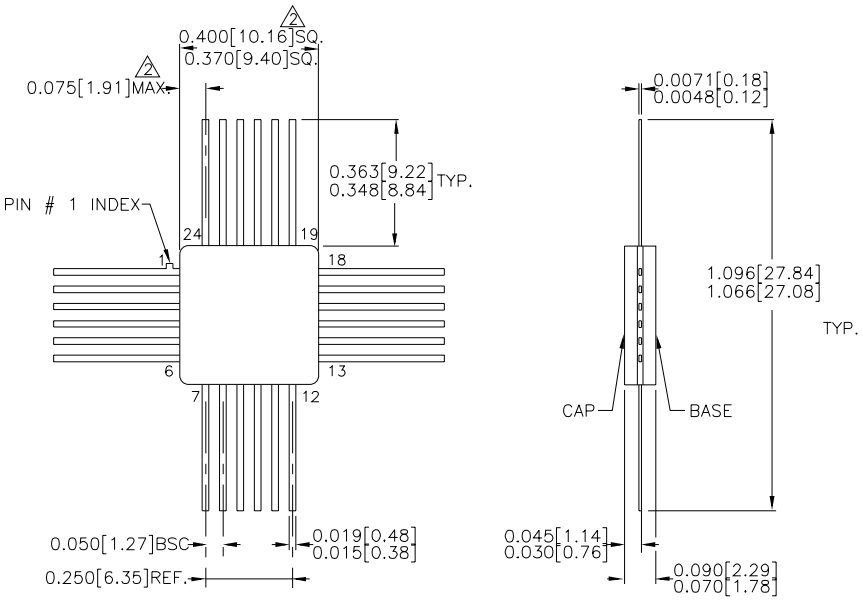
Propagation Delay and Transition Times

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S317FC	F24-1	Commercial
SY100S317JC	J28-1	Commercial
SY100S317JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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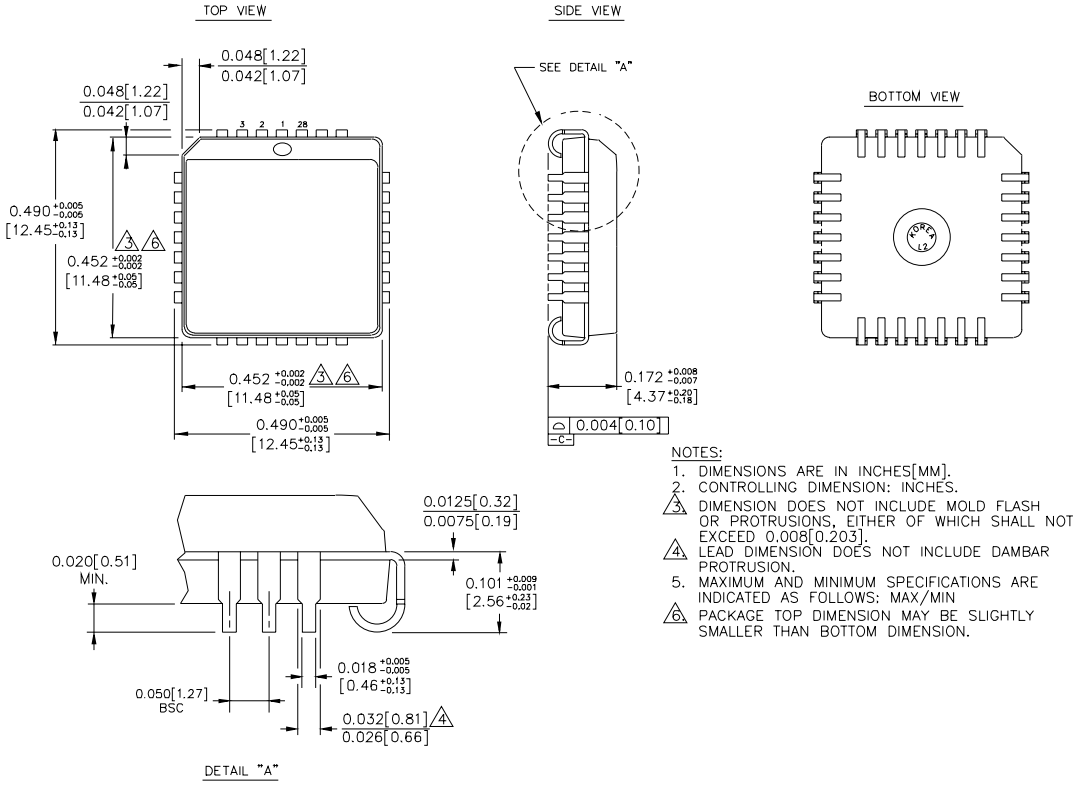
28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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