

SWITCHING REGULATOR APPLICATIONS

**Features**

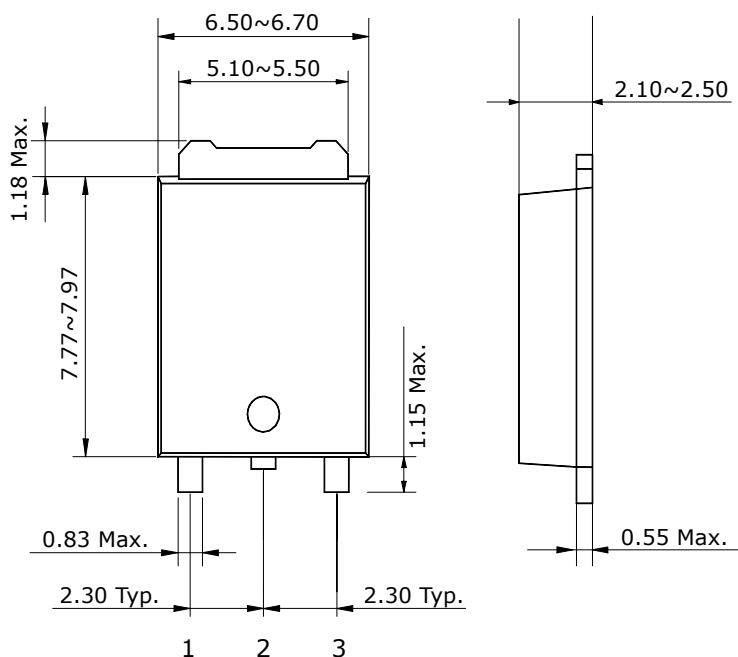
- High Voltage :  $BV_{DSS}=500V(\text{Min.})$
- Low  $C_{rSS}$  :  $C_{rSS}=6.5pF(\text{Typ.})$
- Low gate charge :  $Q_g=8.5nC(\text{Typ.})$
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=3.3\Omega(\text{Max.})$

**Ordering Information**

Type NO.	Marking	Package Code
STK0250D	STK0250	D-PAK

**Outline Dimensions**

unit : mm



**PIN Connections**

1. Gate
2. Drain
3. Source

## Absolute maximum ratings

(Tc=25°C)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	500	V	
Gate-source voltage	$V_{GSS}$	±30	V	
Drain current (DC)	$I_D$	(Tc=25°C)	2.0	A
		(Tc=125°C)	1.7	A
Drain current (Pulsed) *	$I_{DP}$	8.0	A	
Drain Power dissipation	$P_D$	35	W	
Avalanche current (Single) ②	$I_{AS}$	2.0	A	
Single pulsed avalanche energy ②	$E_{AS}$	59	mJ	
Avalanche current (Repetitive) ①	$I_{AR}$	2.0	A	
Repetitive avalanche energy ①	$E_{AR}$	3.0	mJ	
Junction temperature	$T_J$	150	°C	
Storage temperature range	$T_{stg}$	-55~150		

\* Limited by maximum junction temperature

Characteristic		Symbol	Typ.	Max	Unit
Thermal resistance	Junction-case	$R_{th(J-C)}$	-	3.57	°C/W
	Junction-ambient	$R_{th(J-a)}$	-	62.5	

## Electrical Characteristics

(Tc=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu A, V_{GS}=0$	500	-	-	V	
Gate-threshold voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=V_{GS}$	3.0	-	5.0	V	
Drain-source leakage current	$I_{DSS}$	$V_{DS}=500V, V_{GS}=0V$	-	-	1	$\mu A$	
Gate-source leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 30V$	-	-	$\pm 100$	nA	
Drain-Source on-resistance ④	$R_{DS(on)}$	$V_{GS}=10V, I_D=1.0A$	-	3.1	3.4	$\Omega$	
Forward transfer admittance ④	$g_{fs}$	$V_{DS}=10V, I_D=1.0A$	-	1.4	-	S	
Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V, f=1MHz$	-	268	402	pF	
Output capacitance	$C_{oss}$		-	13	19.5		
Reverse transfer capacitance	$C_{rss}$		-	6.5	9.8		
Turn-on delay time	$t_{d(on)}$	$V_{DD}=250V, V_{GS}=10V$ $I_D=2.0A, R_G=25\Omega$	-	8.5	-	ns	
Rise time	$t_r$		-	10.2	-		
Turn-off delay time	$t_{d(off)}$		③④	-	19		-
Fall time	$t_f$		-	10.2	-		
Total gate charge	$Q_g$	$V_{DD}=250V, V_{GS}=10V$ $I_D=2.0A$	-	8.5	12.8	nC	
Gate-source charge	$Q_{gs}$		-	1.7	2.6		
Gate-drain charge	$Q_{gd}$		③④	-	3.0		4.5

## Source-Drain Diode Ratings and Characteristics

(Tc=25°C)

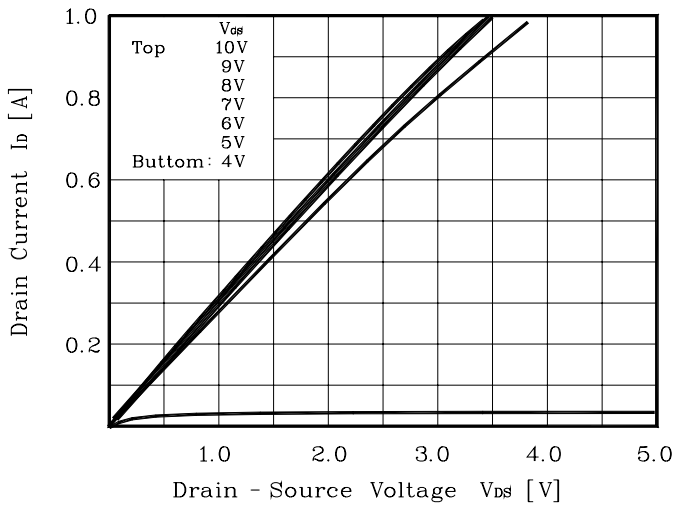
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Continuous source current	$I_S$	Integral reverse diode in the MOSFET	-	-	2	A
Source current (Pulsed) ①	$I_{SP}$		-	-	8	
Forward voltage ④	$V_{SD}$	$V_{GS}=0V, I_S=2.0A$	-	-	1.4	V
Reverse recovery time	$t_{rr}$	$I_S=2.0A, V_{GS}=0V$ $di_s/dt=100A/us$	-	200	-	ns
Reverse recovery charge	$Q_{rr}$		-	0.7	-	$\mu C$

Note ;

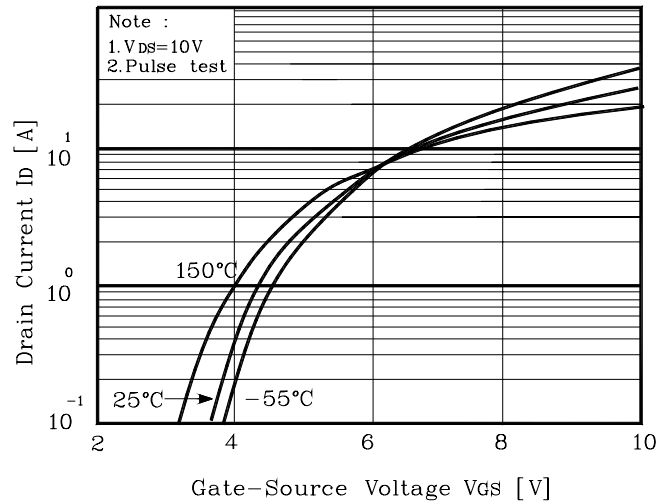
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=26.5mH, I_{AS}=2.0A, V_{DD}=50V, R_G=25\Omega$
- ③ Pulse Test : Pulse Width < 300us, Duty cycle  $\leq 2\%$
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

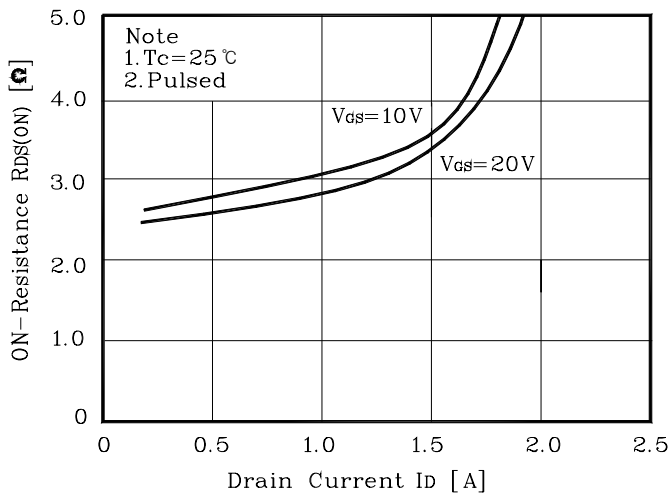
**Fig. 1  $I_D - V_{DS}$**



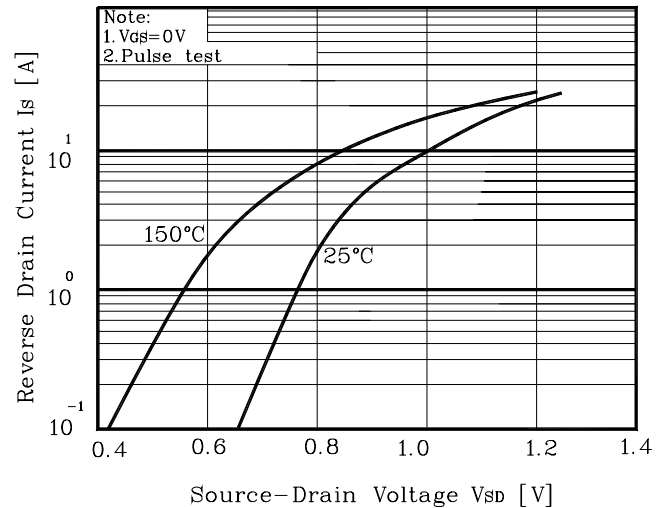
**Fig. 2  $I_D - V_{GS}$**



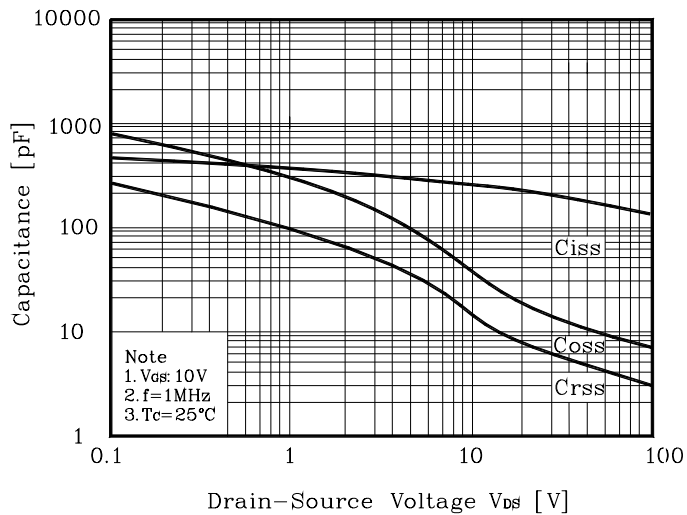
**Fig. 3  $R_{DS(on)} - I_D$**



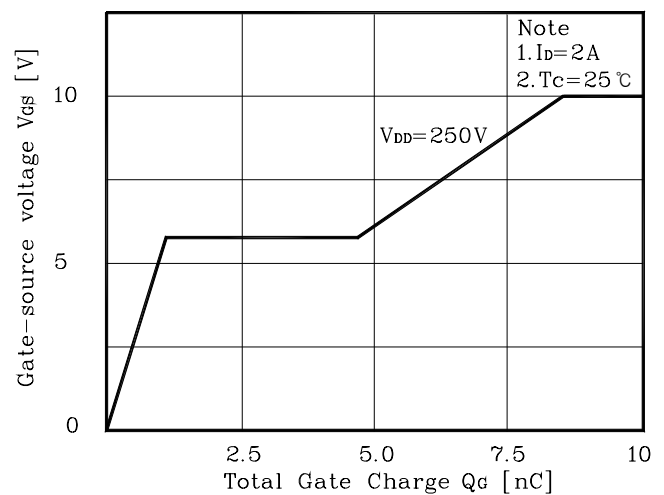
**Fig. 4  $I_S - V_{SD}$**



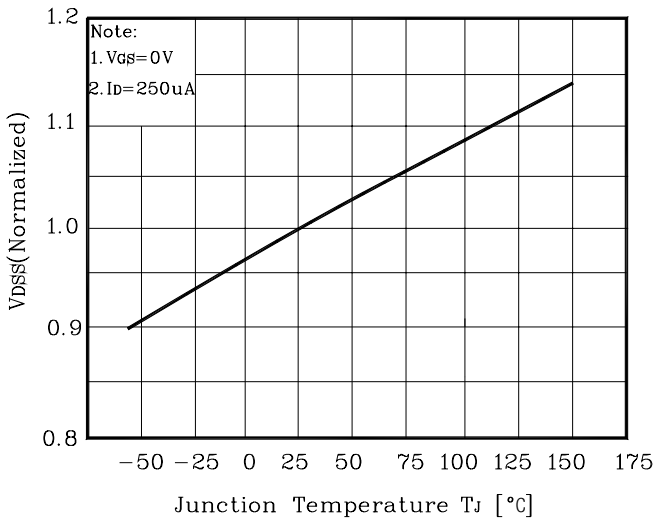
**Fig. 5 Capacitance -  $V_{DS}$**



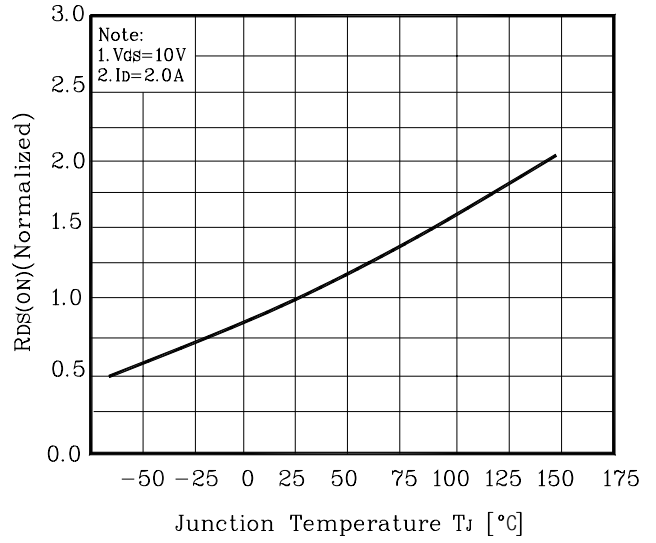
**Fig. 6  $V_{GS} - Q_G$**



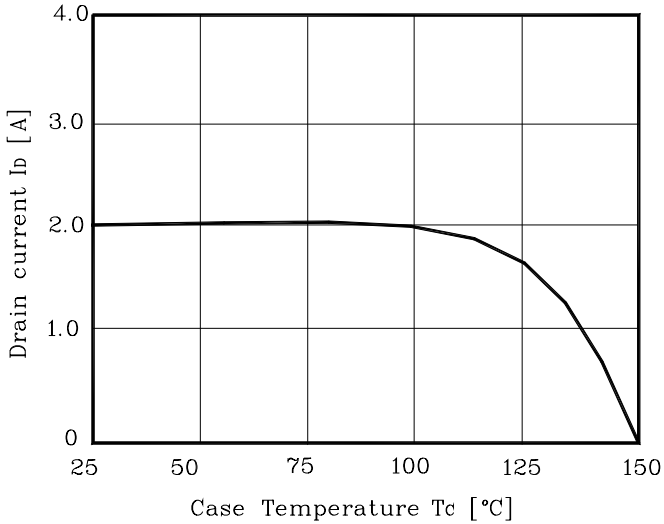
**Fig. 7  $V_{DSS} - T_J$**



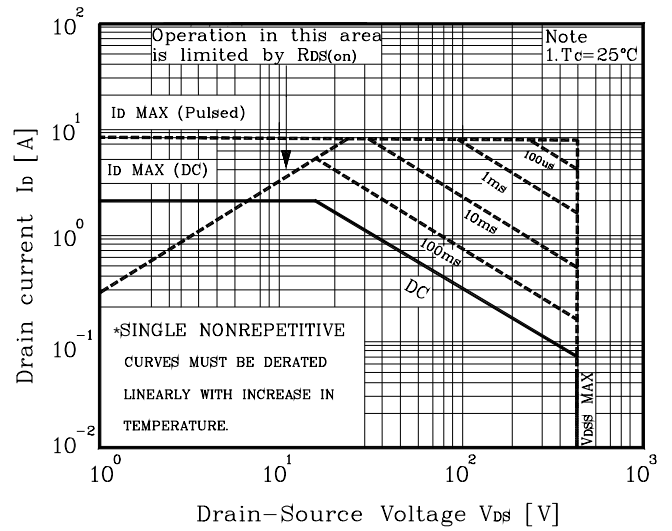
**Fig. 8  $R_{DS(on)} - T_J$**



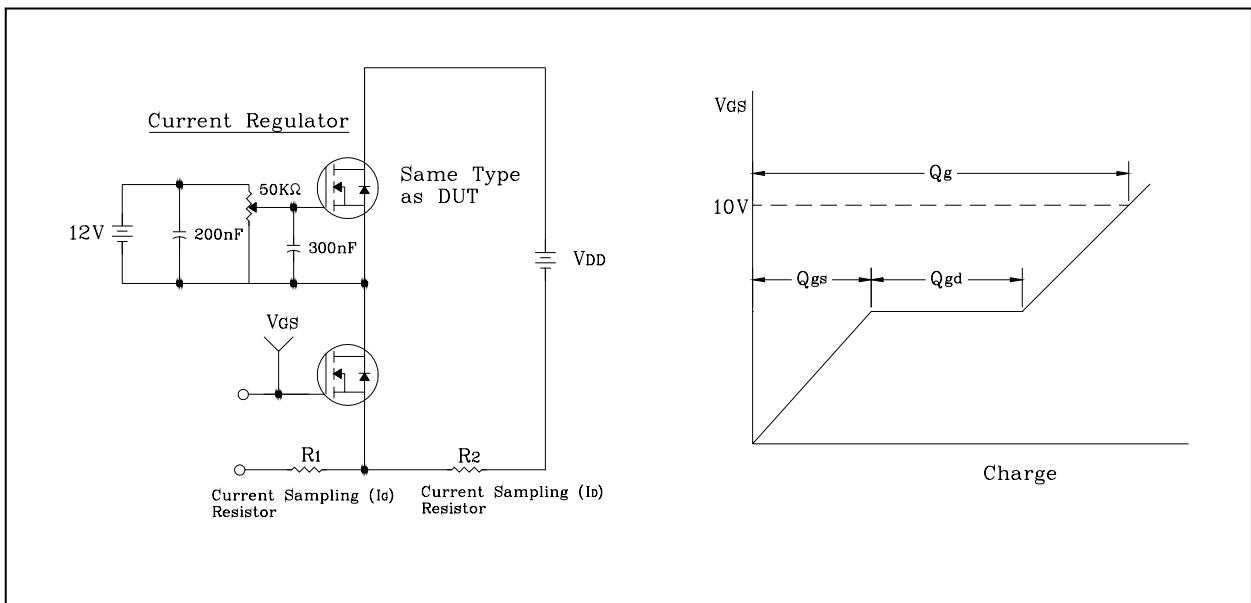
**Fig. 9  $I_D - T_C$**



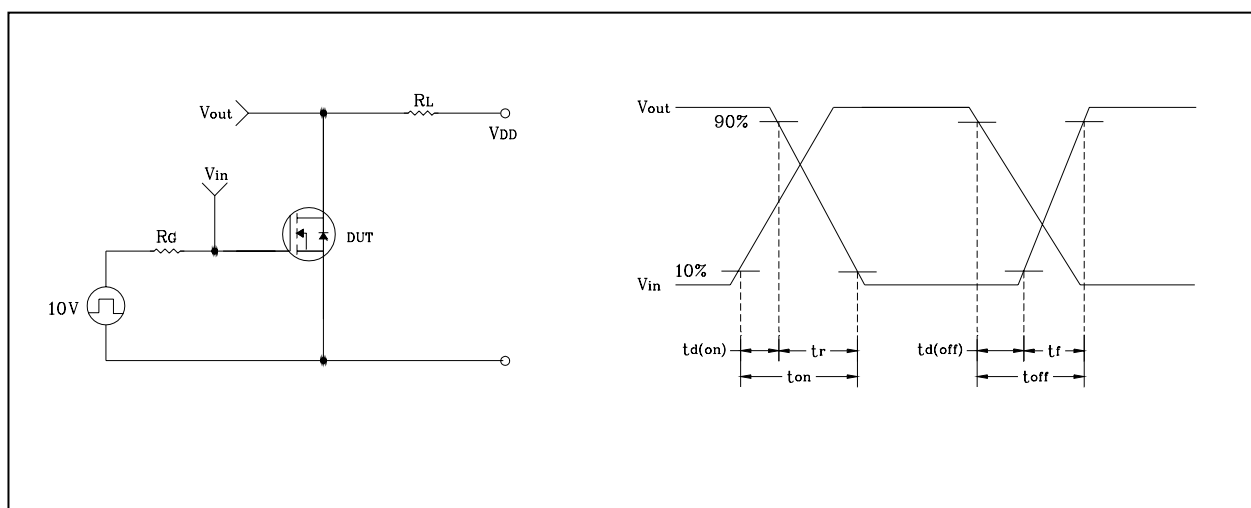
**Fig. 10 Safe Operating Area**



**Fig. 11 Gate Charge Test Circuit & Waveform**



**Fig. 12 Resistive Switching Test Circuit & Waveform**



**Fig. 13 EAS Test Circuit & Waveform**

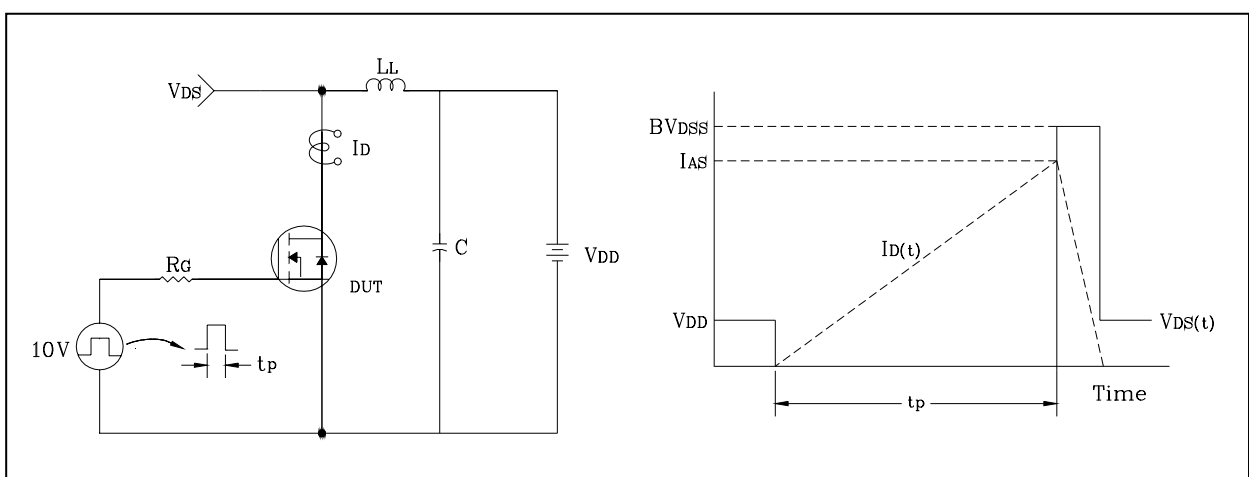
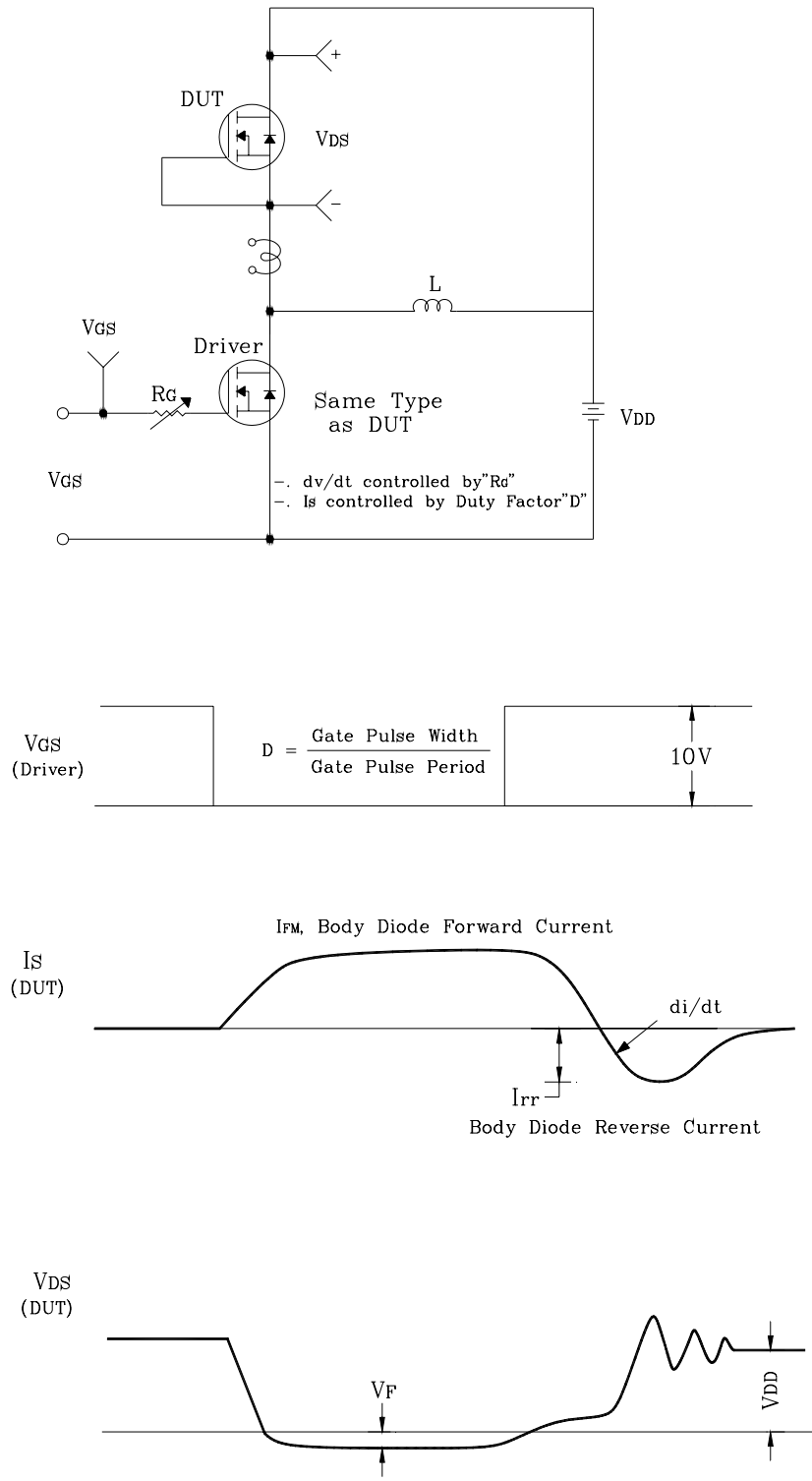


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



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