SIEMENS

12-Bit A/D Converter with 4-Channel Multiplexer

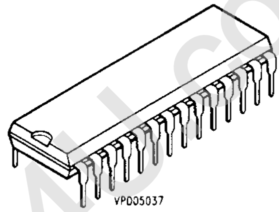
SDA 0812 A
SDA 1812 D

Preliminary Data

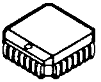
CMOS

Features

- 12-bit resolution
- Autocalibration circuitry
- No offset or gain adjustments required
- Total unadjusted error ± 1/2 LSB max. (SDA 0812 A) respectively ± 3/4 LSB max. (SDA 1812 D)
- Fast conversion time (6 µs)
- SDA 1812 D with over 100 kHz sampling rate
- No missing codes
- *S/N* + *THD* together 71 dB typ
- Single 5 V supply
- 4-channel multiplexer with latched control logic
- Easy interfacing to 8- and 16-bit microprocessors
- Data output in a 2-byte format
- 0 V to 5 V analog input voltage range
- Digital inputs and outputs are TTL compatible
- Standby mode (50 µW typ)
- CMOS low power consumption (10 mW typ)
- Temperature range – 40 to 85 °C



P-DIP-28



P-LCC-28-2

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Type	Ordering Code	Package
S SDA 0812 A	Q67100-A8233	P-DIP-28
SDA 0812 AN	Q67100-H8300	P-LCC-28-2 (SMD)
S SDA 1812 D	Q67100-H8291	P-DIP-28
SDA 1812 DN	Q67100-H8301	P-LCC-28-2 (SMD)

General Description

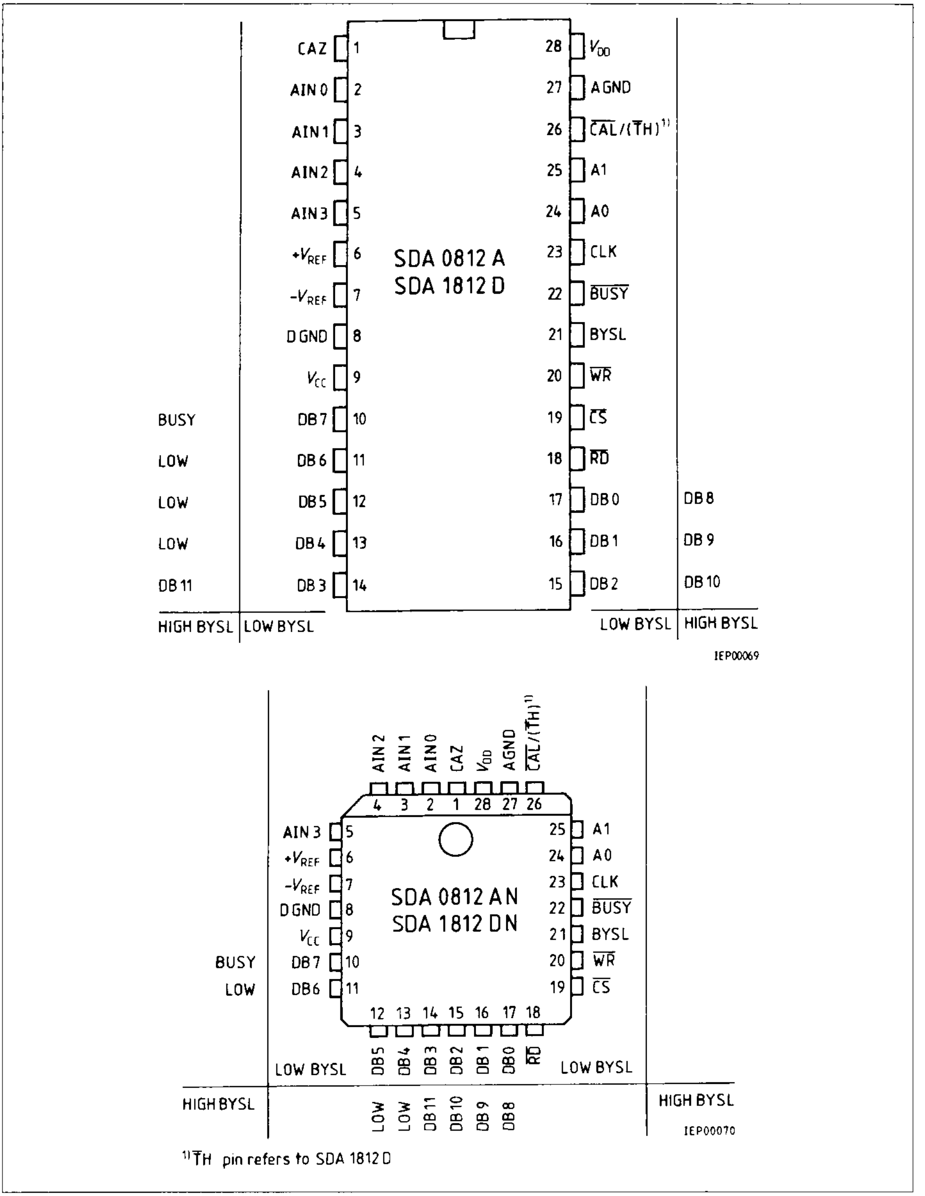
SDA 0812 A and SDA 1812 D are monolithic CMOS 12-bit analog to digital converters with a 4-channel analog multiplexer. They need only a 5 V supply and achieve a conversion time of 6 μs plus 2.5 μs sample time.

They use the method of successive approximation based on a capacitor network. **An autocalibration circuit guarantees a total unadjusted error within ± 1/2 LSB max. (SDA 0812 A) respectively ± 1/2 LSB typ. (SDA 1812 D).** Therefore the device needs no external offset or gain adjustments. The converters feature a temperature stabilized differential comparator, a sample and hold function and a 12-bit data output in a 2-byte format. Designed for easy microprocessor interface using the standard control signals $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ the 4-channel input multiplexer is controlled via address inputs A0 and A1.

Two converter busy flags are available to facilitate polling of the converter's status.

With a sample and hold circuit on chip, the SDA 1812 D is suited for digitizing AC signals as well as DC signals. The maximum sampling rate of the SDA 1812 D is more than 100 kHz according to 2.5 μs sample time plus 6 μs conversion time. The SDA 1812 D is specified with traditional static specifications as well as with dynamic specifications (SNR, THD, effective number of bits).

The temperature range of the SDA 0812 A/1812 D is – 40 °C to 85 °C.



Pin Configurations
(top view)

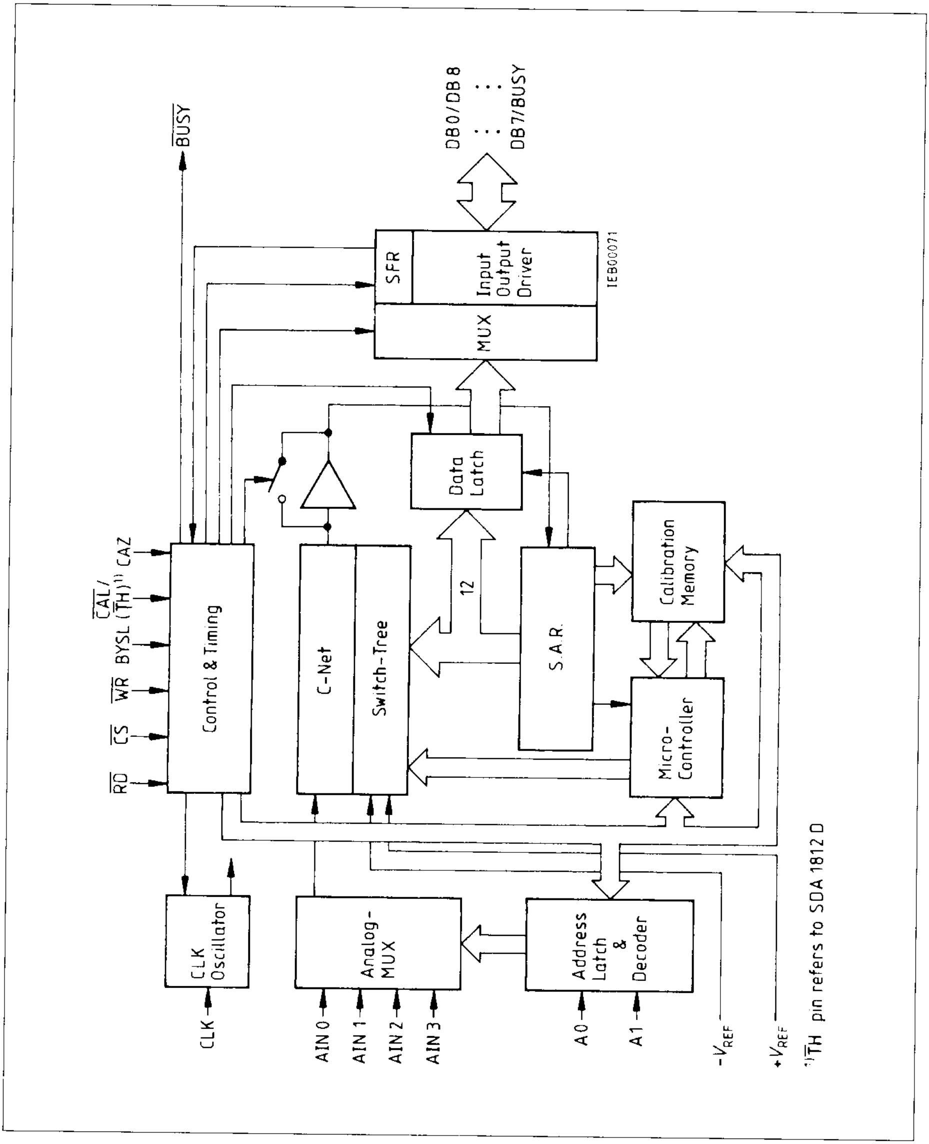
Pin Definitions and Functions

Pin	Symbol	Function
1	CAZ	Special function pin (see Reading the Conversion Results, SFR and Internal Clock Operation). Connect to a MP address pin. If not used, CAZ can be connected to AGND or DGND or can be unconnected.
2-5	AIN 0 to AIN 3	**Analog Input,** channel 0 to channel 3
6	+ V_{REF}	Pos. voltage reference input, + V_{REF} = 5 V
7	– V_{REF}	Neg. voltage reference input, – V_{REF} = 0 V
8	DGND	**Digital Ground,** DGND = 0 V
9	V_{CC}	Logic supply voltage, V_{CC} = 5 V must not be applied before V_{DD}!
10-17	DB7-DB0	Three-state data outputs. **Data Bus** output (CS, RD = LOW)
	Symbol (BYSL = HIGH)	Symbol (BYSL = LOW)
10	BUSY	DB7 BUSY is an active high converter status flag. It is high
11	LOW	DB6 during a conversion and during autocalibration.
12	LOW	DB5 LOW Pin 11 to pin 13 are tied to DGND when
13	LOW	DB4 BYSL = HIGH
14	DB11 (MSB)	DB3 DB11 is the MSB.
15	DB10	DB2
16	DB9	DB1
17	DB8	DB0 (LSB) DB0 is the LSB.
18	RD	Read input, active low, is used to read the data outputs in combination with CS and BYSL.
19	CS	**Chip Select** input, active low.
20	WR	**Write** input, active low, is used to start a new conversion and to select an analog channel via address inputs A0, A1 in combination with CS low. The minimum WR pulse width is 100 ns. It is independent of internal/external clock operation.
21	BYSL	**Byte Select** input, is used to select high or low data output byte in combination with CS and RD, or to select SFR.

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Function</th></tr>
<tr><td>22</td><td>$\overline{\text{BUSY}}$</td><td>Converter status output. $\overline{\text{BUSY}}$ is low during conversion or autocalibration. $\overline{\text{BUSY}}$ is high after the converter has finished its operation.</td></tr>
<tr><td>23</td><td>CLK</td><td>Clock input for internal/external clock operation. For external clock operation connect pin 23 to a 74HC compatible clock source. For internal clock operation connect pin 23 to a R timing component (see Clock Operation description).</td></tr>
<tr><td>24-25</td><td>A0 to A1</td><td>Address inputs, are used to select one of four analog input channels, in combination with $\overline{\text{CS}}$ and $\overline{\text{WR}}$. The address inputs are latched with the rising edge of $\overline{\text{WR}}$.
<table>
<tr><th>A1</th><th>A0</th><th>Selected Channel</th></tr>
<tr><td>LOW</td><td>LOW</td><td>AIN0</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>AIN1</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>AIN2</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>AIN3</td></tr>
</table></td></tr>
<tr><td>26</td><td>$\overline{\text{CAL}}/\overline{\text{TH}}$[1)]</td><td>Calibration input. An autocalibration cycle is initiated with $\overline{\text{CAL}}$ = LOW. If not used, CAL can be connected to V_{CC} or unconnected. In this case autocalibration is only initiated by power-up/power-fail, or by SFR. The minimum pulse width of CAL is 100 ns. Using the SDA 1812 D, via SFR the function of pin 26 can be defined as an external Track-Hold ($\overline{\text{T}}$H) pin (see SFR description).</td></tr>
<tr><td>27</td><td>AGND</td><td>Analog Ground, AGND = 0 V</td></tr>
<tr><td>28</td><td>V_{DD}</td><td>Analog supply, V_{DD} = 5 V, must not be applied after V_{CC}!</td></tr>
</table>

1) TH-pin refers to SDA 1812 D



Block Diagram

Functional Description

SDA 0812 A and 1812 D are 4-channel 12-bit A/D converters. The successive approximation technique provides 6 µs conversion time. The required sampling time of the on-chip sample-and-hold-circuit is 2.5 µs. An autocalibration technique guarantees a total unadjusted error within ± 1/2 LSB max. (SDA 0812 A) and ± 3/4 LSB max. (SDA 1812 D) over the entire temperature range. The major components are shown in the **block diagram.**

The comparator is a fully differential autozeroed one for a high power supply rejection ratio and very low offset voltages. The charge redistribution design using a binary weighted capacitor network inherents the sampling function to convert AC-signals (SDA 1812 D). A Sub-C Network is used to correct linearity-errors in the Main-Capacitor Network. The correction terms are calculated by a microcontroller in an autocalibration cycle, started by power-up or CAL signal. The correction terms are stored in a calibration memory. The stability of integrated C-Networks guarantees the correction terms to be valid over time and temperature. In the case of a power up/power fail (V_{CC} less then 3 V typical) new calibration cycles will be initiated automatically. This guarantees the integrity of the correction terms.

Three-state output drivers with multiplexer for 2-byte data format, an analog multiplexer with address latch and a clock oscillator with external or internal clock operation complete the functional components of the device.

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A/D Converter Timing

SDA 0812 A

After a conversion has been started with the rising edge of WR the analog input voltage is sampled for 5 clock cycles. The analog source must be capable to charge the capacitor network of appr. 50 pF to full accuracy in this time. In parallel an offset compensation mechanism reduces the comparators offset error below 1/4 LSB. During this period the converter is susceptable to spikes and noise at the analog input, which may cause erroneous codes at the digital outputs. Therefore RC-filtering at the analog inputs is recommended.

Conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle. The CAZ pin is not used for normal operation. However CAZ serves as an additional programming pin. (See Special Function Register).

SDA 1812 D

After a conversion has been started with the rising edge of WR the analog input voltage is sampled for 5 clock cycles. The analog source must be capable to charge the capacitor network of appr. 50 pF to full accuracy in this time.

By starting a conversion with WR sampling of the analog signal is defined by the first rising edge of the internal CLK pulse + 4.5 clock cycles + 100 ns (typ) after the rising edge of WR. For precisely defined sampling point WR has to be synchronized with CLK. The conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle.

To avoid synchronizing problems between WR and CLK the CAL pin is programmable into an external Track-Hold pin (TH) via SFR. A low to high transition at this pin defines the sampling point of the ADC with a delay time of 5 ns typ. without synchronizing to CLK. The low pulse width of TH defines the tracking period of internal sample and hold circuit and should be 2.5 µs min. Using this TH pin an additional offset error of ± 1 LSB may occure. This TH pin should be used in combination with on chip clock generator. Using external clock generator in combination with asynchronous TH function brings offset errors up to ± 4 LSB via pin coupling effects. By synchronizing the TH signal with external CLK this offset error can be reduced again to ± 1 LSB. The best conditions are given by delaying the falling clock slope 20 ns to the rising edge of TH.

The SDA 1812 D operates with the master clock. The conversion cycle may not begin until up to 1.5 clock cycles after TH goes high.

The CAZ pin is not used for normal operation. However CAZ serves as an additional programming pin (see Special Function Register).

Autocalibration

An autocalibration cycle is started

- with the rising edge of a CAL low pulse
- by setting the DB1 in the Special Function Register (SFR)
- by power-up/power-fail

and takes 168 clock cycles. Finally a normal conversion (17 clock cycles) is added automatically. During an autocalibration or conversion cycle each power supply voltage and each reference voltage has to be stable. Therefore an internal timer provides a waiting period of 42 240 clock cycles between power up/power fail and autocalibration function. Power up calibration is finished after 42425 (42240 + 168 + 17) clock cycles.

Reading the Conversion Results

Normal Mode (Transparent)

The data is read as two 8-bit bytes. The converters digital outputs are positive true. Data is presented in right justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the BYSL input determines which byte is to be read. Because the conversion results are held in a successive approximation register the high byte may be read out before the conversion is finished.

The 4 most significant bits are valid in the 10^{th} clock cycle after starting a conversion with WR. Valid 12-bit data are available for reading after the BUSY pin has gone high, or internal status flag BUSY (available on pin 10) has gone low.

Latched Output Mode

An additional function is reading the data is available via an integrated data latch, which is transparent in normal function mode.

The latched output function may be activated by writing high on DB0 and low on DB7 (see Special Function Register SFR) with WR, CS active in combination with CAZ and BYSL pin high.

The data latch is set transparent by power-up.

When the latch function is active an internal generated latch enable signal shifts the data from the SAR into a 12-bit latch. This occures when BUSY gets inactive (high). The conversion result is valid during the next conversion cycle until new data is latched. Therefore it may be read out even after starting a new conversion.

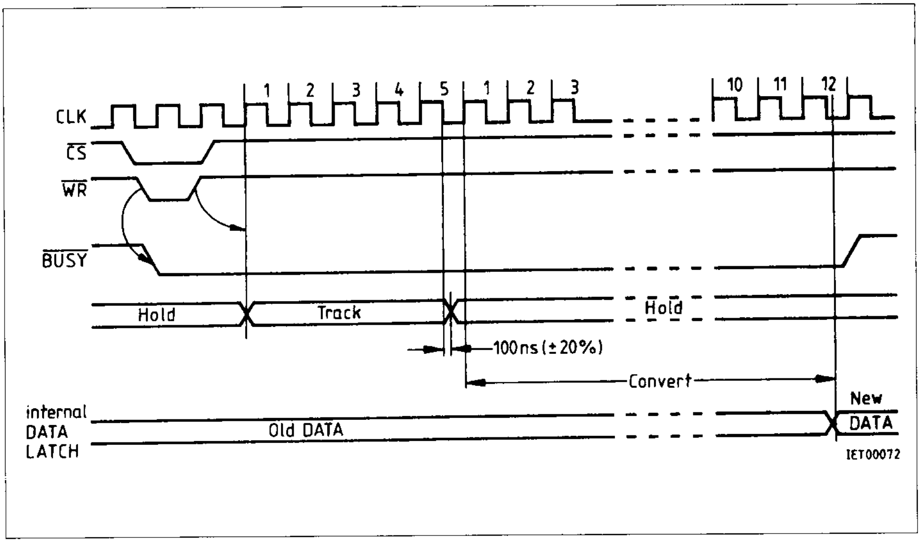


Figure 1
Starting a Conversion with WR

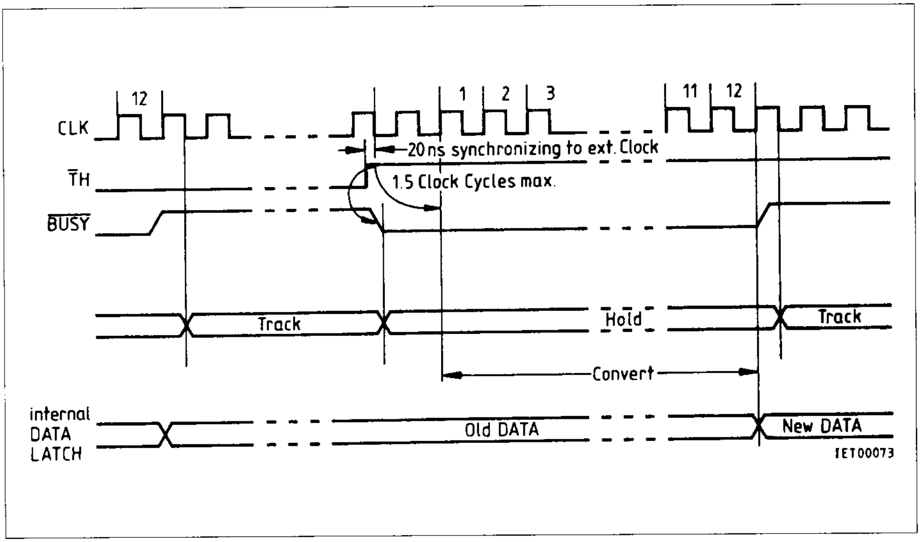


Figure 2
Starting a Conversion with TH (SDA 1812 D)
may be synchronous with internal clock generator and should be synchronized with external clock for best performance.

The Special Function Register (SFR)

An internal register for additional functions programmed by the microprocessor is available.

Special Functions

SDA 0812 A

- 12-bit data latch is enabled by setting SFR DB0 high.
- INT-CAL starts a calibration by setting SFR DB1 high, the timing of this calibration refers to EXT-CAL function (168 + 17 clock cycles).
- The converter is set to a standby mode by programming DB3 high. In this mode the analog circuit and the internal CLK-generator are deactivated, total power consumption reduced to 50 µW typ. Wake up the converter by writing low to DB3, ext. CAL, INT-CAL (DB1) or power-up function (V_{CC} < 3 V). Applying CS and WR (start of conversion) during standby mode (DB3 high) delivers one correct conversion result, subsequently the converter goes back to standby mode until new conversion start or wake-up signal.
- POWER FAIL FLAG is set if a power fail occured, showing that a new calibration was started (BUSY active) and that the data of SFR (data latch enable) are lost. To reset this flag write low to DB5.
- CAL-ERROR flag is set on DB6 if a calibration overflow occurs (may be in very noisy systems). It is reset by starting a calibration and remains low after a properly finished calibration.
- BUSY flag is high (DB7) if a calibration or a conversion is in process.

SDA 1812 D

- 12-bit data latch is enabled by setting SFR DB0 high.
- INT-CAL starts a calibration by setting SFR DB1 high, the timing of this calibration refers to EXT-CAL function (168 + 17 clock cycles).
- The CAL pin function is modified to an ext. Track-Hold (TH) function by setting DB2 high. Reset the function to CAL by writing low into DB2. The ext. Track-Hold pin (TH) guarantees sampling points precisely defined by the rising edge of TH signal. The internal sampling point is delayed 5 ns typ. to the external TH slope.
- The SDA 1812 D is set to a standby mode by programming DB3 high. In this mode the analog circuit and the internal CLK-generator are deactivated, total power consumption reduces to 50 µW typ. Wake up the SDA 1812 with writing low to DB3, EXT-CAL, INT-CAL (DB1) or power-up function (V_{CC} > 3 V). Applying WR and CS or a rising edge on TH pin (Conversion Start) during standby mode (DB3 high) delivers one correct conversion result, subsequently the SDA 1812 D goes back to standby mode until new SOC or WAKE UP signal.
- POWER FAIL FLAG is set if power fail occured (DB5), showing that a new calibration has been started (BUSY active) and that the data of SFR (data latch enable CAL/TH pin programming) are lost. To reset this flag write low to DB5.
- CAL-ERROR flag is set on DB6 if a calibration overflow occures (may be in very noisy systems), is reset by starting a calibration and remains low after a properly finished calibration.
- BUSY FLAG is high (DB7) if a calibration or a conversion is in process.

Note that all programmable bits of the SFR are reset to low by power-up.

Writing the SFR (SDA 0812 A/1812 D, see figure 9)

The SFR is activated by pulling CAZ and BYSL pins high and loading a data word with a general low on DB7 by a microprocessor WRITE cycle.

other DB	DB7	DB5	DB3	DB2*)	DB1	DB0	$\overline{CS}$/ $\overline{WR}$	CAZ/ BYSL	Function
reserved	LOW	LOW					active	HIGH	Reset of POWER FAIL FLAG
reserved	LOW	HIGH					active	HIGH	Set POWER FAIL FLAG (not locked)
reserved	LOW		LOW				active	HIGH	Wake-up from STANDBY
reserved	LOW		HIGH				active	HIGH	STANDBY mode active
reserved	LOW			LOW			active	HIGH	$\overline{CAL}$ function on pin 26
reserved	LOW			HIGH			active	HIGH	$\overline{TH}$ function on pin 26
reserved	LOW				LOW		active	HIGH	–
reserved	LOW				HIGH		active	HIGH	INT-$\overline{CAL}$ is initiated
reserved	LOW					LOW	active	HIGH	Output data latch transparent
reserved	LOW					HIGH	active	HIGH	Output data latch enabled

Reading the SFR (SDA 0812 A; see figure 10)

The contents of SFR are put to the DATA BUS by a microprocessor READ cycle in combination with BYSL and CAZ high.

Data Bus Pin	Function
DB0	DATA LATCH State: HIGH enabled, LOW transparent
DB1	CAL FLAG: HIGH during calibration
DB2	RESERVED
DB3	HIGH if STANDBY mode is active
DB4	RESERVED
DB5	POWER FAIL FLAG: HIGH if power fail occured
DB6	CAL ERROR FLAG: HIGH if calibration overflow occured
DB7	BUSY FLAG: HIGH during calibration or conversion

Warning: Reading on CAZ high and BYSL low is prevented for factory use, unpredictable data may appear on the data bus.

*) Refers to SDA 1812 D

Reading the SFR (SDA 1812 D; see figure 10)

The contents of SFR are put to the DATA BUS by a microprocessor READ cycle in combination with BYSL and CAZ high.

Data Bus Pin	Definition
DB0	DATA LATCH State: HIGH enabled, LOW transparent
DB1	CAL FLAG: HIGH during calibration
DB2	CAL/$\overline{\text{TH}}$: HIGH for $\overline{\text{TH}}$, LOW for $\overline{\text{CAL}}$ function
DB3	HIGH if STANDBY mode is active
DB4	RESERVED
DB5	POWER FAIL FLAG: HIGH if power fail occured
DB6	CAL ERROR FLAG: HIGH if calibration overflow occured
DB7	BUSY FLAG: HIGH during calibration or conversion

Reading on CAZ high and BYSL low is reserved for factory use only, unpredictable data may appear on the data bus.

Internal Clock Operation

The external circuitry for internal clock operation is shown in **figure 3**.

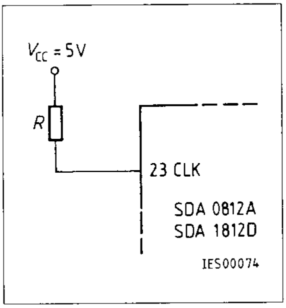
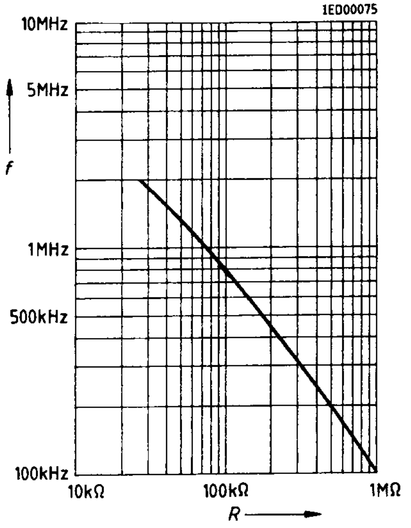


Figure 3
The Internal Clock Frequency only depends on the *R* Value

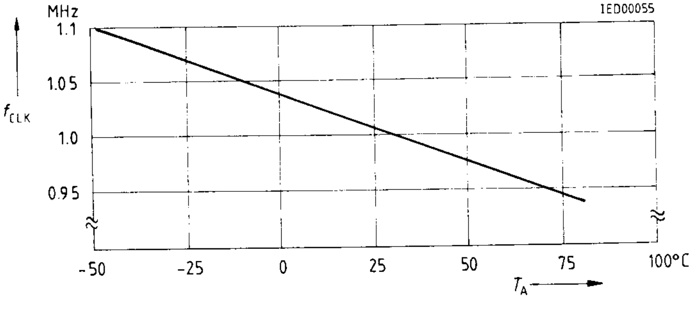
Figure 4
Clock Frequency of Internal Clock Generator versus External Resistor Value



The clock generator can be operated between 100 kHz and 2 MHz. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.0 MHz.

The actual operating frequency of the internal clock oscillator can vary from device to device. Therefore for precisely defined conversion times usage of an external clock generator is recommended.

Figure 5
Typical Internal Clock Frequency versus Temperature



External Clock Operation

The required circuitry for external clock operation is shown in **figure 6**.

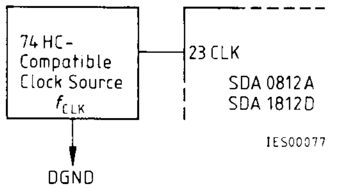


Figure 6

The external clock source has to provide 0.8 Vmax for low voltage level and 3.5 Vmin for high voltage level. The rise and fall times have to be 200 ns max. The minimal pulse width of ext. CLK has to be 200 ns.

There is no synchronizing between external clock and ext. TH signal. Synchronizing should be provided for optimal performance, see A/D converter timing on page 9. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.2 MHz.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Units
		min.	max.	
Supply voltages[1]	V_{CC}, V_{DD}		6.5	V
Input voltage range (all inputs)	V_I	– 0.3	V_{CC} + 0.3	V
Package dissipation (at or below 25 °C free-air temperature range)			875	mW
Ambient temperature	T_A	– 40	85	°C
Storage temperature	T_{stg}	– 65	125	°C

Note:
[1] All voltage values are with respect to network ground terminal

Characteristics (SDA 0812 A)

V_{CC} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, $V_{REF} \leq V_{DD} \geq V_{CC}$, $-V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications t_{min} to t_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Accuracy						
Resolution		12			Bit	No missing codes guaranteed
Total unadjusted error[1]	*TUE*			+/– 1/2	LSB	All channels, AIN0-AIN3
Differential nonlinearity	*DNL*			+/– 1/2	LSB	
Full scale error (gain error)	*GE*			+/– 1/4	LSB	All channels, AIN0-AIN3
Offset error	*OFS*			+/– 1/4	LSB	All channels, AIN0-AIN3
Channel to channel mismatch				+/– 1/4	LSB	
Analog Inputs						
Analog input range	V_{AIN}	$-V_{REF}$		V_{REF}	V	
Slew rate[2]	*SR*			8	mV/µs	
Multiplexer						
Settling time			20		ns	Switch delay after
ON-resistance	R_{ON}		2		kΩ	programming
OFF-resistance	R_{OFF}		10		MΩ	the input channel
On channel input capacitance	C_{AIN}		50		pF	
Input leakage current						
at 25 °C	I_{AIN}			10	nA	AIN0-AIN3
at t_{min} to t_{max}	I_{AIN}			100	nA	
On-state bias current			+/– 5		µA	Depends on analog input voltage
Reference Inputs						
Positive reference voltage	$+V_{REF}$	4.75	5	V_{DD}	V	For specified
Negative reference voltage	$-V_{REF}$		0		V	performance
Input reference current	I_{REF}		10	100	µA	
Power supply rejection	V_{DD}		± 1/8		LSB	V_{REF} = 4.75 V to 5.25 V
Logic Inputs						
CAZ (pin 1), RD (pin 18), $\overline{CS}$ (pin 19), WR (pin 20), BYSL (pin 21), A0 (pin 24), A1 (pin 25), $\overline{CAL}$ (pin 26)						
L-input voltage	V_{IL}	2.4		0.8	V	
H-input voltage	V_{IH}				V	

Notes see next page

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Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Logic Inputs						
Input current at 25 °C at – 40 °C … 85 °C	 I_{IN} I_{IN}	 – 1 – 10		 1 10	 µA µA	 V_{IN} = 0 V to V_{CC}
CLK (pin 23) L-input voltage H-input voltage L-input current H-input current	 V_{IL} V_{IH} I_{IL} I_{IH}	 3.5 – 10 		 0.8 10 1.5	 V V µA mA	 100 nA max. during standby
Logic Outputs						
DB0 to DB7 (pins 10 to 17), BUSY (pin 22) L-output voltage H-output voltage	 V_{QL} V_{QH}	 4.0		 0.4 	 V V	 I_{SINK} = 1.6 mA I_{SQURCE} = 200 µA
Floating state leakage current (pins 10-17)		– 1		1	µA	V_{OUT} = 0 V to V_{CC}
Floating state output capacitance	C_Q			15	pF	
Conversion Time						
With external clock	t			24	µs	f_{CLK} = 500 kHz
	t	6			µs	f_{CLK} = 2 MHz
with internal clock (T_A = 25 °C)	t	7.5			µs	Using recommended clock components as shown in **fig. 4**.
	t			38	µs	See internal clock operation
sampling time	t	2.5			µs	

Notes

1) Includes full scale error, offset error, integral and differential nonlinearity.

2) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full scale errors. Filtering by a low pass (R = 2 kΩ, C = 100 nF) or use of an external sample-and-hold is required then.

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Functional Range						
Supply voltage	V_{DD}		5		V	± 5 % for specified performance
	V_{CC}		5		V	± 5 % for specified performance
Supply current	I_{DD}			2.5	mA	Typ. 1 mA with V_{DD} = 5 V
	I_{CC}		1.0	2.0	mA	$V_{IN} = V_{IL}$ = or V_{IH}
Power dissipation	P_D		10	25	mW	WR = RD = CS = BUSY = HIGH
Power dissipation (standby mode)	P_{DSB}		50		µW	WR = RD = CS = BUSY = HIGH

Characteristics (SDA 1812 D)

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, $V_{REF} \leq V_{DD} \geq V_{CC}$, $- V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications t_{min} to t_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DC Accuracy						
Resolution		12			Bits	No missing codes guaranteed
Total unadjusted error[1]	*TUE*		± 1/2	± 3/4	LSB	All channels, AIN0-AIN3
Differential nonlinearity	*DNL*		± 1/4	± 1/2	LSB	
Full scale error (gain error)	*GE*		± 1/8	± 1/4	LSB	All channels, AIN0-AIN3
Offset error	*OFS*		± 1/8	± 1/4	LSB	All channels, AIN0-AIN3
Offset error with TH function			± 1/2	± 1	LSB	with internal clock generator or synchronizing TH to ext. CLK
Channel to channel mismatch				± 1/4	LSB	
Dynamic Performance[2) 3)]						
Signal to noise ratio	*SNR*	69	71		dB	Full scale input sinwave, 1 kHz *f* sampling is 100 kHz
		66	69		dB	Full scale input sinwave, 50 kHz *f* sampling is 100 kHz
Total harmonic distortion	*THD*		75		dB	Full scale input sinwave, 50 kHz *f* sampling is 100 kHz
Full power bandwidth (– 3 dB)	*BW*		4		MHz	
Aperture delay time			5		ns	T/H pin
Analog Inputs						
Analog input range Multiplexer	*AIN*	$-V_{REF}$		$+V_{REF}$	V	Selected and unselected channels AIN0-AIN3;
Settling time			10		ns	
On channel input Capacitance	C_{AIN}		50		pF	
ON-resistance	R_{ON}		2		kΩ	
OFF-resistance	R_{OFF}		10		MΩ	
Input leakage current + 25 °C	I_{AIN}			10	nA	
t_{min} to t_{max}	I_{AIN}			100	nA	
On-state bias current			± 5		µA	Depends on analog input voltage

Notes see next page

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference Inputs						
Positive reference voltage	$+V_{REF}$	4.75		V_{DD}	V	(For specified performance)
Negative reference voltage	$-V_{REF}$	0			V	(For specified performance)
Input reference current	I_{REF}			100	µA	$+V_{REF}$ = 5.0 V
Power Supply Rejection						
Supply voltage	V_{DD}		± 1/8		LSB	V_{DD} = 4.75 V to 5.25 V
Logic Inputs						
CAZ (pin 1)						
RD (pin 18), CS (pin 19),						
WR (pin 20) BYSL (pin 21),						
A0 (pin 24), A1 (pin 25)						
CAL (pin 26)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	2.4			V	
Input current						
+ 25 °C	I_{IN}	– 1		1	µA	V_{IN} = 0 V to V_{CC}
T_{min} to T_{max}	I_{IN}	– 10		10	µA	
CLK (pin 23)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	3.5			V	
L-input current	I_{IL}	– 10		10	µA	
H-input current	I_{IH}			1.5	mA	100 nA max. during standby
Logic Outputs						
DB0-DB7 (pins 10-17),						
BUSY (pin 22)						
L-output voltage	V_{OL}			0.4	V	I_{SINK} = 1.6 mA
H-output voltage	V_{OH}	4.0			V	I_{SOURCE} = 200 µA
Floating state leakage current (Pins 10-17)		– 1		1	µA	
Floating state output Capacitance	C_Q			15	pF	V_{OUT} = 0 V to V_{CC}

Notes

1) Includes full scale error, offset error, integral and differential nonlinearity.
2) *S/N* includes harmonic distortion
3) Sample tested at 25 °C

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Conversion Time						
With external clock	t_{ext}	6			µs	f_{CLK} = 2 MHz symmetrically
				24	µs	f_{CLK} = 500 kHz
With internal clock	t_{int}		6		µs	Using recommended clock components as shown in **figure 4**. See internal clock operation
Sampling time [1]	t_s	2.5			µs	
Power Requirements						
Analog supply voltage	V_{DD}	4.75	5	5.25	V	
Logic supply voltage	V_{CC}	4.75	5	5.25	V	
Analog supply current	I_{DD}		0.75	2.5	mA	V_{DD} = 5 V
Logic supply current	I_{CC}		1.0	2.0	mA	$V_{IN} = V_{IL}$ or V_{IH}
Power dissipation	P_D		10	25	mW	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ = Logic HIGH
Power dissipation (standby)	P_{DS}		50		µW	

Note:
[1] Ensures the analog input source to load 50pF during sampling time to required accuracy.

Timing Specifications[1]

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, $V_{REF} \leq V_{DD} \geq V_{CC}$, $-V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications t_{min} to t_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Min. TH LOW pulse width (SDA 1812 D)	t_{THL}	2.5			µs
AMUX-settling time after programming the input channel	t_{AMUX}		20		ns
CS to WR setup time	t_1[2]	0			ns
WR pulse width	t_2[2]	100			ns
CS to WR hold time	t_3[2]	0			ns
WR to BUSY propagation delay	t_4	20	50	150	ns
BYSL, CAZ valid to WR setup time	t_5	100			ns
BYSL, CAZ valid to WR hold time	t_6	20			ns
BUSY to CS setup time	t_7	0			ns
CS to RD setup time	t_8[2]	0			ns
RD pulse width	t_9[2]	100			ns
CS to RD hold time	t_{10}[2]	0			ns
BYSL, CAZ to RD setup time	t_{11}	50			ns
BYSL, CAZ to RD hold time	t_{12}	0			ns
RD to valid data					
Bus Access Time (100 pF Load)	t_{13}[3]		80	150	ns
Bus Access Time (50 pF Load)	t_{13}[3]		40	75	ns
RD to three-state output	t_{14}[4]	20		60	ns
Bus relinquish time	t_{15}[5]		90	180	ns
Data valid to WR setup time	t_{16}	100			ns
Data valid to WR hold time	t_{17}	20			ns

Notes:

1) All input control signals are specified with $t_r = t_f$ = 20 ns (10 % to 90 % of 5 V) and timed from a voltage level of 1.6 V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}/\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}/\overline{WR}$.
3) t_{13} is measured with the load circuits of **figure 11** and defined as the time required for an output to cross 0.8 V or 2.4 V.
4) t_{14} is defined as the time required for the data lines to change three-state, **see figure 11.**
5) t_{15} is defined as the time required for the data lines to change 10 %/90 % when loaded with the circuits of **figure 11.**

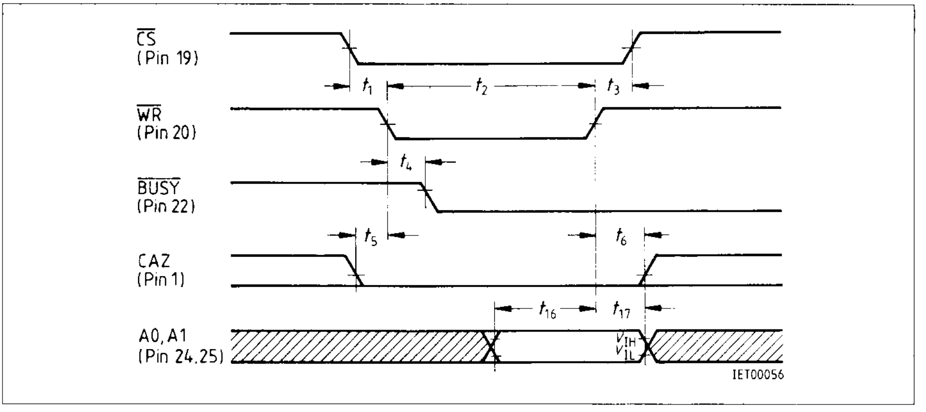

Figure 7
Red Cycle Timing

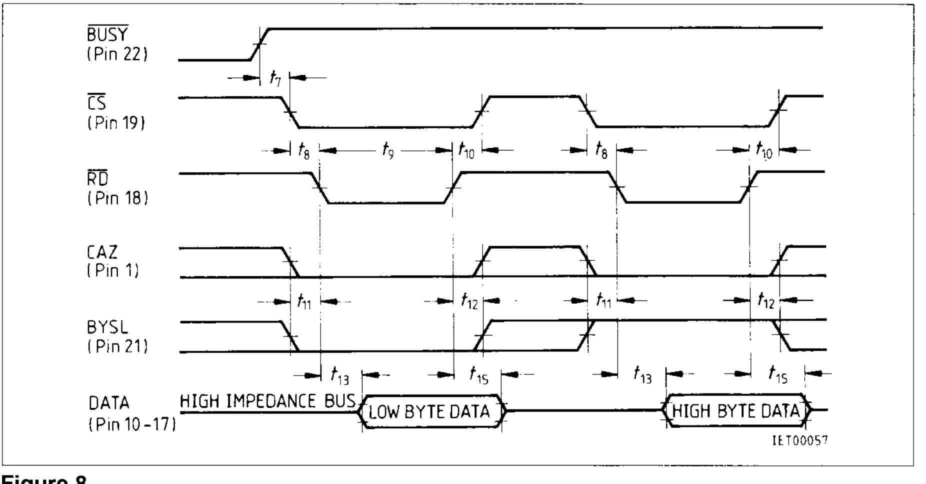

Figure 8
Red Cycle Timing

Notes

The 2-byte conversion result can be read in either order. The figure shows the sequence low byte to high byte. If BYSL changes while $\overline{CS}$ and $\overline{RD}$ are low the data will change to reflect the BYSL input.

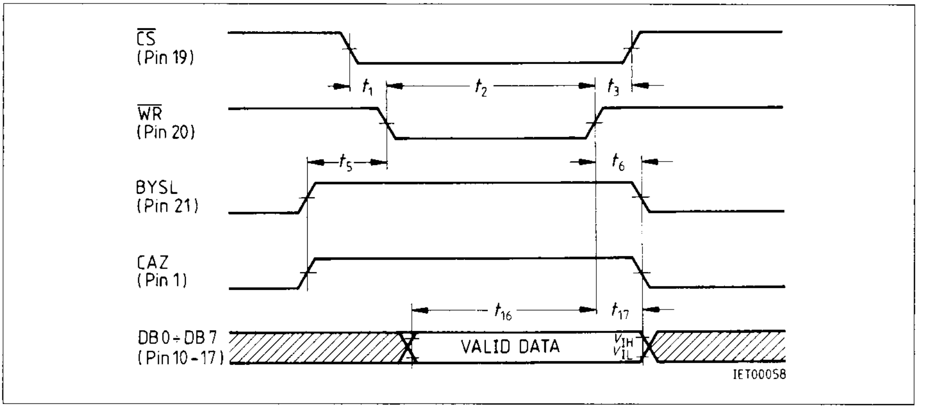

Figure 9
Writing to the SFR

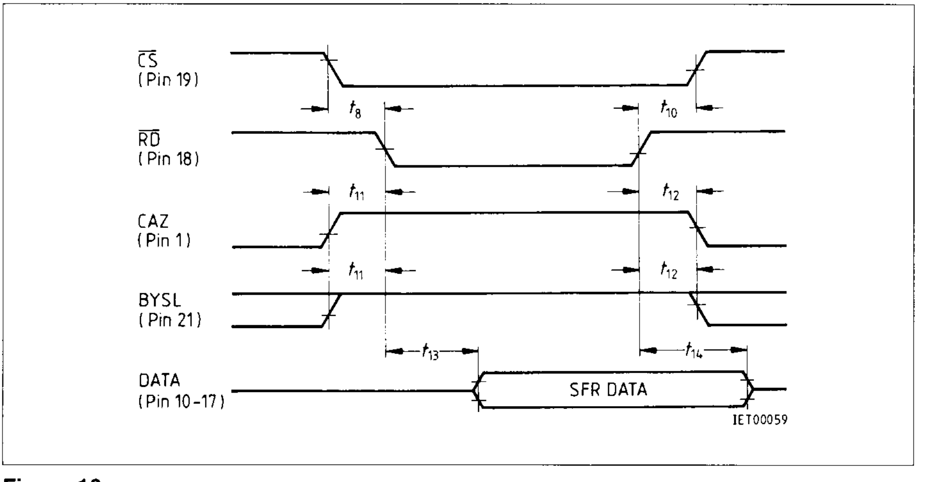

Figure 10
Reading the SFR

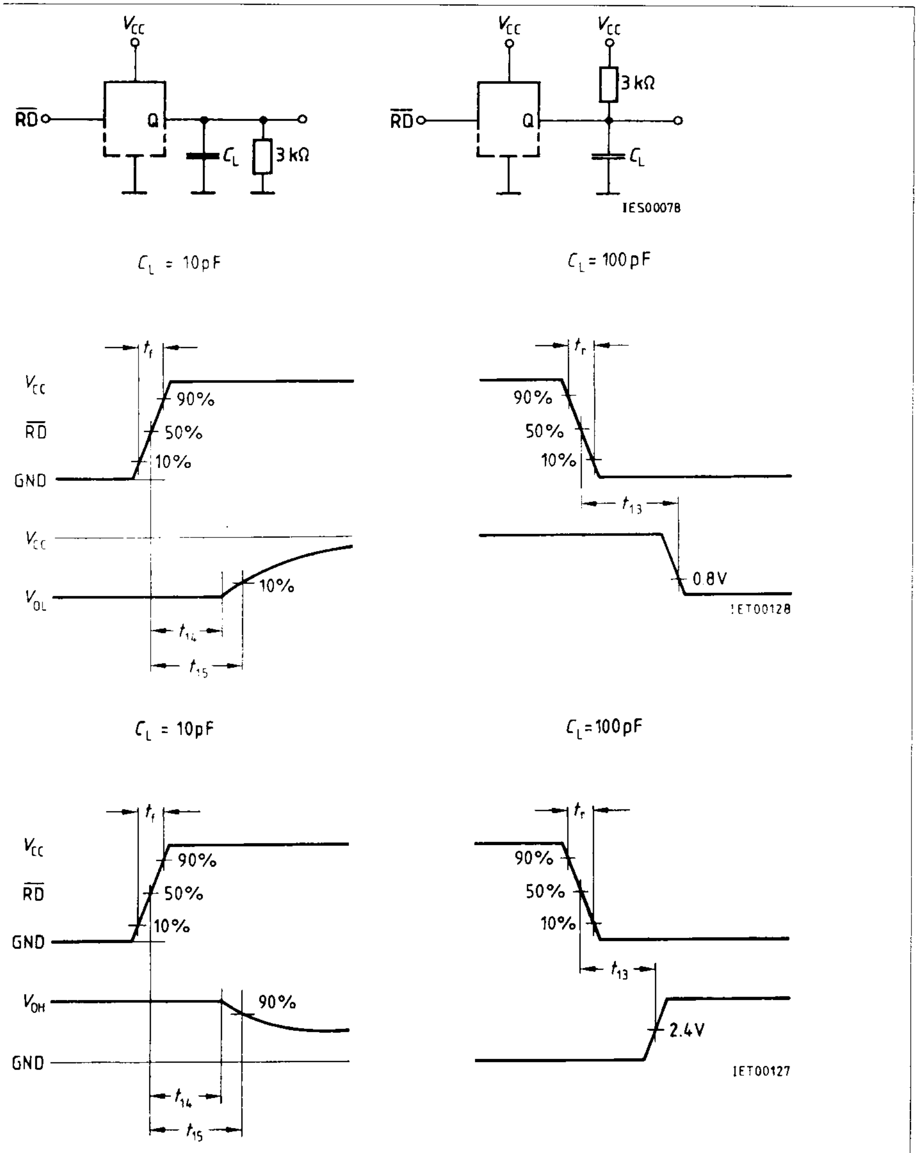

Figure 11
THREE-STATE Test Circuits and Timing Diagrams

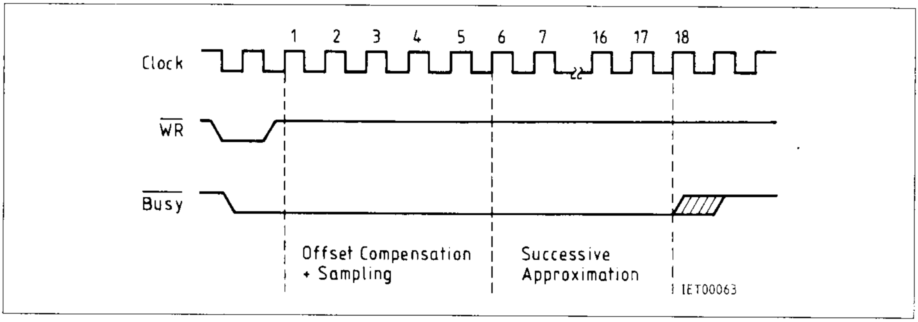

Figure 12
Converter Timing (SDA 0812 A)

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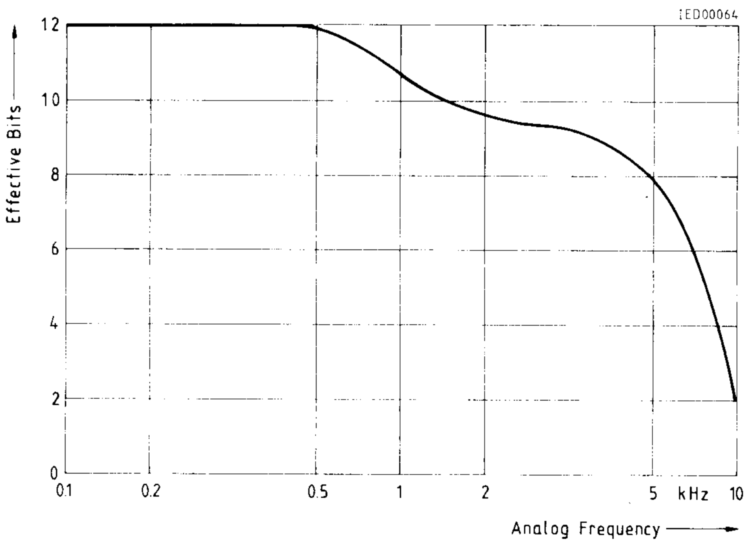
Figure 13

Effective Number of Bits versus Analog Input Frequency (SDA 0812 A)
$V_{CC} = V_{DD} = + V_{REF} = 5$ V, $- V_{REF} = 0$ V; $f_{CLK} = 1$ MHz



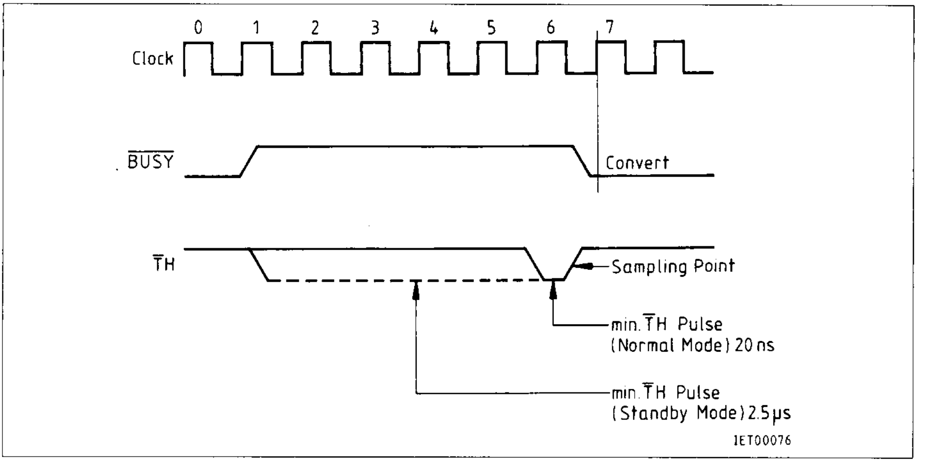


Figure 14
TH-Timing (SDA 1812 D)

Dynamic Performance (SDA 1812 D)

The SDA 1812 D is specified dynamically as well as with standard DC specifications.

Figures 15 and 16 show 2048 point FFT plots of the SDA 1812 D with analog input signals of 1 kHz and 50 kHz. When the SNR is calculated it includes harmonics.

Figure 15

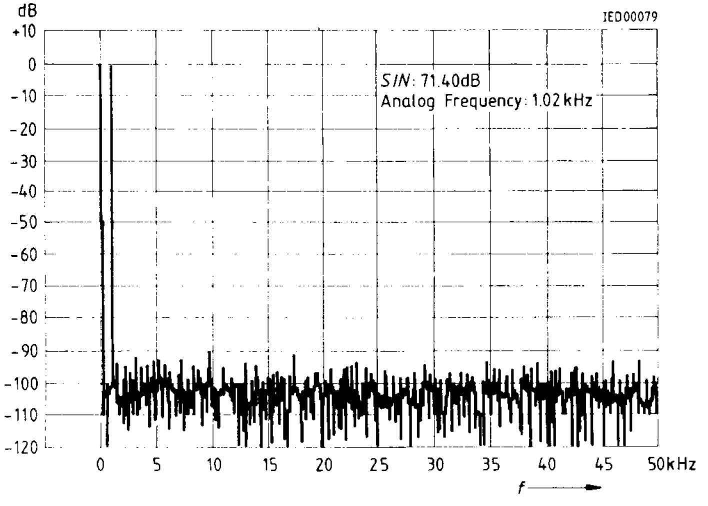
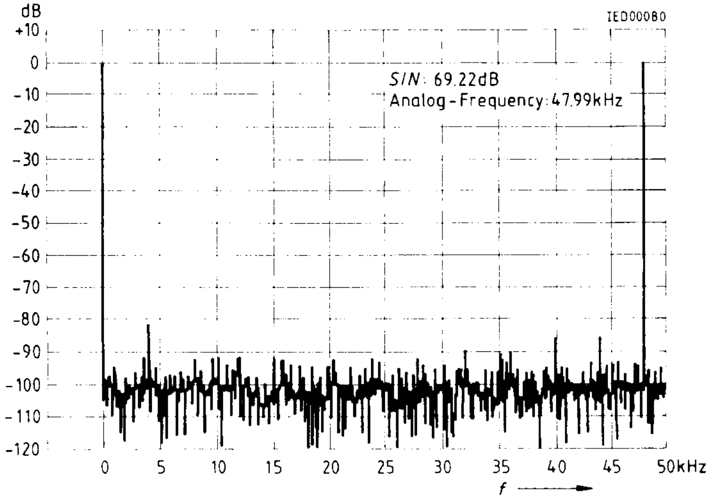


Figure 16

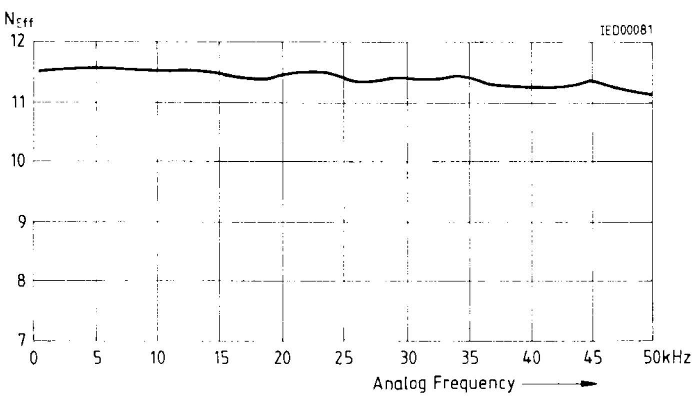


The relationship between Signal-to-Noise Ratio (*SNR* including harmonics) and the resolution of an ideal ADC with no differential or integral linearity errors is expressed in the following equation:

$$N_{eff} = \frac{SNR\,[\text{dB}] - 1.76}{6.02}$$

Figure 17

Typ. Effective Number of Bits versus Analog Input Frequency



7

Micorprocessor Interfacing

Microprocessor interfacing is straight forward and requires only a few external gates.

Siemens/Intel Microprocessors

A typical interface is shown in **figure 15**.

- Start of Conversion
  A write instruction selects one of the analog input channels and starts the conversion. Write Address: ADC-CS , DATA pins DO0 and DO1 select the analog input channel. The BUSY signal can be used to generate an interrupt to the micorprocessor (INT).
- Read the Conversion Result:
  A read instruction from the: ADC-CS -address fetches the low byte, a read instruction from ADC-CS -address + 2 the high byte.

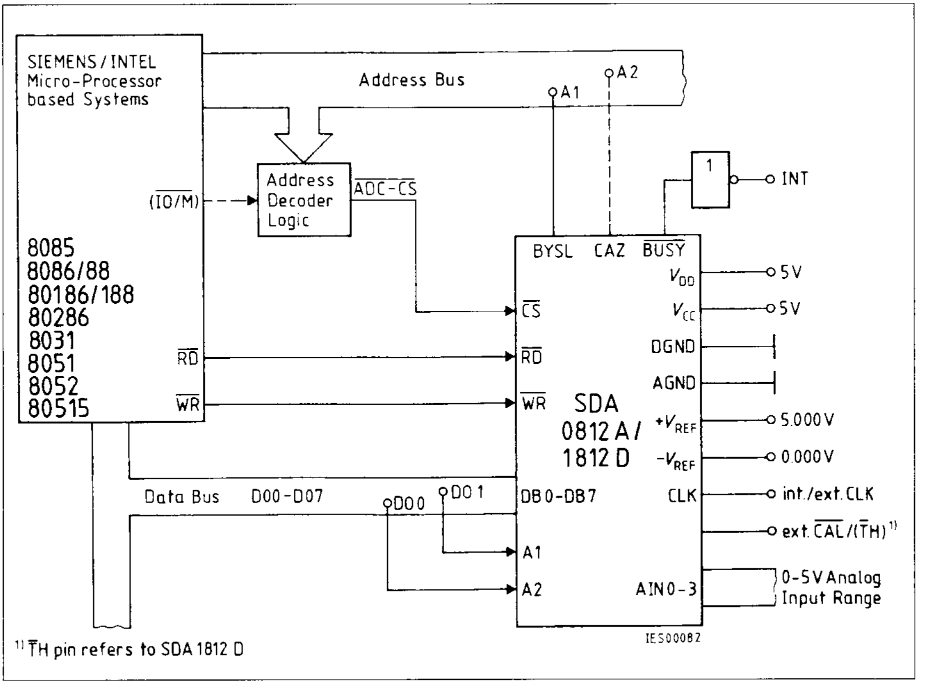


Figure 18

Motorola Microprocessors

A typical interface is shown below

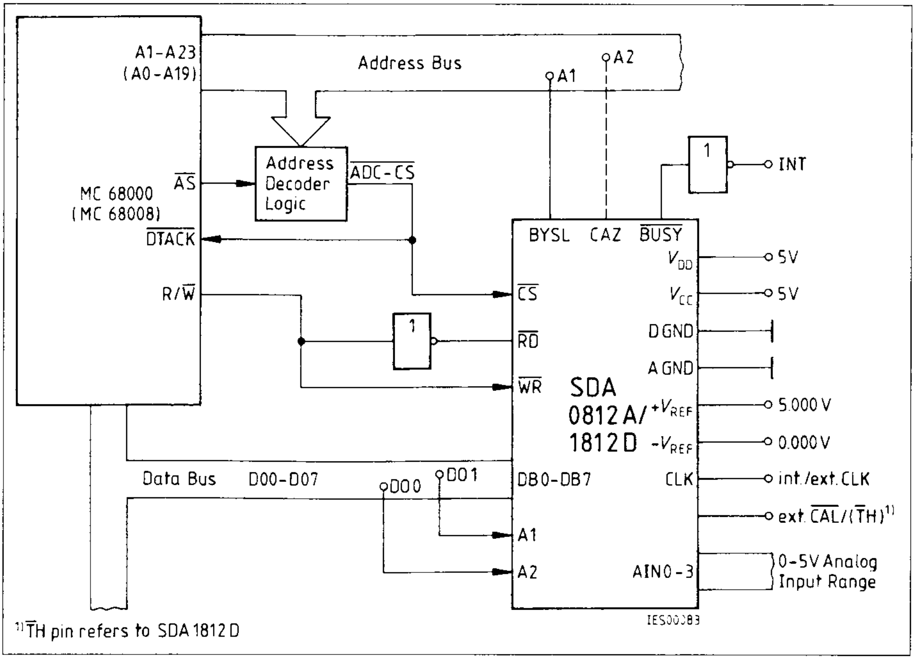


Figure 19

- **Start of Conversion**
  A WRITE instruction to an address decoded by the address decoder logic will start a conversion. The lower 2 bits of the data bus select the input channel. MOVE.W D0, ADC-ADDRESS.

- **Read the Conversion Result**
  A READ instruction to the ADC-ADDRESS puts the conversion result to the data bus: MOVE.PW$000 (ADC-ADDRESS), D0 places the 12-bit result of the conversion in the D0 register. The address decoder has to pull down ADC-CS wire at ADC-ADDRESS and ADC-ADDRESS + 2.
  Figure 20 shows how the result is placed in register D0.

		BUSY	0	0	0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Figure 20

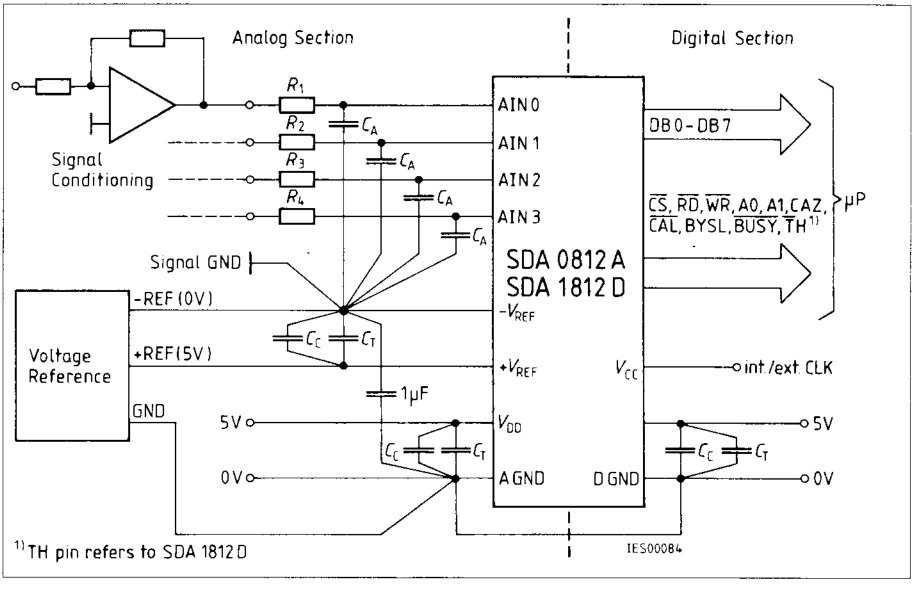


Figure 21
Application Hints

	SDA 0812 A	SDA 1812 D
C_A	… 5 nF	… 10 nF
C_C	… 10 nF Ceramic	… 10 nF Ceramic
C_T	… 10 µF Tantal	… 10 µF Tantal
R_1 … R_4	… 50 Ω	… 100 Ω

Power Supply Decoupling

The digital respectively analog 5 V power supply should be connected with a 10 μF tantalum capacitor to DGND respectively AGND. To ensure good HF performance this capacitor should be connected in parallel with a 10 nF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Note, that logic supply voltage V_{CC} must not be applied before V_{DD}!

Reference Voltage

To avoid dynamic errors a 10 μF tantalum capacitor connected in parallel with a 10 nF ceramic capacitor should be placed as close as possible to the component between pins + V_{REF} and – V_{REF}. Also an 1 μF capacitor should be placed between – V_{REF} and AGND.

Analog Inputs

The high input impedance of the analog channels AIN 0 to AIN 3 allows simple analog interfacing. Signal sources – V_{REF} ≤ AIN ≤ + V_{REF} can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 5 clock cycles.

All converter measurements are done with respect to the reference voltages, analog ground only powers the chip. Therefore – V_{REF} has to be used as the signal ground. The simple RC-filter 50 Ω, 5 nF (100 Ω, 10 nF) is recommended in order to protect the analog input against spikes and noise during the offset compensation period.

Application Note

For operation without any interferences, + V_{REF} must not exceed V_{DD} (see characteristics: $V_{DD} \geq V_{CC}$, $V_{DD} \geq + V_{REF}$), especially not during switching-on. Please start autocalibration using pin CAL after all voltages (V_{DD}, V_{CC}, + V_{REF}, – V_{REF}) are stable.

Note
Values in brackets refer to SDA 1812 D.