19-3047; Rev 0; 10/03

EVALUATION KIT AVAILABLE

# TFT-LCD Power-Supply Controllers



## General Description

The MAX1513/MAX1514 provide complete power-supply solutions for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs). Both devices include a high-performance step-up regulator controller, three linear-regulator controllers, and an adjustable delay block for startup sequencing. The MAX1513 includes an additional linear-regulator controller and a high-performance buffer amplifier. The MAX1513/MAX1514 can operate from 2.7V to 5.5V input supplies and provide overload protection with timer delay latch on all the regulated outputs.

The step-up regulator controller drives an external N-channel MOSFET to generate the regulated supply voltage for the panel source-driver ICs. Its current-mode control architecture provides fast transient response to pulsed loads. The high switching frequency (up to 1.5MHz) allows the use of ultra-small inductors and ceramic capacitors while achieving efficiencies over 85% using lossless current sensing. The internal soft-start limits the input surge current during startup.

The gate-on and gate-off linear-regulator controllers of the MAX1513/MAX1514 provide regulated TFT gate-on and gate-off supplies. The gate-on supply is activated after an adjustable delay following the step-up regulator. The logic linear-regulator controller can be used to create a low-voltage logic supply. The gamma linear-regulator controller of the MAX1513 can be used to generate a gamma-correction reference supply or another general-purpose supply rail. The MAX1513's high-performance buffer amplifier can drive the LCD backplane (VCOM) or the gamma-correction divider string.

The MAX1513/MAX1514 are available in 4mm × 4mm 20-pin thin QFN packages with a maximum thickness of 0.8mm, suitable for ultra-thin LCD panel design.

## Applications

Notebook Computer Displays

LCD Monitors and TVs

Automotive Displays

***Pin Configuration appears at end of data sheet.***

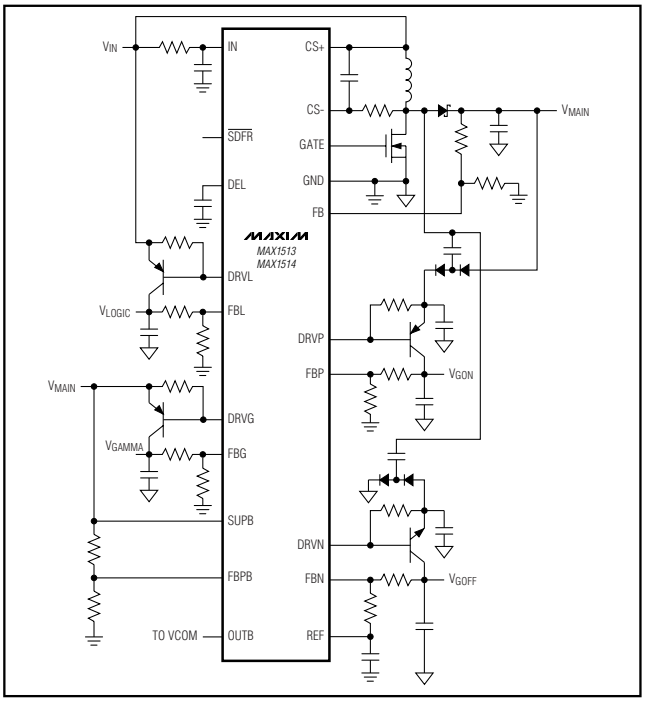
## Features

- **2.7V to 5.5V Input Supply Range**
- **Input-Supply Undervoltage Lockout**
- **Current-Mode Step-Up Controller**
  - **Fast Transient Response to Pulsed Load**
  - **High Efficiency**
  - **Lossless Current Sensing**
  - **430kHz/750kHz/1.5MHz Switching Frequency**
- **Linear-Regulator Controllers for $V_{GON}$, $V_{GOFF}$**
- **Linear-Regulator Controller for Logic Supply**
- **High-Performance Buffer Amplifier (MAX1513 Only)**
- **Additional Linear-Regulator Controller (MAX1513 Only)**
- **Power-Up Sequence and $V_{GON}$ Delay Control**
- **$V_{MAIN}$, $V_{GON}$, $V_{GOFF}$, $V_{GAMMA}$ Shutdown Control**
- **Timer-Delay Fault Latch for All Outputs**
- **Thermal-Overload Protection**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX1513**ETP | -40°C to +85°C | 20 Thin QFN 4mm x 4mm |
| **MAX1514**ETP | -40°C to +85°C | 20 Thin QFN 4mm x 4mm |

## Minimal Operating Circuit



## ABSOLUTE MAXIMUM RATINGS

FB, FBP, FBN, FBG, FBL, IN, CS+, CS-, $\overline{SDFR}$ to GND .....-0.3V to +6V
DEL, GATE, REF to GND .....-0.3V to ($V_{IN}$ + 0.3V)
SUPB to GND .....-0.3V to +14V
OUTB, FBPB to GND .....-0.3V to ($V_{SUPB}$ + 0.3V)
DRVP, DRVG, DRVL to GND .....-0.3V to +30V
DRVN to GND .....($V_{IN}$ - 28V) to ($V_{IN}$ + 0.3V)
OUTB Continuous Output Current .....±75mA
Continuous Power Dissipation ($T_A$ = +70°C)
20-Pin TQFN (derate 16.9mW/°C above +70°C) .....1349mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN}$ = 3V, $V_{SUPB}$ = 10V, $\overline{SDFR}$ = IN, $C_{REF}$ = 0.22µF, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| IN Supply Range | $V_{IN}$ | | | 2.7 | | 5.5 | V |
| IN Undervoltage-Lockout Threshold | $V_{UVLO}$ | 350mV typical hysteresis | $V_{IN}$ rising | 2.5 | 2.7 | 2.9 | V |
| | | | $V_{IN}$ falling | 2.2 | 2.35 | 2.5 | |
| IN Quiescent Current | $I_{IN}$ | $V_{FB}$ = $V_{FBP}$ = $V_{FBL}$ = $V_{FBG}$ = 1.5V, $V_{FBN}$ = 0 | | | | 1.25 | mA |
| IN Shutdown Current | | $V_{\overline{SDFR}}$ = 0, $V_{FBL}$ = 1.5V | | | | 150 | µA |
| REF Output Voltage | | -2µA < $I_{REF}$ < 100µA, 2.7V < $V_{IN}$ < 5.5V | | 1.231 | 1.250 | 1.269 | V |
| Thermal Shutdown | | Temperature rising | | | +160 | | °C |
| | | Hysteresis | | | 15 | | |
| Duration to Trigger Fault Latch | | | | | 43.6 | | ms |
| **MAIN STEP-UP CONTROLLER** | | | | | | | |
| Operating Frequency | $f_{OSC}$ | $\overline{SDFR}$ = IN | | 1.275 | 1.500 | 1.725 | MHz |
| | | $\overline{SDFR}$ = REF | | 0.60 | 0.75 | 0.90 | |
| | | $\overline{SDFR}$ = unconnected | | | 0.43 | | |
| Oscillator Maximum Duty Cycle | | | | 80 | 85 | 90 | % |
| FB Regulation Voltage | $V_{FB}$ | $V_{CS+}$ - $V_{CS-}$ = 0 | | 1.237 | 1.25 | 1.263 | V |
| FB Fault Trip Level | | $V_{FB}$ falling | | 0.96 | 1.00 | 1.04 | V |
| FB Load Regulation | | 0 < ($V_{CS+}$ - $V_{CS-}$) < 50mV | | | -1 | | % |
| FB Line Regulation | | $V_{IN}$ = 2.7V to 5.5V | | | 0.1 | 0.2 | %/V |
| FB Input Bias Current | | $V_{FB}$ = 1.5V | | -100 | | +100 | nA |
| CS+ Input Current | | 2.2V < $V_{CS+}$ < 6V | | | | 90 | µA |
| CS- Input Current | | 2.2V < $V_{CS-}$ < 6V | | -1 | | +1 | µA |
| Current-Limit Threshold | | $V_{CS+}$ - $V_{CS-}$, 2.2V < $V_{CS+}$ < 6V | | 100 | 125 | 150 | mV |
| Gate-Drive Output | | High or low | | | 3 | 5 | Ω |
| Soft-Start Period | $t_{SS}$ | | | | 2.7 | | ms |
| Soft-Start Step Size | | | | | $V_{REF}$ / 128 | | V |
| **GATE-ON LINEAR-REGULATOR CONTROLLER (REG P)** | | | | | | | |
| FBP Regulation Voltage | $V_{FBP}$ | $I_{DRVP}$ = 50µA | | 1.225 | 1.250 | 1.275 | V |
| FBP Fault Trip Level | | $V_{FBP}$ falling | | 0.96 | 1.00 | 1.04 | V |
| FBP Input Bias Current | | $V_{FBP}$ = 1.5V | | -250 | | +250 | nA |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = 3V, $V_{SUPB}$ = 10V, $\overline{SDFR}$ = IN, $C_{REF}$ = 0.22µF, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| FBP Effective Load-Regulation Error (Transconductance) | | $V_{DRVP}$ = 10V, $I_{DRVP}$ = 25µA to 500µA | | -1.5 | -2 | % |
| FBP Line (IN)-Regulation Error | | $I_{DRVP}$ = 50µA, 2.7V < $V_{IN}$ < 5.5V | | | 8 | mV |
| DRVP Sink Current | $I_{DRVP}$ | $V_{FBP}$ = 1.1V, $V_{DRVP}$ = 10V | 1 | | | mA |
| DRVP Off-Leakage Current | | $V_{FBP}$ = 1.5V, $V_{DRVP}$ = 28V | | 0.15 | 10 | µA |
| DEL Charge Current | | During startup, $V_{DEL}$ = 1.0V | 4 | 5 | 6 | µA |
| DEL Turn-On Threshold | $V_{TH(DEL)}$ | | 1.19 | 1.25 | 1.31 | V |
| DEL Discharge Switch On-Resistance | | $V_{IN}$ = 3.0V, $V_{FB}$ = 0.8V | | 15 | | Ω |
| Soft-Start Period | $t_{SS}$ | | | 2.7 | | ms |
| Soft-Start Step Size | | | | $V_{REF}$ / 128 | | V |
| **GAMMA LINEAR-REGULATOR CONTROLLER (REG G, MAX1513 ONLY)** | | | | | | |
| FBG Regulation Voltage | $V_{FBG}$ | $I_{DRVG}$ = 0.35mA | 1.235 | 1.250 | 1.265 | V |
| FBG to FB Regulation Voltage Matching | | $I_{DRVG}$ = 0.5mA, $V_{CS+}$ - $V_{CS-}$ = 0 | -1.2 | | +1.2 | % |
| FBG Fault Trip Level | | $V_{FBG}$ falling | 0.96 | 1.00 | 1.04 | V |
| FBG Input Bias Current | | $V_{FBG}$ = 1.5V | -250 | | +250 | nA |
| FBG Effective Load-Regulation Error (Transconductance) | | $V_{DRVG}$ = 10V, $I_{DRVG}$ = 0.175mA to 3.5mA | | -1.5 | -2 | % |
| FBG Line (IN)-Regulation Error | | $I_{DRVG}$ = 0.5mA, 2.7V < $V_{IN}$ < 5.5V | | | 5 | mV |
| DRVG Sink Current | $I_{DRVG}$ | $V_{FBG}$ = 1.1V, $V_{DRVG}$ = 10V | 5 | | | mA |
| DRVG Off-Leakage Current | | $V_{FBG}$ = 1.5V, $V_{DRVG}$ = 28V | | 0.15 | 10 | µA |
| Soft-Start Period | $t_{SS}$ | | | 2.7 | | ms |
| Soft-Start Step Size | | | | $V_{REF}$ / 128 | | V |
| **LOGIC LINEAR-REGULATOR CONTROLLER (REG L)** | | | | | | |
| FBL Regulation Voltage | $V_{FBL}$ | $I_{DRVL}$ = 0.8mA | 1.225 | 1.250 | 1.275 | V |
| FBL Fault Trip Level | | $V_{FBL}$ falling | 0.96 | 1.00 | 1.04 | V |
| FBL Input Bias Current | | $V_{FBL}$ = 1.5V | -250 | | +250 | nA |
| FBL Effective Load-Regulation Error (Transconductance) | | $V_{DRVL}$ = 3V, $I_{DRVL}$ = 0.4mA to 8mA | | -1.5 | -2 | % |
| FBL Line (IN)-Regulation Error | | $I_{DRVL}$ = 1mA, 2.7V < $V_{IN}$ < 5.5V | | | 8 | mV |
| DRVL Sink Current | $I_{FBL}$ | $V_{FBL}$ = 1.1V, $V_{DRVL}$ = $V_{IN}$ | 15 | 20 | | mA |
| DRVL Off-Leakage Current | | $V_{FBL}$ = 1.5V, $V_{DRVL}$ = 28V | | 0.15 | 10 | µA |
| Soft-Start Period | $t_{SS}$ | | | 2.7 | | ms |
| Soft-Start Step Size | | | | $V_{REF}$ / 128 | | V |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = 3V, $V_{SUPB}$ = 10V, $\overline{SDFR}$ = IN, $C_{REF}$ = 0.22µF, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GATE-OFF LINEAR-REGULATOR CONTROLLER (REG N)** | | | | | | |
| FBN Regulation Voltage | $V_{FBN}$ | $I_{DRVN}$ = 0.2mA | 220 | 250 | 280 | mV |
| FBN Fault Trip Level | | $V_{FBN}$ rising | 380 | 420 | 460 | mV |
| FBN Input Bias Current | | $V_{FBN}$ = 0V | -250 | | +250 | nA |
| FBN Effective Load-Regulation Error (Transconductance) | | $V_{DRVN}$ = -10V, $I_{DRVN}$ = 0.1mA to 2mA | | 18 | 25 | mV |
| FBN Line (IN)-Regulation Error | | $I_{DRVN}$ = 0.2mA, 2.7V < $V_{IN}$ < 5.5V | | | 5 | mV |
| DRVN Source Current | $I_{FBN}$ | $V_{FBN}$ = 0.3V, $V_{DRVN}$ = -10V | 5 | | | mA |
| DRVN Off-Leakage Current | | $V_{FBN}$ = -0.1V, $V_{DRVN}$ = -20V | | 0.1 | 10 | µA |
| Soft-Start Period | $t_{SS}$ | | | 2.7 | | ms |
| Soft-Start Step Size | | | | $V_{REF}$ / 128 | | V |
| **BUFFER AMPLIFIER** | | | | | | |
| SUPB Supply Range | $V_{SUPB}$ | | 4.5 | | 13.0 | V |
| SUPB Supply Current | $I_{SUPB}$ | No load, $V_{FBPB}$ = 4V | | 0.75 | 1.1 | mA |
| FBPB Input Offset Voltage | $V_{OS}$ | $V_{FBPB}$ = $V_{SUPB}$ / 2 | | 0 | 12 | mV |
| FBPB Input Bias Current | $I_{BIAS}$ | $V_{FBPB}$ = $V_{SUPB}$ / 2 | | | 50 | nA |
| FBPB Input Common-Mode Range | $V_{CM}$ | | 0 | | $V_{SUPB}$ | V |
| Common-Mode Rejection Ratio | CMRR | 0 < $V_{FBPB}$ < $V_{SUPB}$ | 50 | | | dB |
| Output-Voltage-Swing High | $V_{OH}$ | $I_{OUTB}$ = 5mA | $V_{SUPB}$ - 150 | $V_{SUPB}$ - 80 | | mV |
| Output-Voltage-Swing Low | $V_{OL}$ | $I_{OUTB}$ = -5mA | | 80 | 150 | mV |
| Short-Circuit Current | | | ±50 | ±150 | | mA |
| Power-Supply Rejection Ratio | PSRR | DC, 6V ≤ $V_{SUPB}$ ≤ 13V, $V_{FBPB}$ = 4V | 60 | 80 | | dB |
| Slew Rate | | | | 10 | | V/µs |
| -3dB Bandwidth | | $R_L$ = 10kΩ, $C_L$ = 10pF | | 12 | | MHz |
| **CONTROL INPUTS AND OUTPUTS** | | | | | | |
| $\overline{SDFR}$ Input Level | | $\overline{SDFR}$ = IN (1.5MHz operation) | 0.9 × $V_{IN}$ | | | V |
| | | $\overline{SDFR}$ = unconnected (430kHz operation) | 0.69 × $V_{IN}$ | | 0.77 × $V_{IN}$ | |
| | | $\overline{SDFR}$ = REF (750kHz operation) | 1.00 | | 1.35 | |
| | | $\overline{SDFR}$ = GND (LCD shutdown) | | | 0.5 | |
| $\overline{SDFR}$ Input Current | | $\overline{SDFR}$ = IN | | | +3.0 | µA |
| | | $\overline{SDFR}$ = REF | -3.0 | | | |
| | | $\overline{SDFR}$ = GND | -3.0 | | | |

## ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN}$ = 3V, $V_{SUPB}$ = 10V, $\overline{SDFR}$ = IN, $C_{REF}$ = 0.22µF, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| IN Supply Range | $V_{IN}$ | | | 2.7 | | 5.5 | V |
| IN Undervoltage-Lockout Threshold | $V_{UVLO}$ | 350mV typical hysteresis | $V_{IN}$ rising | 2.5 | | 2.9 | V |
| | | | $V_{IN}$ falling | 2.2 | | 2.5 | |
| IN Quiescent Current | $I_{IN}$ | $V_{FB} = V_{FBP} = V_{FBL} = V_{FBG}$ = 1.5V, $V_{FBN}$ = 0 | | | | 1.25 | mA |
| REF Output Voltage | | -2µA < $I_{REF}$ < 100µA, 2.7V < $V_{IN}$ < 5.5V | | 1.225 | | 1.275 | V |
| **MAIN STEP-UP CONTROLLER** | | | | | | | |
| Operating Frequency | $f_{OSC}$ | $\overline{SDFR}$ = IN | | 1.275 | | 1.725 | MHz |
| | | $\overline{SDFR}$ = REF | | 0.60 | | 0.90 | |
| FB Regulation Voltage | $V_{FB}$ | $V_{CS+} - V_{CS-}$ = 0 | | 1.230 | | 1.270 | V |
| FB Line Regulation | | $V_{IN}$ = 2.7V to 5.5V | | | | 0.2 | %/V |
| FB Input Bias Current | | $V_{FB}$ = 1.5V | | -100 | | +100 | nA |
| CS+ Input Current | | 2.2V < $V_{CS+}$ < 6V | | | | 90 | µA |
| CS- Input Current | | 2.2V < $V_{CS-}$ < 6V | | -1 | | +1 | µA |
| Current-Limit Threshold | | $V_{CS+} - V_{CS-}$, 2.2V < $V_{CS+}$ < 6V | | 100 | | 150 | mV |
| Gate-Drive Output | | High or low | | | | 5 | Ω |
| **GATE-ON LINEAR-REGULATOR CONTROLLER (REG P)** | | | | | | | |
| FBP Regulation Voltage | $V_{FBP}$ | $I_{DRVP}$ = 0.1mA | | 1.225 | | 1.275 | V |
| FBP Input Bias Current | | $V_{FBP}$ = 1.5V | | -250 | | +250 | nA |
| FBP Effective Load-Regulation Error (Transconductance) | | $V_{DRVP}$ = 10V, $I_{DRVP}$ = 0.05mA to 1mA | | | | -2 | % |
| DRVP Sink Current | $I_{DRVP}$ | $V_{FBP}$ = 1.1V, $V_{DRVP}$ = 10V | | 2 | | | mA |
| DEL Turn-On Threshold | $V_{TH(DEL)}$ | | | 1.19 | | 1.31 | V |
| **GAMMA LINEAR-REGULATOR CONTROLLER (REG G, MAX1513 ONLY)** | | | | | | | |
| FBG Regulation Voltage | $V_{FBG}$ | $I_{DRVG}$ = 0.5mA | | 1.235 | | 1.265 | V |
| FBG to FB Regulation Voltage Matching | | $I_{DRVG}$ = 0.5mA, $V_{CS+} - V_{CS-}$ = 0 | | -1.2 | | +1.2 | % |
| FBG Input Bias Current | | $V_{FBG}$ = 1.5V | | -250 | | +250 | nA |
| FBG Effective Load-Regulation Error (Transconductance) | | $V_{DRVG}$ = 10V, $I_{DRVG}$ = 0.25mA to 5mA | | | | -2 | % |
| DRVG Sink Current | $I_{DRVG}$ | $V_{FBG}$ = 1.1V, $V_{DRVG}$ = 10V | | 10 | | | mA |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = 3V, $V_{SUPB}$ = 10V, $\overline{SDFR}$ = IN, $C_{REF}$ = 0.22µF, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 1)

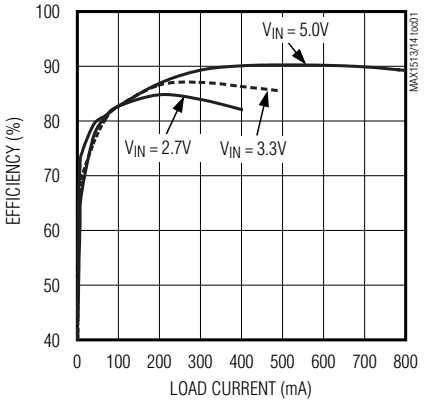
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **LOGIC LINEAR-REGULATOR CONTROLLER (REG L)** | | | | | | |
| FBL Regulation Voltage | $V_{FBL}$ | $I_{DRVL}$ = 1mA | 1.225 | | 1.275 | V |
| FBL Input Bias Current | | $V_{FBL}$ = 1.5V | -250 | | +250 | nA |
| FBL Effective Load-Regulation Error (Transconductance) | | $V_{DRVL}$ = 3V, $I_{DRVL}$ = 0.5mA to 10mA | | | -2 | % |
| DRVL Sink Current | $I_{FBL}$ | $V_{FBL}$ = 1.1V, $V_{DRVL}$ = $V_{IN}$ | 20 | | | mA |
| **GATE-OFF LINEAR-REGULATOR CONTROLLER (REG N)** | | | | | | |
| FBN Regulation Voltage | $V_{FBN}$ | $I_{DRVN}$ = 0.2mA | 220 | | 280 | mV |
| FBN Input Bias Current | | $V_{FBN}$ = 0V | -250 | | +250 | nA |
| FBN Effective Load-Regulation Error (Transconductance) | | $V_{DRVN}$ = -10V, $I_{DRVN}$ = 0.1mA to 2mA | | | 25 | mV |
| DRVN Source Current | $I_{FBN}$ | $V_{FBN}$ = 0.3V, $V_{DRVN}$ = -10V | 5 | | | mA |
| **BUFFER AMPLIFIER** | | | | | | |
| SUPB Supply Range | $V_{SUPB}$ | | 4.5 | | 13.0 | V |
| SUPB Supply Current | $I_{SUPB}$ | No load, $V_{FBPB}$ = 4V | | | 1.1 | mA |
| FBPB Input Offset Voltage | $V_{OS}$ | $V_{FBPB}$ = $V_{SUPB}$ / 2 | | | 12 | mV |
| FBPB Input Bias Current | $I_{BIAS}$ | $V_{FBPB}$ = $V_{SUPB}$ / 2 | | | 50 | nA |
| FBPB Input Common-Mode Range | $V_{CM}$ | | 0 | | $V_{SUPB}$ | V |
| Output-Voltage-Swing High | $V_{OH}$ | $I_{OUTB}$ = 5mA | $V_{SUPB}$ - 150 | | | mV |
| Output-Voltage-Swing Low | $V_{OL}$ | $I_{OUTB}$ = -5mA | | | 150 | mV |
| **CONTROL INPUTS AND OUTPUTS** | | | | | | |
| $\overline{SDFR}$ Input Level | | $\overline{SDFR}$ = IN (1.5MHz operation) | 0.9 × $V_{IN}$ | | | V |
| | | $\overline{SDFR}$ = unconnected (430kHz operation) | 0.69 × $V_{IN}$ | | 0.77 × $V_{IN}$ | |
| | | $\overline{SDFR}$ = REF (750kHz operation) | 1.00 | | 1.35 | |
| | | $\overline{SDFR}$ = GND (LCD shutdown) | | | 0.5 | |
| $\overline{SDFR}$ Input Current | | $\overline{SDFR}$ = IN | | | +3.0 | µA |
| | | $\overline{SDFR}$ = REF | -3.0 | | | |
| | | $\overline{SDFR}$ = GND | -3.0 | | | |

**Note 1:** Specifications to -40°C are guaranteed by design, not production tested.

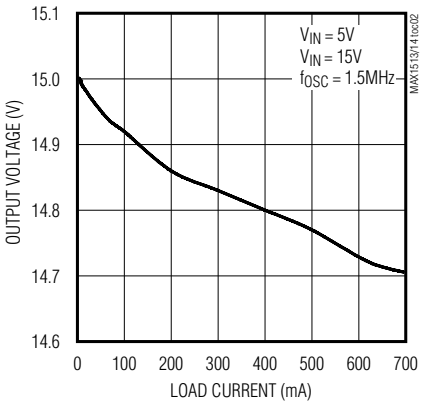
## Typical Operating Characteristics

(Circuit of Figure 1, $V_{IN}$ = 5V, $V_{MAIN}$ = 15V, $V_{GON}$ = 25V, $V_{GOFF}$ = -10V, $V_{LOGIC}$ = 3.3V, $V_{GAMMA}$ = 14.7V, $T_A$ = +25°C, unless otherwise noted.)

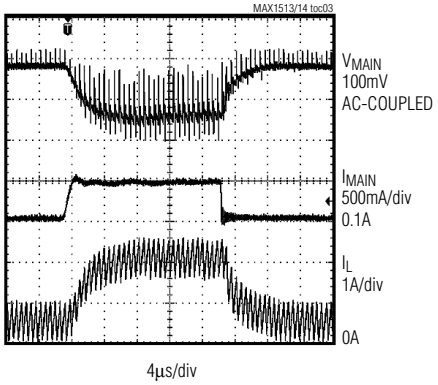
**STEP-UP EFFICIENCY vs. LOAD CURRENT (1.5MHz)**



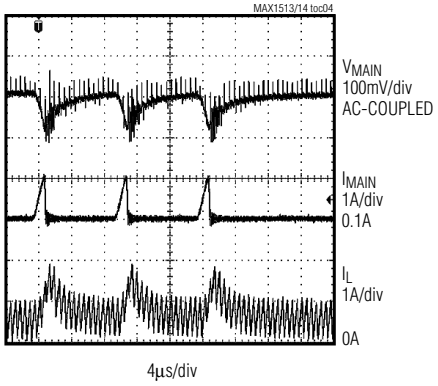

**STEP-UP OUTPUT VOLTAGE vs. LOAD CURRENT**



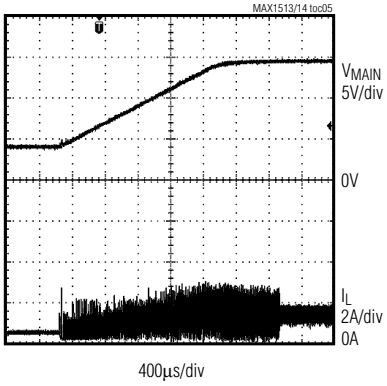

**STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE**



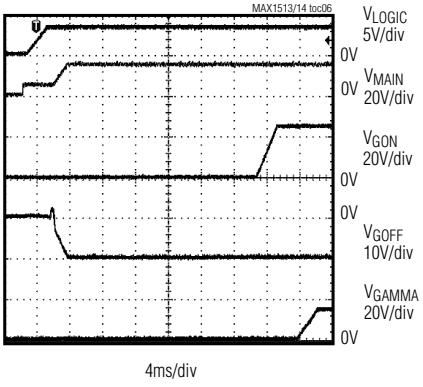

**STEP-UP REGULATOR PULSED-LOAD-TRANSIENT RESPONSE**



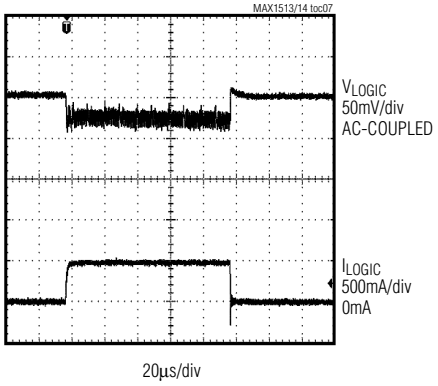

**STEP-UP REGULATOR SOFT-START**



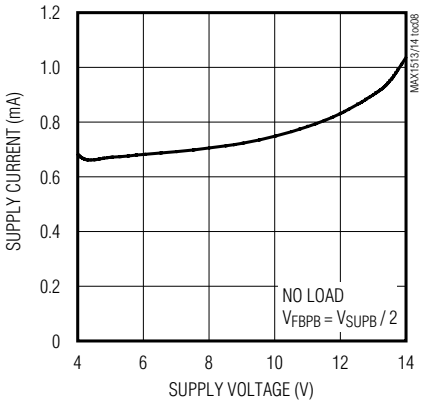

**POWER-UP SEQUENCE**



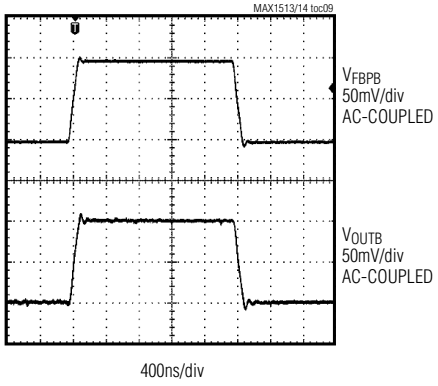

**LINEAR REGULATOR REG L LOAD-TRANSIENT RESPONSE**




**BUFFER-AMPLIFIER SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**BUFFER-AMPLIFIER SMALL-SIGNAL STEP RESPONSE**

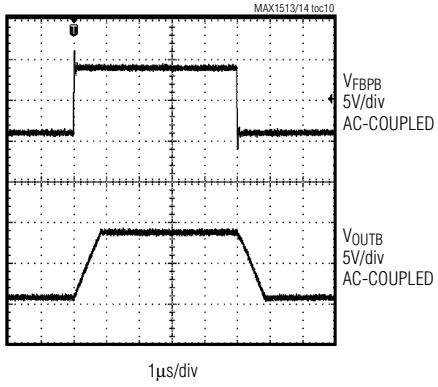


# TFT-LCD Power-Supply Controllers

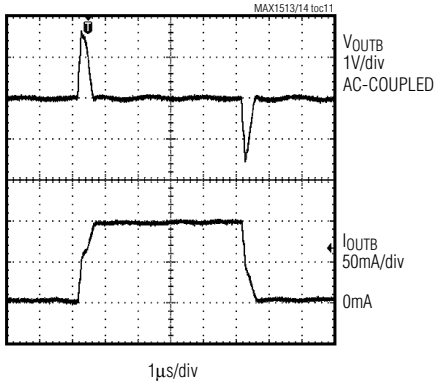
## Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN}$ = 5V, $V_{MAIN}$ = 15V, $V_{GON}$ = 25V, $V_{GOFF}$ = -10V, $V_{LOGIC}$ = 3.3V, $V_{GAMMA}$ = 14.7V, $T_A$ = +25°C, unless otherwise noted.)

**BUFFER-AMPLIFIER LARGE-SIGNAL STEP RESPONSE**




**BUFFER-AMPLIFIER LOAD-TRANSIENT RESPONSE**




## Pin Description

| PIN | NAME | | FUNCTION |
|---|---|---|---|
| | MAX1513 | MAX1514 | |
| 1 | REF | REF | Internal Reference. Connect a 0.22µF ceramic capacitor from REF to the analog ground plane, which is connected to GND. External load capability is at least 100µA. |
| 2 | $\overline{SDFR}$ | $\overline{SDFR}$ | LCD Shutdown and Frequency-Select Input.<br>$\overline{SDFR}$ = GND, LCD shutdown, REF, buffer amplifier and the logic regulator (REG L) output stay on<br>$\overline{SDFR}$ = IN, 1.5MHz switching frequency<br>$\overline{SDRF}$ = REF, 750kHz switching frequency<br>$\overline{SDFR}$ = unconnected, 430kHz switching frequency |
| 3 | FBPB | N.C. | Buffer-Amplifier Noninverting Input for the MAX1513. Not internally connected for the MAX1514. |
| 4 | OUTB | N.C. | Buffer-Amplifier Output for the MAX1513. Not internally connected for the MAX1514. |
| 5 | SUPB | N.C. | Buffer-Amplifier Supply Input for the MAX1513. Bypass to GND with a 0.1µF capacitor. Not internally connected for the MAX1514. |
| 6 | FBN | FBN | Gate-Off Linear Regulator (REG N) Feedback Input. FBN regulates to 125mV nominal. Connect to the center tap of a resistive voltage-divider between the REG N output and the reference voltage (REF) to set the output voltage. Place the resistive-divider close to this pin. |
| 7 | DEL | DEL | Delay-Control Timing Capacitor. Connect a capacitor from DEL to GND to set the gate-on linear-regulator startup delay. See the *Power-Up Sequence and Delay Control Block* section. |

## Pin Description (continued)

| PIN | NAME | | FUNCTION |
|---|---|---|---|
| | MAX1513 | MAX1514 | |
| 8 | DRVN | DRVN | REG N Base Drive. Open drain of an internal P-channel MOSFET. Connect to the base of an external NPN linear-regulator pass transistor. |
| 9 | DRVL | DRVL | Logic Linear-Regulator (REG L) Base Drive. Open drain of an internal N-channel MOSFET. Connect to the base of an external PNP linear-regulator pass transistor. |
| 10 | FBL | FBL | REG L Feedback Input. FBL regulates to 1.25V (typ). Connect to the center tap of a resistive voltage-divider between the REG L output and the analog ground plane to set the output voltage. Place the resistive voltage-divider close to this pin. |
| 11 | DRVG | N.C. | Gamma Linear-Regulator (REG G) Base Drive for the MAX1513. Open drain of an internal N-channel MOSFET. Connect to the base of an external PNP linear-regulator pass transistor. Not internally connected for the MAX1514. |
| 12 | FBG | N.C. | REG G Feedback Input for MAX1513. FBG regulates to 1.25V (typ). Connect to the center tap of a resistive voltage-divider between the REG G output and the analog ground plane to set the output voltage. Place the divider close to the FBG pin. Not internally connected for the MAX1514. |
| 13 | FBP | FBP | Gate-On Linear-Regulator (REG P) Feedback Input. FBP regulates to 1.25V (typ). Connect to the center tap of a resistive voltage-divider between the REG P output and the analog ground plane to set the output voltage. Place the resistive-divider close to this pin. |
| 14 | DRVP | DRVP | REG P Base Drive. Open drain of an internal N-channel MOSFET. Connect to the base of an external PNP linear-regulator pass transistor. |
| 15 | GND | GND | Ground |
| 16 | GATE | GATE | External MOSFET Gate Drive. Drives the gate of the step-up switching regulator's MOSFET. |
| 17 | IN | IN | Supply Input. IN powers all the internal circuitry of the MAX1513/MAX1514. The input voltage range is from 2.7V to 5.5V. Bypass with a 0.1µF ceramic capacitor between IN and GND. Place the capacitor within 5mm of IN. |
| 18 | CS+ | CS+ | Current-Sense-Comparator Noninverting Input. Connect CS+ and CS- to the lossless current-sense network. See the *Lossless Current Sense* section. |
| 19 | CS- | CS- | Current-Sense-Comparator Inverting Input. Connect CS+ and CS- to the lossless current-sense network. See the *Lossless Current Sense* section. |
| 20 | FB | FB | Main Step-Up Regulator Feedback Input. FB regulates to 1.25V (typ). Connect to the center tap of a resistive voltage-divider between the main output ($V_{MAIN}$) and the analog ground plane to set the main step-up regulator output voltage. Place the resistive-divider close to this pin. |

# TFT-LCD Power-Supply Controllers

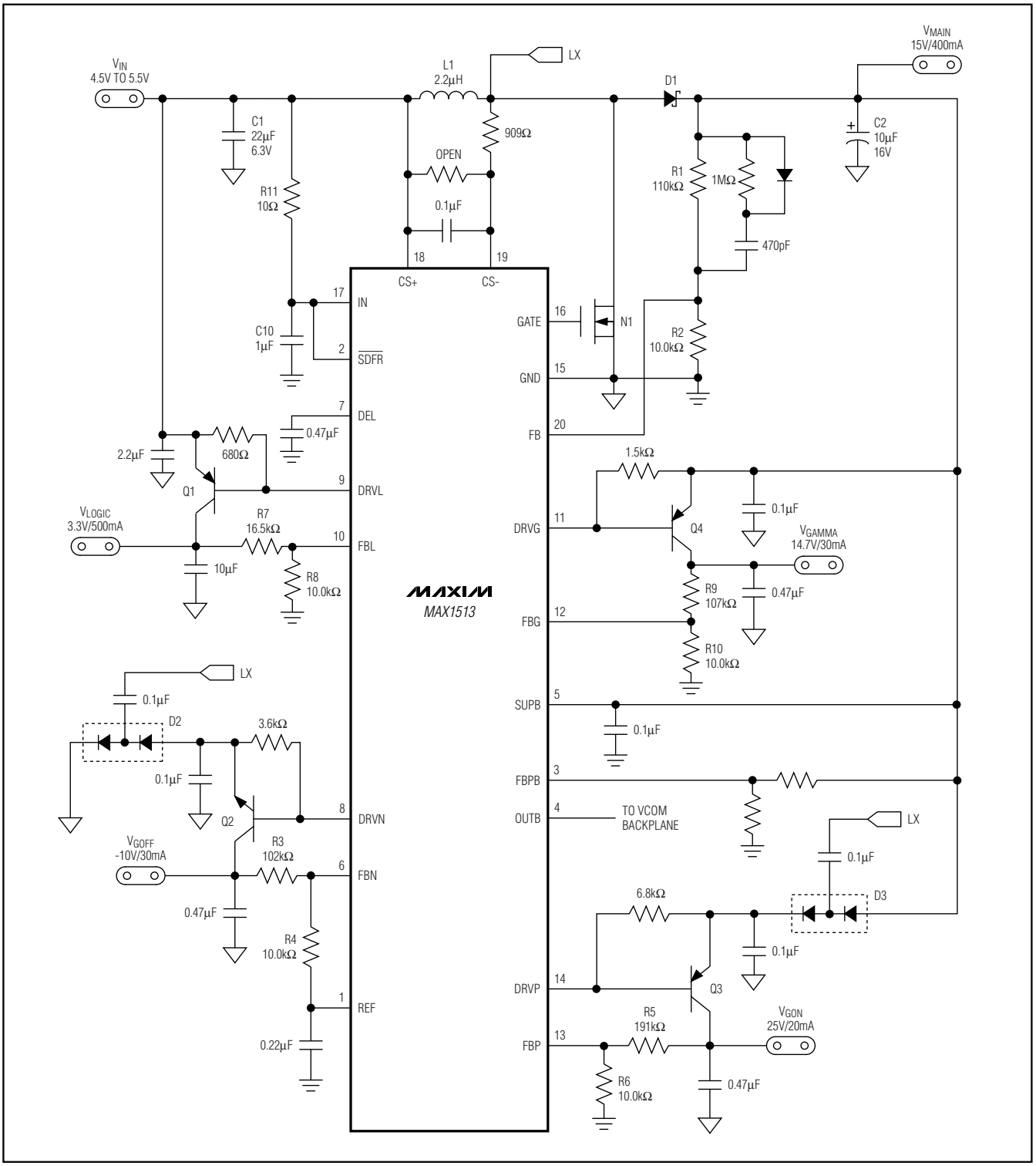



*Figure 1. Typical Operating Circuit of the MAX1513*

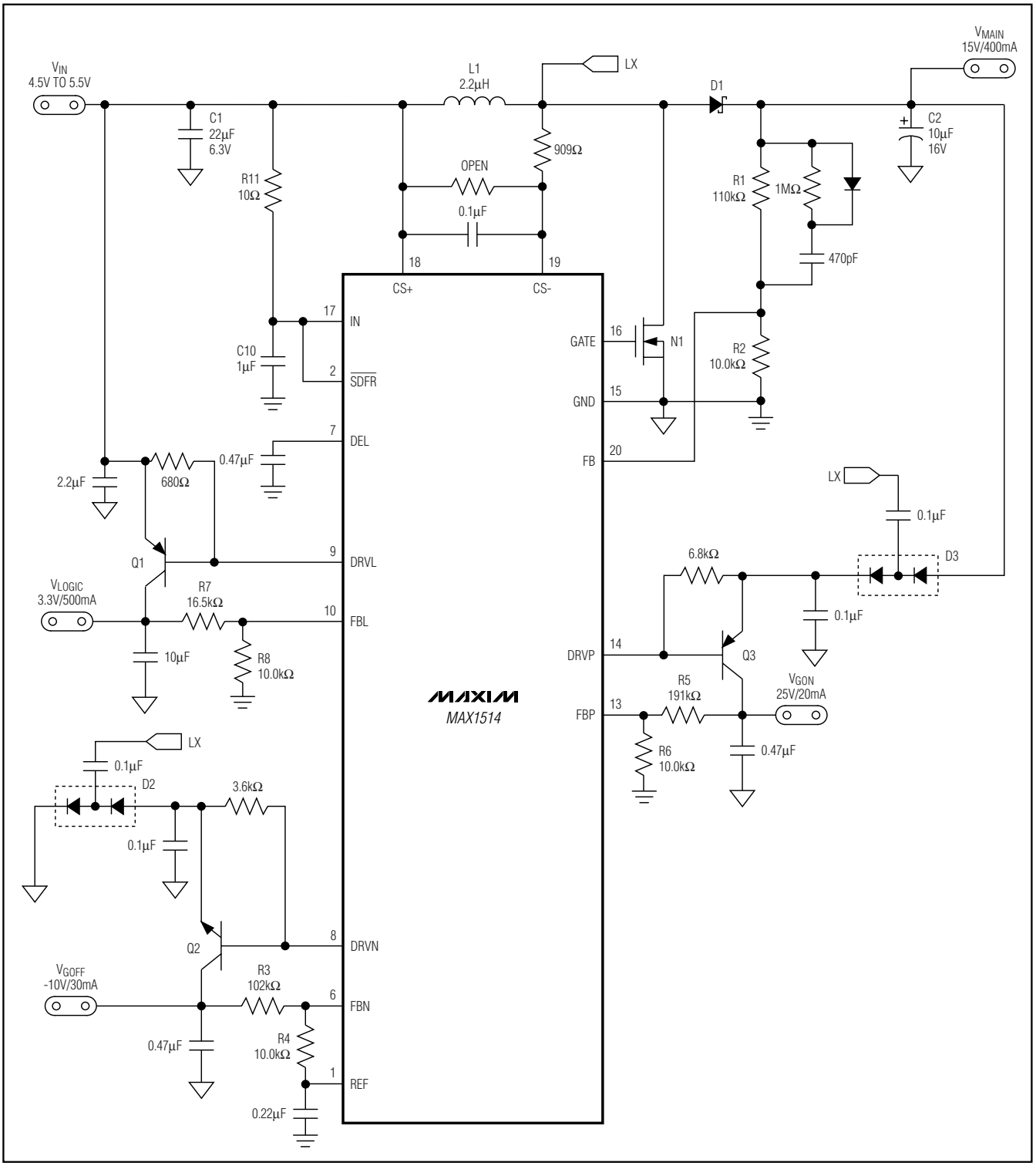



*Figure 2. Typical Operating Circuit of the MAX1514*

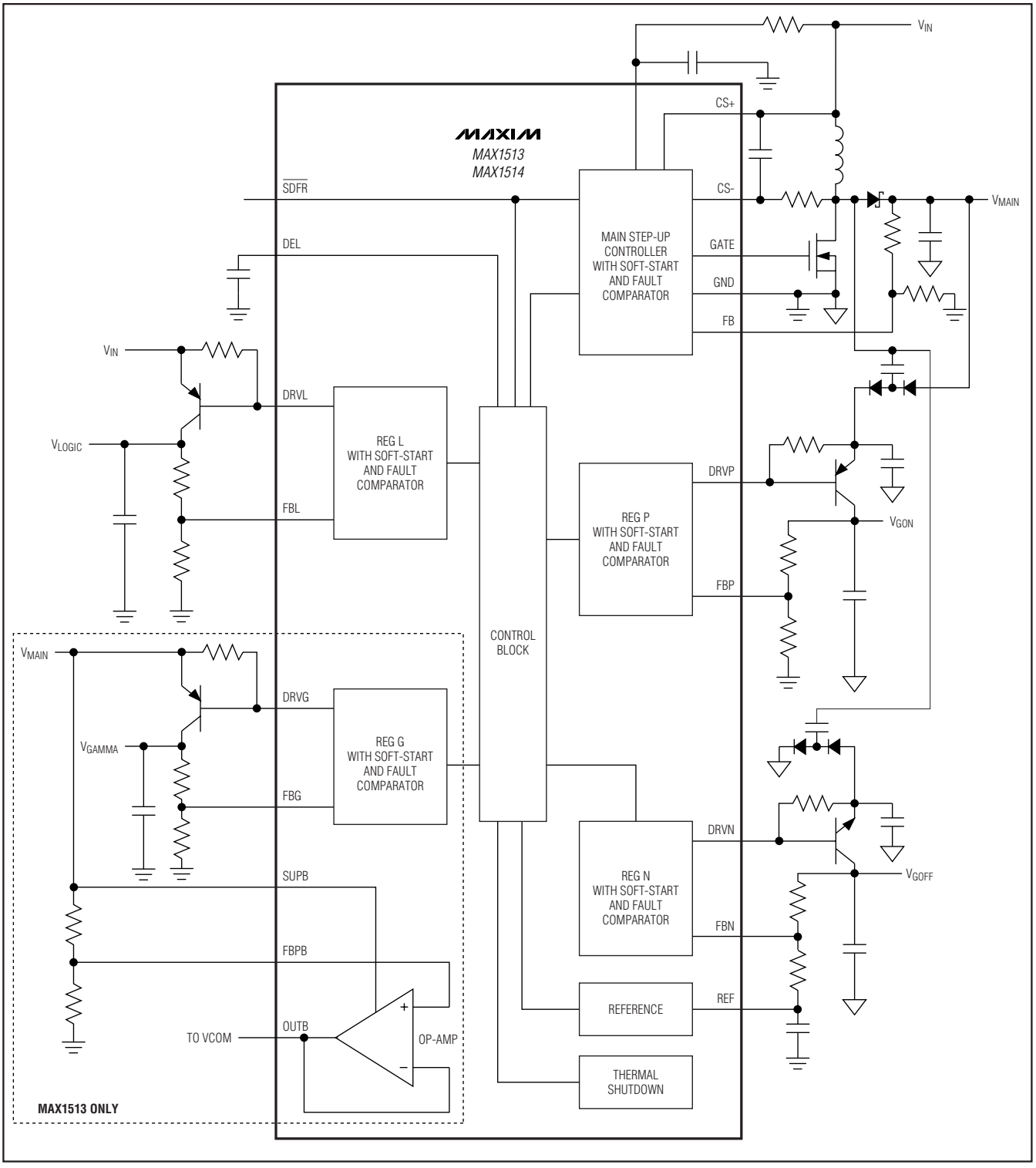



*Figure 3. MAX1513/MAX1514 Functional Diagram*

## Typical Operating Circuit

The typical operating circuit of the MAX1513 (Figure 1) is a complete power-supply system for TFT LCDs. The circuit generates a +15V source-driver supply, +25V and -10V gate-driver supplies, a +3.3V logic supply for the timing controller, a 14.7V gamma-correction string supply and a VCOM buffer. The typical operating circuit of the MAX1514 (Figure 2) is similar to that of the MAX1513 except the gamma-correction string supply and the VCOM buffer have been eliminated. The input voltage range for the IC is from +2.7V to +5.5V. The typical operating circuits' listed load currents are available from a +4.5V to +5.5V supply. Table 1 lists recommended component options, and Table 2 lists the component suppliers' contact information.

### Table 1. Component List

| DESIGNATION | DESCRIPTION |
|---|---|
| C1 | 22µF ±20%, 6.3V X5R ceramic capacitor (1206)<br>Taiyo Yuden JMK316BJ226ML |
| C2 | 10µF ±20%, 16V POSCAP (D10)<br>Sanyo 16AQU10M |
| D1 | 1A, 30V Schottky diode (S-Flat)<br>Toshiba CRS02 |
| D2, D3 | 200mA, 100V diodes (SOT23)<br>Fairchild MMBT4148SE |
| L1 | 2.2µH, 3.3A inductor<br>Sumida CLS7D16NP-2R2NC |
| N1 | 3A, 20V N-channel MOSFET (SOT23)<br>Fairchild FDN339AN |
| Q1 | 3A, 60V PNP bipolar transistor (SOT23)<br>Fairchild NZT660 |
| Q2 | 200mA, 40V NPN bipolar transistor (SOT23)<br>Fairchild MMBT3904 |
| Q3, Q4 | 200mA, 40V PNP bipolar transistors (SOT23)<br>Fairchild MMBT3906 |

## Detailed Description

The MAX1513 and MAX1514 contain a high-performance, step-up switching-regulator controller and three linear-regulator controllers (two positive and one negative). The MAX1513 also includes an additional linear-regulator controller and a high-current buffer amplifier. Figure 3 shows the MAX1513/MAX1514 functional diagram.

### Main Step-Up Regulator Controller

The main step-up regulator controller drives an external N-channel power MOSFET to generate the TFT-LCD source-driver supply. The controller employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads found in source-driver applications. The multilevel control input $\overline{SDFR}$ sets the switching frequency to 430kHz, 750kHz, or 1.5MHz. The high switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs, while maintaining high efficiency using a lossless current-sense method. The IC's built-in soft-start function reduces the inrush current during startup.

The controller regulates the output voltage and the power delivered to the output by modulating the duty cycle (D) of the power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Figure 4 shows the functional diagram of the step-up regulator controller. The core of the controller is a multi-input summing comparator that sums three signals: the output-voltage error signal with respect to the reference voltage, the current-sense signal, and the slope-compensation ramp. On the rising edge of the internal clock, the controller sets a flip-flop, which turns on the external N-channel MOSFET, applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the feedback voltage error, slope compensation, and current-sense signals trip the multi-

### Table 2. Component Suppliers

| SUPPLIER | PHONE | FAX | WEBSITE |
|---|---|---|---|
| Fairchild Semiconductor | 408-822-2000 | 408-822-2102 | www.fairchildsemi.com |
| Sumida | 847-545-6700 | 847-545-6720 | www.sumida.com |
| Taiyo Yuden | 800-348-2496 | 847-925-0899 | www.t-yuden.com |
| TDK | 847-803-6100 | 847-390-4405 | www.component.tdk.com |
| Toshiba | 949-455-2000 | 949-859-3963 | www.toshiba.com |

input PWM comparator, the flip-flop is reset and the MOSFET turns off. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp down, transferring the energy stored in the magnetic field to the output capacitor and the load. The N-channel MOSFET is kept off for the rest of the clock cycle.

### Current Limiting and Current-Sense Amplifier (CS+, CS-)

The internal current-limit circuit resets the PWM flip-flop and turns off the external power MOSFET whenever the voltage difference between CS+ and CS- exceeds 125mV (typ). The tolerance on this current limit is ±20%. Use the minimum value of the current limit to select components of the current-sense network.

### Lossless Current Sense

The lossless current-sense method uses the DC resistance (DCR) of the inductor as the sense element. Figure 5 shows a simplified step-up regulator using the basic lossless current-sensing method. An RC network is connected in parallel with the step-up inductor (L). The voltage across the sense capacitor ($C_S$) is the input to the current-sense amplifier. To prevent the sense amplifier from seeing large common-mode switching voltages, the sense capacitor should always be connected to the nonswitching end of the inductor (i.e., the input of the step-up regulator).

Lossless current sense can be easily understood using complex frequency domain analysis. The voltage across the inductor is given by:

$$V_L = I_L(sL + R_L)$$

where L is the inductance, $R_L$ is the DCR of the inductor, and $I_L$ is the inductor current. The voltage across the sense capacitor is given by:

$$V_S = \frac{1}{1 + sR_SC_S}V_L$$

where $R_S$ is the series resistor in the sense network and $C_S$ is the sense capacitor. The above equation can be rewritten as:

$$V_S = \frac{sL + R_L}{1 + sR_SC_S}I_L = \frac{1 + sL/R_L}{1 + sR_SC_S}R_LI_L$$

If $\frac{L}{R_L} = R_SC_S$, then the equation becomes:

$$V_S = R_LI_L$$

Therefore, the sense capacitor voltage is directly proportional to the inductor current if the time constant of the RC sense network matches the time constant of the inductor/DCR. The sense method is equivalent to using a current-sense resistor that has the same value as the inductor DCR.

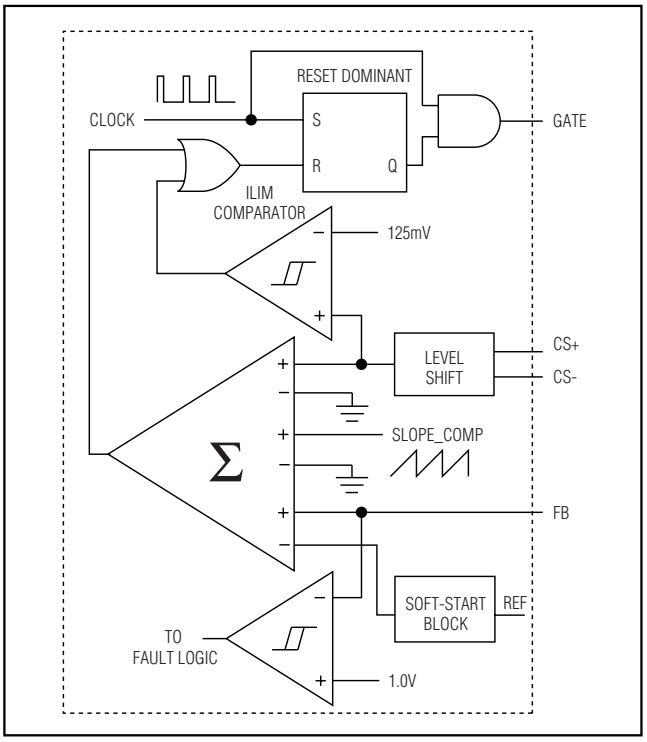



*Figure 4. Step-Up Regulator-Controller Functional Diagram*

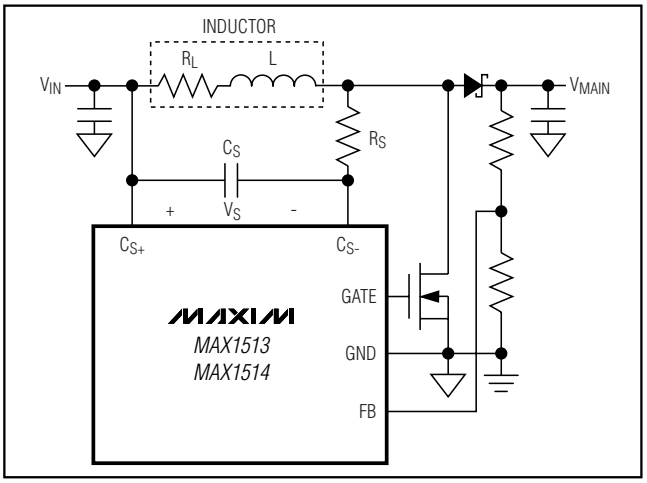



*Figure 5. Step-Up Regulator Using Lossless Current Sensing*

### Logic Linear-Regulator Controller

The logic linear-regulator controller (REG L) is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 680Ω base-to-emitter resistor (Figure 1). Its guaranteed base-drive sink current is at least 10mA. The regulator, including transistor Q1 in Figure 1, uses a 10µF ceramic output capacitor and is designed to deliver 500mA at 3.3V. Other output voltages and currents are possible by scaling the pass transistor, input capacitor, and output capacitor. See the *Pass-Transistor Selection* and *Stability Requirements* sections.

REG L is typically used to generate low-voltage logic supplies for the timing controller and the digital sections of the TFT-LCD source/gate-drive ICs.

REG L is automatically enabled when the input voltage is above the UVLO threshold. Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC in 128 steps.

### Gate-Off Linear-Regulator Controller

The gate-off linear-regulator controller (REG N) is an analog gain block with an open-drain P-channel output. It drives an external NPN pass transistor with a 3.6kΩ base-to-emitter resistor (Figure 1). Its guaranteed base-drive source current is at least 2mA. The regulator, including Q2 in Figure 1, uses a 0.47µF ceramic output capacitor and is designed to deliver 30mA at -10V. Other output voltages and currents are possible by scaling the pass transistor, input capacitor, and output capacitor. See the *Pass-Transistor Selection* and *Stability Requirements* sections.

REG N is typically used to provide the TFT-LCD gate drivers' gate-off voltage. A negative voltage can be produced using a charge-pump circuit as shown in Figure 1.

REG N is enabled after the logic linear-regulator REG L soft-start has completed. Each time it is enabled, the control goes through a soft-start routine that ramps down its internal reference DAC from $V_{REF}$ to 250mV in about 100 steps.

### Gate-On Linear-Regulator Controller

The gate-on linear-regulator controller (REG P) is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 1). Its guaranteed base-drive sink current is at least 1mA. The regulator including Q3 in Figure 1 uses a 0.47µF ceramic output capacitor and is designed to deliver 20mA at 25V. Other output voltages and currents are possible by scaling the pass transistor, input capacitor, and output capacitor. See the *Pass-Transistor Selection* and *Stability Requirements* sections.

REG P is typically used to provide the TFT-LCD gate drivers' gate-on voltage. Use a charge pump with as many stages as necessary to obtain a voltage exceeding the required gate-on voltage (see the *Selecting the Number of Charge-Pump Stages* section). Note that the voltage rating of the DRVP output is 28V. If the charge-pump output voltage can exceed 28V, an external cascode-connected NPN transistor should be added (Figure 6). Alternately, the linear regulator can control an intermediate charge-pump state while regulating the final charge-pump output (Figure 7).

REG P is enabled after the step-up regulator soft-start has completed and the voltage on DEL exceeds 1.25V. Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC in 128 steps.

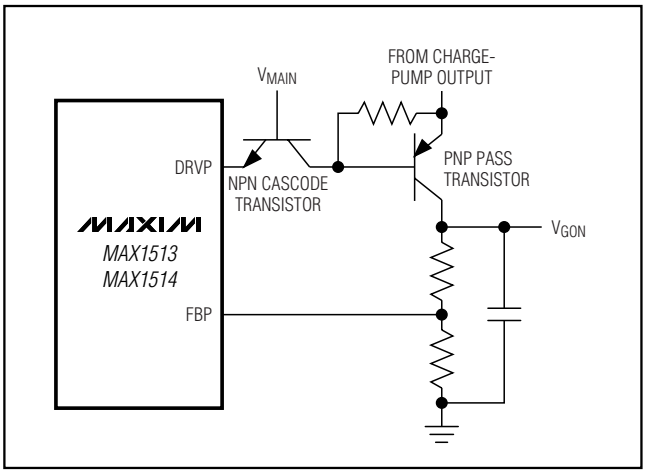



*Figure 6. Using an NPN Cascode for Charge-Pump Output Voltages > 28V*

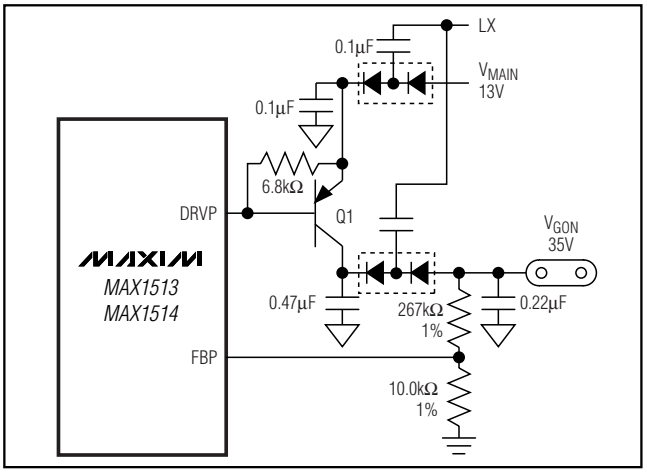



*Figure 7. Linear Regulator Controls Intermediate Charge-Pump Stage*

### Gamma Linear-Regulator Controller (MAX1513 Only)

The gamma linear-regulator controller REG G is an analog gain block with an open-drain N-channel output. It drives an external PNP pass transistor with a 1.5kΩ base-to-emitter resistor (Figure 1). Its guaranteed base-drive sink current is at least 5mA. The regulator, including Q4 in Figure 1, uses a 0.47µF ceramic output capacitor, and the controller is designed to deliver 40mA at 14.7V. Other output voltages and currents are possible by scaling the pass transistor, input capacitor, and output capacitor. See the *Pass-Transistor Selection* and *Stability Requirement*s sections.

REG G is typically used to provide the TFT-LCD gamma reference voltage, which is usually 0.3V below the source-drive supply voltage.

REG G is enabled 2.7ms after REG P's soft-start has completed. Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC in 128 steps.

### Buffer Amplifier (MAX1513 Only)

The MAX1513 includes a buffer amplifier that is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The buffer amplifier features ±150mA output short-circuit current, 10V/µs slew rate, and 12MHz bandwidth. The Rail-to-Rail® input and output capability maximizes its flexibility.

#### Short-Circuit Current Limit

The MAX1513's buffer amplifier limits short-circuit current to approximately ±150mA if the output is directly shorted to SUPB or to GND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled below $V_{UVLO}$.

#### Driving Pure Capacitive Load

The buffer amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the buffer amplifier. When driving a pure capacitive load, the amplifier's gain peaking increases. A 5Ω to 50Ω resistor placed between OUTB and the capacitive load reduces peaking.

### Undervoltage Lockout

The undervoltage-lockout (UVLO) circuit compares the voltage at the IN pin with the UVLO threshold (2.7V rising, 2.35V falling, typ) to ensure the input voltage is high enough for reliable operation. The 350mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, the IC is allowed to start. When the input voltage falls below the UVLO falling threshold, all the regulator outputs (including REF) are disabled until the input voltage exceeds the UVLO rising threshold.

### Reference Voltage (REF)

The reference output is nominally 1.25V and can source at least 100µA without degrading its accuracy (see the *Typical Operating Characteristics*). Bypass REF with a 0.22µF ceramic capacitor connected between REF and the analog ground plane (which connects to GND).

### Shutdown and Oscillator-Frequency Selection

The four-level logic input $\overline{SDFR}$ controls shutdown and oscillator-frequency selection. Connecting $\overline{SDFR}$ to ground shuts off all the regulator outputs except the logic linear-regulator controller (REG L), buffer amplifier, and REF. Connecting $\overline{SDFR}$ to IN sets the oscillator frequency to 1.5MHz. Connecting $\overline{SDFR}$ to REF sets the oscillator frequency to 750kHz. Leaving $\overline{SDFR}$ unconnected sets the oscillator frequency to 430kHz. When $\overline{SDFR}$ is left unconnected, bypass the pin to ground with a 1000pF to 0.1µF capacitor to prevent switching noise from coupling into the pin's high input impedance. Note the soft-start period and the fault-timer period do not change with the oscillator frequency.

### Power-Up Sequence and Delay Control Block

Once the voltage on IN exceeds the UVLO rising threshold (2.7V typ), the internal reference is enabled. With a 0.22µF REF bypass capacitor, the reference reaches its regulation voltage of 1.25V in approximately 1ms. When the reference voltage is ready, the MAX1513/MAX1514 enable the logic linear regulator. The MAX1513 also enables the buffer amplifier at the same time. Once the logic linear-regulator soft-start is completed, the MAX1513/MAX1514 enable the step-up regulator and REG N simultaneously. Once the soft-start of the step-up regulator is completed, the MAX1513/MAX1514 enable the delay control block. An internal 5µA current starts charging the timing capacitor on DEL. When the voltage on DEL reaches 1.25V, the MAX1513/MAX1514 enable REG P. With a 0.1µF capacitor on DEL, the DEL voltage reaches 1.25V in about 25ms. The MAX1513 enables the gamma linear regulator 2.7ms after the soft-start of REG P is completed.

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

### Soft-Start

Each positive regulator (step-up regulator, REG P, REG L, and REG G) includes a 7-bit soft-start DAC whose input is the reference, and whose output is stepped in 128 steps from zero up to the reference voltage. The soft-start DAC of the negative regulator (REG N) steps from the reference down to 250mV in about 100 steps. The outputs of the soft-start DACs determine the set points of each regulator. The soft-start duration is 2.7ms (typ) for each positive regulator and about 2.2ms for the negative regulator. The soft-start is independent of the selected operating frequency.

### Fault Protection

During steady-state operation, if the step-up regulator output or any of the linear-regulator outputs does not exceed its respective fault detection threshold, the MAX1513/MAX1514 activate an internal fault timer. If any condition or the combination of conditions indicates a continuous fault for the fault-timer duration (43.6ms typ), the MAX1513/MAX1514 set the fault latch, shutting down all the outputs except the reference. Once the fault condition is removed, toggle $\overline{SDFR}$ (below 0.4V) or cycle the input voltage (below 2.2V) to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time of each regulator.

### Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX1513/MAX1514. When the junction temperature exceeds +160°C, a thermal sensor immediately activates the fault-protection circuit, which shuts down all the outputs except the reference, allowing the device to cool down. Once the device cools down by approximately 15°C, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of $T_J$ = +150°C.

## Design Procedure

### Main Step-Up Regulator

#### Inductor Selection

The minimum inductance value, peak current rating, and DC series resistance (DCR) are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output voltage ripple. Size and cost are also important factors to consider.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and $I^2R$ losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increases size and can increase $I^2R$ losses in the inductor. Low inductance values decrease the size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant, LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and the ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once an inductor is chosen, higher and lower values for the inductor should be evaluated for efficiency improvements in typical operating regions.

Determine the inductor value and peak current requirement as follows:

Since the current delivered by charge pumps connected to LX adds to the inductor current, calculate the effective maximum output current, $I_{MAIN(EFF)}$:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{NEG} \times I_{NEG} + (n_{POS} + 1) \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum output current including any gamma-regulator current, $n_{NEG}$ is the number of negative charge-pump stages, $n_{POS}$ is the number of positive charge-pump stages, $I_{NEG}$ is the negative charge-pump output current, and $I_{POS}$ is the positive charge-pump output current, assuming the pump source for $I_{POS}$ is $V_{MAIN}$.

Calculate the approximate inductor value using the typical input voltage ($V_{IN}$), the expected efficiency ($\eta_{TYP}$)

taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above paragraphs:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2\left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage ($V_{IN(MIN)}$) using the following equation:

$$I_{IN(DC,\ MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

The expected efficiency at that operating point ($\eta_{MIN}$) can be taken from an appropriate curve in the *Typical Operating Characteristics.*

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX1513/MAX1514s' current limit ($I_{LIM}$) should exceed $I_{PEAK}$, and the inductor's DC current rating should exceed $I_{IN(DC,\ MAX)}$.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 400mA for $I_{MAIN}$ directly and 30mA for REG G to provide $V_{GAMMA}$. The one-stage negative charge pump provides 30mA to REG N for $V_{GOFF}$, and the one-stage positive charge pump provides 20mA to REG P for $V_{GON}$. Altogether, the effective maximum output current ($I_{MAIN(EFF)}$) is 500mA with a 15V output and a typical 5V input voltage. The switching frequency is set to 1.5MHz. Choosing an LIR of 0.6 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{5V}{15V}\right)^2\left(\frac{15V - 5V}{0.5A \times 1.5MHz}\right)\left(\frac{0.85}{0.6}\right) \approx 2.2\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,\ MAX)} = \frac{0.5A \times 15V}{4.5V \times 0.8} \approx 2.1A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{4.5V \times (15V - 4.5V)}{2.2\mu H \times 15V \times 1.5MHz} \approx 1.0A$$

$$I_{PEAK} = 2.1A + \frac{1.0A}{2} \approx 2.6A$$

The inductor DCR should be low enough for reasonable efficiency. As a rule of thumb, do not allow the voltage drop across the inductor DCR to exceed a few percent of the input voltage at $I_{PEAK}$.

Many notebook panel designs have height constraints on the components. If a thin inductor with the required current rating is not available, use two thin inductors in series or parallel.

### *Current-Sense Network Selection*

After selecting the inductor, use the following steps to design the current-sense network for lossless current sensing.

1) Calculate the RC time constant of the sense network using the typical inductance and typical DCR:

$$\tau = \frac{L}{R_{L(TYP)}}$$

2) Determine the component values of the sense network. Select $C_S$, and then calculate $R_S$ using:

$$R_S = \frac{\tau}{C_S}$$

3) Calculate the worst-case high sense voltage over temperature using the maximum DCR value ($R_{L(MAX)}$) found in the inductor technical specifications:

$$V_{SENSE} = I_{PEAK} \times R_{L(MAX)} \times (1 + TC \times \Delta T)$$

where $I_{PEAK}$ is the peak inductor current calculated in the *Inductor Selection* section, TC is the temperature coefficient of copper (0.5%/°C) and $\Delta T$ is the difference between the specified temperature for $R_{L(MAX)}$ and the maximum expected inductor temperature.

4) Compare the calculated sense voltage with the minimum value of the current-limit threshold in the *Electrical Characteristics* (100mV). If the sense voltage is between 80mV and 100mV, use the current-sense configuration in Figure 8 with the calculated $C_S$ and $R_S$ above.

5) If $V_{SENSE}$ is greater than 100mV, the current-feedback signal is too high and can trip the current limit before the full load current is delivered. Use the current-sense configuration in Figure 9 to attenuate the sense signal. Define the scale factor (SF) as:

$$SF = \frac{100mV}{V_{SENSE}}$$

Calculate $R_{S1}$ and $R_{S2}$:

$$R_{S1} = \frac{R_S}{SF}$$

$$R_{S2} = \frac{R_{S1} \times SF}{1 - SF}$$

6) If $V_{SENSE}$ is less than 80mV, the current-feedback signal is low relative to the current-limit threshold. Use the Figure 8 configuration, or, if good current-limit accuracy is desired, use the optional current-sense configuration in Figure 10 to increase the amplitude of the sense signal. Calculate $R_{S3}$ and $R_{S4}$:

$$R_{S3} = \frac{V_{MAIN} - V_{IN(MIN)}}{V_{MAIN} - V_{IN(MIN)} - 100mV + V_{SENSE}} \times R_S$$

$$R_{S4} = R_S - R_{S3}$$

If the 2.2µH inductor used in the typical operating circuit (Figures 1 and 2) had a typical DCR of 24mΩ and a maximum DCR of 30mΩ, the RC time constant of the sense network would be:

$$\tau = \frac{2.2\mu H}{24m\Omega} = 91.7\mu s$$

Select $C_S$ = 0.1µF and calculate $R_S$:

$$R_S = \frac{91.7\mu s}{0.1\mu F} = 917\Omega$$

Assuming ΔT is 40°C and TC is 0.5%, the worst-case high sense voltage over temperature is:

$$V_{SENSE} = 2.6A \times 30m\Omega \left(1 + 0.005 \times 40°C\right) = 93.6mV$$

Because $V_{SENSE}$ would be between 80mV and 100mV, the circuit in Figure 8 should be used. The closest 1% standard value for $R_S$ is 909Ω.

If the 2.2µH inductor used in the typical operating circuit (Figures 1 and 2) has a typical DCR of 45mΩ and a maximum DCR of 56mΩ, the RC time constant of the sense network is:

$$\tau = \frac{2.2\mu H}{45m\Omega} = 48.9\mu s$$

Select $C_S$ = 0.1µF and calculate $R_S$:

$$R_S = \frac{48.9\mu s}{0.1\mu F} = 489\Omega$$

Assuming ΔT is 40°C and TC is 0.5%, the worst-case high sense voltage over temperature is:

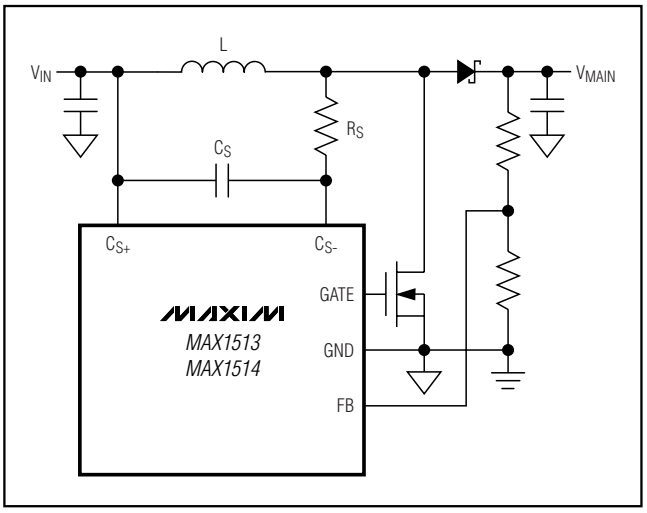



*Figure 8. Lossless Current Sensing with 80mV < $V_{SENSE}$ < 100mV*

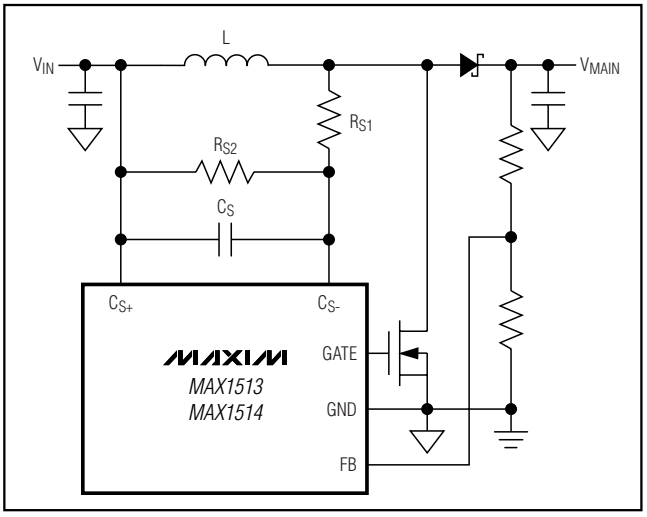



*Figure 9. Lossless Current Sensing with $V_{SENSE}$ > 100mV*

# TFT-LCD Power-Supply Controllers

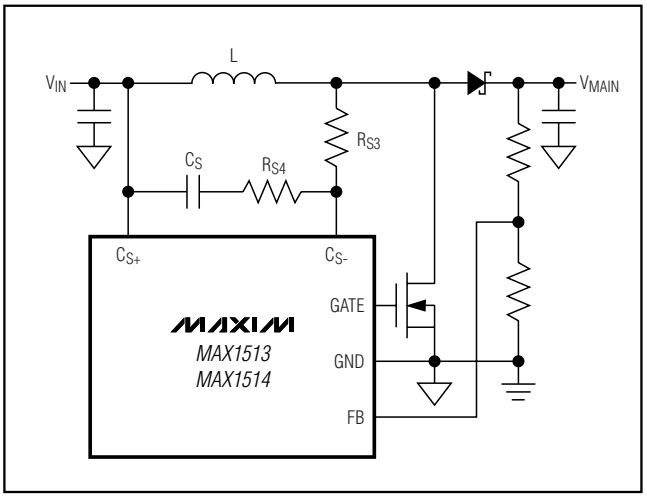



*Figure 10. Lossless Current Sensing with $V_{SENSE}$ < 80mV*

$$V_{SENSE} = 2.6A \times 56m\Omega\left(1 + 0.005 \times 40°C\right) = 175m\backslash$$

Because $V_{SENSE}$ would be greater than 100mV, the circuit in Figure 9 should be used and the scale factor is:

$$SF = \frac{100mV}{175mV} = 0.571$$

Calculate $R_{S1}$ and $R_{S2}$:

$$R_{S1} = \frac{489\Omega}{0.571} = 856\Omega$$

$$R_{S2} = \frac{856 \times 0.571}{1 - 0.571} = 1139\Omega$$

The closest 1% standard values for $R_{S1}$ and $R_{S2}$ are 866Ω and 1.13kΩ, respectively.

If the 2.2µH inductor used in the typical operating circuit (Figures 1 and 2) has a typical DCR of 10mΩ and a maximum DCR of 14mΩ, the RC time constant of the sense network is:

$$\tau = \frac{2.2\mu H}{10m\Omega} = 220\mu s$$

Select $C_S$ = 0.1µF, $R_S$ is:

$$R_S = \frac{220\mu s}{0.1\mu F} = 2200\Omega$$

Assuming ΔT is 40°C and TC is 0.5%, the worst-case high sense voltage over temperature is:

$$V_{SENSE} = 2.6A \times 14m\Omega \left(1 + 0.005 \times 40°C\right) = 44mV$$

Because $V_{SENSE}$ would be much less than 80mV, the circuit in Figure 10 can be used to improve the current-limit accuracy. Calculate $R_{S3}$ and $R_{S4}$:

$$R_{S3} = \frac{15V - 4.5V}{15V - 4.5V - 0.1V + 0.044V} \times 2600\Omega = 2614\Omega$$

$$R_{S4} = 2614\Omega - 2600\Omega = 14\Omega$$

The closest 1% standard values for $R_{S3}$ and $R_{S4}$ are 2.61kΩ and 14.0Ω, respectively.

### *Output-Capacitor Selection*

The output capacitor and its equivalent series resistance (ESR) affect the circuit's stability, output voltage ripple, and transient response. The *Output-Capacitor Stability Requirement* section discusses the output capacitance requirement based on the loop stability. This section deals with how to determine the output capacitance according to the ripple voltage and load-transient requirements.

The total output voltage ripple has two components: the ohmic ripple due to the capacitor's equivalent series resistance (ESR), and the capacitive ripple caused by the charging and discharging of the output capacitance:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} \times R_{ESR}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}} \times \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{OSC}}\right)$$

where $V_{MAIN}$ is the output voltage of the step-up regulator, $I_{MAIN}$ is the output current, $C_{OUT}$ is the output capacitance, $R_{ESR}$ is the ESR of the output capacitor, $f_{OSC}$ is the switching frequency, and $I_{PEAK}$ is the peak inductor current (see the *Inductor Selection* section).

In the circuits of Figures 1 and 2, the maximum total voltage ripple is 1% (peak-to-peak) of the 15V output, which corresponds to 150mV peak-to-peak ripple. A conservative way to calculate the maximum ESR and minimum capacitance is to assume the ESR ripple and the capacitive ripple each should not exceed 50% of the total ripple budget.

$$R_{ESR(MAX)} \le \frac{V_{RIPPLE(MAX)}}{2 \times I_{PEAK}}$$

$$C_{OUT(MIN)} \ge \frac{2 \times I_{MAIN}}{V_{RIPPLE(MAX)}} \times \left( \frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{OSC}} \right)$$

where $V_{RIPPLE(MAX)}$ is the total peak-to-peak output ripple. Since the peak inductor current calculated in the *Inductor Selection* section is 2.6A, the maximum ESR of the output capacitor should be less than 29mΩ. On the other hand, only 3.1µF capacitance is needed to meet the capacitive ripple requirement based on the calculation. A 10µF AQU-series POSCAP with maximum ESR of 20mΩ is selected for the typical operating circuits in Figures 1 and 2, which meets both the voltage-ripple and minimum capacitance requirements.

The typical load on the step-up regulator for source-driver applications is a large pulsed load, with a peak current of approximately 1A and a pulse width of approximately 2µs. The shape of the pulse is close to triangular, so it is equivalent to a square pulse with 1A height and 1µs pulse width. The total voltage dip during the pulsed load transient also has two components: the ohmic dip due to the output capacitor's ESR and the capacitive dip caused by discharging the output capacitance:

$$V_{DIP} = V_{DIP(ESR)} + V_{DIP(C)}$$

$$V_{DIP(ESR)} = I_{PULSE} \times R_{ESR}$$

$$V_{DIP(C)} \approx \frac{I_{PULSE} \times t_{PULSE}}{C_{OUT}}$$

where $I_{PULSE}$ is the height of the pulse load and $t_{PULSE}$ is the pulse width. Higher capacitance and lower ESR result in less voltage dip. Again, assume the ESR dip and the capacitive dip each should not exceed 50% of the total maximum allowed output-voltage dip caused by a load pulse ($V_{DIP(MAX)}$).

$$R_{ESR(MAX)} \le \frac{V_{DIP(MAX)}}{2 \times I_{PULSE}}$$

$$C_{OUT(MIN)} \ge \frac{2 \times I_{PULSE} \times t_{PULSE}}{V_{DIP(MAX)}}$$

For the typical load pulse described above, assuming the voltage dip must be limited to 200mV, the minimum output capacitor is 10µF, and the maximum ESR is 100mΩ.

The voltage rating and temperature characteristics of the output capacitor must also be considered.

### Input-Capacitor Selection

The input capacitor ($C_{IN}$) reduces the current peaks drawn from the input supply and reduces noise injection into the device. A 22µF ceramic capacitor is used in the typical operating circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, $C_{IN}$ can be reduced below the values used in the typical operating circuit. Ensure a low noise supply at IN by using adequate $C_{IN}$. Alternately, greater voltage variation can be tolerated on $C_{IN}$ if IN is decoupled from $C_{IN}$ using an RC lowpass filter (see R11 and C10 in Figure 1).

### Rectifier Diode

The MAX1513/MAX1514s' high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, use a Schottky diode with a current rating exceeding the peak inductor current calculated in the *Inductor Selection* section.

### Output-Voltage Selection

The output voltage of the main step-up regulator is adjustable by connecting a resistive voltage-divider from the output ($V_{MAIN}$) to the analog ground plane with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equations:

$$R1 = R2 \times \left( \frac{V_{MAIN}}{V_{FB}} - 1 \right)$$

where $V_{FB}$, the step-up regulator's feedback set point, is 1.25V. Connect the divider close to the IC.

### Output-Capacitor Stability Requirement

The step-up regulator controller of the MAX1513/MAX1514 uses a peak current-mode control method. The loop stability of a current-mode step-up regulator can be analyzed using a small-signal model. In continuous-conduction mode, the loop-gain transfer function consists of a DC loop gain, a dominant pole, a right-half-plane (RHP) zero and an ESR zero.

The DC loop gain ($A_{DC}$) is approximately:

$$A_{DC} = \frac{R2}{R1 + R2} \times \frac{1 - D}{0.554 \times R_{CS}} \times \frac{V_{MAIN}}{I_{MAIN(EFF)}}$$

where R1 and R2 are the feedback-divider resistors (Figure 1), D is the duty cycle, $I_{MAIN(EFF)}$ is the effective maximum output current as described in the *Inductor Selection* section, 0.554 is the gain of the current-sense amplifier, and $R_{CS}$ is the equivalent sense-resistor value given by:

$$R_{CS} = SF \times R_{L(TYP)}$$

where $R_{L(TYP)}$ is the typical value of the inductor DCR, and SF is either 1 or the scale factor in step 5 of the *Current-Sense Network Selection* section.

The frequency of the dominant pole is:

$$f_{P(DOMINANT)} = \frac{I_{MAIN(EFF)}}{2\pi \times V_{MAIN} \times C_{OUT}}$$

The frequency of the RHP zero is:

$$f_{Z(RHP)} = (1 - D)^2 \times \frac{V_{MAIN}}{2\pi \times L \times I_{MAIN(EFF)}}$$

The frequency of the ESR zero is:

$$f_{Z(ESR)} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

The unity-gain crossover frequency is:

$$f_{CROSSOVER} = A_{DC} \times f_{P(DOMINANT)}$$

For stable operation, select an output capacitor with enough capacitance and a low enough ESR to ensure that the dominant pole is low enough so the loop gain reaches unity well before either the ESR zero or the RHP zero, the lower of which should preferably occur at or above 5 times the unity-gain frequency as long as the two zeros are well separated. Calculate the minimum output capacitance for stable operation using:

$$C_{OUT(MIN)} = \frac{5 \times A_{DC} \times I_{MAIN(EFF)}}{2\pi \times \min\left[f_{Z(RHP)}, f_{Z(ESR)}\right] \times V_{MAIN}}$$

If the RHP zero and the ESR zero occur simultaneously, place the dominant pole so that the unity-gain frequency is less than 1/10th the frequency of the zeros. Calculate the minimum output capacitance for stable operation using:

$$C_{OUT(MIN)} = \frac{10 \times A_{DC} \times I_{MAIN(EFF)}}{2\pi \times f_Z \times V_{MAIN}}$$

where $f_Z$ is the frequency of the RHP zero and the ESR zero.

Using the typical operating circuit in Figure 1 as an example: the duty cycle is 0.67, the effective maximum output current is 500mA, the inductor is 2.2µH with a typical DCR of 24mΩ, and the output capacitor is 10µF with a maximum ESR of 20mΩ. The scale factor for the current-sense network is 1, so $R_{CS}$ is 24mΩ. The DC loop gain $A_{DC}$ is 62, the RHP zero is at 236kHz, and the ESR zero is at 796kHz. Since the frequency of the ESR zero is higher than that of the RHP zero, the unity-gain crossover frequency should be determined based on the RHP zero. The minimum output capacitance for stable operation is:

$$C_{OUT(MIN)} = \frac{5 \times 62 \times 500mA}{2\pi \times 236kHz \times 15V} \approx 6.97\mu F$$

Lead or lag compensation can be useful to compensate for particular component choices or to optimize the transient response for various output capacitor or inductor values.

Adding lead compensation (the R3/C1 network from $V_{MAIN}$ to FB in Figure 11) increases the loop bandwidth, which can increase the speed of response to transients. Too much speed can destabilize the loop and is not needed or recommended for Figure 1's components. Lead compensation adds a zero-pole pair, providing gain at higher frequencies and increasing loop bandwidth. The frequencies of the zero and pole for lead compensation depend on the feedback-divider resistors and the RC network between $V_{MAIN}$ and FB. The frequencies of the zero and pole for the lead compensation are:

$$f_{Z\_LEAD} = \frac{1}{2\pi \times (R1 + R3) \times C1}$$

$$f_{P\_LEAD} = \frac{1}{2\pi \times \left(R3 + \frac{R1 \times R2}{R1 + R2}\right) \times C1}$$

At high frequencies, R3 is effectively in parallel with R1, determining the amount of added high-frequency gain. If R3 is very large, there is no added gain and as R3 approaches zero, the added gain approaches the inverse of the feedback-divider's attenuation. A typical value for R3 is greater than 1/2 of R1. The value of C1

determines the frequency placement of the zero and pole. A typical value of C1 is between 100pF and 10nF. When adding lead compensation, always check the loop stability by monitoring the transient response to a pulsed output load.

Adding lag compensation (the R4/C2 network from FB to ground in Figure 11) decreases the loop bandwidth and improves FB noise immunity. Lag compensation slows the transient response but can increase the stability margin, which may be needed for particular component choice or high values of FB-divider resistors. Lag compensation adds a pole-zero pair, attenuating gain at higher frequencies and lowering loop bandwidth. The frequencies of the pole and zero for lag compensation depend on the feedback-divider resistors and the RC network between FB and GND. The frequencies of the pole and zero for the lag compensation are:

$$f_{P\_LAG} = \frac{1}{2\pi \times \left(R4 + \frac{R1 \times R2}{R1 + R2}\right) \times C2}$$

$$f_{Z\_LAG} = \frac{1}{2\pi \times R4 \times C2}$$

At high frequencies, R4 is effectively in parallel with R2, increasing the divider attenuation ratio. If R4 is very large, the attenuation ratio remains unchanged and as R4 approaches zero, the attenuation ratio approaches infinity. A typical value for R4 is greater than 0.1 times R2. If high-value divider-resistors are used, choose R4 < 1.5kΩ for FB noise immunity. The value of C2 determines the frequency placement of the pole and zero. A typical value of C2 is between 100pF and 1000pF. When adding lag compensation, always check the loop stability by monitoring the transient response to a pulsed output load.

### *Using Lead Compensation to Reduce Startup Inrush Current*

The digital soft-start of the main step-up regulator limits the average input current during startup. If even smoother startup is needed, add a low-frequency lead-compensation network (Figure 12). The improved soft-start is active only during soft-start when the output voltage rises. Positive changes in the output are instantaneously coupled to the FB pin through D1 and the feed-forward capacitor C1. This arrangement generates a smoothly rising output voltage. When the output voltage reaches regulation, capacitor C1 charges up through R3 and diode D1 turns off. If desired, C1 and R3 can be chosen to also provide some lead compensation in normal operation. In most applications, lead compensation in normal operation is not needed and can be avoided by making R3 large. With R3 much greater than R1, the pole and the zero in the compensation network are very close to one another after start-up and cancel out, eliminating the effect of the lead compensation. With R2 at 10kΩ, an effective value for C1 is approximately 1000pF.

### *Charge Pumps*

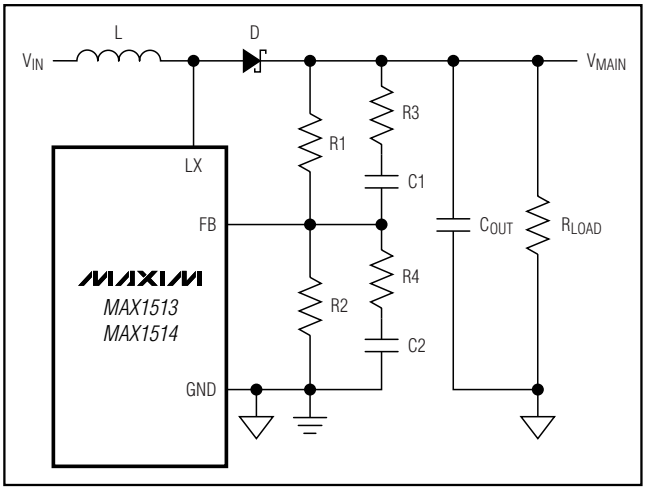



*Figure 11. Feedback Compensation*

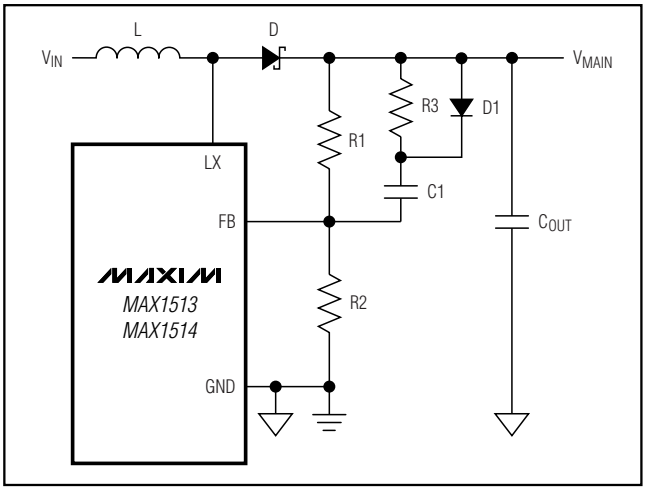



*Figure 12. Using Lead Compensation for Improved Soft-Start*

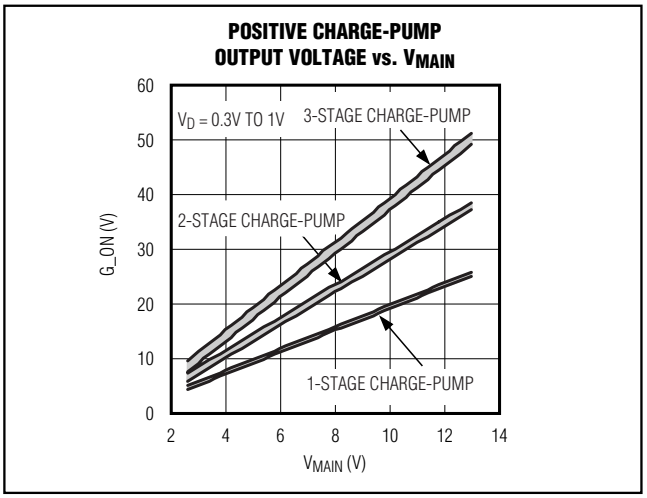



*Figure 13. Positive Charge-Pump Output Voltage vs. $V_{MAIN}$*

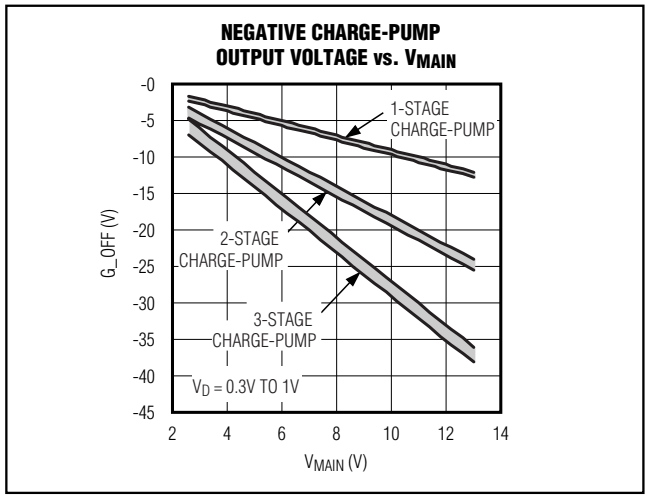



*Figure 14. Negative Charge-Pump Output Voltage vs. $V_{MAIN}$*

### *Selecting the Number of Charge-Pump Stages*

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output voltage requirement. Figures 13 and 14 show the positive and negative charge-pump output voltages for a given $V_{MAIN}$ for one-, two-, and three-stage charge pumps.

The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GON} + V_{DROPOUT} - V_{MAIN}}{V_{MAIN} - 2 \times V_D}$$

where $n_{POS}$ is the number of positive charge-pump stages, $V_{GON}$ is the gate-on linear-regulator REG P output, $V_{MAIN}$ is the main step-up regulator output, $V_D$ is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 0.3V.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{MAIN} - 2 \times V_D}$$

where $n_{NEG}$ is the number of negative charge-pump stages, $V_{GOFF}$ is the gate-off linear-regulator REG N output, $V_{MAIN}$ is the main step-up regulator output, $V_D$ is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 0.3V.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to $V_{MAIN}$ and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to $V_{IN}$ or another available supply. If the first charge-pump stage is powered from $V_{IN}$, then the above equations become:

$$n_{POS} = \frac{V_{GON} + V_{DROPOUT} - V_{IN}}{V_{MAIN} - 2 \times V_D}$$

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

### *Flying Capacitors*

Increasing the flying capacitor ($C_X$) value lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{MAIN}$$

where n is the stage number in which the flying capacitor appears, and $V_{MAIN}$ is the output voltage of the main step-up regulator.

### *Charge-Pump Output Capacitor*

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak voltage during load transients. With ceramic

capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} \geq \frac{I_{LOAD\_CP}}{2f_{OSC}V_{RIPPLE\_CP}}$$

where $C_{OUT\_CP}$ is the output capacitor of the charge pump, $I_{LOAD\_CP}$ is the load current of the charge pump, and $V_{RIPPLE\_CP}$ is the peak-to-peak value of the output ripple.

The charge-pump output capacitor is typically also the input capacitor for a linear regulator. Often, its value must be increased to maintain the linear regulator's stability.

#### *Charge-Pump Rectifier Diodes*

Use low-cost silicon switching diodes with a current rating equal to or greater than twice the average charge-pump input current. If their low forward voltage helps to avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with equivalent current ratings.

### *Linear-Regulator Controllers*

#### *Output-Voltage Selection*

Adjust the positive linear-regulator (REG P, REG L, and REG G) output voltages by connecting a resistive voltage-divider from their respective outputs to the analog ground plane (which connects to GND) with the center tap connected to FB_ (Figure 1). Select the lower resistor of the divider in the range of 10kΩ to 30kΩ. Calculate the upper resistor with the following equation:

$$R_{UPPER} = R_{LOWER} \times \left(\frac{V_{OUT\_}}{V_{FB\_}} - 1\right)$$

where $V_{OUT\_}$ is the output voltage of the respective linear regulator, and $V_{FB\_}$ = 1.25V (typ).

Adjust the gate-off linear-regulator REG N output voltage by connecting a resistive voltage-divider from $V_{GOFF}$ to REF with the center tap connected to FBN (Figure 1). Select R4 between 20kΩ and 50kΩ. Calculate R3 with the following equation:

$$R3 = R4 \times \left(\frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}\right)$$

where $V_{FBN}$ = 250mV, $V_{REF}$ = 1.25V. Note that REF can only source up to 50µA; using a resistor less than 20kΩ for R4 results in higher bias current than REF can supply without degrading REF accuracy.

#### *Pass-Transistor Selection*

The pass transistor must meet specifications for current gain ($h_{FE}$), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = \left(I_{DRV} - \frac{V_{BE}}{R_{BE}}\right) \times h_{FE(MIN)}$$

where $I_{DRV}$ is the minimum guaranteed base-drive current and $R_{BE}$ is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended unless needed to meet output-current requirements.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator supports. Also, the package's power dissipation limits the useable maximum power-dissipation capability of the transistor's package, and mounting must exceed the actual power dissipation in the device. The power dissipation equals the maximum load current ($I_{LOAD(MAX)\_LR}$) times the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)\_LR} \times \left(V_{IN(MAX)\_LR} - V_{OUT\_LR}\right)$$

where $V_{IN(MAX)\_LR}$ is the maximum input voltage of the linear regulator and $V_{OUT\_LR}$ is the output voltage of the linear regulator.

#### *Stability Requirements*

The MAX1513/MAX1514 linear-regulator controllers use an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability. The following applies equally to all linear regulators in the MAX1513 and MAX1514.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V\_LR} \approx \left(\frac{4}{V_T}\right) \times \left[1 + \left(\frac{I_{BIAS} \times h_{FE}}{I_{LOAD\_LR}}\right)\right] \times V_{REF}$$

where $V_T$ is 26mV at room temperature and $I_{BIAS}$ is the current through the base-to-emitter resistor ($R_{BE}$). Each of the four linear-regulator controllers is designed for a different maximum output current, so they have different output drive currents and different bias currents ($I_{BIAS}$). Each controller's bias current can be found in the *Electrical Characteristics* table. The current listed in the conditions column for the FB_ regulation voltage specification is the individual controller's bias current. The base-to-emitter resistor for each controller should be chosen to set the correct $I_{BIAS}$:

$$R_{BE} = \frac{V_{BE}}{I_{BIAS}}$$

The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, the pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system. The output capacitor's ESR generates a zero. For proper operation, use the following equations to verify the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE\_LR} = \frac{I_{LOAD(MAX)\_LR}}{2\pi \times C_{OUT\_LR} \times V_{OUT\_LR}}$$

The unity-gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V\_LR} \times f_{POLE\_LR}$$

2) The pole created by the internal amplifier delay is about 1MHz:

$$f_{POLE\_AMP} \approx 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance $C_{IN}$, the transistor's input resistance $R_{IN}$, and the base-to-emitter pullup resistor:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times \left(R_{BE} \,||\, R_{IN}\right)}$$

where $C_{IN} = \frac{g_m}{2\pi f_T}$, $R_{IN} = \frac{h_{FE}}{g_m}$,

$g_m$ is the transconductance of the pass transistor, and $f_T$ is the transition frequency. Both parameters can be found in the transistor's data sheet. Because $R_{BE}$ is much greater than $R_{IN}$, the above equation can be simplified:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times R_{IN}}$$

The equation can be further simplified:

$$f_{POLE\_IN} = \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the linear regulator's feedback resistance and the capacitance between FB_ and GND (including stray capacitance):

$$f_{POLE\_FB} = \frac{1}{2\pi \times C_{FB} \times \left(R_{UPPER} \,||\, R_{LOWER}\right)}$$

where $C_{FB}$ is the capacitance between FB_ and ground, $R_{UPPER}$ is the upper resistor of the linear regulator's feedback divider, and $R_{LOWER}$ is the lower resistor of the divider.

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{POLE\_ESR} = \frac{1}{2\pi \times C_{OUT\_LR} \times R_{ESR}}$$

where $R_{ESR}$ is the equivalent series resistance of $C_{OUT\_LR}$.

6) To ensure stability, choose $C_{OUT\_LR}$ large enough so the crossover occurs well before the poles and zero calculated in steps 2 to 5. The poles in steps 3 and 4 generally occur at several megahertz and using ceramic capacitors ensures the ESR zero occurs at several megahertz as well. Placing the crossover below 500kHz is sufficient to avoid the amplifier-delay pole and generally works well, unless unusual component choices or extra capacitances move the other poles or zero below 1MHz.

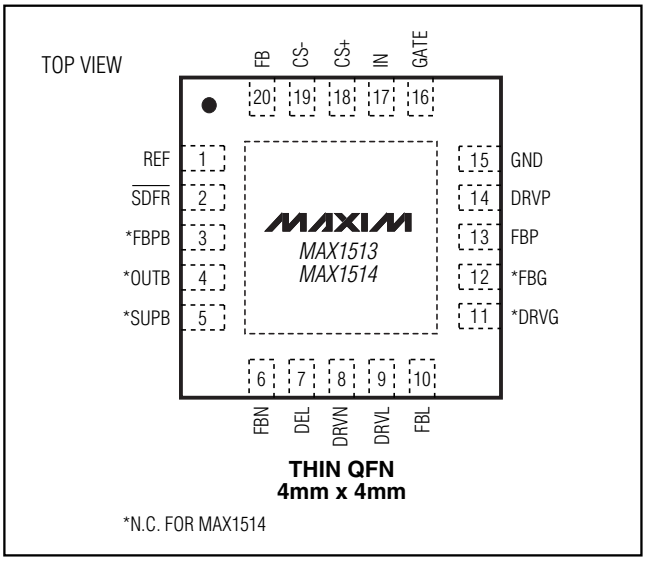
### PC Board Layout and Grounding

Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

1) Minimize the area of high-current loops. The high-current input loop goes from the positive terminals of the input capacitors to the inductor, to the power MOSFET, and to the negative terminals of the input capacitors. The high-current output loop is from the positive terminals of the input capacitors to the inductor, to the output diode, and to the positive terminals of the output capacitors, reconnecting between the output-capacitor and input-capacitor ground terminals. Connect these loops with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create a power ground plane consisting of the input and output-capacitor ground terminals, the source of the power MOSFET, and any ground terminals of the charge-pump components. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane consisting of the IC's backside pad, all the feedback-divider ground connections, the buffer-amplifier-divider ground connection, the REF capacitor ground connection, and the DEL capacitor ground connection. The power ground plane and the analog ground plane should be connected at only one location, which is the IC's GND pin. All other ground connections, such as the IN pin bypass capacitor and the linear-regulator output capacitors, should be star-connected directly to the backside pad of the IC through a via with wide traces, not otherwise connecting to either the power ground plane or the analog ground plane. Connect the IC's backside pad to the IC's GND pin. Make no other connections between the analog and power ground planes.
3) Place IN and REF bypass capacitors as close to the device as possible.
4) Place all feedback-voltage-divider resistors as close to their respective feedback pins as possible. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near the switching nodes in the step-up regulator and charge pumps.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the switching node while keeping it wide and short. Keep the switching node away from feedback nodes (FB, FBP, FBL, FBG, and FBN) and analog ground. Use DC traces to shield if necessary.

Refer to the MAX1513 evaluation kit for an example of proper board layout.

## Pin Configuration




## Chip Information

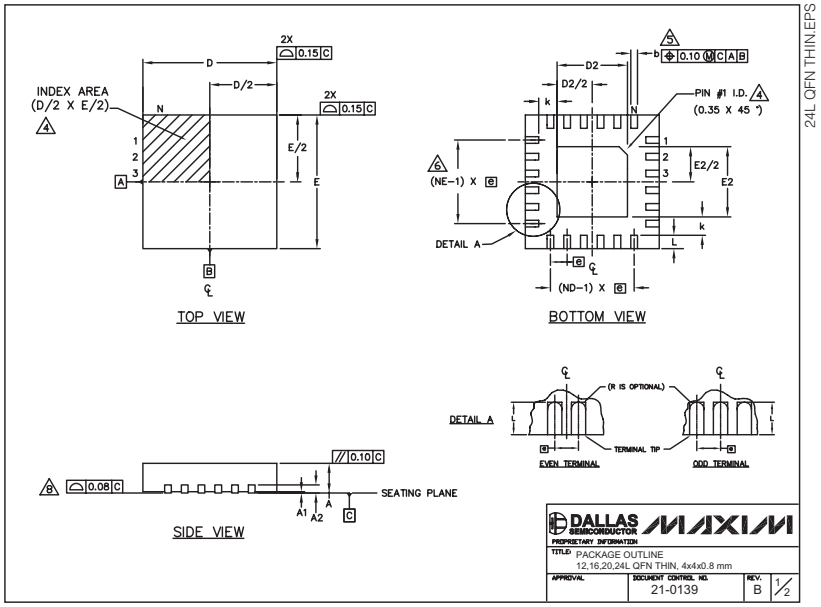
TRANSISTOR COUNT: 4807

PROCESS: BiCMOS

# TFT-LCD Power-Supply Controllers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




**COMMON DIMENSIONS**

| PKG | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | |
| Jedec Var. | WGGB | | | WGGC | | | WGGD-1 | | | WGGD-2 | | |

**EXPOSED PAD VARIATIONS**

| PKG. CODES | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1244-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-1 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-1 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0139
REV.
B
2/2