LTC2207/LTC2206

16-Bit, 105Msps/80Msps ADCs

FEATURES

- **Sample Rate: 105Msps/80Msps**
- **78.2dBFs Noise Floor**
- **100dB SFDR**
- **SFDR >83dB at 250MHz (1.5V_{P-P} Input Range)**
- **PGA Front End (2.25V_{P-P} or 1.5V_{P-P} Input Range)**
- **700MHz Full Power Bandwidth S/H**
- **Optional Internal Dither**
- **Optional Data Output Randomizer**
- Single 3.3V Supply
- Power Dissipation: 900mW/650mW
- Optional Clock Duty Cycle Stabilizer
- Out-of-Range Indicator
- Pin Compatible Family
  - 105Msps: LTC2207 (16-Bit), LTC2207-14 (14-Bit)
  - 80Msps: LTC2206 (16-Bit), LTC2206-14 (14-Bit)
- 48-Pin QFN Package

APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems
- ATE

DESCRIPTION

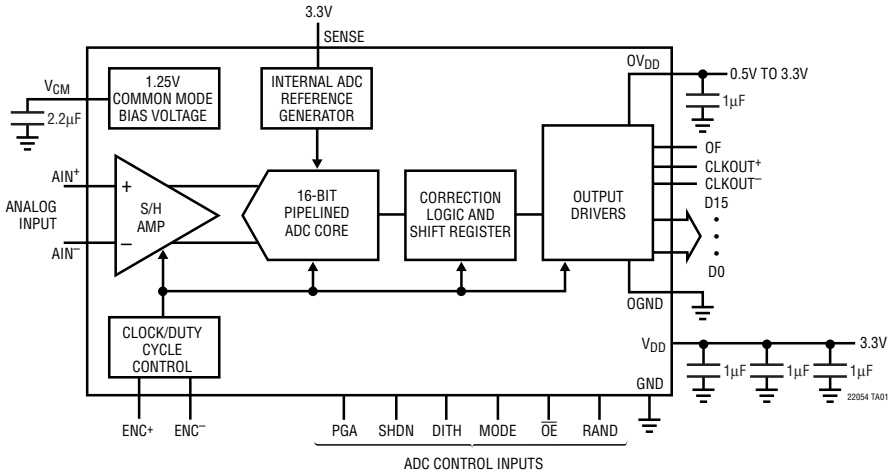
The LTC®2207/LTC2206 are 105Msps/80Msps, sampling 16-bit A/D converters designed for digitizing high frequency, wide dynamic range signals up to input frequencies of 700MHz. The input range of the ADC can be optimized with the PGA front end.

The LTC2207/LTC2206 are perfect for demanding communications applications, with AC performance that includes 78dB SNR and 100dB spurious free dynamic range (SFDR). Ultralow jitter of 80fs_{RMS} allows undersampling of high input frequencies with excellent noise performance. Maximum DC specs include ±4LSB INL, ±1LSB DNL (no missing codes) over temperature.

A separate output power supply allows the CMOS output swing to range from 0.5V to 3.3V.

The ENC+ and ENC– inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycle.

TYPICAL APPLICATION

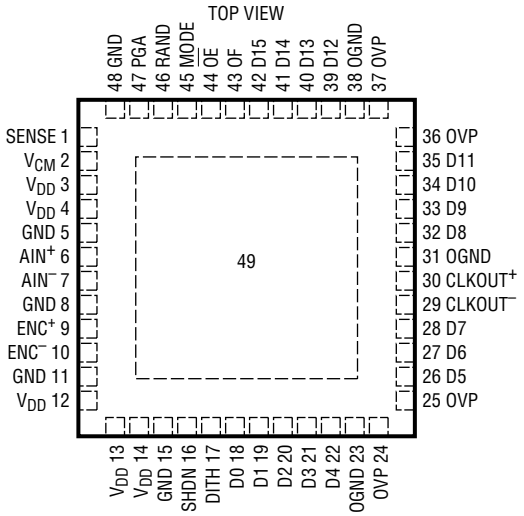


ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 4V
Digital Output Ground Voltage (OGND)..... –0.3V to 1V
Analog Input Voltage (Note 3) .....–0.3V to (V_{DD} + 0.3V)
Digital Input Voltage .....–0.3V to (V_{DD} + 0.3V)
Digital Output Voltage..... –0.3V to (OV_{DD} + 0.3V)
Power Dissipation..... 2000mW
Operating Temperature Range
LTC2207C/LTC2206C..... 0°C to 70°C
LTC2207I/LTC2206I ..... v40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Digital Output Supply Voltage (OV_{DD})..... –0.3V to 4V

PACKAGE/ORDER INFORMATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
EXPOSED PAD IS GND (PIN 49)
MUST BE SOLDERED TO PCB BOARD
T_{JMAX} = 125°C, θ_{JA} = 29°C/W

ORDER PART NUMBER	UK PART MARKING*
LTC2207CUK LTC2206CUK LTC2207IUK LTC2206IUK	LTC2207UK LTC2206UK LTC2207UK LTC2206UK

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult factory for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Integral Linearity Error	Differential Analog Input (Note 5)	●		±0.7	±4	LSB
Differential Linearity Error	Differential Analog Input	●		±0.3	±1	LSB
Offset Error	(Note 6)	●		±1	±5	mV
Offset Drift				±10		µV/°C
Gain Error	External Reference	●		±0.2	±1.0	%FS
Full-Scale Drift	Internal Reference External Reference			±30 ±15		ppm/°C ppm/°C
Transition Noise				2.8		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	3.135V ≤ V_{DD} ≤ 3.465V	●		1.5 to 2.25		V_{P-P}
$V_{IN, CM}$	Analog Input Common Mode	Differential Input (Note 7)	●	1	1.25	1.5	V
I_{IN}	Analog Input Leakage Current	0V ≤ A_{IN}^+, A_{IN}^- ≤ V_{DD}	●	–1		1	µA
I_{SENSE}	SENSE Input Leakage Current	0V ≤ SENSE ≤ V_{DD}	●	–1		1	µA
I_{MODE}	MODE Pin Pull-Down Current to GND				10		µA
C_{IN}	Analog Input Capacitance	Sample Mode $ENC^+ < ENC^-$ Hold Mode $ENC^+ > ENC^-$			6.5 1.4		pF
t_{AP}	Sample-and-Hold Acquisition Delay Time				–0.7		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				80		fs RMS
CMRR	Analog Input Common Mode Rejection Ratio	1V < ($A_{IN}^+ = A_{IN}^-$) <1.5V			80		dB
BW-3dB	Full Power Bandwidth				700		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC2206 MIN	LTC2206 TYP	LTC2206 MAX	LTC2207 MIN	LTC2207 TYP	LTC2207 MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			77.9 75.5			77.9 75.5		dBFS dBFS
		25MHz Input (2.25V Range, PGA = 0) 25MHz Input (1.5V Range, PGA = 1)	●	TBD	77.8 75.4		TBD	77.8 75.4		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			77.5 75.3			77.5 75.3		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 TBD	76.7 74.8		 TBD	76.7 74.8		dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			76.2 75.4			76.2 75.4		dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			100 100			100 100		dB dB
		25MHz Input (2.25V Range, PGA = 0) 25MHz Input (1.5V Range, PGA = 1)	●	TBD	95 100		TBD	95 100		dB dB
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			90 95			90 95		dB dB
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 TBD	85 90		 TBD	85 90		dB dB
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			82 86			82 86		dB dB
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			100 100			100 100		dB dB
		25MHz Input (2.25V Range, PGA = 0) 25MHz Input (1.5V Range, PGA = 1)	●	TBD	100 100		TBD	100 100		dB dB
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			100 100			100 100		dB dB
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 TBD	95 100		 TBD	95 100		dB dB
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			90 95			90 95		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC2206 MIN	LTC2206 TYP	LTC2206 MAX	LTC2207 MIN	LTC2207 TYP	LTC2207 MAX	UNITS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			77.9 75.5			77.9 75.5		dBFS dBFS
		25MHz Input (2.25V Range, PGA = 0) 25MHz Input (1.5V Range, PGA = 1)	●	TBD	77.8 75.4		TBD	77.8 75.4		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			77.1 75.2			77.1 75.2		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 TBD	75.6 74.5		 TBD	75.6 74.5		dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			74.4 73.9			74.4 73.9		dBFS dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS Dither "OFF"	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			105 105			105 105		dBFS dBFS
		25MHz Input (2.25V Range, PGA = 0) 25MHz Input (1.5V Range, PGA = 1)	●	TBD	105 105		TBD	105 105		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			105 105			105 105		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 TBD	100 100		 TBD	100 100		dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			100 100			100 100		dBFS dBFS
SFDR	Spurious Free Dynamic Range at –25dBFS Dither "OFF"	5MHz Input (2.25V Range, PGA = 0) 5MHz Input (1.5V Range, PGA = 1)			115 115			115 115		dBFS dBFS
		25MHz Input (2.25V Range, PGA = 0) 25MHz Input (1.5V Range, PGA = 1)	●	TBD	115 115		TBD	115 115		dBFS dBFS
		70MHz Input (2.25V Range, PGA = 0) 70MHz Input (1.5V Range, PGA = 1)			115 115			115 115		dBFS dBFS
		140MHz Input (2.25V Range, PGA = 0) 140MHz Input (1.5V Range, PGA = 1)	 ●	 TBD	110 110		 TBD	110 110		dBFS dBFS
		170MHz Input (2.25V Range, PGA = 0) 170MHz Input (1.5V Range, PGA = 1)			105 105			105 105		dBFS dBFS

COMMON MODE BIAS CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	1.15	1.25	1.35	V
V_{CM} Output Tempco	I_{OUT} = 0		±100		ppm/°C
V_{CM} Line Regulation	3.135V ≤ V_{DD} ≤ 3.465V		0.01		mV/V
V_{CM} Output Resistance	1mA ≤ | I_{OUT} | ≤ 1mA		2		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC+, ENC–)							
V_{ID}	Differential Input Voltage		●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)	 	 1.4	1.6 	 3.0	V
R_{IN}	Input Resistance	(See Figure 2)			6		kΩ
C_{IN}	Input Capacitance	(Note 7)			3		pF
LOGIC INPUTS (DITH, PGA, SHDN, RAND)							
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3.3V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 7)			1.5		pF
LOGIC OUTPUTS							
OV_{DD} = 3.3V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –10µA I_O = –200µA	 ●	 3.1	3.299 3.29	 	V V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 160µA I_O = 1.6mA	 ●	 	0.01 0.10	 0.4	V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3.3V			50		mA
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.60mA			0.1		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.3V, I_O = 1.60mA			0.1		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTC2206 MIN	LTC2206 TYP	LTC2206 MAX	LTC2207 MIN	LTC2207 TYP	LTC2207 MAX	UNITS
V_{DD}	Analog Supply Voltage		●	3.135	3.3	3.465	3.315	3.3	3.465	V
P_{SHDN}	Shutdown Power	SHDN = V_{DD}			2			2		mW
OV_{DD}	Output Supply Voltage		●	0.5		V_{DD}	0.5	3.3	V_{DD}	V
I_{VDD}	Analog Supply Current		●		194	214		257	280	mA
P_{DIS}	Power Dissipation		●		640	705		850	940	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC2206 MIN	LTC2206 TYP	LTC2206 MAX	LTC2207 MIN	LTC2207 TYP	LTC2207 MAX	UNITS
f_S	Sampling Frequency		●	1		80	1		105	MHz
t_L	ENC Low Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	5.94 4.06	6.25 6.25	500 500	4.52 3.10	4.762 4.762	500 500	ns ns
t_H	ENC High Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	5.94 4.06	6.25 6.25	500 500	4.52 3.10	4.762 4.762	500 500	ns ns
t_{AP}	Sample-and-Hold Aperture Delay				–0.7			–0.7		ns
t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.1	3.5	1.3	2.1	3.5	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1.3	2.1	3.5	1.3	2.1	3.5	ns
t_{SKEW}	DATA to CLKOUT Skew	(t_C-t_D) (Note 7)	●	–0.6	0	0.6	–0.6	0	0.6	ns
t_{OE}	DATA Access time Bus Relinquish time	CL = 5pF (Note 7) (Note 7)	● ●		5 5	15 15		5 5	15 15	ns ns
Pipeline Latency					7			7		Cycles

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND, with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 3.3V, f_{SAMPLE} = 105MHz (LTC2207), 80MHz (LTC2206) differential ENC^+/ENC^- = $2V_{P-P}$ sine wave with 1.6V common mode, input range = $2.25V_{P-P}$ with differential drive (PGA = 0), unless otherwise specified.

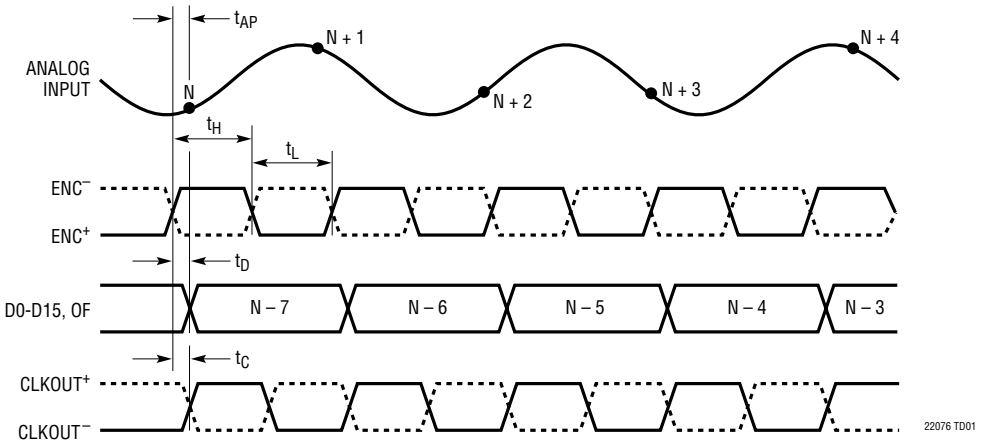
Note 5: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Offset error is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

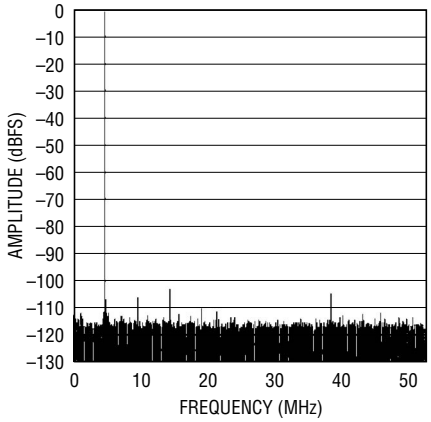
Note 8: Recommended operating conditions.

TIMING DIAGRAM



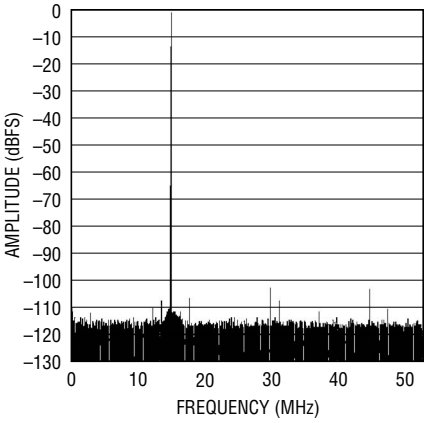
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2207: 64K Point FFT, f_{IN} = 4.8MHz, –1dB, PGA = 0



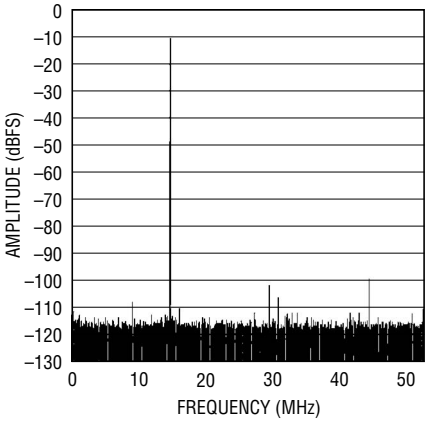
22076 G01

LTC2207: 64K Point FFT, f_{IN} = 14.8MHz, –1dB, PGA = 0



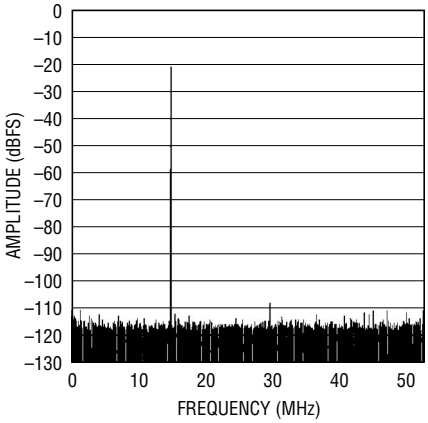
22076 G02

LTC2207: 64K Point FFT, f_{IN} = 14.8MHz, –10dB, PGA = 0



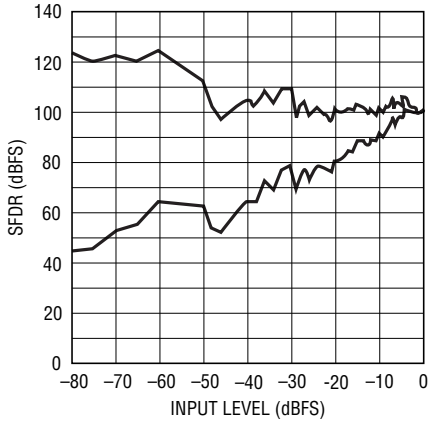
22076 G03

LTC2207: 64K Point FFT, f_{IN} = 14.8MHz, –20dB, PGA = 0



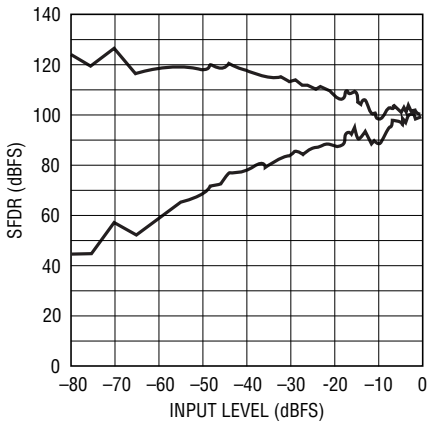
22076 G04

LTC2207: SFDR vs Input Level, f_{IN} = 15MHz, PGA = 0, Dither "Off"



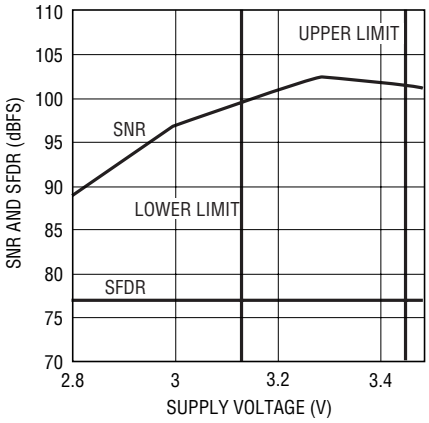
22076 G05

LTC2207: SFDR vs Input Level, f_{IN} = 15MHz, PGA = 0, Dither "On"



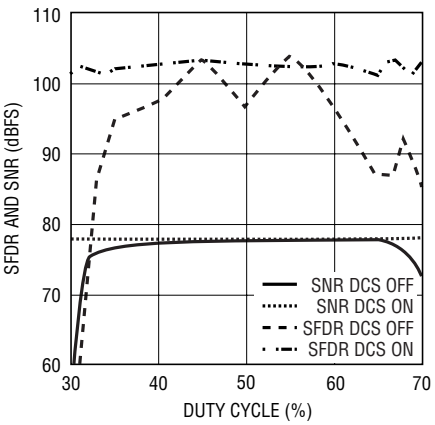
22076 G06

LTC2207: SNR and SFDR vs Supply Voltage (V_{DD}), f_{IN} = 5MHz



22076 G07

LTC2207: SNR and SFDR vs Duty Cycle



22076 G08

LTC2207: 32768 Point FFT, f_{IN} = 25.1MHz, –20dB, PGA = 0, DITH = 0, RAND = 0

PIN FUNCTIONS

SENSE (Pin 1): Reference Mode Select and External Reference Input. Tie SENSE to V_{DD} to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V (PGA = 0).

V_{CM} (Pin 2): 1.25V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2µF. Ceramic chip capacitors are recommended.

V_{DD} (Pins 3, 4, 12, 13, 14): 3.3V Analog Supply Pin. Bypass to GND with 0.1µF ceramic chip capacitors.

GND (Pins 5, 8, 11, 15, 48, 49): ADC Power Ground.

A_{IN}^+ (Pin 6): Positive Differential Analog Input.

A_{IN}^- (Pin 7): Negative Differential Analog Input.

ENC^+ (Pin 9): Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC^+. Internally biased to 1.6V through a 6.2kΩ resistor.

ENC^- (Pin 10): Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC^-. Internally biased to 1.6V through a 6.2kΩ resistor. Bypass to ground with a 0.1µF capacitor for a single-ended Encode signal.

SHDN (Pin 16): Power Shutdown Pin. SHDN = high results in normal operation. SHDN = low results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

DITH (Pin 17): Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

D0-D15 (Pins 18-22, 26-28, 32-35 and 39-42): Digital Outputs. D15 is the MSB.

OGND (Pins 23, 31 and 38): Output Driver Ground.

OV_{DD} (Pins 24, 25, 36, 37): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF capacitor.

$CLKOUT^-$ (Pin 29): Data Valid Output. $CLKOUT^-$ will toggle at the sample rate. Latch the data on the falling edge of $CLKOUT^-$.

$CLKOUT^+$ (Pin 30): Inverted Data Valid Output. $CLKOUT^+$ will toggle at the sample rate. Latch the data on the rising edge of $CLKOUT^+$.

OF (Pin 43): Over/Under Flow Digital Output. OF is high when an over or under flow has occurred.

$\overline{OE}$ (Pin 44): Output Enable Pin. Low enables the digital output drivers. High puts digital outputs in Hi-Z state.

MODE (Pin 45): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects straight binary output format and disables the clock duty cycle stabilizer. Connecting MODE to $1/3V_{DD}$ selects straight binary output format and enables the clock duty cycle stabilizer. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to V_{DD} selects 2's complement output format and disables the clock duty cycle stabilizer.

RAND (Pin 46): Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference.

PGA (Pin 47): Programmable Gain Amplifier Control Pin. Low selects a front-end gain of 1, input range of $2.25V_{P-P}$. High selects a front-end gain of 1.5, input range of $1.5V_{P-P}$.

GND (Exposed Pad, Pin 49): ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

BLOCK DIAGRAM

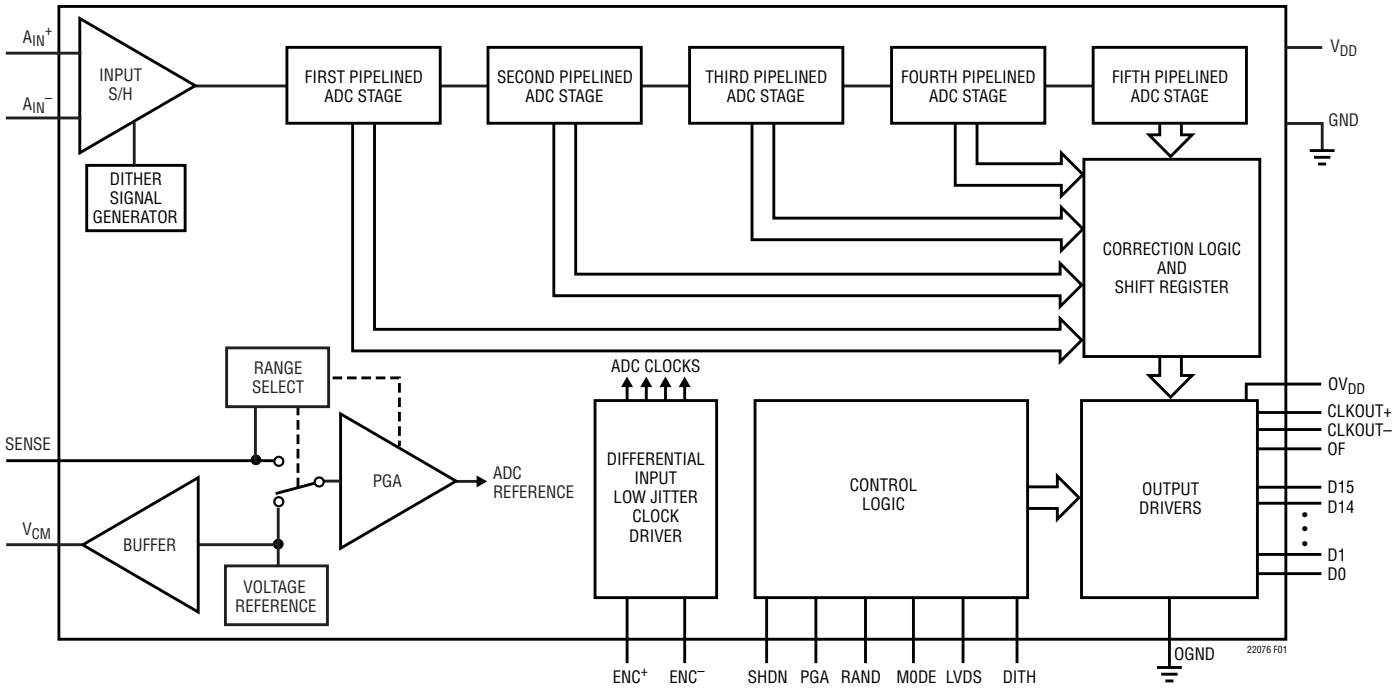


Figure 1. Functional Block Diagram

OPERATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = -20Log\sqrt{(V_2^2 + V_3^2 + V_4^2 + ... V_N^2)/V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through nth harmonics.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 3nd order IMD terms include (2fa + fb), (fa + 2fb), (2fa - fb) and (fa - 2fb). The 3rd order IMD is defined as the ration of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Spurious Free Dynamic Range (SFDR)

Spurious Free Dynamic Range is difference between the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibel relative to the RMS value of a full scale input signal.

Full Power Bandwidth

The Full Power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample-and-hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from convertion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20log\ (2\pi) \bullet f_{IN} \bullet t_{JITTER}$$

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2207/LTC2206 are CMOS pipelined multistep converters with a front-end PGA. As shown in Figure 1, the converter has five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagram section). The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample and hold circuit. The encode input is also differential for improved common mode noise immunity.

The LTC2207/LTC2206 have two phases of operation, determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the voltage on the sample capacitors is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H amplifier during the high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally delayed such that the results can be properly combined in the correction logic before being sent to the output buffer.

APPLICATIONS INFORMATION

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2207/LTC2206 CMOS differential sample and hold. The differential analog inputs are sampled directly onto sampling capacitors (C_{SAMPLE}) through NMOS transitors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the NMOS transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions for high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing ±0.5625V for the 2.25V range (PGA = 0) or ±0.375V for the 1.5V range (PGA = 1), around a common mode voltage of 1.25V. The V_{CM} output pin (Pin 3) is designed to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with 2.2µF or greater.

Input Drive Impedence

As with all high performance, high speed ADCs the dynamic performance of the LTC2207/LTC2206 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC the sample-and-hold circuit will connect the 4.9pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally, the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance it is recomended to have a source impedence of 100Ω or less for each input. The source impedence should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

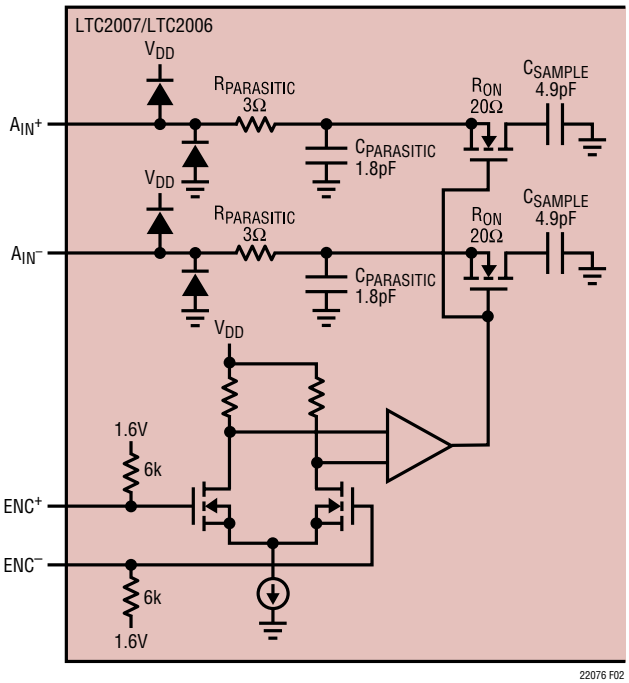


Figure 2. Equivalent Input Circuit

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

Input Filtering

A first order RC lowpass filter at the input of the ADC can serve two functions: limit the noise from input circuitry and provide isolation from ADC S/H switching. The LTC2207/LTC2206 have a very broadband S/H circuit, DC to 700MHz; it can be used in a wide range of applications; therefore, it is not possible to provide a single recommended RC filter.

Figures 3, 4a and 4b show three examples of input RC filtering at three ranges of input frequencies. In general it is desirable to make the capacitors as large as can be tolerated—this will help suppress random noise as well as noise coupled from the digital circuitry. The LTC2207/LTC2206 do not require any input filter to achieve data sheet specifications; however, no filtering will put more stringent noise requirements on the input drive circuitry.

Transformer Coupled Circuits

Figure 3 shows the LTC2207/LTC2206 being driven by an RF transformer with a center-tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used; however, as the turns ratio increases so does the impedance seen by the ADC. Source impedance greater than 50Ω can reduce the input bandwidth and increase high frequency distortion. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Center-tapped transformers provide a convenient means of DC biasing the secondary; however, they often show poor balance at high input frequencies, resulting in large 2nd order harmonics.

Figure 4a shows transformer coupling using a transmission line balun transformer. This type of transformer has much better high frequency response and balance than flux coupled center tap transformers. Coupling capacitors are added at the ground and input primary terminals to allow the secondary terminals to be biased at 1.25V. Figure 4b shows the same circuit with components suitable for higher input frequencies.

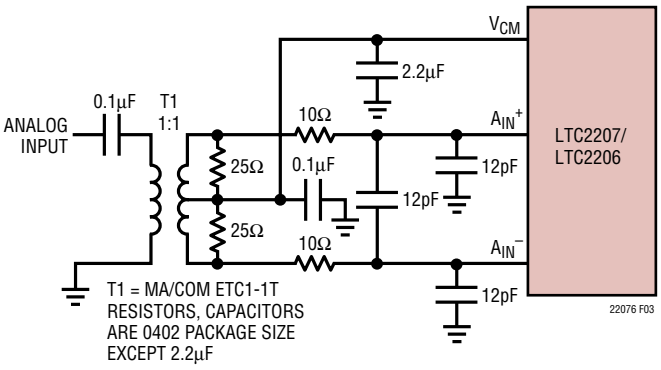


Figure 4a. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 50MHz to 250MHz

Figure 4b. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 250MHz to 500MHz

Figure 3. Single-Ended to Differential Conversion Using a Transformer. Recommended for Input Frequencies from 5MHz to 50MHz

APPLICATIONS INFORMATION

Direct Coupled Circuits

Figure 5 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of any op amp or closed-loop amplifier will degrade the ADC SFDR at high input frequencies. Additionally, wideband op amps or differential amplifiers tend to have high noise. As a result, the SNR will be degraded unless the noise bandwidth is limited prior to the ADC input.

Reference Operation

Figure 6 shows the LTC2207/LTC2206 reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. The LTC2207/LTC2206 have three modes of reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to V_{DD}. To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in a full scale range of $2.25V_{P-P}$ (PGA = 0). A 1.25V output, V_{CM} is provided for a common mode bias for input drive circuitry. An external bypass capacitor is required for the V_{CM} output. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference; it will not be stable without this capacitor. The minimum value required for stability is 2.2µF.

The internal programmable gain amplifier provides the internal reference voltage for the ADC. This amplifier has very stringent settling requirements and is not accessible for external use.

The SENSE pin can be driven ±5% around the nominal 2.5V or 1.25V external reference inputs. This adjustment range can be used to trim the ADC gain error or other system gain errors. When selecting the internal reference, the SENSE pin should be tied to V_{DD} as close to the converter as possible. If the sense pin is driven externally it should be bypassed to ground as close to the device as possible with 1µF (or larger) ceramic capacitor.

PGA Pin

The PGA pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of $2.25V_{P-P}$; PGA = 1 selects an input range of $1.5V_{P-P}$. The 2.25V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applications with high input frequencies, the low input range will have improved distortion; however, the SNR will be 1.8dB worse. See the typical performance curves section.

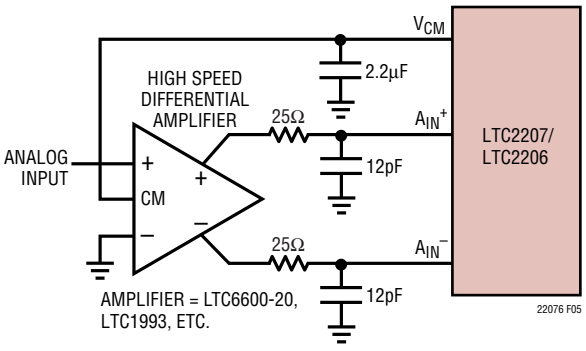


Figure 5. DC Coupled Input with Differential Amplifier

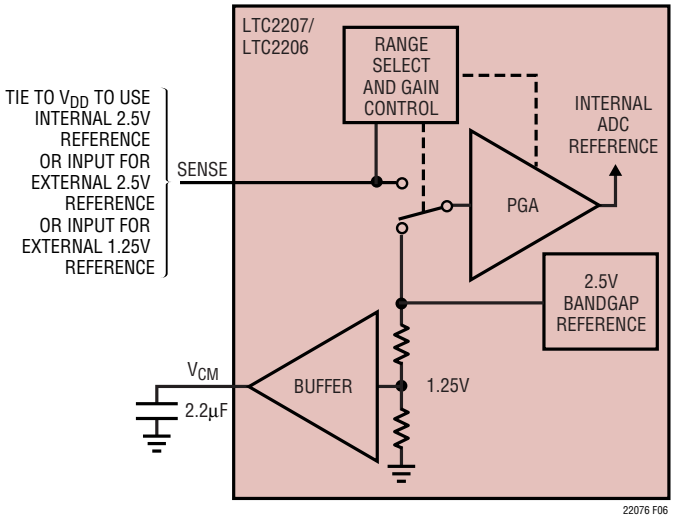


Figure 6. Reference Circuit

APPLICATIONS INFORMATION

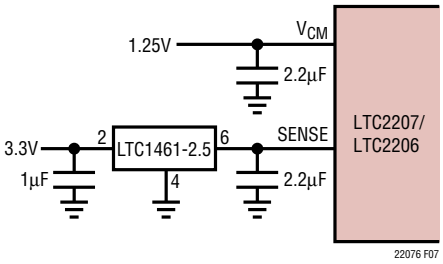


Figure 7. A 2.25V Range ADC with an External 2.5V Reference

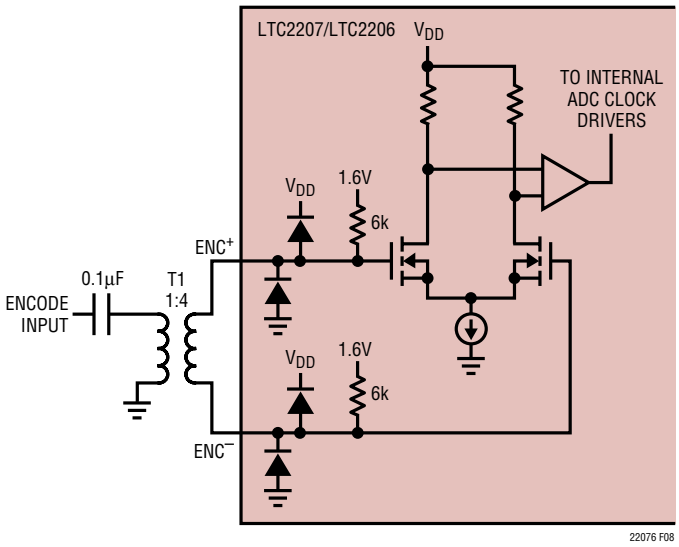


Figure 8. Transformer Driven Encode

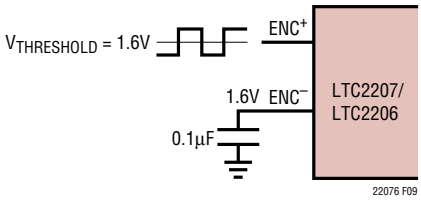


Figure 9. Single-Ended ENC Drive, Not Recommended for Low Jitter

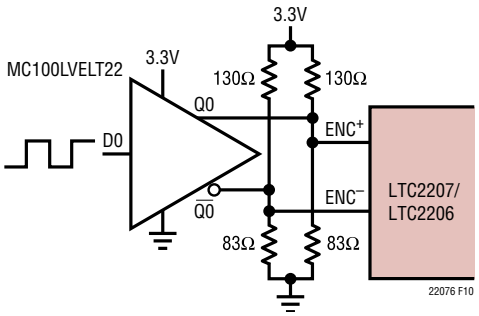


Figure 10. ENC Drive Using a CMOS to PECL Translator

APPLICATIONS INFORMATION

Driving the Encode Inputs

The noise performance of the LTC2207/LTC2206 can depend on the encode signal quality as much as for the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a fixed frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to V_{DD}. Each input may be driven from ground to V_{DD} for single-ended drive.

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC2207 is 105Msps. The maximum encode rate for the LTC2206 is 80Msps. For the ADC to operate properly the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 4.52ns for the LTC2207 internal circuitry to have enough settling time for proper operation. For the LTC2206, each half cycle must be at least 5.94ns. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS. When using a single-ended ENCODE signal asymmetric rise and fall times can result in duty cycles that are far from 50%.

An optional clock duty cycle stabilizer can be used if the input clock does not have a 50% duty cycle. This circuit uses the rising edge of ENC pin to sample the analog input. The falling edge of ENC is ignored and an internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin must be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2207/LTC2206 sample rate is determined by droop of the sample and hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2207/LTC2206 is 1Msps.

APPLICATIONS INFORMATION

DIGITAL OUTPUTS

Digital Output Buffers

Figure 11 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output eliminates the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2207/LTC2206 should drive a minimum capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as a ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the output buffer has a series resistor of 33Ω on chip.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Data Format

The LTC2207/LTC2206 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. This pin has a four level logic input, centered at 0, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD}. An external resistor divider can be user to set the $1/3V_{DD}$ and $2/3V_{DD}$ logic levels. Table 1 shows the logic states for the MODE pin.

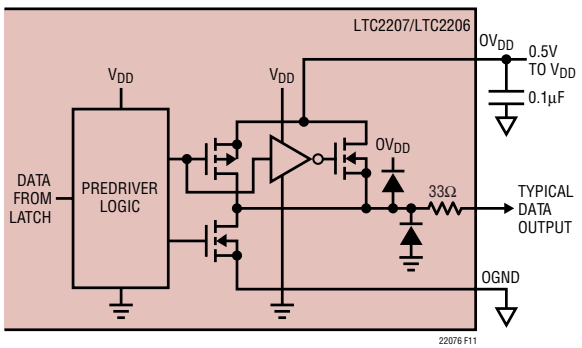


Figure 11. Equivalent Circuit for a Digital Output Buffer

Table 1. MODE Pin Function

MODE	Output Format	Clock Duty Cycle Stabilizer
0(GND)	Straight Binary	Off
$1/3V_{DD}$	Straight Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

An overflow output bit (OF) indicates when the converter is over-ranged or under-ranged. A logic high on the OF pin indicates an overflow or underflow.

Output Clock

The ADC has a delayed version of the encode input available as a digital output. Both a noninverted version, CLKOUT+ and an inverted version CLKOUT– are provided. The CLKOUT+/CLKOUT– can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. Data can be latched on the rising edge of CLKOUT+ or the falling edge of CLKOUT–. CLKOUT+ falls and CLKOUT– rises as the data outputs are updated.

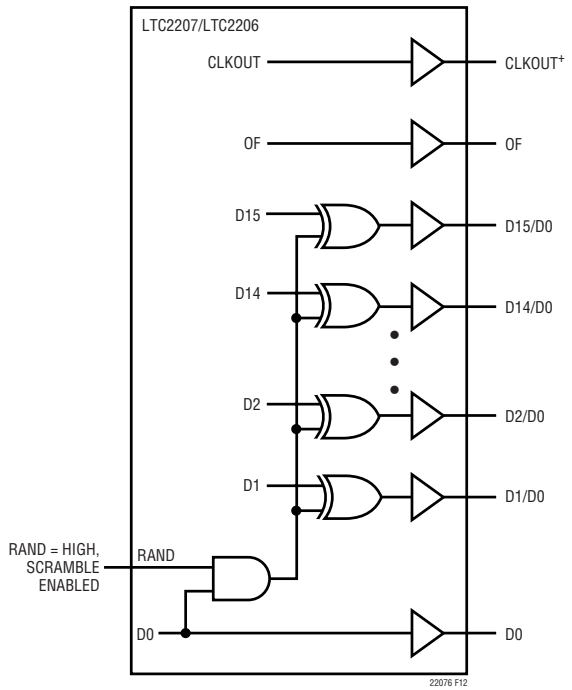


Figure 12. Functional Equivalent of Digital Output Randomizer

APPLICATIONS INFORMATION

Digital Output Randomizer

Interference from the ADC digital outputs is sometimes unavoidable. Interference from the digital outputs may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can result in discernible unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, trading a slight increase in the noise floor for a large reduction in unwanted tone amplitude.

The digital output is "Randomized" by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied; that is, an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output Randomizer function is active when the RAND pin is high.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example, if the converter is driving a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. In CMOS mode OV_{DD} can be powered with any logic voltage up to the V_{DD} of the ADC. OGND can be powered with any voltage from ground up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Internal Dither

The LTC2207/LTC2206 are 16-bit ADCs with very linear transfer functions; however, at low input levels even slight imperfections in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.

APPLICATIONS INFORMATION

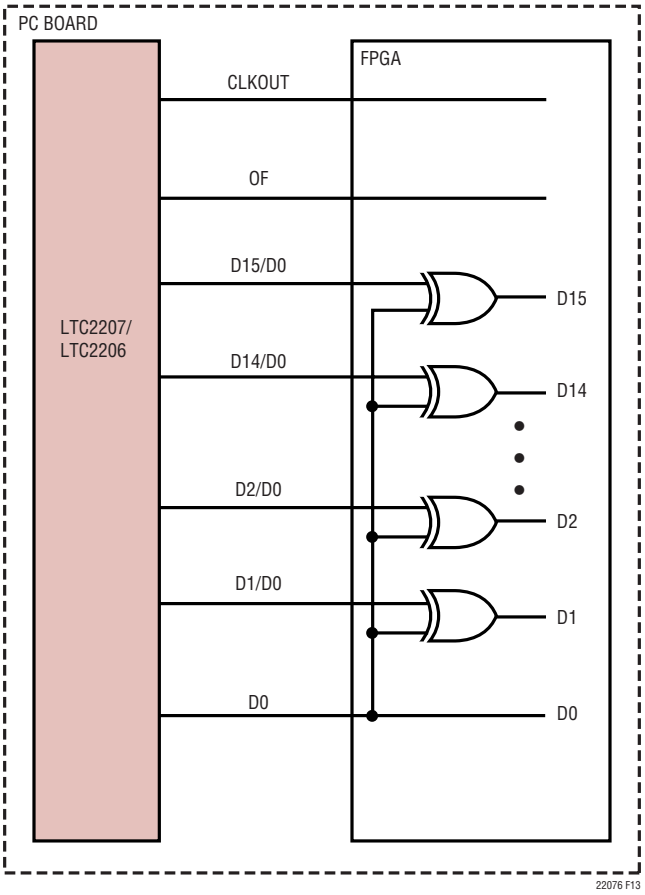


Figure 13. Descrambling a Scrambled Digital Output

APPLICATIONS INFORMATION

Grounding and Bypassing

The LTC2207/LTC2206 require a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTC2207/LTC2206 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, V_{CM}, and OV_{DD} pins. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

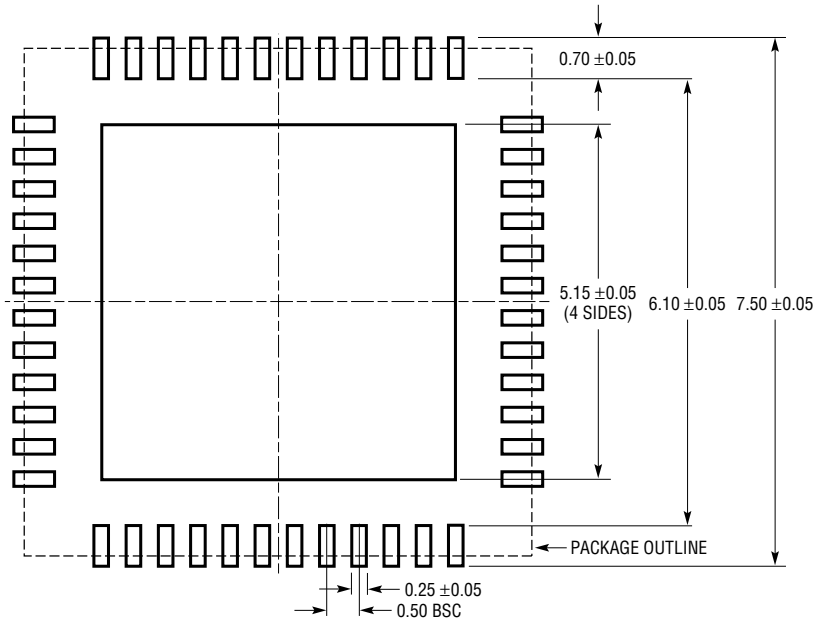
The LTC2207/LTC2206 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

Heat Transfer

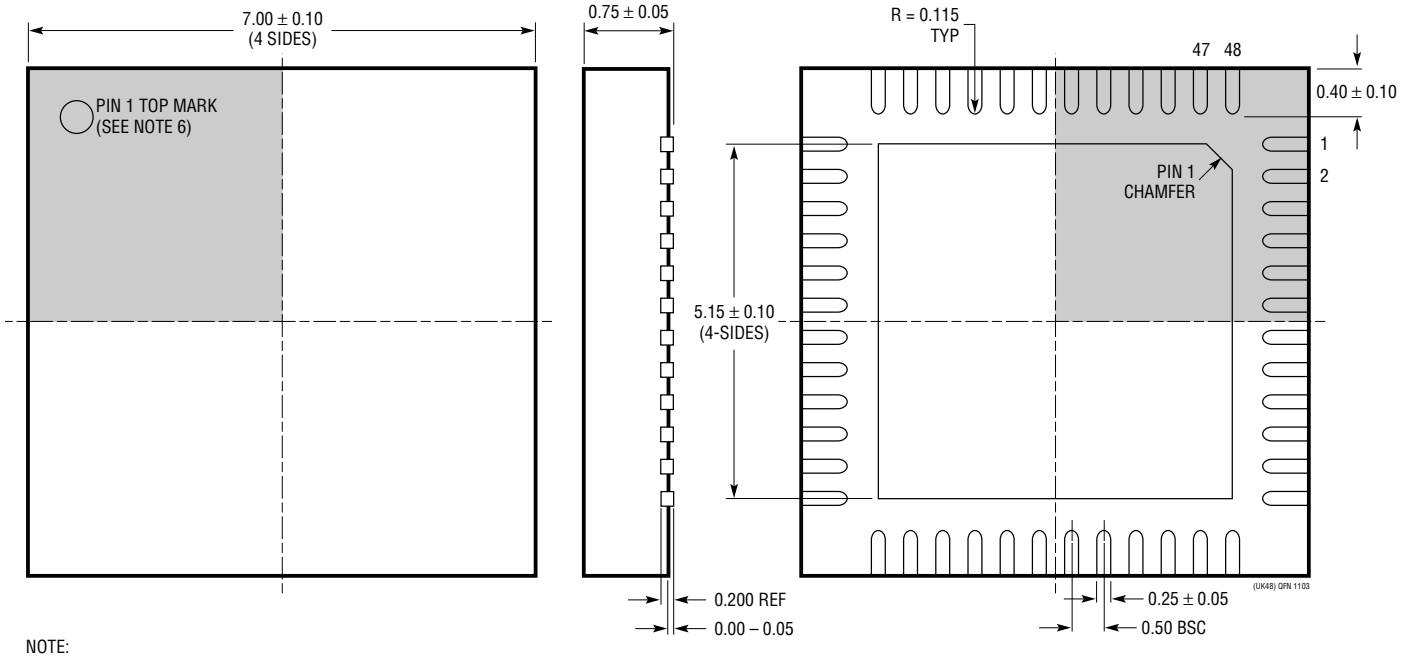
Most of the heat generated by the LTC2207/LTC2206 is transferred from the die through the bottom-side exposed pad. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. It is critical that the exposed pad and all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

PACKAGE DESCRIPTION

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1747	12-Bit, 80Msps ADC	72dB SNR, 87dB SFDR, 48-Pin TSSOP Package
LTC1748	14-Bit, 80Msps ADC	76.3dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1749	12-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 87dB SFDR
LTC1750	14-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 90dB SFDR
LTC1993	High Speed Differential Op Amp	600MHz BW, 75dBc Distortion at 70MHz
LTC2202	16-Bit, 10Msps ADC	150mW, 80dB SNR, 100dB SFDR
LTC2203	16-Bit, 25Msps ADC	250mW, 80dB SNR, 100dB SFDR
LTC2204	16-Bit, 40Msps ADC	350mW, 79dB SNR, 100dB SFDR
LTC2205	16-Bit, 65Msps ADC	450mW, 79dB SNR, 100dB SFDR
LTC2208	16-Bit, 130Msps ADC	1200mW, 78dB SNR, 100dB SFDR
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2220-1	12-Bit, 185Msps ADC	910mW, 67.5dB SNR, 9mm × 9mm QFN Package
LTC2249	14-Bit, 80Msps ADC	230mW, 73dB SNR, 5mm × 5mm QFN Package
LTC2250	10-Bit, 105Msps ADC	320mW, 61.6dB SNR, 5mm × 5mm QFN Package
LTC2251	10-Bit, 125Msps ADC	395mW, 61.6dB SNR, 5mm × 5mm QFN Package
LTC2252	12-Bit, 105Msps ADC	320mW, 70.2dB SNR, 5mm × 5mm QFN Package
LTC2253	12-Bit, 125Msps ADC	395mW, 70.2dB SNR, 5mm × 5mm QFN Package
LTC2254	14-Bit, 105Msps ADC	320mW, 72.5dB SNR, 5mm × 5mm QFN Package
LTC2255	14-Bit, 125Msps ADC	395mW, 72.4dB SNR, 5mm × 5mm QFN Package
LTC2299	Dual 14-Bit, 80Msps ADC	230mW, 71.6dB SNR, 5mm x 5mm QFN Package
LTC5512	DC-3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LTC5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer 10.5dB to 33dB in 1.5dB/Step
LTC5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/TP 0805 500 • PRINTED IN USA