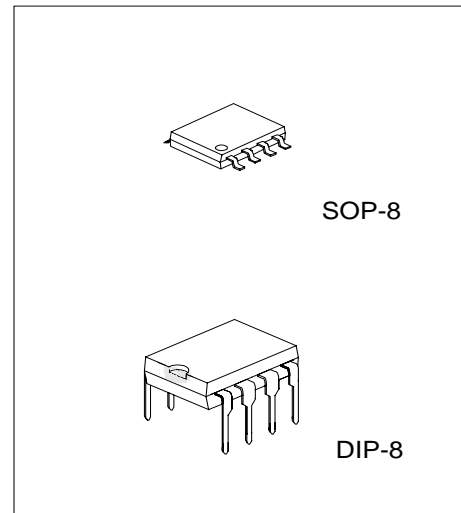# UNISONIC TECHNOLOGIES CO.,LTD

UA2311

16 BITS DIGITAL to ANALOG CONVERTER

■ **DESCRIPTION**

UTC **UA2311** is a 16-bits Digital-to-Analog Converter(DAC) designed for stereo audio applications and manufactured by CMOS Technologies with low power consumption It converts the 16 bits serial data into an analog output voltage by an R-string voltage divider. Each output channel voltage is driven by an operational amplifier allowing easy analog output. In sound cards test, the 44.1KHz or higher sampling rate is available.

SOP-8

DIP-8

*Pb-free plating product number: UA2311L

■ **FEATURES**

* CMOS Technology
* Low Power Consumption
* Two Voltage Output Channels in the same chip
* 16-bits Dynamic Range
* Low Total Harmonic Distortion
* 5V(typ.) Single Power Supply

■ **PIN DESCRIPTION**

PIN NO	PIN NAME	DESCRIPTION
1	BCK	Bit Clock Input
2	WS	Word Select Input
3	DATA	Data Input
4	GND	Ground
5	V_{DD}	Positive Power Supply
6	V_{OL}	Left Channel Output
7	NC	Not Connected
8	V_{OR}	Right Channel Output

■ **ORDERING INFORMATION**

Ordering Number		Package	Packing
Normal	Lead Free Plating		
UA2311-S08-R	UA2311L-S08-R	SOP-8	Tape Reel
UA2311-S08-T	UA2311L-S08-T	SOP-8	Tube
UA2311-D08-T	UA2311L-D08-T	DIP-8	Tube

■ **PIN CONFIGURATION**

BCK	1		8	V$_{OR}$
WS	2		7	NC
DATA	3		6	V$_{OL}$
GND	4		5	V$_{DD}$
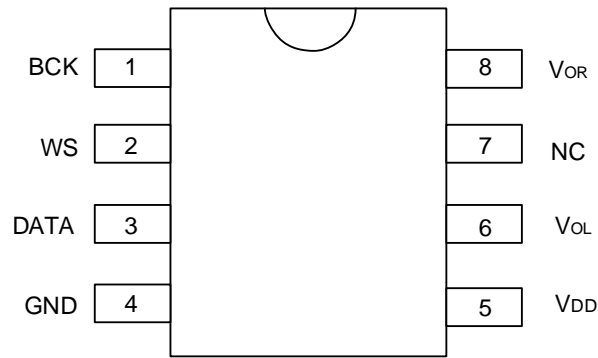
■ **BLOCK DIAGRAM**
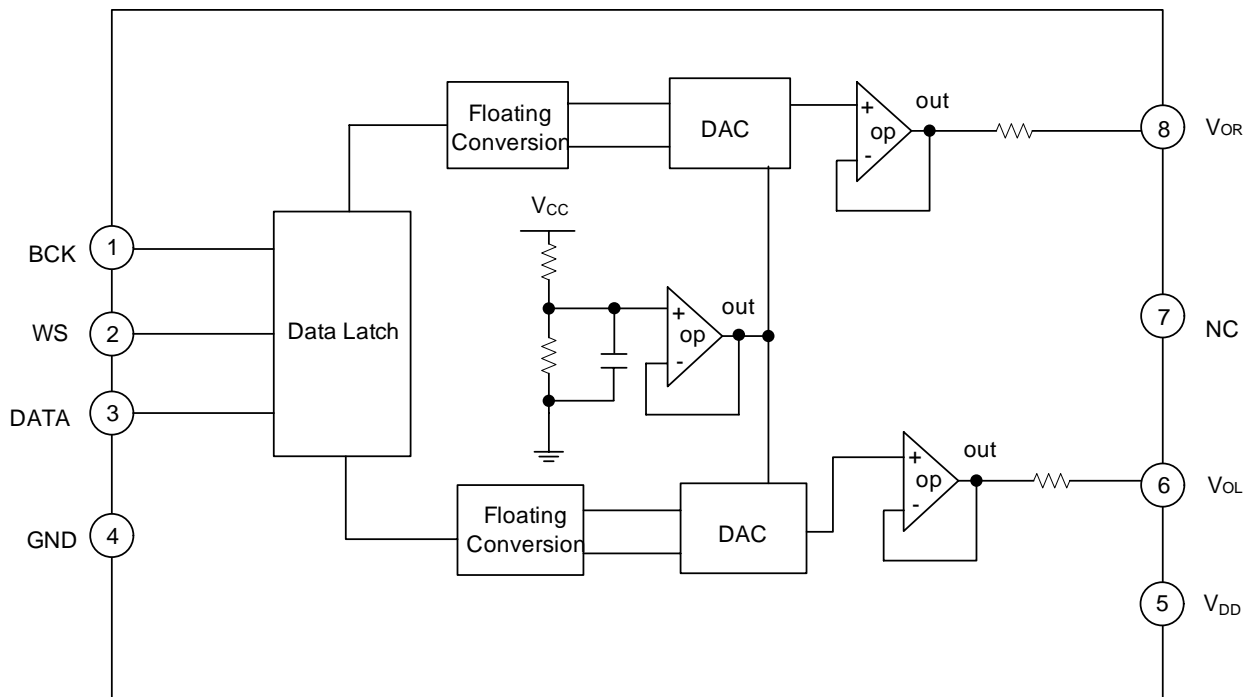
■ **ABSOLUTE MAXIMUM RATING**

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	-3.0 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0 ~ +70	℃
Storage Temperature	T_{STG}	-40 ~ +150	℃

Note: 1. The typical power supply voltage propose at 5V, and range from 4.75V~6V is recommended.
   2. Operating temperature range between 0~+50℃ is strongly recommended, Ta=25 is typical.

■ **ELECTRICAL CHARACTERISTICS**

DC CHARACTERISTICS (Ta=0 ~ 70℃, V_{DD}=5.0 ± 0.25V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Level	High	V_{IH}	Note	$0.66V_{DD}$			V
	Low	V_{IL}	Note			$0.30V_{DD}$	
Input Leakage Current		$I_{IN(LEAK)}$	Note			0.1	μA
Input Capacitance		C_{IN}	Note			5	pF
Power Consumption		W	V_{DD}=5.0V		30		mW
Clock Frequency		fc			5.6448	18.4	MHz

Note: Applicable to BCK, WS & DATA.

ANALOG CHARACTERISTICS (Ta=25℃, V_{DD}=5.0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Output Amplitude	V_{OUT}			2.5		V_{pp}
Total Harmonic Distortion (Note 1)	THD	1KHz, 0dB		0.13		%
Dynamic Range	DR			16		bit
Signal-to-Noise Ratio (Note 2)	S/N	1KHz, 0dB		82		dB
Cross Talk (Note 2)	CT	1KHz, 0dB		-85		dB

Note 1. Measured with 176.4KHz sampling rate, 2K~ 20K Harmonics
   2. Measured with an A/D & D/A Evaluation Board at sampling rate of 48KHz.

TIMING CHARACTERISTICS (refer to Figure 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High Level Time	t_H	25			ns
Rise Time	t_R			20	ns
Fall Time	t_F			20	ns

■ FUNCTIONAL DESCRIPTION

The UTC **UA2311** accepts serial input data format of 16-bits word length. Both left and right data words are time multiplexed. The last 16 bits word before "WS" changes is recognized as the input data. The timing and input signal formats are shown in Figure 1 and 2.

The most significant bit (bit 1) must always be first. The serial input data is shifted and latched for the Right and Left Channels. With a HIGH level on the word select input (WS), data is placed in the left input register and with a LOW level on the WS input, data is placed in the right input register(see Block Diagram). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

The 16 bits Right/Left Data is then converted to floating point expression whose format consists of 10 bits mantissa and 7 step exponent. This floating point expression is then converted to analog output voltage by the resistor-string. This signal is driven to the Right/Left Channel (V_{OR}/V_{OL}) by the buffer operational amplifier.
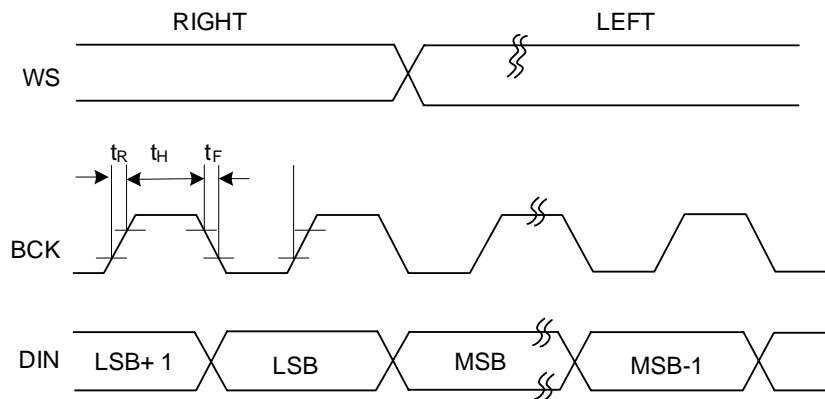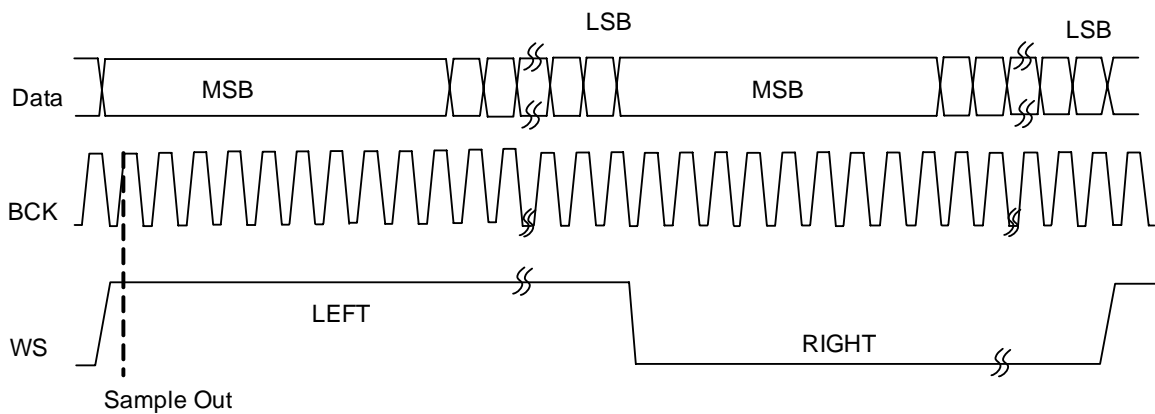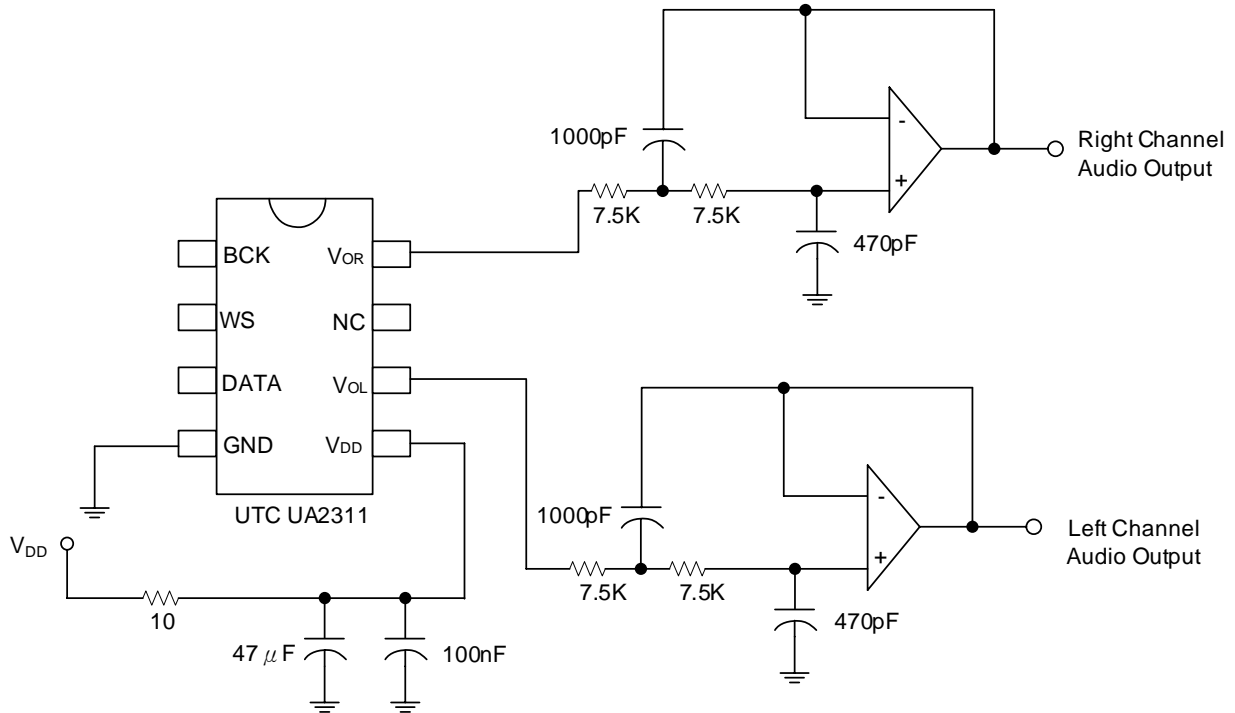
Figure.1 Input Signal Format

Figure.2 Timing and Input Signal Formats

■ **APPLICATION CIRCUIT**

A typical example of CD-ROM application is showed as below. It features typical decoupling components and a second-order analog post-filter stage providing a line output.