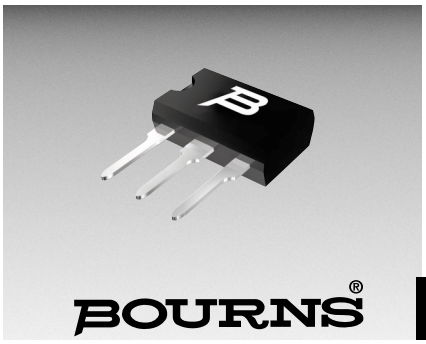

BOURNS®

TISP3070H3SL THRU TISP3115H3SL, TISP3125H3SL THRU TISP3210H3SL, TISP3250H3SL THRU TISP3350H3SL

DUAL BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP3xxxH3SL Overvoltage Protector Series

TISP3xxxH3SL Overview

This TISP® device series protects central office, access and customer premise equipment against overvoltages on the telecom line. The TISP3xxxH3SL protects R-G and T-G. In addition, the device is rated for simultaneous R-G and T-G impulse conditions. The TISP3xxxH3SL is available in a wide range of voltages and has a high current capability, allowing minimal series resistance to be used. These protectors have been specified mindful of the following standards and recommendations: GR-1089-CORE, FCC Part 68, UL1950, EN 60950, IEC 60950, ITU-T K.20, K.21 and K.45. The TISP3350H3SL meets the FCC Part 68 "B" ringer voltage requirement and survives both Type A and B impulse tests. These devices are housed in a through-hole 3-pin single-in-line (SL) plastic package.

Summary Electrical Characteristics

Part #	V_{DRM} V	$V_{(BO)}$ V	V_T @ I_T V	I_{DRM} µA	$I_{(BO)}$ mA	I_T A	I_H mA	C_o @ -2 V pF	Functionally Replaces
TISP3070H3	58	70	3	5	600	5	150	140	P1402AC†
TISP3080H3	65	80	3	5	600	5	150	140	P1602AC†
TISP3095H3	75	95	3	5	600	5	150	140	
TISP3115H3	90	115	3	5	600	5	150	74	P2202AC†
TISP3125H3	100	125	3	5	600	5	150	74	
TISP3135H3	110	135	3	5	600	5	150	74	
TISP3145H3	120	145	3	5	600	5	150	74	P2702AC†
TISP3180H3	145	180	3	5	600	5	150	74	P3002AC
TISP3210H3	160	210	3	5	600	5	150	74	P3602AC†
TISP3250H3	190	250	3	5	600	5	150	62	P4202AC
TISP3290H3	220	290	3	5	600	5	150	62	P4802AC†
TISP3350H3	275	350	3	5	600	5	150	62	P6002AC

† Bourns part has an improved protection voltage

Summary Current Ratings

Parameter	I_{TSP} A						I_{TSM} A	di/dt A/µs
Waveshape	2/10	1.2/50, 8/20	10/160	5/320	10/560	10/1000	1 cycle 60 Hz	2/10 Wavefront
Value	500	300	250	200	130	100	60	400

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TISP3xxxH3SL Overvoltage Protector Series

BOURNS®

ITU-T K.20/21 Rating . . . . . 8 kV 10/700, 200 A 5/310

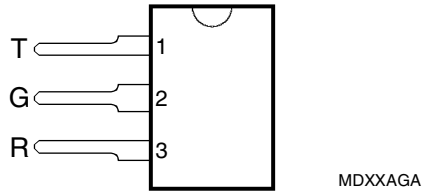
Ion-Implanted Breakdown Region
Precise and Stable Voltage
Low Voltage Overshoot under Surge

Device	V_{DRM} V	$V_{(BO)}$ V
‘3070	58	70
‘3080	65	80
‘3095	75	95
‘3115	90	115
‘3125	100	125
‘3135	110	135
‘3145	120	145
‘3180	145	180
‘3210	160	210
‘3250	190	250
‘3290	220	290
‘3350	275	350

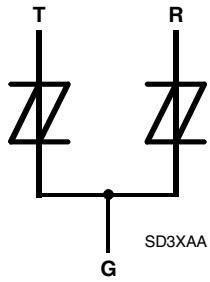
Rated for International Surge Wave Shapes
- Single and Simultaneous Impulses

Waveshape	Standard	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	300
10/160 µs	FCC Part 68	250
10/700 µs	FCC Part 68 ITU-T K.20/21	200
10/560 µs	FCC Part 68	160
10/1000 µs	GR-1089-CORE	100

SL Package (Top View)



Device Symbol



Terminals T, R and G correspond to the alternative line designators of A, B and C

3-Pin Through-Hole Packaging
- Compatible with TO-220AB pin-out
- Low Height 8.3mm

Low Differential Capacitance ..... < 67 pF

..... UL Recognized Component

Description

The TISP3xxxH3SL limits overvoltages between the telephone line Ring and Tip conductors and Ground. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line.

The protector consists of two symmetrical voltage-triggered bidirectional thyristors. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

How To Order

Device	Package	Carrier	Order As
TISP3xxxH3	SL (Single-in-Line)	Tube	TISP3xxxH3SL

Insert xxx value corresponding to protection voltages of 070, 080, 095, 115 etc.

This TISP3xxxH3SL range consists of twelve voltage variants to meet various maximum system voltage levels (58 V to 275 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These high current protection devices are in a 3-pin single-in-line (SL) plastic package and are supplied in tube pack. For alternative impulse rating, voltage and holding current values in SL packaged protectors, consult the factory. For lower rated impulse currents in the SL package, the 35 A 10/1000 TISP3xxxF3SL series is available. These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	'3070	V_{DRM}	± 58	V
	'3080		± 65	
	'3095		± 75	
	'3115		±90	
	'3125		±100	
	'3135		±110	
	'3145		±120	
	'3180		±145	
	'3210		±160	
	'3250		±190	
	'3290		±220	
	'3350		±275	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)		I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)			500	
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 current combination wave generator)			300	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			250	
5/200 µs (VDE 0433, 10/700 µs voltage wave shape)			220	
0.2/310 µs (I3124, 0.5/700 µs voltage wave shape)			200	
5/310 µs (ITU-T K.20/21, 10/700 µs voltage wave shape)			200	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)			200	
5/320 µs (FCC Part 68, 9/720 µs voltage wave shape)			200	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)		I_{TSM}		A
20 ms (50 Hz) full sine wave			55	
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			1	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. See Figure 9 for voltage values at lower temperatures.
2. Initially the TISP3xxxH3SL must be in thermal equilibrium.
3. These non-repetitive rated currents are peak values of either polarity. The rated current values may be applied to the R or T terminals. Additionally, both R and T terminals may have their rated current values applied simultaneously (in this case the G terminal return current will be the sum of the currents applied to the R and T terminals). The surge may be repeated after the TISP3xxxH3SL returns to its initial conditions.
4. See Figure 10 for impulse current ratings at other temperatures. Above 85 °C, derate linearly to zero at 150 °C lead temperature.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 8 for the current ratings at other durations. Figure 8 shows the R and T terminal current rating for simultaneous operation. In this condition, the G terminal current will be $2xI_{TSM(t)}$, the sum of the R and T terminal currents. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

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Electrical Characteristics for the R and G or T and G Terminals, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25 °C			±5	µA
			T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'3070			±70	V
			'3080			±80	
			'3095			±95	
			'3115			±115	
			'3125			±125	
			'3135			±135	
			'3145			±145	
			'3180			±180	
			'3210			±210	
			'3250			±250	
			'3290			±290	
			'3350			±350	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V, di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'3070			±78	V
			'3080			±88	
			'3095			±103	
			'3115			±124	
			'3125			±134	
			'3135			±144	
			'3145			±154	
			'3180			±189	
			'3210			±220	
			'3250			±261	
			'3290			±302	
			'3350			±362	
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = - /+30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	µA
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0,	'3070 thru '3115			170	pF
			'3125 thru '3210			90	
			'3250 thru '3350			84	
		f = 100 kHz, V_d = 1 V rms, V_D = -1 V	'3070 thru '3115			150	
			'3125 thru '3210			79	
			'3250 thru '3350			67	
		f = 100 kHz, V_d = 1 V rms, V_D = -2 V	'3070 thru '3115			140	
			'3125 thru '3210			74	
			'3250 thru '3350			62	
		f = 100 kHz, V_d = 1 V rms, V_D = -50 V	'3070 thru '3115			73	
			'3125 thru '3210			35	
			'3250 thru '3350			28	
		f = 100 kHz, V_d = 1 V rms, V_D = -100 V (see Note 6)	'3125 thru '3210			33	
			'3250 thru '3350			26	

NOTE 6: To avoid possible voltage clipping, the '3125 is tested with V_D = -98 V.

Electrical Characteristics for the R and T Terminals, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = 2V_{DRM}$				±5	µA
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'3070			±140	V
			'3080			±160	
			'3095			±190	
			'3115			±230	
			'3125			±250	
			'3135			±270	
			'3145			±290	
			'3180			±360	
			'3210			±420	
			'3250			±500	
			'3290			±580	
			'3350			±700	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'3070			±156	V
			'3080			±176	
			'3095			±206	
			'3115			±248	
			'3125			±268	
			'3135			±288	
			'3145			±308	
			'3180			±378	
			'3210			±440	
			'3250			±252	
			'3290			±604	
			'3350			±724	

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 7)			50	°C/W

NOTE 7: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

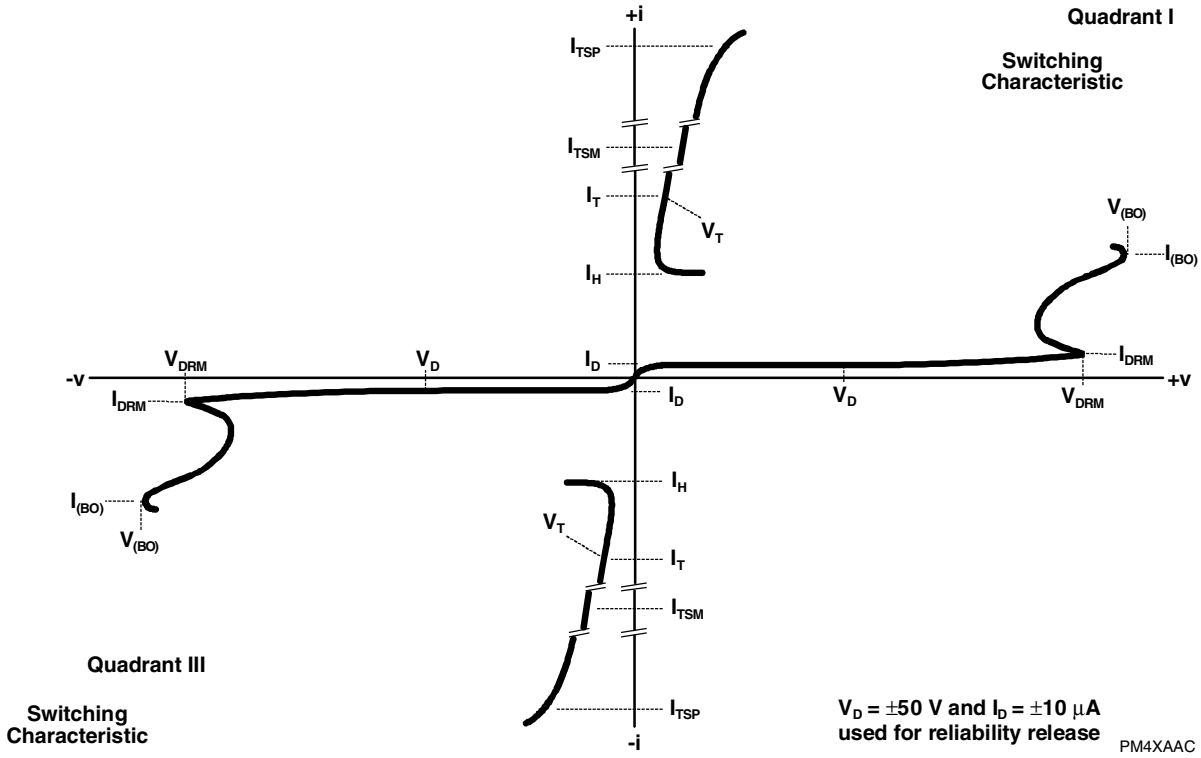


Figure 1. Voltage-current Characteristic for Terminal Pairs

Typical Characteristics

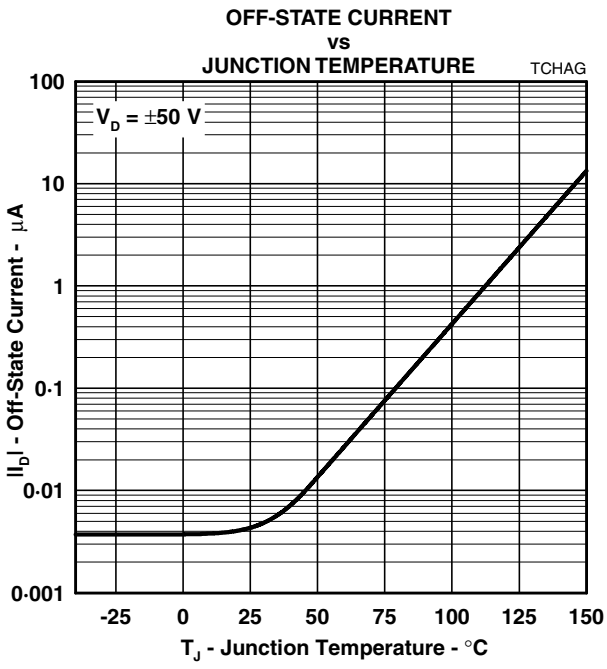


Figure 2.

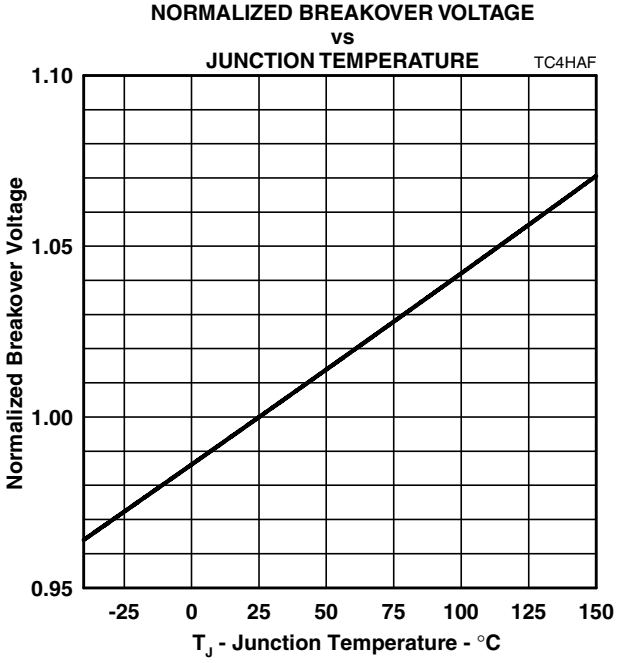


Figure 3.

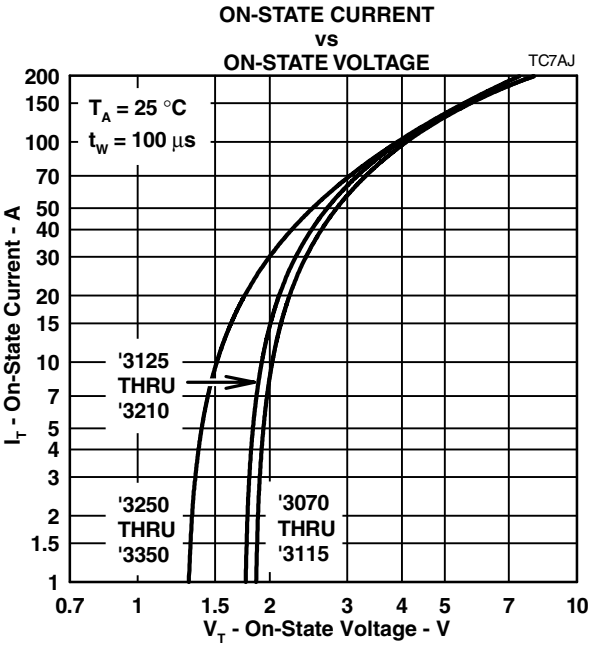


Figure 4.

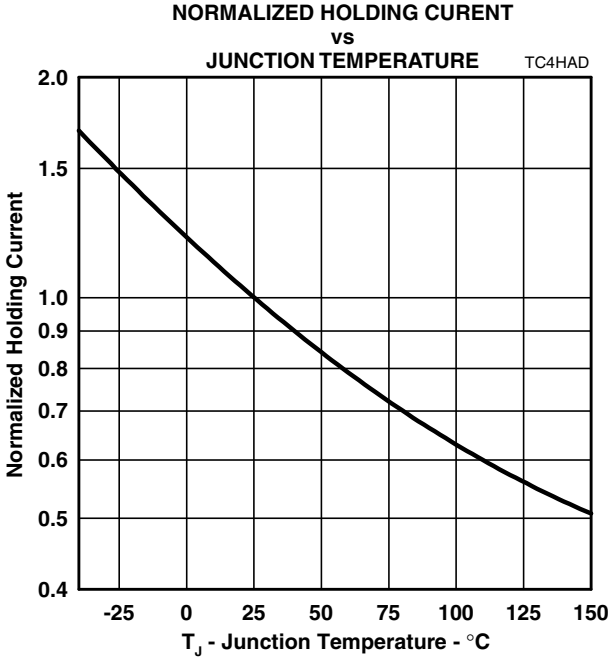


Figure 5.

Typical Characteristics

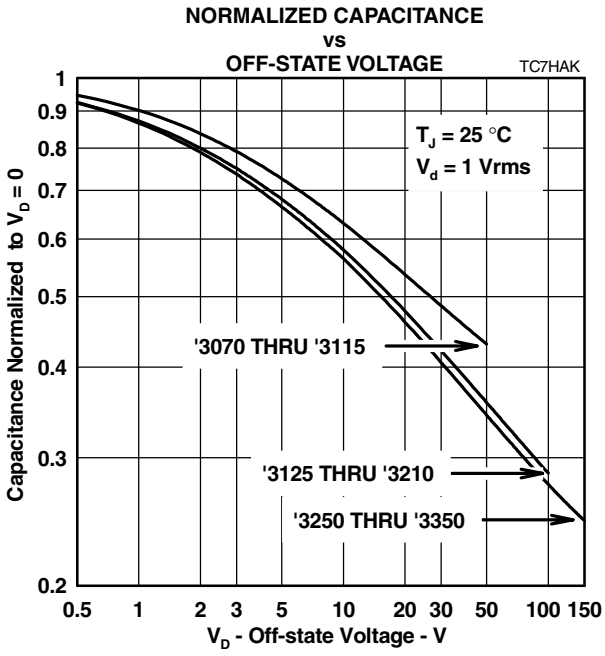


Figure 6.

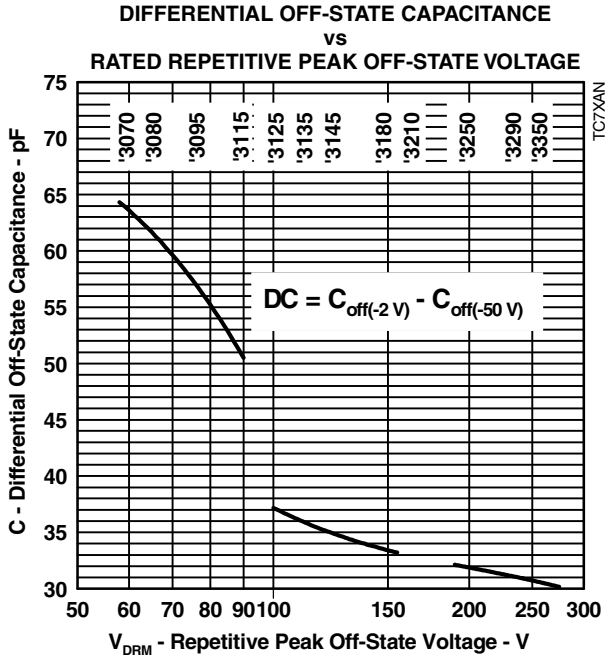


Figure 7.

Typical Characteristics

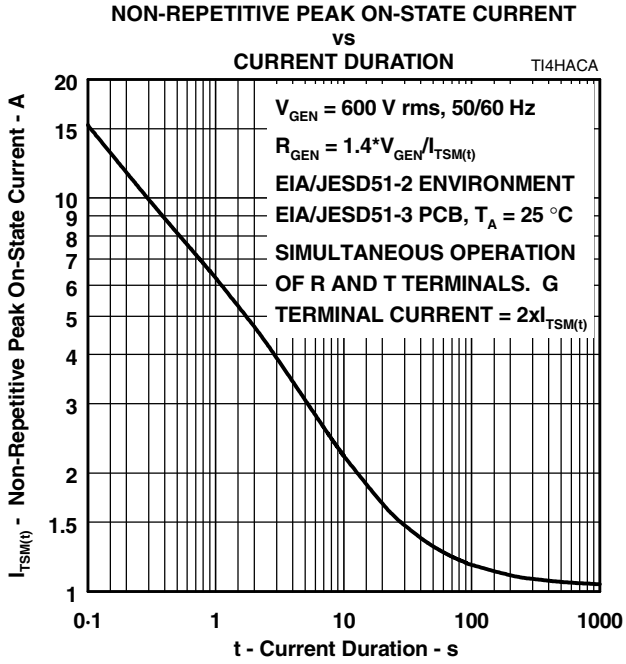


Figure 8.

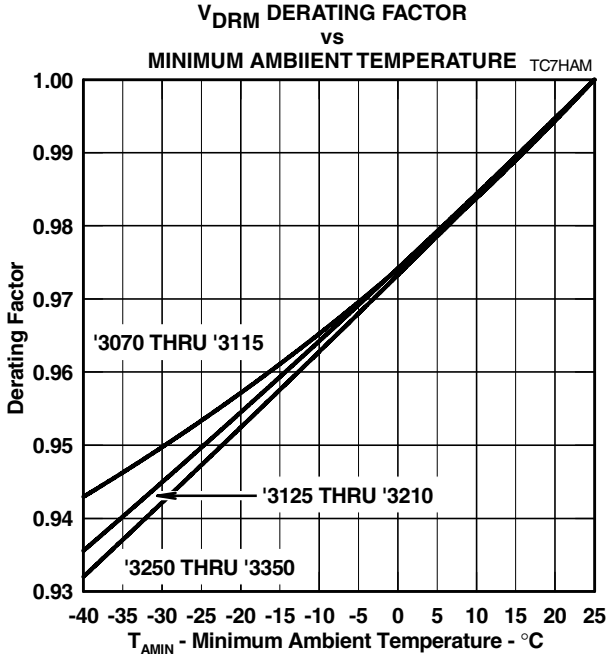


Figure 9.

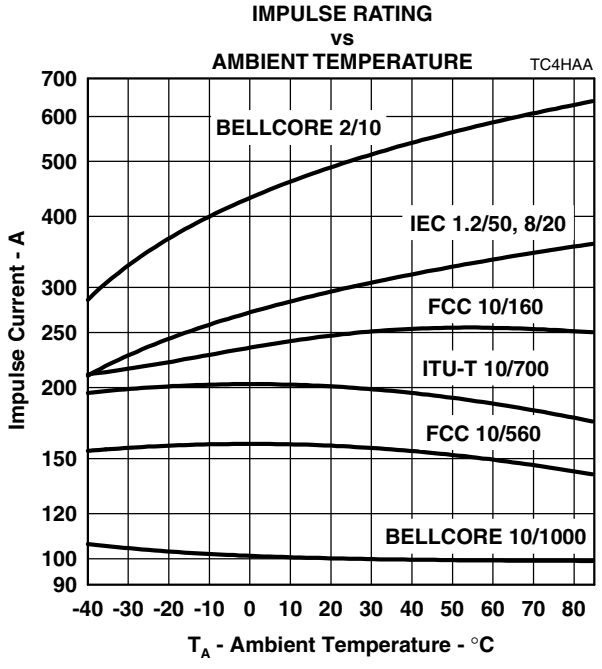


Figure 10.

APPLICATIONS INFORMATION

Impulse Testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

Standard	Peak Voltage Setting V	Voltage Waveform µs	Peak Current Value A	Current Waveform µs	TISP3xxxH3 25 °C Rating A	Series Resistance Ω
GR-1089-CORE	2500	2/10	500	2/10	500	0
	1000	10/1000	100	10/1000	100	
FCC Part 68 (March 1998)	1500	10/160	200	10/160	250	0
	800	10/560	100	10/560	160	0
	1500	9/720 †	37.5	5/320 †	200	0
	1000	9/720 †	25	5/320 †	200	0
I3124	1500	0.5/700	37.5	0.2/310	200	0
ITU-T K.20/K.21	1500 4000	10/700	37.5 100	5/310	200	0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K.21 10/700 impulse generator

If the impulse generator current exceeds the protector's current rating, then a series resistance can be used to reduce the current to the protector's rated value to prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generator's peak voltage by the protector's rated current. The impulse generator's fictitious impedance (generator's peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance. In some cases, the equipment will require verification over a temperature range. By using the rated waveform values from Figure 10, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

AC Power Testing

The protector can withstand the G return currents applied for times not exceeding those shown in Figure 8. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) resistors and fusible resistors are overcurrent protection devices which can be used to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases, it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 8. In some cases, there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

Capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, V_D, values of 0, -1 V, -2 V, and -50 V. Where possible, values are also given for -100 V. Values for other voltages may be calculated by multiplying the V_D = 0 capacitance value by the factor given in Figure 6. Up to 10 MHz, the capacitance is essentially independent of frequency. Above 10 MHz, the effective capacitance is strongly dependent on connection inductance. In many applications, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V.

Normal System Voltage Levels

The protector should not clip or limit the voltages that occur in normal system operation. For unusual conditions, such as ringing without the line connected, some degree of clipping is permissible. Under this condition, about 10 V of clipping is normally possible without activating the ring trip circuit. Figure 9 allows the calculation of the protector V_{DRM} value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP3290H3, with a V_{DRM} of 220 V, can be used for the protection of ring generators producing 105 V rms of ring on a battery voltage of -58 V. The peak ring voltage will be 58 + 1.414*105 = 206.5 V. However, this is the open circuit voltage and the connection of the line and its equipment will reduce the peak voltage.

APPLICATIONS INFORMATION

Normal System Voltage Levels (continued)

For the extreme case of an unconnected line, the temperature at which clipping begins can be calculated using the data from Figure 9. To possibly clip, the V_{DRM} value has to be 206.5 V. This is a reduction of the 220 V 25 °C V_{DRM} value by a factor of 206.5/220 = 0.94. Figure 9 shows that a 0.94 reduction will occur at an ambient temperature of -32 °C. In this example, the TISP3290H3 will allow normal equipment operation, even on an open-circuit line, provided that the minimum expected ambient temperature does not fall below -32 °C.

JESD51 Thermal Measurement Method

To standardize thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the center. Part 3 of the standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm (1.06 ”) on a side and the other for packages up to 48 mm (1.89 ”). The thermal measurements used the smaller 76.2 mm x 114.3 mm (3.0 ” x 4.5 ”) PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worse case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance and so can dissipate higher power levels than indicated by the JESD51 values.

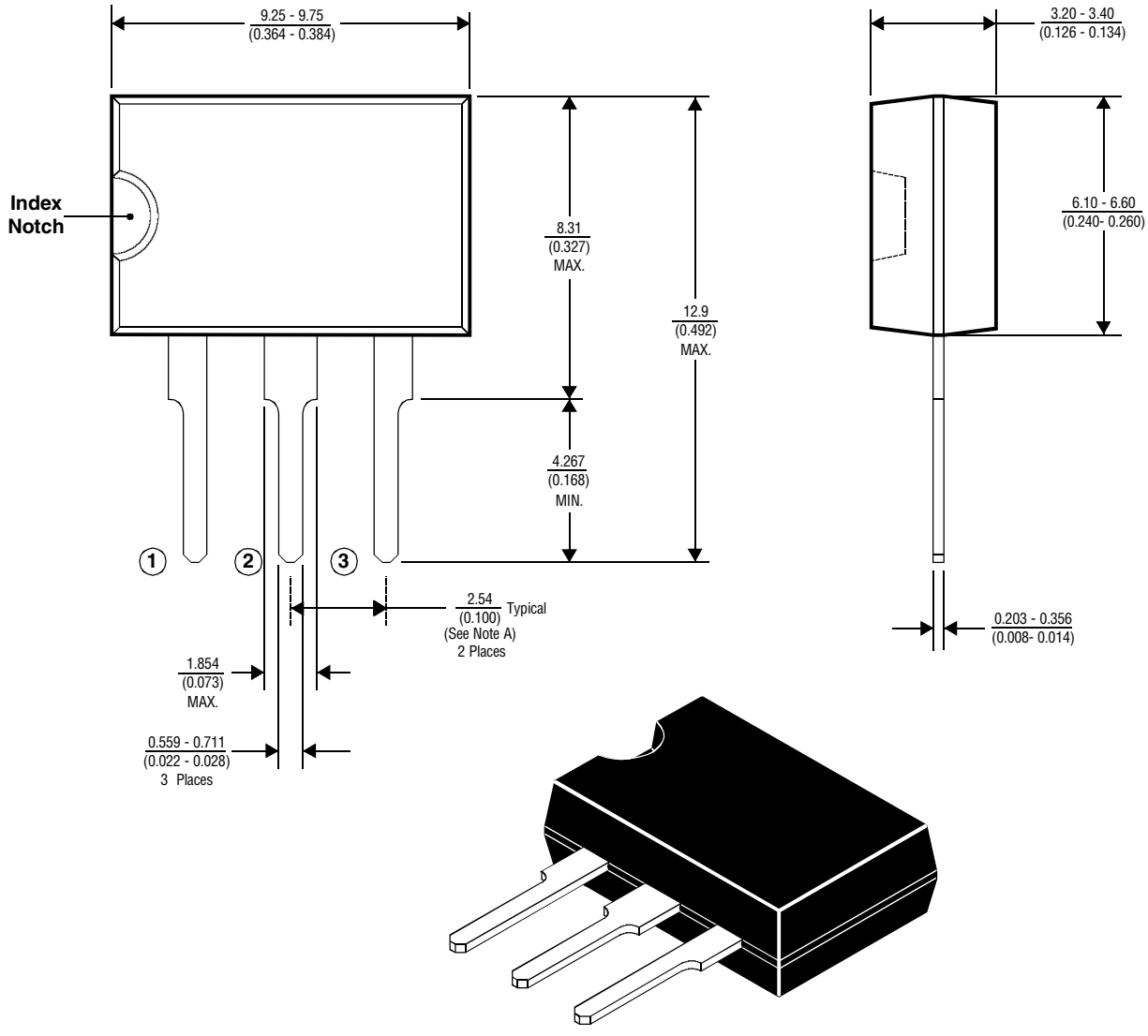
MECHANICAL DATA

SL003 3-pin Plastic Single-in-line Package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

SL003

DIMENSIONS ARE: METRIC (INCHES)



MDXXCE

NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
B. Body molding flash of up to 0.15 (0.006) may occur in the package lead plane.