SED1336

CMOS GRAPHIC LCD/TV CONTROLLER

- **For Medium-Scale LCD**
- **Output to LCD-Screen**
- **Virtual Screen Display RAM**
- **Enhanced Control Function**
- **Simultaneous LCD & TV Display**

■ DESCRIPTION

The SED1336 is a CMOS low-power dot matrix liquid crystal graphic display controller with built-in TV support. The built-in TV support IC is capable of displaying characters and graphic images simultaneously on TV monitors and flat panels.

The SED1336 has a built-in TV control circuit that generates either NTSC or PAL system synchronous signals, memory. The device stores the display data in external SRAM that is sent by an 8-bit microcomputer, and generates all the control signals required by the LCD drivers.

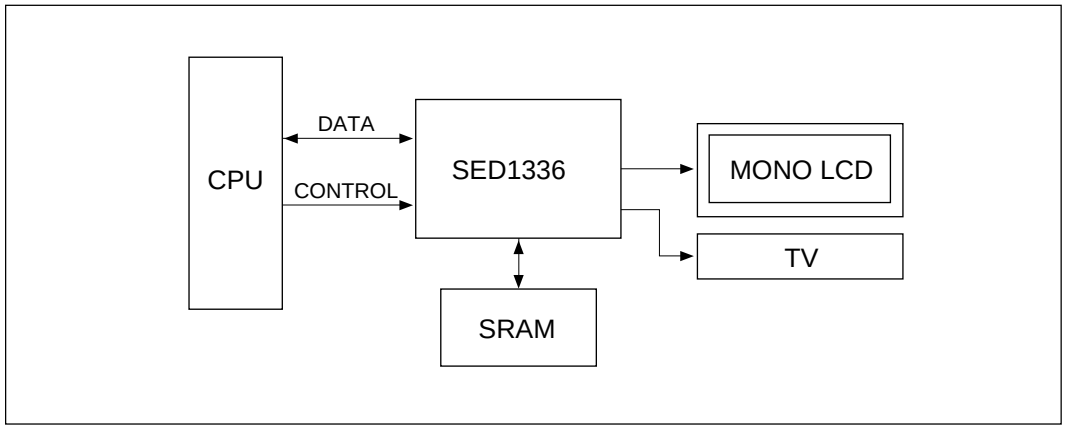
The controller incorporates an internal character generator ROM which supports user-defined characters. An external CG ROM can also be supported to provide additional characters.

The SED1336 can be interfaced to high-speed microprocessors such as the Intel 80xx family or the Motorola 68xx family. The controller supports a set of commands that allow the user to create a layered display of characters and graphics.

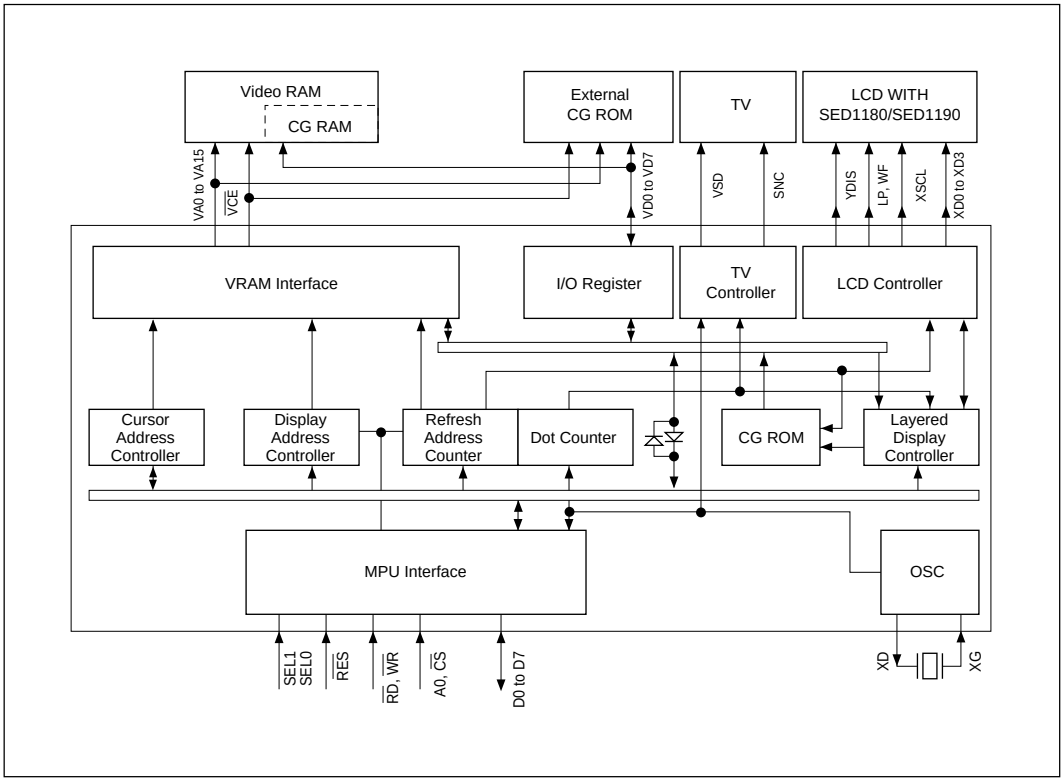
■ FEATURES

- Low-power CMOS fabrication
- Compatible with both Intel 80XX and Motorola 68XX high-speed MPU
- Display duty:
  LCD ..... 1/2 to 1/256 can be selected
  TV ..... 256 × 200 dots
- Internal and external character generator ROM
- Simultaneous LCD and TV operation
- Selectable display synthesis
- Programmable cursor movement
- Multimode display:
  2 layers of overlapping character and graphic
  3 layers of overlapping graphic
- Supports 64K bytes of memory
- Single power supply ..... 3.0V to 5.5V
- Package ..... Plastic QFP6-60 pin (F_{0A})

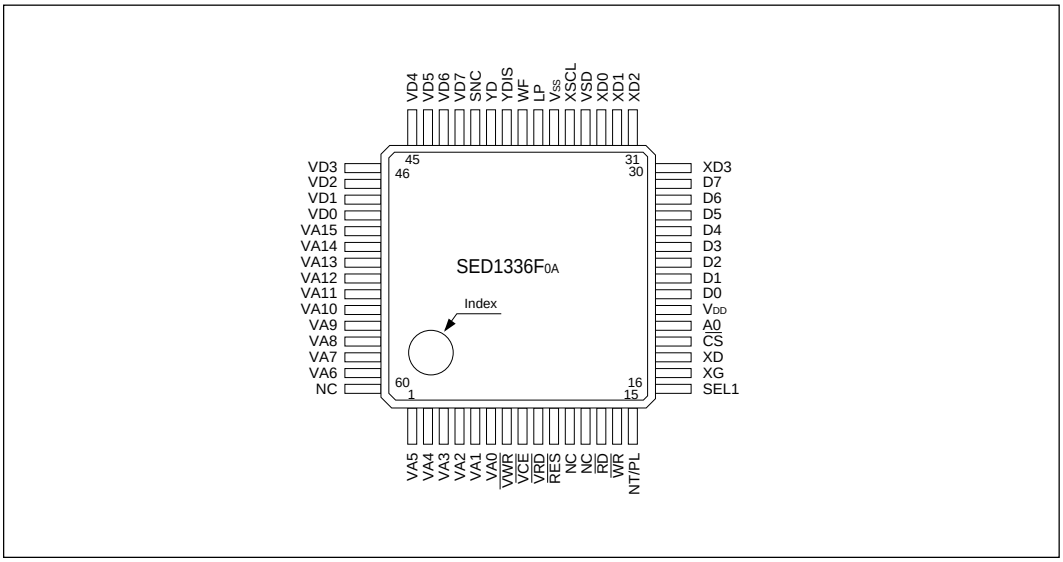
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN ASSIGNMENT DIAGRAM



■ PIN DESCRIPTION

Name	Number	Type	Description
VA0 to VA5 VA6 to VA15	6 to 1 59 to 50	Output	VRAM address bus
$\overline{VWR}$	7	Output	VRAM write signal
$\overline{VCE}$	8	Output	Memory control signal
$\overline{VRD}$	9	Output	VRAM read signal
$\overline{RES}$	10	Input	Reset
NC	11, 60	—	No connection
CLO	12	Output	Clock output
$\overline{RD}$	13	Input	8080-family: Read signal 6800-family: Enable clock (E)
$\overline{WR}$	14	Input	8080-family: Write signal 6800-family: R/$\overline{W}$ signal
NT/PL	15	Input	NTSC or PAL TV mode select
SEL1	16	Input	8080- or 6800-family interface select
OSC1	17	Input	Oscillator connection
OSC2	18	Output	Oscillator connection
$\overline{CS}$	19	Input	Chip select
A0	20	Input	Data type select
VDD	21	Supply	3.0 to 5.5V supply
D0 to D7	22 to 29	Input/output	Data bus
XD0 to XD3	30 to 33	Output	Data to LCD X-driver
VSD	34	Output	Video data
XSCL	35	Output	Data shift clock
VSS	36	Supply	Ground
LP	37	Output	Latch pulse
WF	38	Output	Frame signal
YDIS	39	Output	Power-down signal when display is blanked
YD	40	Output	Scan start pulse
SNC	41	Output	TV sync signal
VD0 to VD7	42 to 49	Input/output	VRAM data bus

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Operating temperature range	T_{opr}	–20 to 75	°C
Storage temperature range	T_{stg}	–65 to 150	°C
Soldering temperature (10 seconds). See note 1.	T_{solder}	260	°C

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.
2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines.
3. All supply voltages are referenced to V_{SS} = 0V.

- **DC Electrical Characteristics**

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Register data retention voltage	V_{HO}		2.0	—	6.0	V
Input leakage current	I_{LI}	V_I = V_{DD}. See note 6.	—	0.05	2.0	µA
Output leakage current	I_{LO}	V_I = V_{SS}. See note 6.	—	0.10	5.0	µA
Operating supply current	I_{opr}	See note 4.	—	11	15	mA
Quiescent supply current	I_Q	Sleep mode, V_{OSC1} = $V_{\overline{CS}}$ = $V_{\overline{RD}}$ = V_{DD}	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 7.	1.0	—	10.0	MHz
External clock frequency	f_{CL}		1.0	—	10.0	MHz
Oscillator feedback resistance	R_f		0.5	1.0	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V^{OHT}	I_{OH} = –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 5.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA. See note 5.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes:

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1 and NT/PL are CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS and CLO are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. fOSC = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. SNC and VSD are n-channel, open-drain outputs. The voltage on the outputs should not exceed V_{DD} as internal diodes connect the pins to V_{DD} (SED1336F only).
6. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
7. Because the oscillator circuit input bias current is in the order of µA, design the printed circuit board so as to reduce leakage currents.

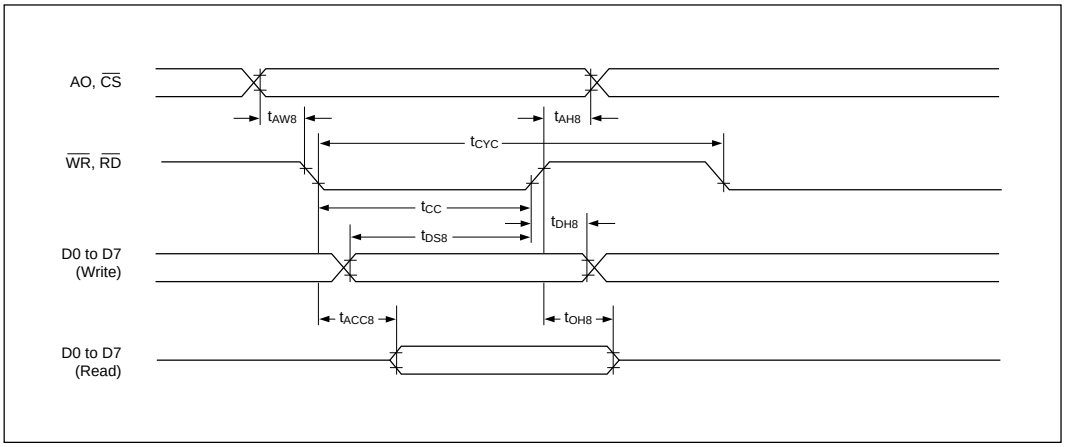
V_{DD} = 3.0 to 4.5V, V_{SS} = 0V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}	See note 8.	3.0	3.5	4.5	V
Register data retention voltage	V_{HO}		2.0	—	6.0	V
Input leakage current	I_{LI}	V_I = V_{DD}. See note 6.	—	0.05	2.0	µA
Output leakage current	I_{LO}	V_I = V_{SS}. See note 6.	—	0.10	5.0	µA
Operating supply current	I_{opr}	V_{DD} = 3.5V. See note 4. See note 4.	— —	3.5 —	— 7.0	mA
Quiescent supply current	I_Q	Sleep mode, V_{OSC1} = $V\overline{CS}$ = $V\overline{RD}$ = V_{DD}	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 7.	1.0	—	8.0	MHz
External clock frequency	f_{CL}		1.0	—	8.0	MHz
Oscillator feedback resistance	R_f		0.7	—	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –3.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 3.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA. See note 5.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Falling edge threshold voltage	V_{T-}	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes:

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1 and NT/PL are CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS and CLO are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. fOSC = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. SNC and VSD are n-channel, open-drain outputs. The voltage on the outputs should not exceed V_{DD} as internal diodes connect the pins to V_{DD}.
6. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
7. Because the oscillator circuit input bias current is in the order of µA, design the printed circuit board so as to reduce leakage currents.
8. V_{DD} = 2.7 to 4.5V (SED1335F)

- **Timing Diagrams**
  - **8080-Family Interface Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
A0, CS	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100 pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
WR, RD	t_{CYC}	System cycle time	See note	—	See note	—	ns	
	t_{CC}	Strobe pulsewidth	120	—	140	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	RD access time	—	50	—	70	ns	
	t_{OH8}	Output disable time	10	50	10	50	ns	

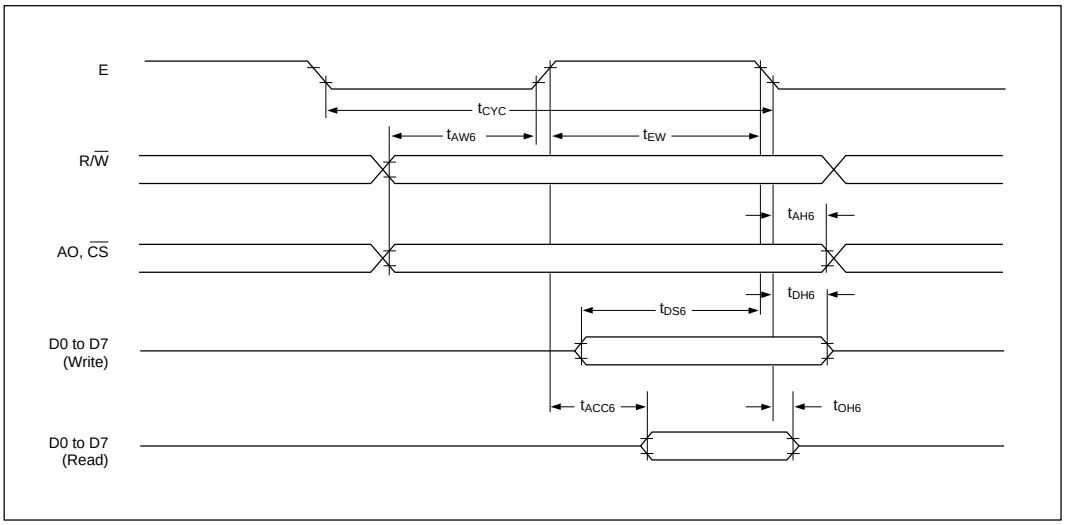
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

○ **6800-Family Interface Timing**



Note: t_{CYC6} indicates the interval during which $\overline{CS}$ is LOW and E is HIGH.

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	t_{CYC6}	System cycle time	See note	—	See note	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	70	ns	
	t_{ACC6}	Access time	—	85	—	120	ns	
E	t_{EW}	Enable pulsewidth	120	—	140	—	ns	

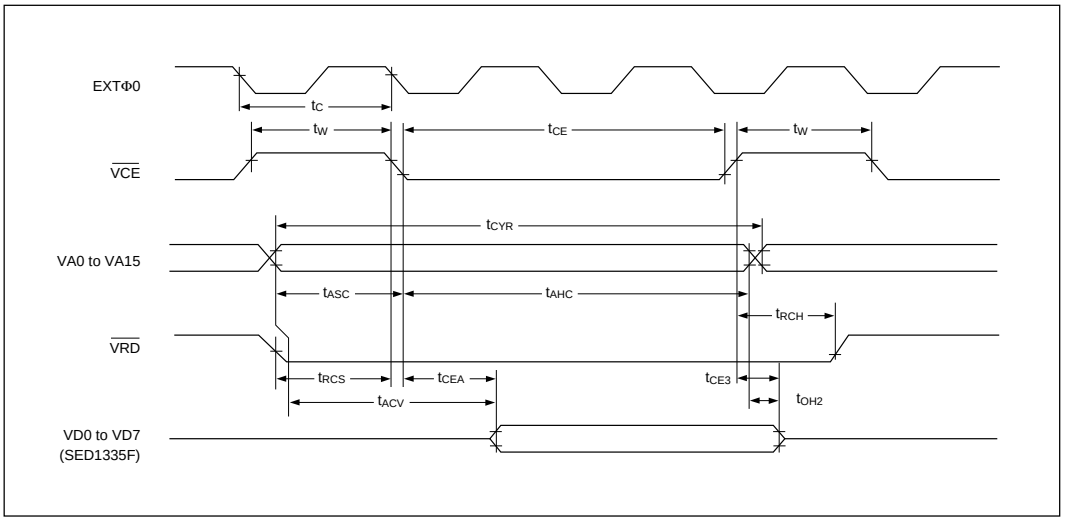
Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

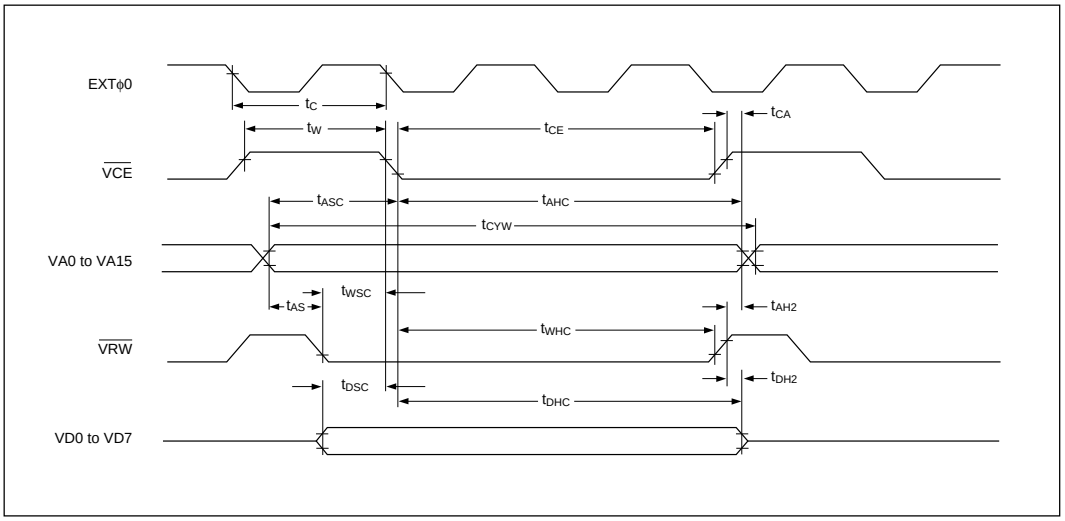
○ **Display Memory Read Timing**



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulsewidth	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulsewidth	2t_C – 30	—	2t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	3t_C	—	3t_C	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 40	—	ns	
$\overline{VRD}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{VCE}$	t_C – 45	—	t_C – 55	—	ns	
	t_{RCH}	Read cycle hold time from rising edge of $\overline{VCE}$	0.5t_C	—	0.5t_C	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	3t_C – 100	—	3t_C – 110	ns	
	t_{CEA}	$\overline{VCE}$ access time	—	2t_C – 80	—	2t_C – 85	ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	—	0	—	ns	

○ **Display Memory Write Timing**

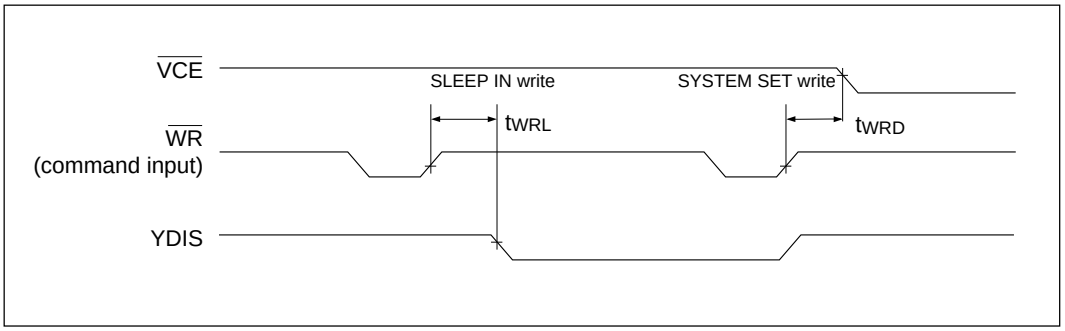


T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	tW	$\overline{VCE}$ HIGH-level pulse-width	tC – 50	—	tC – 50	—	ns	
	tCE	$\overline{VCE}$ LOW-level pulse-width	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tC	—	3tC	—	ns	
	tAHC	Address hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 40	—	ns	
	tASC	Address setup time to falling edge of $\overline{VCE}$	tC – 70	—	tC – 100	—	ns	
	tCA	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	tAS	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	tAH2	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	tWSC	Write setup time to falling edge of $\overline{VCE}$	tC – 80	—	tC – 110	—	ns	
	tWHC	Write hold time from falling edge of $\overline{VCE}$	2tC – 20	—	2tC – 20	—	ns	
VD0 to VD7	tDSC	Data input setup time to falling edge of $\overline{VCE}$	tC – 85	—	tC – 120	—	ns	
	tDHC	Data input hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 30	—	ns	
	tDH2	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

○ **SLEEP IN Command Timing**

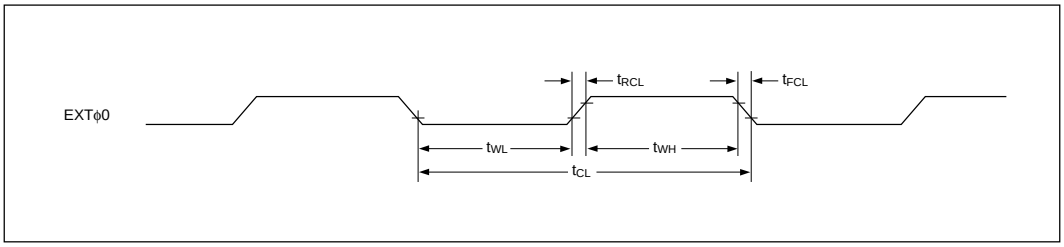


T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	*1	—	*1	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	*2	—	*2	ns	

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

○ **External Oscillator Signal Timing**



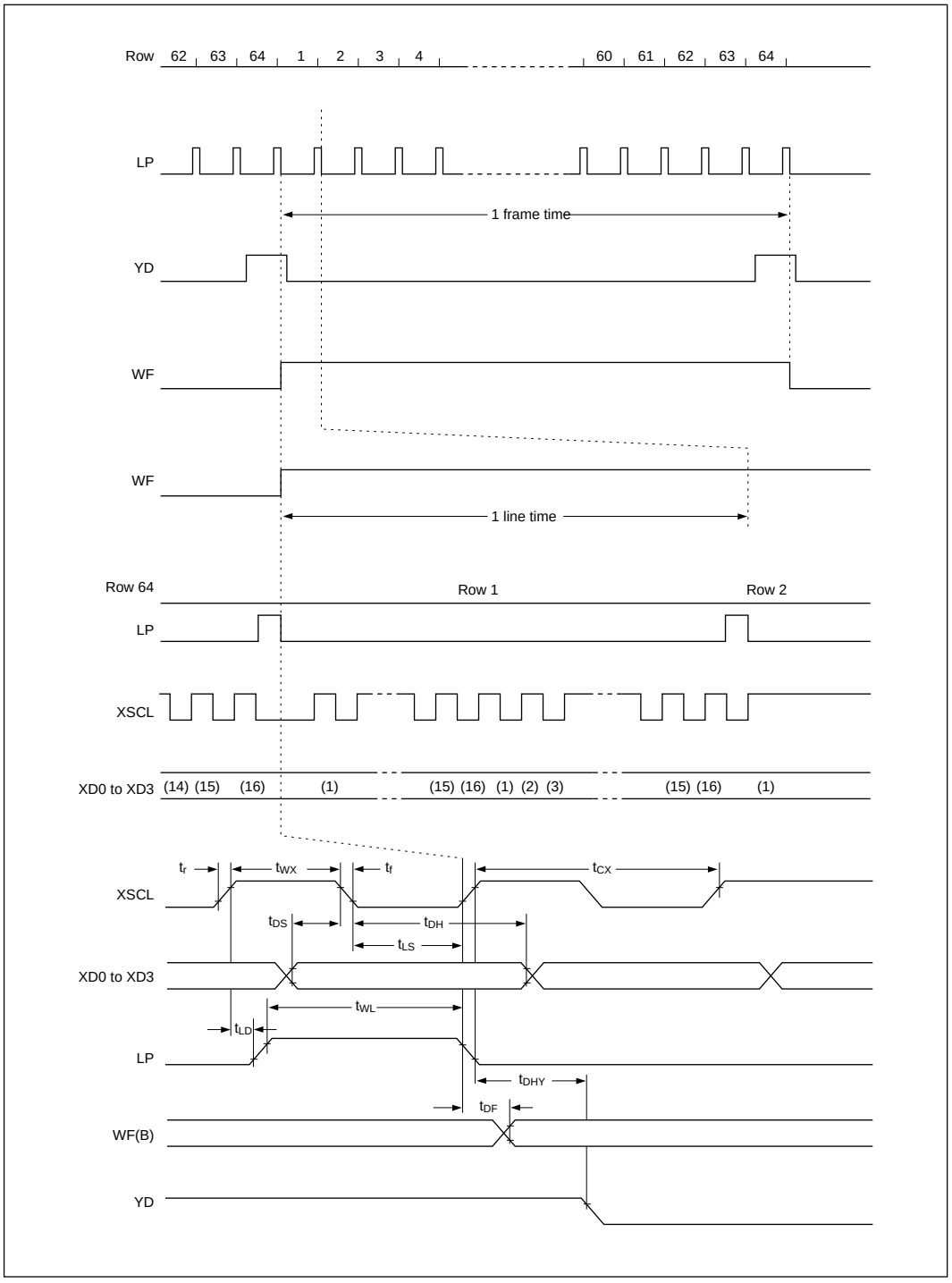
T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_{RCL}	External clock rise time	—	15	—	15	ns	
	t_{FCL}	External clock fall time	—	15	—	15	ns	
	t_{WH}	External clock HIGH-level pulsewidth	*1	*2	*1	*2	ns	
	t_{WL}	External clock LOW-level pulsewidth	*1	*2	*1	*2	ns	
	t_C	External clock period	100	—	125	—	ns	

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

○ **LCD Output Timing**

The following characteristics are for a 1/64 duty cycle.



T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	35	ns	CL = 100 pF
	t_f	Fall time	—	30	—	35	ns	
XSCL	t_{CX}	Shift clock cycle time	4t_C	—	4t_C	—	ns	
	t_{WX}	XSCL clock pulsewidth	2t_C – 60	—	2t_C – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{DS}	X data setup time	2t_C – 100	—	2t_C – 100	—	ns	
LP	t_{LS}	Latch data setup time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{WL}	LP pulsewidth	4t_C – 80	—	4t_C – 100	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2t_C – 20	—	2t_C – 20	—	ns	

Note: The SED1336F reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.