

Features

- Dual Mode Low Drop Out Voltage Regulator
- Programmable Output Voltage Ranging from 1.75V to 2.1V
- 3V to 5.5V Supply Operation
- 180 mA Maximum Load Current in Full Power Mode
- Maximum Current Consumption 70 μ A in Full Power Mode and 15 μ A in Low Power Mode
- Power-down Mode Consumption Less Than 1 μ A
- More Than 70dB (Typical) PSRR at 1 KHz
- 100 μ V_{RMS} Output Noise in Full-power Mode
- 0.35 μ m CMOS Technology
- Typical Application: Baseband Section Supply in Mobile Terminals

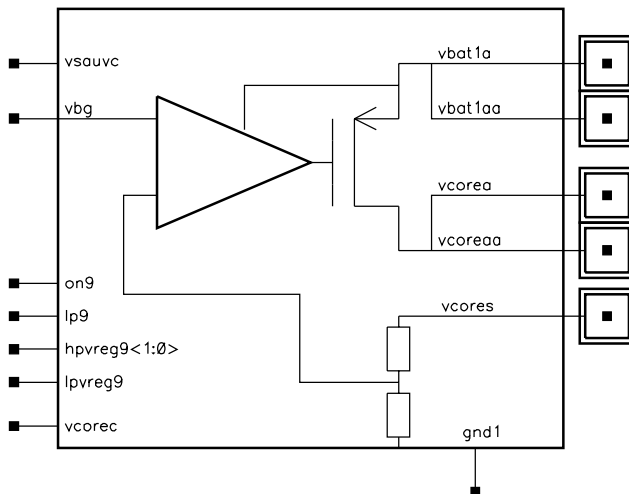
Description

RE030 is a dual mode Low Drop Out (LDO) voltage regulator macrocell with programmable output voltage ranging from 1.75V to 2.1V, rated for loads up to 180 mA in full power mode and 5 mA in low power mode. (Both modes can be selected by the LP9 signal.) It is designed to be integrated with other analog cells, digital logic, microcontrollers, DSP cores and memory blocks into system-on-chip products.

The circuit consists of a PMOS pass device, an error amplifier and a feedback resistive network, sized to achieve the required closed loop gain. These blocks make up the regulating loop. An over-current and short circuit protection circuit has been included to limit the output current delivered by the regulator, thus avoiding destruction in case of a short circuit.

An external reference voltage V_{BG} (bandgap voltage) is necessary for correct functionality. The target reference voltage is 1.231V delivered, for example, by BG019. Double pads on the supply voltage V_{BAT1A}/V_{BAT1AA} and output voltage V_{COREA}/V_{COREAA} are used to reduce the total output resistance. Current reference is generated inside the cell through a circuit supplied by a $2.5V \pm 0.1V$ of regulated input voltage on V_{SAUVC} . Remote sense terminal V_{CORES} provides regulation of the load by connecting it to the output terminal near a critical point to improve performance of the regulator (e.g., connecting it to the package pin by double-bonding, thus avoiding the bonding resistance influence). A ceramic capacitor of 2.2 μ F connected from V_{COREA}/V_{COREAA} to ground is needed as external compensation.

Figure 1. Symbol ⁽¹⁾



Note: 1. Pin names are written as they appear on the user screen when the symbol is opened in the design tool environment.



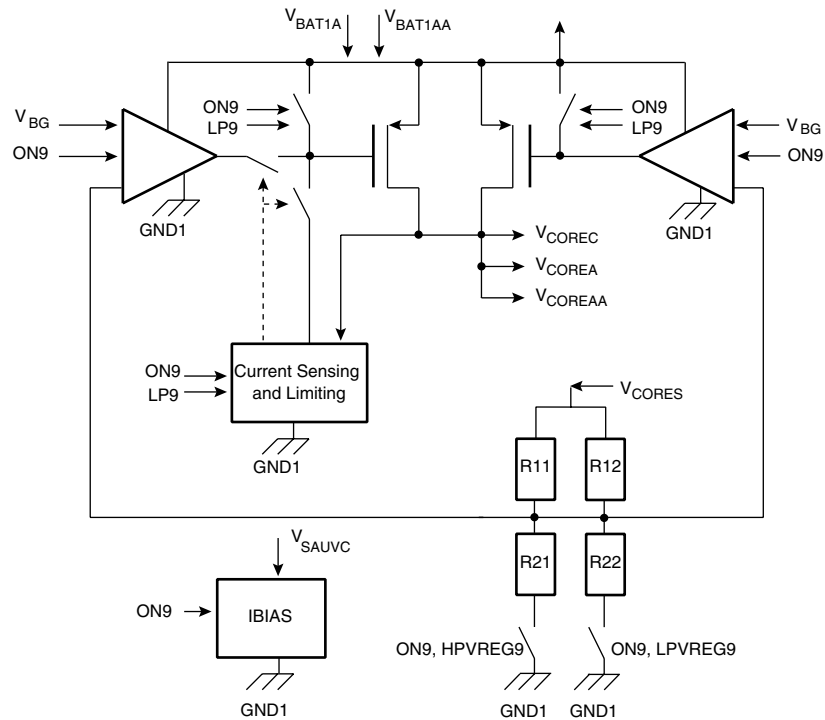
Embedded ASIC Macrocell: Power Management

RE030 1.75V to 2.1V 180 mA Dual Mode LDO Regulator



Functional Diagram

Figure 2. Functional Diagram



Pin Description

Pin Name	I/O	Type	Function	Value
V _{BAT1A}	Power Supply	External Pad	Power Supply	3V to 5.5V
V _{BAT1AA}	Power Supply	External Pad	Power Supply	3V to 5.5V
V _{COREA}	Analog Output	External Pad	Output Voltage	1.75V to 2.1V
V _{COREAA}	Analog Output	External Pad	Output Voltage	1.75V to 2.1V
V _{CORES}	Analog Input	External Pad	Sense Voltage	1.75V to 2.1V
V _{COREC}	Analog Output	Internal Pin	Output Voltage	1.75V to 2.1V
GND1	Ground	Internal Pin	Ground	0
V _{SAUVC}	Power Supply	Internal Pin	Power Supply	2.5V ± 0.1V
V _{BG}	Analog Input	Internal Pin	Voltage Reference	1.231V
ON9	Digital Input	Internal Pin	Enable Command	0V or V _{BAT1A} /V _{BAT1AA}
LP9	Digital Input	Internal Pin	Full/Low Power Selection	0V or V _{BAT1A} /V _{BAT1AA}
HPVREG9<1:0>	Digital Input	Internal Pin	Full Power Output Voltage Selection	0V or V _{BAT1A} /V _{BAT1AA}
LPVREG9	Digital Input	Internal Pin	Low Power Output Voltage Selection	0V or V _{BAT1A} /V _{BAT1AA}

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Absolute Maximum Ratings*

Analog Signals	-0.3V to 6.5V
Digital Signals.....	-0.3V to 5.5V
Output Current.....	Internally limited
Junction Temperature	-20°C to 150°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications⁽¹⁾

$T_J = -20^{\circ}\text{C}$ to 125°C , $V_{\text{BAT1A}}/V_{\text{BAT1AA}} = 3\text{V}$ to 5.5V unless otherwise specified, output capacitance = $2.2\ \mu\text{F}$.

Table 1. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{\text{BAT1A}}/V_{\text{BAT1AA}}$	Operating Supply Voltage		3		5.5	V
V_{SAUVC}	Auxiliary Operating Supply Voltage		2.4	2.5	2.6	V
T_J	Temperature Range		-20		125	°C
Full Power Mode						
$V_{\text{COREA}}/V_{\text{COREAA}}$	Output Voltage	2.1V programmed	2.04	2.1	2.16	V
		2.01V programmed	1.96	2.01	2.06	
		1.88V programmed	1.82	1.88	1.94	
		1.75V programmed	1.7	1.75	1.8	
$I_{\text{COREA}}/I_{\text{COREAA}}$	Output Current				180	mA
I_{QQ}	Quiescent Current				70	μA
ΔV_{DC}	Line Regulation	$V_{\text{BAT1A}}/V_{\text{BAT1AA}} = 3\text{V}$ to 3.4V ; $I_{\text{COREA}}/I_{\text{COREAA}} = 180\text{ mA}$		2	3	mV
ΔV_{TRAN}	Transient Line Regulation	$V_{\text{BAT1A}}/V_{\text{BAT1AA}} = 3\text{V}$ to 3.4V ; $I_{\text{COREA}}/I_{\text{COREAA}} = 180\text{ mA}$ rise time = fall time = $5\ \mu\text{s}$		2	3	mV
ΔV_{DC}	Load Regulation	10% to 90% of max $I_{\text{COREA}}/I_{\text{COREAA}}$;		2	3	mV
ΔV_{TRAN}	Transient Load Regulation	10% to 90% of max $I_{\text{COREA}}/I_{\text{COREAA}}$; rise time = fall time = $5\ \mu\text{s}$		5	7	mV

Table 1. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
PSRR	Power Supply Rejection Ratio at Full Load	$V_{BAT1A}/V_{BAT1AA} = 3V$	@ 100 Hz		-63		dB
			@ 1 kHz		-63		dB
			@ 20 kHz		-49		dB
			@ 100 kHz		-35		dB
		$V_{BAT1A}/V_{BAT1AA} = 4.25V$	@ 100 Hz		-64		dB
			@ 1 kHz		-64		dB
			@ 20 kHz		-56		dB
			@ 100 kHz		-43		dB
		$V_{BAT1A}/V_{BAT1AA} = 5.5V$	@ 100 Hz		-61		dB
			@ 1 kHz		-61		dB
			@ 20 kHz		-56		dB
			@ 100 kHz		-43		dB
$V_N^{(2)}$	Output Noise	Bandwidth = 10 Hz to 100 kHz; $I_{COREA}/I_{COREAA} = 180\text{ mA}$		77	100	μV_{RMS}	
T_R	Rise Time	100% of I_{COREA}/I_{COREAA} ; 10% to 90% of V_{COREA}/V_{COREAA}			60	μs	
I_{SD}	Shut Down Current				1	μA	
I_{CC}	Short-circuit Current			330	400	mA	
Low Power Mode							
V_{COREA}/V_{COREAA}	Output Voltage	1.8V programmed	1.7	1.8	1.9	V	
		2V programmed	1.9	2	2.1		
I_{COREA}/I_{COREAA}	Output Current				5	mA	
I_{QQ}	Quiescent Current				15	μA	
ΔV_{DC}	Line Regulation	$V_{BAT1A}/V_{BAT1AA} = 3V\text{ to }3.4V$; $I_{COREA}/I_{COREAA} = 5\text{ mA}$		2	3	mV	
ΔV_{TRAN}	Transient Line Regulation	$V_{BAT1A}/V_{BAT1AA} = 3V\text{ to }3.4V$; $I_{COREA}/I_{COREAA} = 5\text{ mA}$ rise time = fall time = 5 μs		2	3	mV	
ΔV_{DC}	Load Regulation	10% to 90% of max I_{COREA}/I_{COREAA}		4	6	mV	
ΔV_{TRAN}	Transient Load Regulation	10% to 90% of max I_{COREA}/I_{COREAA} ; rise time = fall time = 5 μs		2	5	mV	

RE030 1.75/2.1V 180 mA Dual Mode LDO Regulator

Table 1. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
PSRR	Power Supply Rejection Ratio at Full Load	$V_{BAT1A}/V_{BAT1AA} = 3V$	@ 100 Hz		-69		dB
			@ 1 kHz		-69		dB
			@ 20 kHz		-66		dB
			@ 100 kHz		-52		dB
		$V_{BAT1A}/V_{BAT1AA} = 4.25V$	@ 100 Hz		-57		dB
			@ 1 kHz		-57		dB
			@ 20 kHz		-57		dB
			@ 100 kHz		-53		dB
		$V_{BAT1A}/V_{BAT1AA} = 5.5V$	@ 100 Hz		-44		dB
			@ 1 kHz		-44		dB
			@ 20 kHz		-45		dB
			@ 100 kHz		-48		dB
$V_N^{(2)}$	Output Noise	Bandwidth = 10 Hz to 100 kHz; $I_{COREA}/I_{COREAA} = 5 \text{ mA}$		110	150	μV_{RMS}	
T_R	Rise Time	100% of I_{COREA}/I_{COREAA} ; 10% to 90% of V_{COREA}/V_{COREAA}			270	μs	
I_{SD}	Shut Down Current				1	μA	
I_{CC}	Short-circuit Current			330	400	mA	

- Notes: 1. Obtained by considering the parasitics of a TFBGA100 Package.
2. Obtained by using BG019 as reference voltage generator.

Control Modes

All digital signals are referred to the supply voltage V_{BAT1A} , V_{BAT1AA} .

Table 2. Truth Table

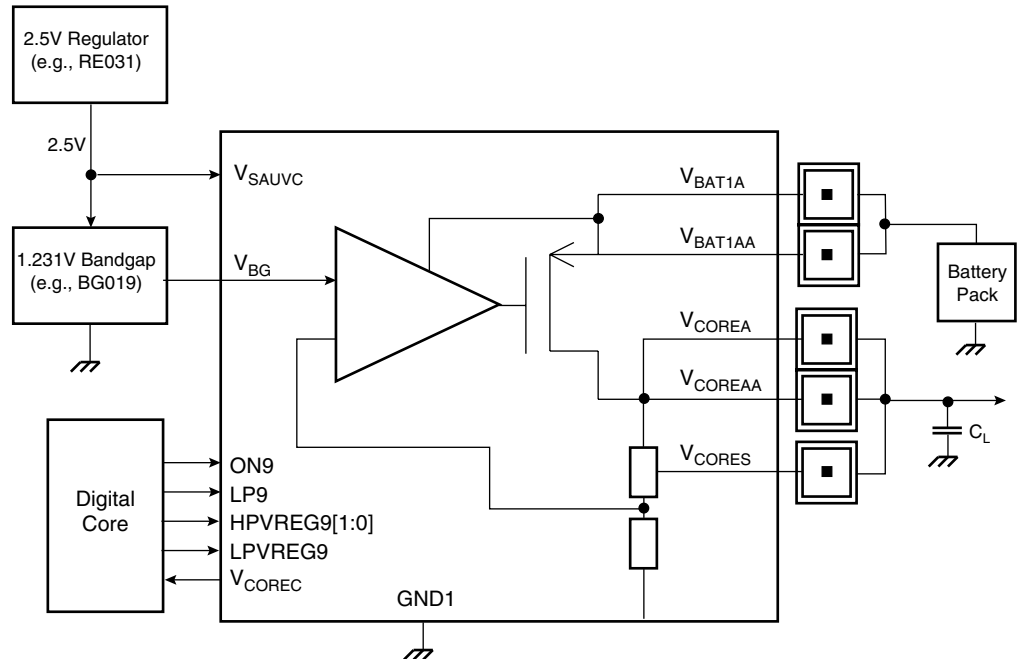
ON9	LP9	HPVREG[1]	HPVREG[0]	LPVREG	V_{COREA}/V_{COREAA}
0	X	X	X	X	Power down (High-Z)
1	0	0	0	X	Power on, Full Power 1.75V
1	0	0	1	X	Power on, Full Power 2.01V
1	0	1	0	X	Power on, Full Power 1.88V
1	0	1	1	X	Power on, Full Power 2.1V
1	1	X	X	0	Power on, Low Power 1.8V
1	1	X	X	1	Power on, Low Power 2V

Application Example

A ceramic capacitor (C_L) of 2.2 μF with ESR between 20 m Ω and 250 m Ω connected from V_{COREA}/V_{COREAA} to ground is needed for external compensation.

Description	Min	Typ	Max	Units
Capacitor (C_L)	1.8	2.2	2.6	μF

Figure 3. Application Example



RE030 1.75/2.1V 180 mA Dual Mode LDO Regulator

Typical Performance Characteristics (Conditions specified on page 11)

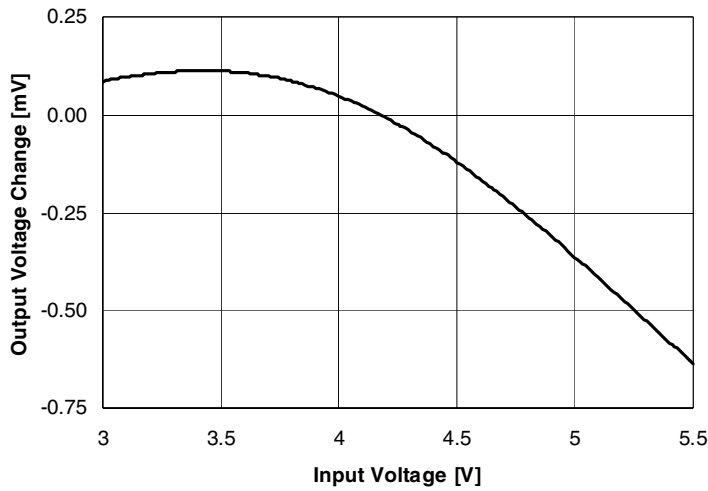
Note:

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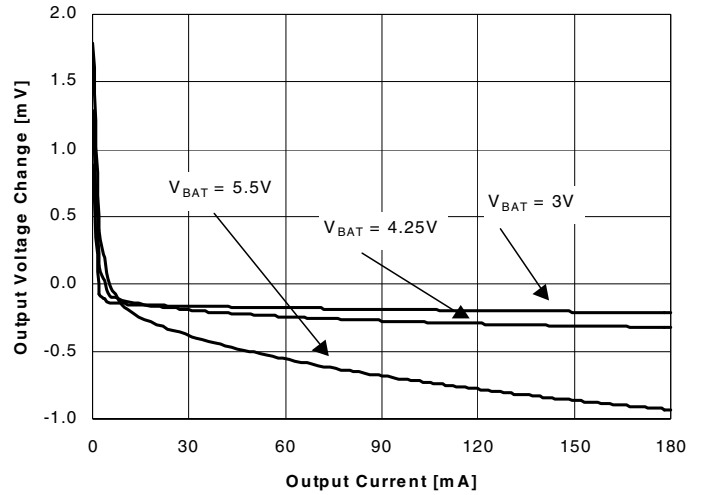
- Output Voltage (V_{CORE}) refers to V_{COREA}/V_{COREAA}
- Battery Voltage (V_{BAT}) refers to V_{BAT1A}/V_{BAT1AA}
- Output Current (I_{CORE}) refers to I_{COREA}/I_{COREAA}

Full-power Mode

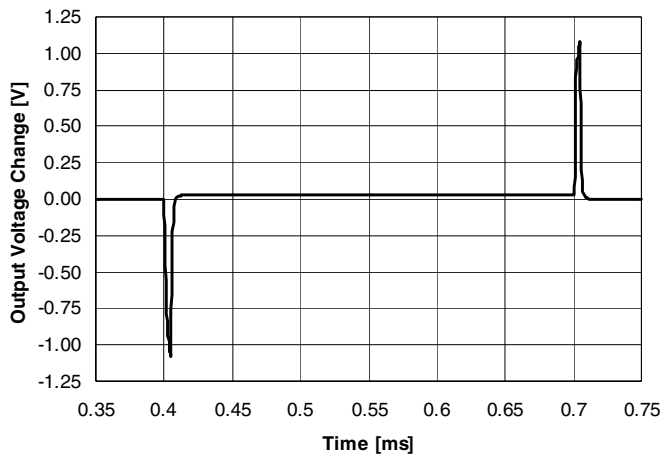
Static Line Regulation at Full Load



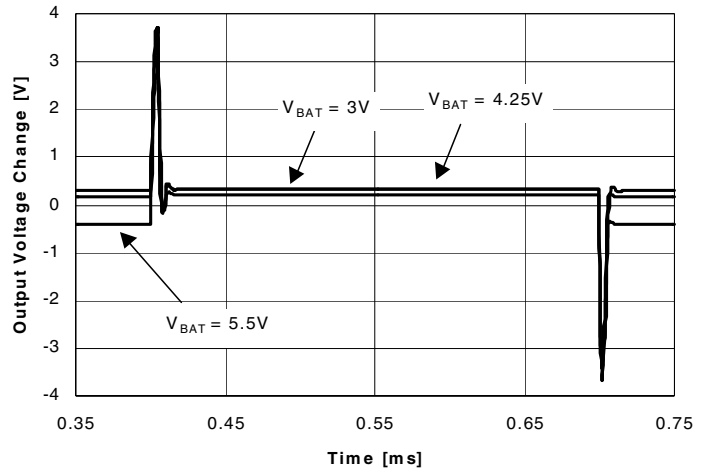
Static Load Regulation at Full Load



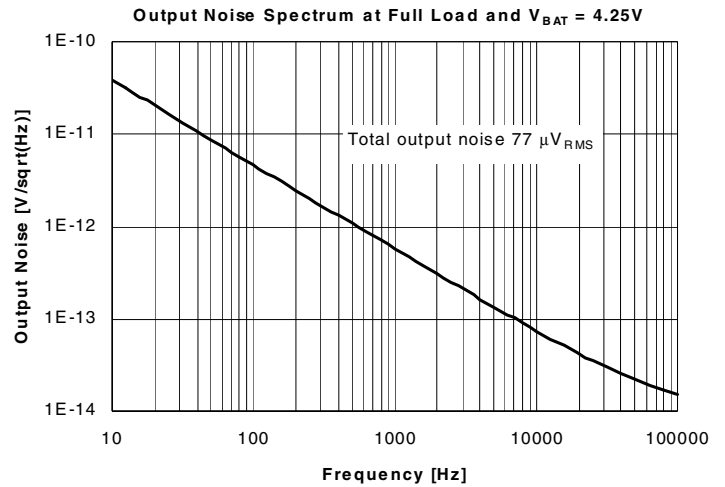
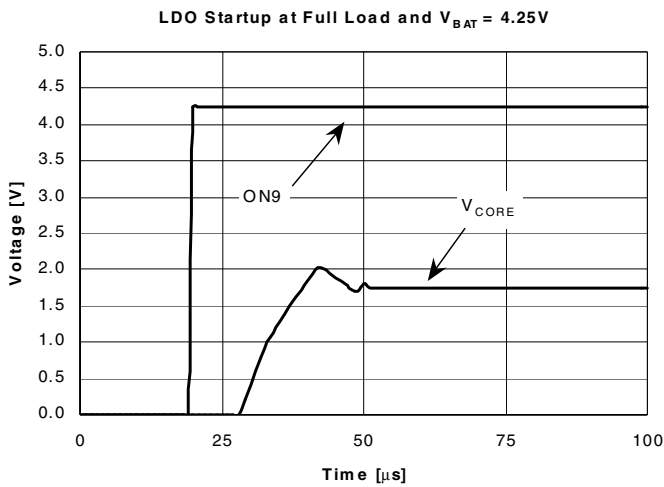
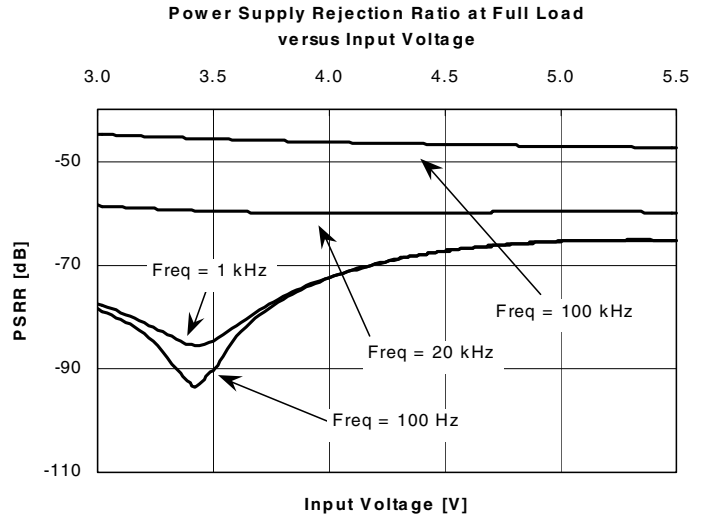
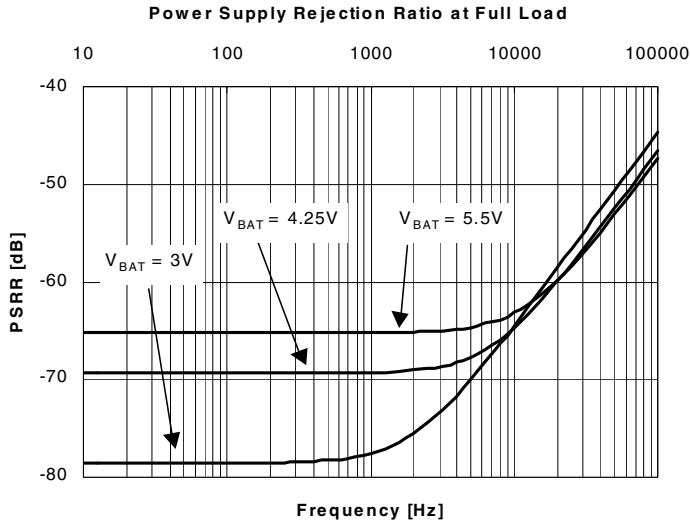
Transient Line Regulation at Full Load



Transient Load Regulation



Typical Performance Characteristics (Conditions specified on page 11)

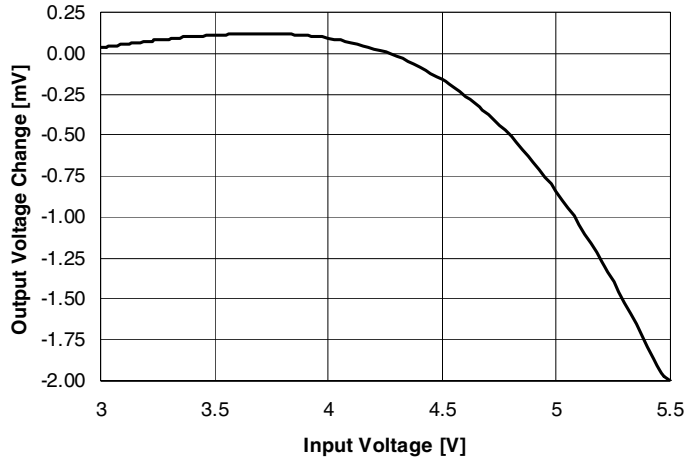


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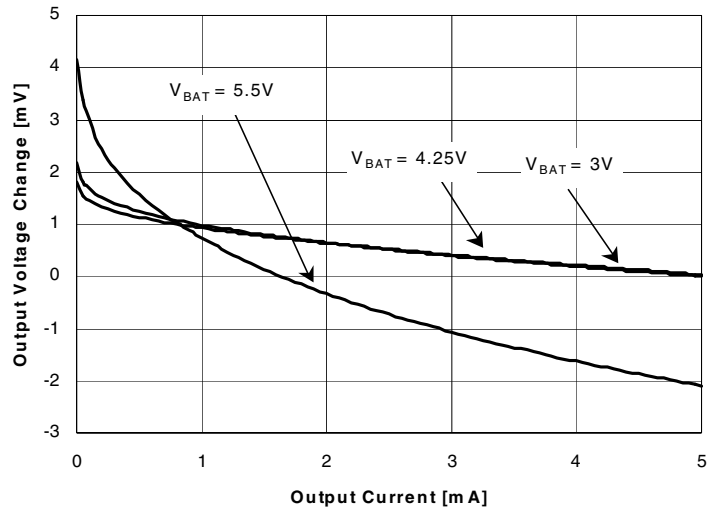
Typical Performance Characteristics (Conditions specified on page 11)

Low-power Mode

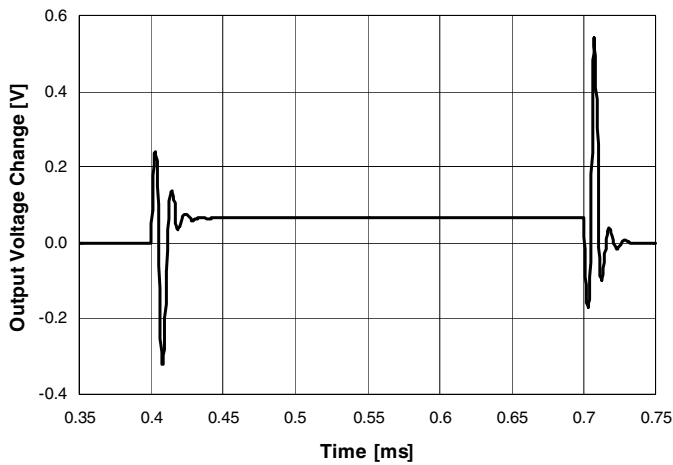
Static Line Regulation at Full Load



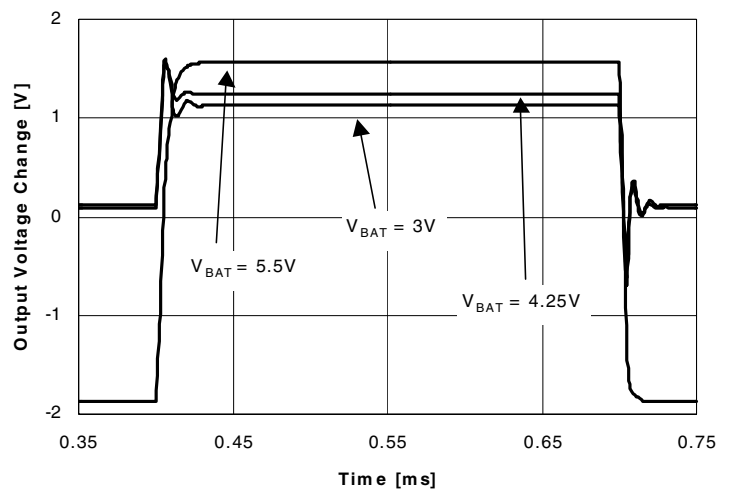
Static Load Regulation at Full Load



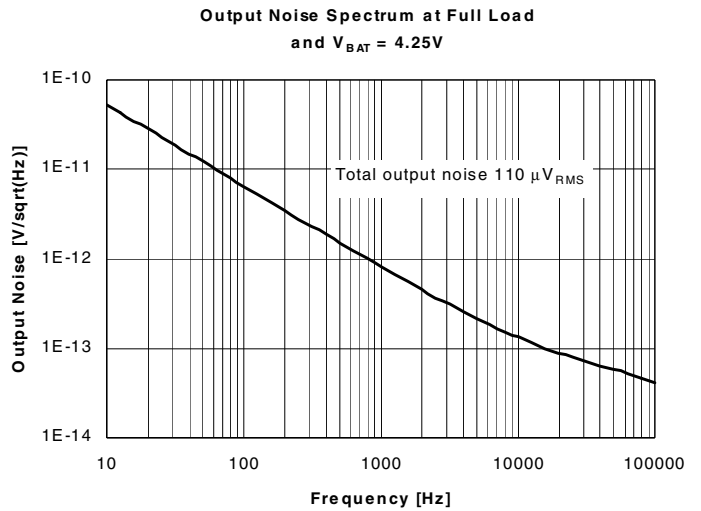
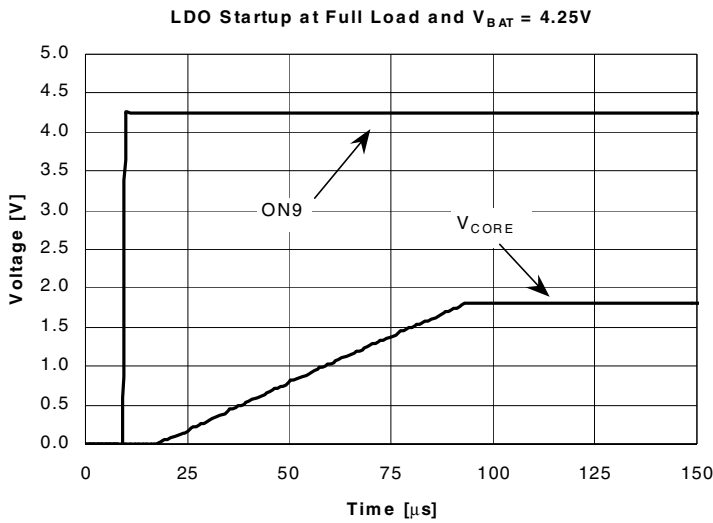
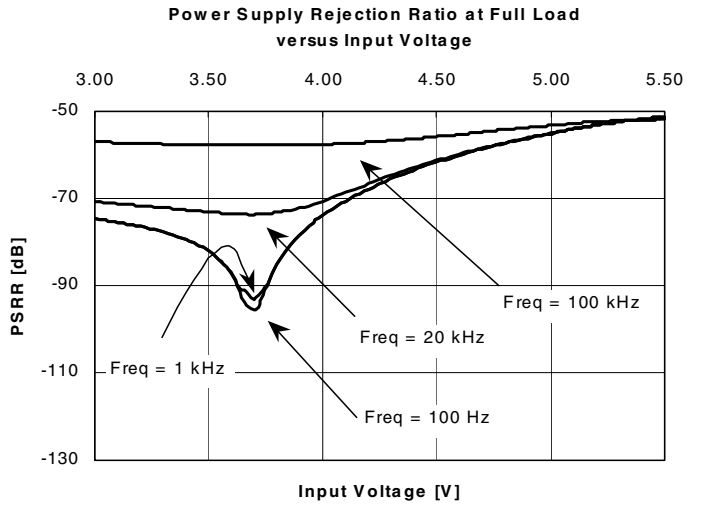
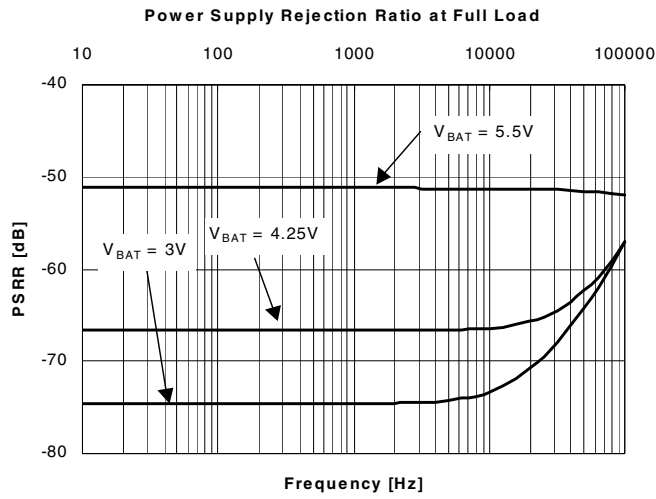
Transient Line Regulation at Full Load



Transient Load Regulation



Typical Performance Characteristics (Conditions specified on page 11)

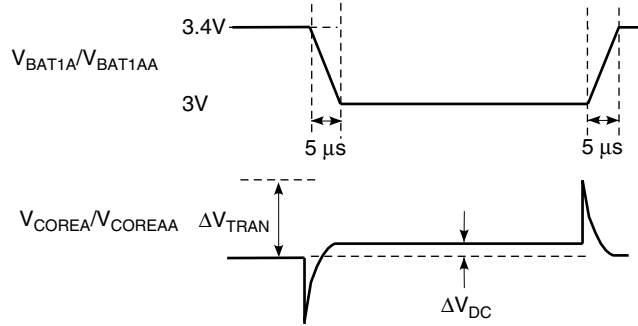


Terminology

Line Regulation

Measures the maximum transient and DC variations of the output voltage of the RE030 when the supply changes between two specified values with fixed load current; minimum rise time and fall time is 5 μ s.

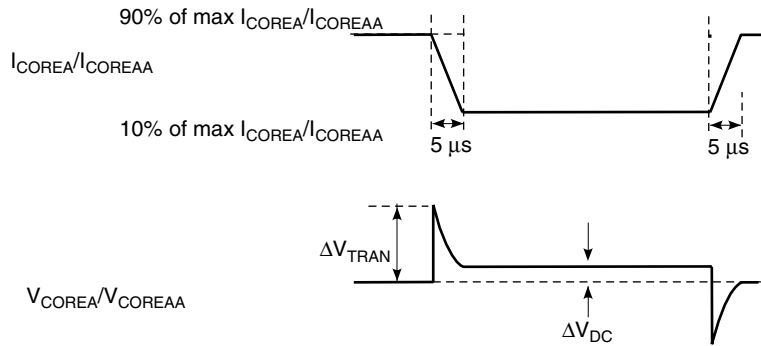
Figure 4. Line Regulation



Load Regulation

Measures the maximum transient and DC variations of the output voltage of the RE030 when the load current changes between two specified values with fixed power supply; minimum rise time and fall time is 5 μ s.

Figure 5. Load Regulation





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