Programmable Timing Control Hub™ for P4™

Recommended Application:

Brookdale and Brookdale-G chipset with P4 processor.

Output Features:

- 3 - Pairs of differential CPU clocks (differential current mode)
- 3 - 3V66 @ 3.3V
- 10 - PCI @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 2 - REF @ 3.3V, 14.318MHz
- 1 - 48_66MHz selectable @ 3.3V fixed
- 1 - 24_48MHz selectable @ 3.3V

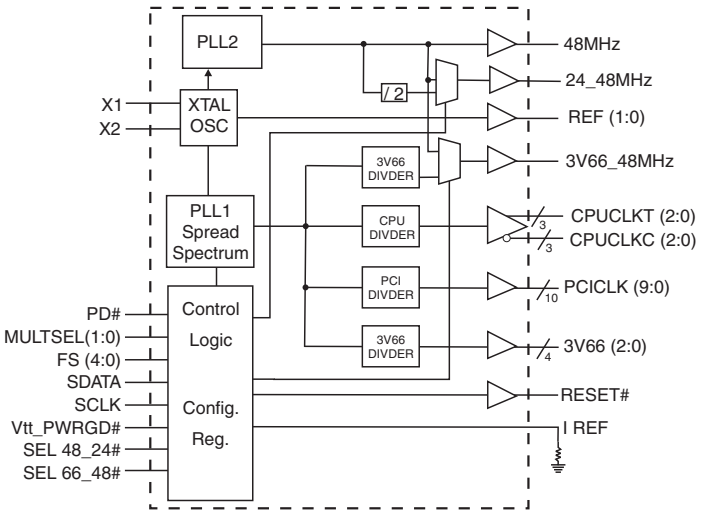
Features/Benefits:

- QuadRom™ frequency selection.
- Programmable output frequency.
- Programmable asynchronous 3V66 & PCI frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watchdog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input.

Key Specifications:

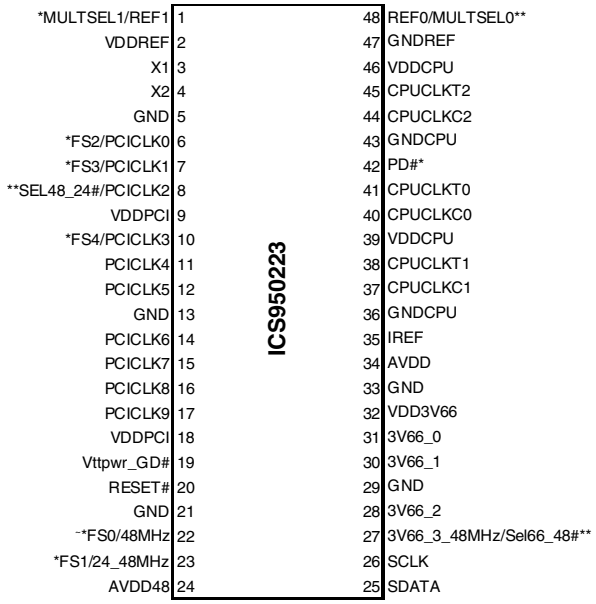
- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

Block Diagram



0496C—05/06/05

Pin Configuration



48-SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

- This output has 2X drive strength

Frequency Table

Bit4 FS4	Bit3 FS3	Bit2 FS2	Bit1 FS1	Bit0 FS0	CPU MHz	3V66 MHz	PCI MHz
0	0	0	0	0	102.00	68.00	34.00
0	0	0	0	1	105.00	70.00	35.00
0	0	0	1	0	108.00	72.00	36.00
0	0	0	1	1	111.00	74.00	37.00
0	0	1	0	0	114.00	76.00	38.00
0	0	1	0	1	117.00	78.00	39.00
0	0	1	1	0	120.00	80.00	40.00
0	0	1	1	1	123.00	82.00	41.00
0	1	0	0	0	126.00	72.00	36.00
0	1	0	0	1	130.00	74.29	37.14
0	1	0	1	0	136.00	68.00	34.00
0	1	0	1	1	140.00	70.00	35.00
0	1	1	0	0	144.00	72.00	36.00
0	1	1	0	1	148.00	74.00	37.00
0	1	1	1	0	152.00	76.00	38.00
0	1	1	1	1	156.00	78.00	39.00
1	0	0	0	0	160.00	80.00	40.00
1	0	0	0	1	164.00	82.00	41.00
1	0	0	1	0	166.60	66.64	33.32
1	0	0	1	1	170.00	68.00	34.00
1	0	1	0	0	175.00	70.00	35.00
1	0	1	0	1	180.00	72.00	36.00
1	0	1	1	0	185.00	74.00	37.00
1	0	1	1	1	190.00	76.00	38.00
1	1	0	0	0	66.80	66.80	33.40
1	1	0	0	1	100.20	66.80	33.40
1	1	0	1	0	133.60	66.80	33.40
1	1	0	1	1	200.40	66.80	33.40
1	1	1	0	0	66.67	66.67	33.34
1	1	1	0	1	100.00	66.67	33.33
1	1	1	1	0	200.00	66.67	33.33
1	1	1	1	1	133.33	66.67	33.33

General Description

The **ICS950223** is a single chip clock solution for desktop designs using the Intel Brookdale chipset with PC133 or DDR memory. It provides all necessary clock signals for such a system.

The **ICS950223** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment. With all these programmable features ICS's, TCH makes mother board testing, tuning and improvement very simple.

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*MULTSEL1/REF1	I/O	3.3V LVTTL input for selection the current multiplier for CPU outputs / 14.318 MHz reference clock.
2	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
3	X1	IN	Crystal input, Nominally 14.318MHz.
4	X2	OUT	Crystal output, Nominally 14.318MHz
5	GND	PWR	Ground pin.
6	*FS2/PCICLK0	I/O	Frequency select latch input pin / 3.3V PCI clock output.
7	*FS3/PCICLK1	I/O	Frequency select latch input pin / 3.3V PCI clock output.
8	**SEL48_24#/PCICLK2	I/O	Latched select input for 48/24MHz output. 0=24MHz, 1 = 48MHz / 3.3V PCI clock output.
9	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
10	*FS4/PCICLK3	I/O	Frequency select latch input pin / 3.3V PCI clock output.
11	PCICLK4	OUT	PCI clock output.
12	PCICLK5	OUT	PCI clock output.
13	GND	PWR	Ground pin.
14	PCICLK6	OUT	PCI clock output.
15	PCICLK7	OUT	PCI clock output.
16	PCICLK8	OUT	PCI clock output.
17	PCICLK9	OUT	PCI clock output.
18	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
19	Vttpwr_GD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input.
20	RESET#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
21	GND	PWR	Ground pin.
22	~*FS0/48MHz	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
23	*FS1/24_48MHz	I/O	Frequency select latch input pin / Fixed 24 or 48MHz clock output. 3.3V.
24	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

~ This output has 2X drive

Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
26	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
27	3V66_3_48MHz/Sel66_48#**	I/O	Selectable 66.66MHz, 48MHz clock output / Select input for 66.66/48MHz output. 0=48mHz, 1 = 66.66MHz
28	3V66_2	OUT	3.3V 66.66MHz clock output
29	GND	PWR	Ground pin.
30	3V66_1	OUT	3.3V 66.66MHz clock output
31	3V66_0	OUT	3.3V 66.66MHz clock output
32	VDD3V66	PWR	Power pin for the 3V66 clocks.
33	GND	PWR	Ground pin.
34	AVDD	PWR	3.3V Analog Power pin for Core PLL
35	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
36	GNDCPU	PWR	Ground pin for the CPU outputs
37	CPUCLKC1	OUT	"Complimentary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
38	CPUCLKT1	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
39	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
40	CPUCLKC0	OUT	"Complimentary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	PD#*	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms.
43	GNDCPU	PWR	Ground pin for the CPU outputs
44	CPUCLKC2	OUT	"Complimentary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	CPUCLKT2	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
46	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
47	GNDREF	PWR	Ground pin for the REF outputs.
48	REF0/MULTSEL0**	I/O	3.3V LVTTL input for selection the current multiplier for CPU outputs / 14.318 MHz reference clock.

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

~ This output has 2X drive

Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PWRDWN# = 0)	40mA
Full Active	360mA

CPUCLK Swing Select Functions

MULTSEL0	MULTSEL1	Board Target Trace/Term Z	Reference R, Iref= Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
0	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.71V @ 50
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

General I^2C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

Table1: QuadRom Frequency Selection Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	3V66	PCI	Spreading
X	X	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	
0	0	0	0	0	0	0	102.00	68.00	34.00	Spread Off
0	0	0	0	0	0	1	105.00	70.00	35.00	Spread Off
0	0	0	0	0	1	0	108.00	72.00	36.00	Spread Off
0	0	0	0	0	1	1	111.00	74.00	37.00	Spread Off
0	0	0	0	1	0	0	114.00	76.00	38.00	Spread Off
0	0	0	0	1	0	1	117.00	78.00	39.00	Spread Off
0	0	0	0	1	1	0	120.00	80.00	40.00	Spread Off
0	0	0	0	1	1	1	123.00	82.00	41.00	Spread Off
0	0	0	1	0	0	0	126.00	72.00	36.00	Spread Off
0	0	0	1	0	0	1	130.00	74.29	37.14	Spread Off
0	0	0	1	0	1	0	136.00	68.00	34.00	Spread Off
0	0	0	1	0	1	1	140.00	70.00	35.00	Spread Off
0	0	0	1	1	0	0	144.00	72.00	36.00	Spread Off
0	0	0	1	1	0	1	100.99	67.32	33.66	Center Spread
0	0	0	1	1	1	0	134.66	67.32	33.66	Center Spread
0	0	0	1	1	1	1	133.99	67.00	35.00	Center Spread
0	0	1	0	0	0	0	160.00	80.00	40.00	Spread Off
0	0	1	0	0	0	1	164.00	82.00	41.00	Spread Off
0	0	1	0	0	1	0	166.60	66.64	33.32	Center Spread
0	0	1	0	0	1	1	170.00	68.00	34.00	Spread Off
0	0	1	0	1	0	0	175.00	70.00	35.00	Spread Off
0	0	1	0	1	0	1	180.00	72.00	36.00	Spread Off
0	0	1	0	1	1	0	185.00	74.00	37.00	Spread Off
0	0	1	0	1	1	1	190.00	76.00	38.00	Spread Off
0	0	1	1	0	0	0	66.80	66.80	33.40	Center Spread
0	0	1	1	0	0	1	100.20	66.80	33.40	Center Spread
0	0	1	1	0	1	0	200.40	66.80	33.40	Center Spread
0	0	1	1	0	1	1	133.60	66.80	33.40	Center Spread
0	0	1	1	1	0	0	66.67	66.67	33.34	Down Spread
0	0	1	1	1	0	1	100.00	66.67	33.33	Down Spread
0	0	1	1	1	1	0	200.00	66.67	33.33	Down Spread
0	0	1	1	1	1	1	133.33	66.67	33.33	Down Spread

Table1: QuadRom Frequency Selection Table Continued

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	3V66	PCI
X	X	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz
0	1	0	0	0	0	0	114.00	76.00	38.00
0	1	0	0	0	0	1	115.00	76.67	38.33
0	1	0	0	0	1	0	116.00	77.33	38.67
0	1	0	0	0	1	1	117.00	78.00	39.00
0	1	0	0	1	0	0	118.00	78.67	39.33
0	1	0	0	1	0	1	119.00	79.33	39.67
0	1	0	0	1	1	0	120.00	80.00	40.00
0	1	0	0	1	1	1	121.00	80.67	40.33
0	1	0	1	0	0	0	122.00	81.33	40.67
0	1	0	1	0	0	1	123.00	82.00	41.00
0	1	0	1	0	1	0	125.00	83.33	41.67
0	1	0	1	0	1	1	127.00	84.67	42.33
0	1	0	1	1	0	0	129.00	86.00	43.00
0	1	0	1	1	0	1	131.00	87.33	43.67
0	1	0	1	1	1	0	133.00	88.67	44.33
0	1	0	1	1	1	1	135.00	90.00	45.00
0	1	1	0	0	0	0	152.00	76.00	38.00
0	1	1	0	0	0	1	153.00	76.50	38.25
0	1	1	0	0	1	0	154.00	77.00	38.50
0	1	1	0	0	1	1	155.00	77.50	38.75
0	1	1	0	1	0	0	156.00	78.00	39.00
0	1	1	0	1	0	1	157.00	78.50	39.25
0	1	1	0	1	1	0	158.00	79.00	39.50
0	1	1	0	1	1	1	159.00	79.50	39.75
0	1	1	1	0	0	0	160.00	80.00	40.00
0	1	1	1	0	0	1	161.00	80.50	40.25
0	1	1	1	0	1	0	162.00	81.00	40.50
0	1	1	1	0	1	1	163.00	81.50	40.75
0	1	1	1	1	0	0	164.00	82.00	41.00
0	1	1	1	1	0	1	165.00	82.50	41.25
0	1	1	1	1	1	0	144.00	72.00	36.00
0	1	1	1	1	1	1	148.00	74.00	37.00

Table1: QuadRom Frequency Selection Table Continued

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	3V66	PCI
X	X	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz
1	0	0	0	0	0	0	66.67	66.67	33.34
1	0	0	0	0	0	1	68.00	68.00	34.00
1	0	0	0	0	1	0	70.00	70.00	35.00
1	0	0	0	0	1	1	72.00	72.00	36.00
1	0	0	0	1	0	0	74.00	74.00	37.00
1	0	0	0	1	0	1	76.00	76.00	38.00
1	0	0	0	1	1	0	78.00	78.00	39.00
1	0	0	0	1	1	1	80.00	80.00	40.00
1	0	0	1	0	0	0	82.00	82.00	41.00
1	0	0	1	0	0	1	84.00	84.00	42.00
1	0	0	1	0	1	0	86.00	86.00	43.00
1	0	0	1	0	1	1	88.00	88.00	44.00
1	0	0	1	1	0	0	90.00	90.00	45.00
1	0	0	1	1	0	1	92.00	92.00	46.00
1	0	0	1	1	1	0	94.00	94.00	47.00
1	0	0	1	1	1	1	96.00	96.00	48.00
1	0	1	0	0	0	0	98.00	98.00	49.00
1	0	1	0	0	0	1	100.00	100.00	50.00
1	0	1	0	0	1	0	102.00	102.00	51.00
1	0	1	0	0	1	1	104.00	104.00	52.00
1	0	1	0	1	0	0	106.00	106.00	53.00
1	0	1	0	1	0	1	108.00	108.00	54.00
1	0	1	0	1	1	0	110.00	110.00	55.00
1	0	1	0	1	1	1	112.00	112.00	56.00
1	0	1	1	0	0	0	166.67	66.67	33.33
1	0	1	1	0	0	1	167.00	66.80	33.40
1	0	1	1	0	1	0	168.00	67.20	33.60
1	0	1	1	0	1	1	169.00	67.60	33.80
1	0	1	1	1	0	0	170.00	68.00	34.00
1	0	1	1	1	0	1	171.00	68.40	34.20
1	0	1	1	1	1	0	172.00	68.80	34.40
1	0	1	1	1	1	1	173.00	69.20	34.60

Table1: QuadRom Frequency Selection Table Continued

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	3V66	PCI
X	X	FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz
1	1	0	0	0	0	0	174.00	69.60	34.80
1	1	0	0	0	0	1	175.00	70.00	35.00
1	1	0	0	0	1	0	176.00	70.40	35.20
1	1	0	0	0	1	1	177.00	70.80	35.40
1	1	0	0	1	0	0	178.00	71.20	35.60
1	1	0	0	1	0	1	179.00	71.60	35.80
1	1	0	0	1	1	0	180.00	72.00	36.00
1	1	0	0	1	1	1	181.00	72.40	36.20
1	1	0	1	0	0	0	160.00	53.33	26.67
1	1	0	1	0	0	1	165.00	55.00	27.50
1	1	0	1	0	1	0	170.00	56.67	28.33
1	1	0	1	0	1	1	175.00	58.33	29.17
1	1	0	1	1	0	0	180.00	60.00	30.00
1	1	0	1	1	0	1	185.00	61.67	30.83
1	1	0	1	1	1	0	190.00	63.33	31.67
1	1	0	1	1	1	1	195.00	65.00	32.50
1	1	1	0	0	0	0	200.00	66.67	33.33
1	1	1	0	0	0	1	201.00	67.00	33.50
1	1	1	0	0	1	0	202.00	67.33	33.67
1	1	1	0	0	1	1	203.00	67.67	33.83
1	1	1	0	1	0	0	204.00	68.00	34.00
1	1	1	0	1	0	1	206.00	68.67	34.33
1	1	1	0	1	1	0	208.00	69.33	34.67
1	1	1	0	1	1	1	210.00	70.00	35.00
1	1	1	1	0	0	0	212.00	70.67	35.33
1	1	1	1	0	0	1	214.00	71.33	35.67
1	1	1	1	0	1	0	216.00	72.00	36.00
1	1	1	1	0	1	1	218.00	72.67	36.33
1	1	1	1	1	0	0	220.00	73.33	36.67
1	1	1	1	1	0	1	222.00	74.00	37.00
1	1	1	1	1	1	0	224.00	74.67	37.33
1	1	1	1	1	1	1	226.00	75.33	37.67

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	FS6	Freq Select Bit 6	RW	See Table 1: QuadRom Frequency Selection Table		0
Bit 5	-	FS5	Freq Select Bit 5	RW			0
Bit 4	-	FS4	Freq Select Bit 4	RW			0
Bit 3	-	FS3	Freq Select Bit 3	RW			0
Bit 2	-	FS2	Freq Select Bit 2	RW			0
Bit 1	-	FS1	Freq Select Bit 1	RW			0
Bit 0	-	FS0	Freq Select Bit 0	RW			0

I²C Table: Spreading and Device Behavior Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS1	Spread Select 1	RW	See Table 2: Spread Spectrum Table		0
Bit 6	-	SS0	Spread Select 0	RW			0
Bit 5	-	SS_EN	Spread Enable Control	RW	OFF	ON	1
Bit 4	-	WDS_Status	WD Soft Alarm Status	RW	Normal	Alarm	0
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	45/44	CPUT2/CPUC2	Output Control	RW	Disable	Enable	1
Bit 1	38/37	CPUT1/CPUC1	Output Control	RW	Disable	Enable	1
Bit 0	41/40	CPUT0/CPUC0	Output Control	RW	Disable	Enable	1

Table2: Spread Spectrum Select

SS1 (Byte 1 bit 7)	SS0 (Byte 1 bit 6)	Spread %	Note
0	0	0.35%	Spread 1
0	1	0.50%	Spread 2
1	0	0.75%	Spread 3
1	1	1.00%	Spread 4

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	AEN#	3V66/PCI Freq Source Select	RW	CPU_PLL Sync	FIX_PLL Async	0
Bit 6	17	PCICLK9	Output Control	RW	Disable	Enable	1
Bit 5	16	PCICLK8	Output Control	RW	Disable	Enable	1
Bit 4	15	PCICLK7	Output Control	RW	Disable	Enable	1
Bit 3	14	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 2	12	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 1	11	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 0	10	PCICLK3	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	23	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 6	22	48MHz	Output Control	RW	Disable	Enable	1
Bit 5	-	GR_EN	Geashift Reset Enable	RW	ON	OFF	0
Bit 4	-	24_48 FS Source	24_48 Frequency H/W / IIC Select	RW	Latch Inputs	IIC	0
Bit 3	-	FS 24_48	Sel24_48	RW	24MHz	48MHz	0
Bit 2	8	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	7	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	6	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	66_48 FS Source	66_48 Frequency H/W / IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	FS 66_48#	Sel66_48#	RW	48MHz	66.66MHz	0
Bit 5	31	3V66_0	Output Control	RW	Disable	Enable	1
Bit 4	30	3V66_1	Output Control	RW	Disable	Enable	1
Bit 3	48	REF0	Output Control	RW	Disable	Enable	1
Bit 2	1	REF1	Output Control	RW	Disable	Enable	1
Bit 1	27	3V66_3	Output Control	RW	Disable	Enable	1
Bit 0	28	3V66_2	Output Control	RW	Disable	Enable	1

I²C Table: 3V66 & PCICLK Asynchronous Frequency Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N PLL2 Div0	The decimal representation of N PLL2 Div (0:7) + 8 is equal to VCO divider value for PLL2.	RW	-	-	X
Bit 6	-	N PLL2 Div1		RW	-	-	X
Bit 5	-	N PLL2 Div2		RW	-	-	X
Bit 4	-	N PLL2 Div3		RW	-	-	X
Bit 3	-	N PLL2 Div4		RW	-	-	X
Bit 2	-	N PLL2 Div5		RW	-	-	X
Bit 1	-	N PLL2 Div6		RW	-	-	X
Bit 0	-	N PLL2 Div7		RW	-	-	X

I²C Table: Read Back Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDHRB	WD Hard Alarm Status Read back	R	-	-	X
Bit 6	-	SEL48_24RB	Sel48_24# Read Back	R	-	-	X
Bit 5	-	SEL66_48RB	Sel66_48# Read Back	R		-	X
Bit 4	-	FS4RB	FS4 Read back	R	-	-	X
Bit 3	-	FS3RB	FS3 Read back	R	-	-	X
Bit 2	-	FS2RB	FS2 Read back	R	-	-	X
Bit 1	-	FS1RB	FS1 Read back	R	-	-	X
Bit 0	-	FS0RB	FS0 Read back	R	-	-	X

I²C Table: Vendor & Revision ID Register

Byte 7		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		RID3	REVISION ID	R	-	-	1
Bit 6	-		RID2		R	-	-	1
Bit 5	-		RID1		R	-	-	0
Bit 4	-		RID0		R	-	-	1
Bit 3	-		VID3	VENDOR ID	R	-	-	0
Bit 2	-		VID2		R	-	-	0
Bit 1	-		VID1		R	-	-	0
Bit 0	-		VID0		R	-	-	1

I²C Table: Byte Count Register

Byte 8		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-		BC6		RW	-	-	0
Bit 5	-		BC5		RW	-	-	0
Bit 4	-		BC4		RW	-	-	0
Bit 3	-		BC3		RW	-	-	1
Bit 2	-		BC2		RW	-	-	1
Bit 1	-		BC1		RW	-	-	1
Bit 0	-		BC0		RW	-	-	1

I²C Table: Watchdog Timer Register

Byte 9		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		WD7	These bits represent X*290ms the watchdog timer will wait before it goes to alarm mode. Default is 8 X 290ms =2.32 seconds	RW	-	-	0
Bit 6	-		WD6		RW	-	-	0
Bit 5	-		WD5		RW	-	-	0
Bit 4	-		WD4		RW	-	-	0
Bit 3	-		WD3		RW	-	-	1
Bit 2	-		WD2		RW	-	-	0
Bit 1	-		WD1		RW	-	-	0
Bit 0	-		WD0		RW	-	-	0

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		M/NEN	M/N Programming Enable	RW	Latched Input	IIC Prog. B(11:17)	0
Bit 6	-		WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-		WDFSEN	WD Safe Frequency Mode	RW	Latched FS/Byte0	WD B10 b(4:0)	0
Bit 4	-		WD SF4	Writing to these bit will configure the safe frequency as Byte 0 Bit (6:0)	RW	-	-	1
Bit 3	-		WD SF3		RW	-	-	1
Bit 2	-		WD SF2		RW	-	-	0
Bit 1	-		WD SF1		RW	-	-	0
Bit 0	-		WD SF0		RW	-	-	1

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	M Div6	The decimal representation of M Div (6:0) +2 is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 5	-	M Div5		RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	The decimal representation of N Div (8:0) + 8 is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	N Div6		RW	-	-	X
Bit 5	-	N Div5		RW	-	-	X
Bit 4	-	N Div4		RW	-	-	X
Bit 3	-	N Div3		RW	-	-	X
Bit 2	-	N Div2		RW	-	-	X
Bit 1	-	N Div1		RW	-	-	X
Bit 0	-	N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	1
Bit 6	-	Reserved	Reserved	R	-	-	0
Bit 5	-	SSP13	It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 4	-	SSP12		RW	-	-	X
Bit 3	-	SSP11		RW	-	-	X
Bit 2	-	SSP10		RW	-	-	X
Bit 1	-	SSP9		RW	-	-	X
Bit 0	-	SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		CPU Div3	CPUCLK2 divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table		X
Bit 6		CPU Div2		RW			X
Bit 5		CPU Div1		RW			X
Bit 4		CPU Div0		RW			X
Bit 3	-	CPU Div3	CPUCLK [1:0] divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table		X
Bit 2	-	CPU Div2		RW			X
Bit 1	-	CPU Div1		RW			X
Bit 0	-	CPU Div0		RW			X

Table 3: CPU, AGP and PCI Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	Bit	00		01		10		11	MSB
			1		2		4		8
	00	0	2	100	4	1000	8	1100	16
	01	1	3	101	6	1001	12	1101	24
	10	10	5	110	10	1010	20	1110	40
	11	11	7	111	14	1011	28	1111	56
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	3V66 Div3	3V66 [3:2] divider ratio can be configured via these 4 bits individually	RW	See Table 3: Divider Ratio Combination Table		X
Bit 6	-	3V66 Div2		RW			X
Bit 5	-	3V66 Div1		RW			X
Bit 4	-	3V66 Div0		RW			X
Bit 3	-	3V66 Div3	3V66 [1:0] divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table		X
Bit 2	-	3V66 Div2		RW			X
Bit 1	-	3V66 Div1		RW			X
Bit 0	-	3V66 Div0		RW			X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	3V66INV	3V66[3:2] Phase Invert	RW	Default	Inverse	X
Bit 6	-	3V66INV	3V66[1:0] Phase Invert	RW	Default	Inverse	X
Bit 5	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-	PCI Div3	PCI divider ratio can be configured via these 4 bits individually.	RW	See Table 3: Divider Ratio Combination Table		X
Bit 2	-	PCI Div2		RW			X
Bit 1	-	PCI Div1		RW			X
Bit 0	-	PCI Div0		RW			X

I²C Table: Group Skew Control Register and Frequency Select PLL3

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUSkw1	CPU_T2/C2 Skew Control	RW	See Table 4: 4-Steps Skew Programming Table		1
Bit 6	-	CPUSkw0		RW			0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	CPUSkw1	CPU_T/C [1:0]Skew Control	RW	See Table 4: 4-Steps Skew Programming Table		1
Bit 2	-	CPUSkw0		RW			0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

Table 4: 4-Steps Skew Programming Table

4 Step	0	1	LSB
0	0ps	250ps	-
1	500ps	750ps	-
MSB	-	-	-

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	3V66Skw3	3V66 [3:0] Skew Control	RW	16-Steps Skew Control. This byte will advance or delay the skew by 100ps per step		0
Bit 2	-	3V66Skw2		RW			1
Bit 1	-	3V66Skw1		RW			0
Bit 0	-	3V66Skw0		RW			0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISkw3	PCI Skew Control	RW	16-Steps Skew Control. This byte will advance or delay the skew by 100ps per step		1
Bit 6	-	PCISkw2		RW			0
Bit 5	-	PCISkw1		RW			0
Bit 4	-	PCISkw0		RW			0
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISlw1	PCICLK_2 Slew Rate Control	RW	-	-	1
Bit 6	-	PCISlw0		RW	-	-	0
Bit 5	-	PCISlw1	PCICLK [1:0] Slew Rate Control	RW	-	-	1
Bit 4	-	PCISlw0		RW	-	-	0
Bit 3	-	3V66Slw1	3V66[3:2] Slew Rate Control	RW	-	-	1
Bit 2	-	3V66Slw1		RW	-	-	0
Bit 1	-	3V66Slw1	3V66 [1:0] Slew Rate Control	RW	-	-	1
Bit 0	-	3V66Slw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REFSlw1	REF Slew Rate Control	RW	-	-	1
Bit 6	-	REFSlw0		RW	-	-	0
Bit 5	-	PCISlw1	PCI [9:7] Slew Rate Control	RW	-	-	1
Bit 4	-	PCISlw0		RW	-	-	0
Bit 3	-	PCISlw1	PCI [6:5] Slew Rate Control	RW	-	-	1
Bit 2	-	PCISlw0		RW	-	-	0
Bit 1	-	PCISlw1	PCI [4:3] Slew Rate Control	RW	-	-	1
Bit 0	-	PCISlw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	48Slw1	48 Slew Rate Control	RW	-	-	1
Bit 2	-	48Slw0		RW	-	-	0
Bit 1	-	24_48Slw1	24_48 Slew Rate Control	RW	-	-	1
Bit 0	-	24_48Slw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 25	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	-	Transfer Mode Control		Transfer	No transfer	0

Absolute Maximum Ratings

Supply Voltage ..... 5.5 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Case Temperature ..... 115°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD(op)}$	C_L = 0 pF; Select @ 100MHz		217	260	mA
Power Down Supply Current	I_{DDPD}	C_L = 0 pF; With input address to Vdd or GND		31	40	mA
Input frequency	F_i	V_{DD} = 3.3 V;	11	14.31818	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.		1	1.8	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V	1.5	2.5	3.5	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKT/C

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Voltage High	VHigh	Statistical measurement on single	660	718	850	mV
Voltage Low	VLow		-150	17	150	
Max Voltage	Vovs	Measurement on single ended signal using		730	1150	mV
Min Voltage	Vuds		-450	-7		
Crossing Voltage (abs)	Vcross(abs)		250	340	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		15	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	324	700	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	453	700	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50.3	55	%
Skew	t_{sk3}	V_T = 50%		58	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		56	150	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			33.33		MHz
Output High Voltage	V_{OH}[1]	I_{OH} = -18mA	2.1			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 9.4mA			0.4	V
Output High Current	I_{OH}[1]	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL}[1]	V_{OL} = 0.8 V	16		57	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.7	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.5	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		61	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		114	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.6		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.9	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.7	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.5	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		71	250	ps
Jitter	$t_{additive}$[1]	V_T = 1.5 V		105	250	ps

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			48		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	V OH@MIN = 1.0 V,	-29			
		$V_{OH@MAX}$ = 3.135 V			-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
48MHz Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1	2	ns
48MHz Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1	2	ns
24MHz Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.3	2	ns
24MHz Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.4	2	ns
48 MHz Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.3	55	%
24MHz Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50.2	55	%
48 MHz Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		139	350	ps
24MHz Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		123	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			14.3		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -12mA			0.4	V
Output Low Voltage	V_{OL}[1]	I_{OL} = 9 mA				V
Output High Current	I_{OH}[1]	V_{OH} = 2.0 V			-33	mA
Output Low Current	I_{OL}[1]	V_{OL} = 0.8 V			38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	2.2	4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	2.3	4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	54.1	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		129	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period. Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

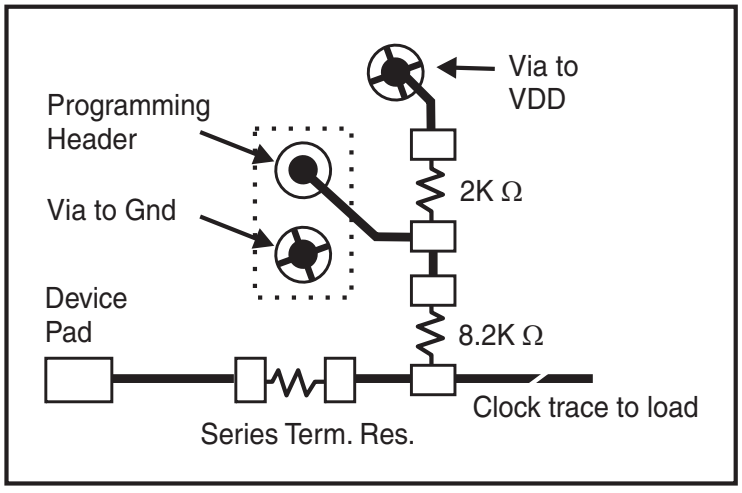
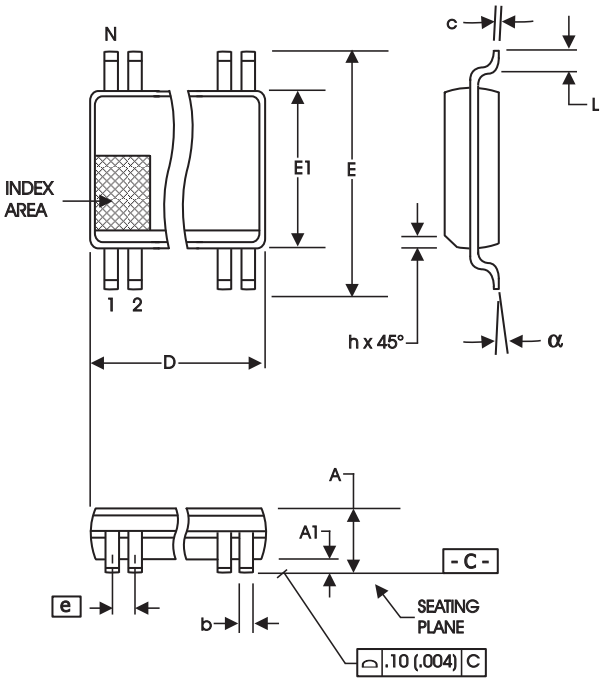


Fig. 1



300 mil SSOP Package

300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950223yFLFT

Example:

ICS XXXXXX y F LF - T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0496C—05/06/05

Revision History

Rev.	Issue Date	Description	Page #
C	5/6/2005	Added LF Ordering Information	23