TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π -MOSV)

TPCS8004

High-Speed Switching Applications Switching Regulator Applications DC-DC Converter Applications

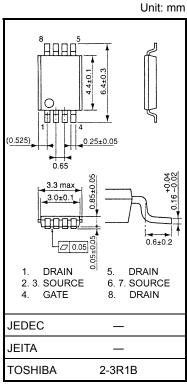
- Small footprint due to small and thin package
- Low drain-source ON resistance: RDS (ON) = $0.56~\Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 1.8 S$ (typ.)
- Low leakage current: $I_{DSS} = 100 \,\mu\text{A}$ (max) ($V_{DS} = 200 \,\text{V}$)
- Enhancement model: $V_{th} = 1.5 \sim 3.5 \text{ V (V}_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA})$

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	200	V	
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	200	V	
Gate-source voltage		V _{GSS}	±20	V	
Drain current	DC (Note 1)	I _D	1.3	Α	
	Pulse (Note 1)	I _{DP}	5.2		
Drain power dissipation (t = 10 s) (Note 2a)		P_{D}	1.5	W	
Drain power dissipation (t = 10 s) (Note 2b)		P _D	0.6	VV	
Single pulse avalanche energy(Note3)		E _{AS}	1.05	mJ	
Avalanche current		I _{AR}	1.3	Α	
Repetitive avalanche energy (Note2a, Note 4)		E _{AR}	0.15	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	−55~150	°C	

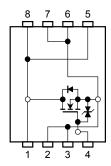
Note 1, Note 2, Note 3 and Note 4: See the next page.

This transistor is an electrostatic-sensitive device. Please handle with caution.



Weight: 0.035 g (typ.)

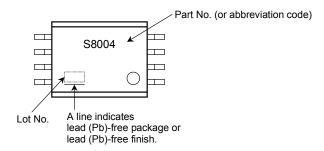
Circuit Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit	
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	R _{th (ch-a)}	83.3	°C/W	
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	R _{th (ch-a)}	208	°C/W	

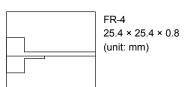
Marking (Note 5)



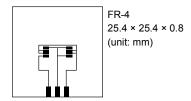
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:

a) Device mounted on a glass-epoxy board (a)



b) Device mounted on a glass-epoxy board (b)



Note 3: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 1.0 mH, R_G = 25 Ω , I_{AR} = 1.3 A

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: O on lower right of the marking indicates Pin 1.

Weekly code: (Three digits)
 Week of manufacture
 (01 for the first week of a year: sequential number up to 52 or 53)
 Year of manufacture
 (The last digit of a year)

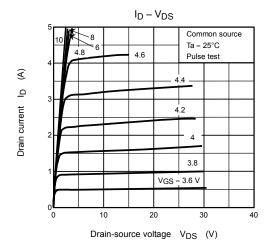
Electrical Characteristics (Ta = 25°C)

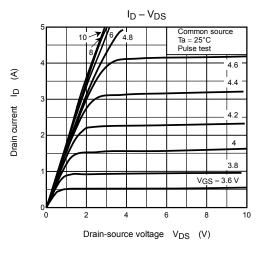
Ch	aracteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cui	rent	I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±10	μА
Drain cut-OFF current		I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V	_	_	100	μА
Drain-source bre	akdown voltage	V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	200	_	_	V
Gate threshold v	oltage	V _{th}	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA}$	1.5	_	3.5	V
Drain-source ON	resistance	R _{DS (ON)}	$V_{GS} = 10 \text{ V}, I_D = 0.6 \text{ A}$	_	0.56	0.8	Ω
Forward transfer	admittance	Y _{fs}	$V_{DS} = 10 \text{ V}, I_D = 0.6 \text{ A}$	0.9	1.8	_	S
Input capacitance		C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	380	_	pF
Reverse transfer capacitance		C _{rss}			40	_	pF
Output capacitance		C _{oss}			140	_	pF
Switching time	Rise time	t _r	V _{GS} 10 V	_	4.5	_	
	Turn-ON time	t _{on}		_	12		
	Fall time	t _f		_	23	_	ns
	Turn-OFF time	t _{off}	Duty ≦ 1%, t _w = 10 μs	_	54	_	
Total gate charge (gate-source plus gate-drain)		Qg	$V_{DD} \simeq 160 \text{ V}, V_{GS} = 10 \text{ V},$ $I_{D} = 1.3 \text{ A}$	_	12	_	nC
Gate-source charge		Q _{gs}			8	_	nC
Gate-drain ("miller") charge		Q _{gd}			4	_	nC

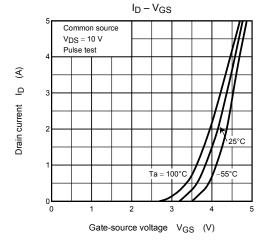
Source-Drain Ratings and Characteristics (Ta = 25°C)

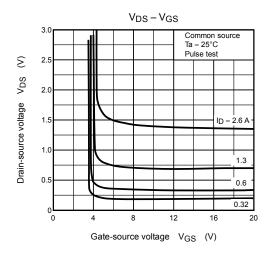
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain reverse current (pulse) (Note 1)	I _{DRP}	_		_	5.2	Α
Forward voltage (diode)	V _{DSF}	I _{DR} = 1.3 A, V _{GS} = 0 V	_	_	-2.0	V
Reverse recovery time	t _{rr}	$I_{DR} = 1.3 \text{ A}, V_{GS} = 0 \text{ V},$	_	89	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 100 A/μs	_	230	_	nC

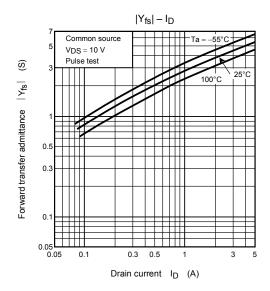
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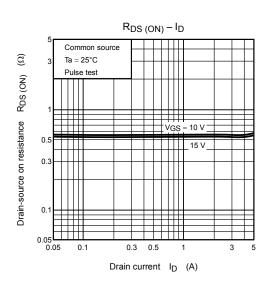


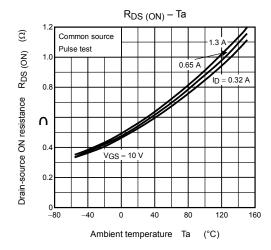


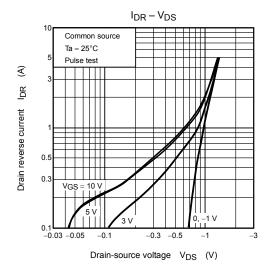


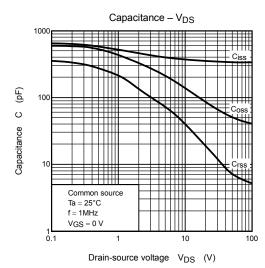


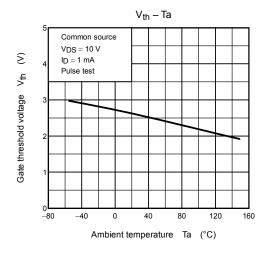


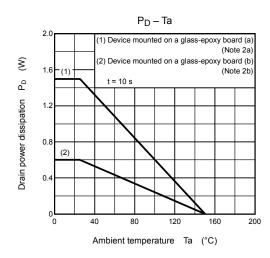


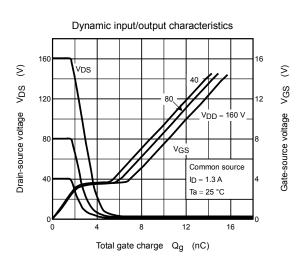


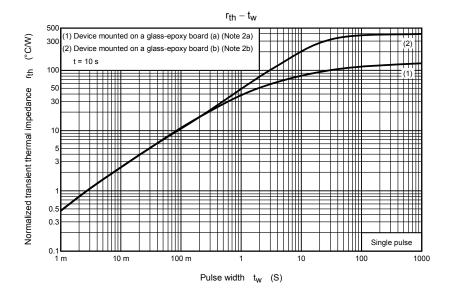




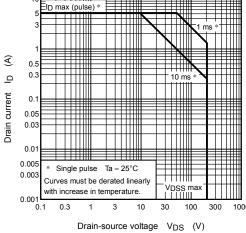


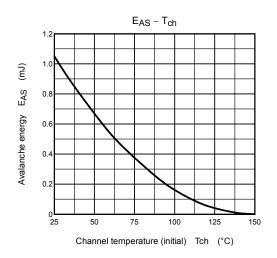




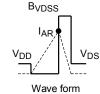


Safe operating area





Test circuit



 $T_{ch} = 25^{\circ}C$ (Initial) Peak I_{AR} = 1.3 A, R_G = 25 Ω E_{AS} = $\frac{1}{2}$ ·L·I²· $\left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}}\right)$ $V_{DD} = 50 \text{ V}, L = 1 \text{ mH}$

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