

DESCRIPTION

The M5M5V32R16 is a family of 32768-word by 16-bit static RAMs, fabricated with the high performance CMOS process and designed for high speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible.

They include a power down feature as well. In write and read cycles, the lower and upper bytes are able to be controled either togethe or separately by /LB and /UB.

FEATURES

- Fast access time M5M5V32R16J,TP-10 ---10ns(max)
 M5M5V32R16J,TP-12 --- 12ns(max)
 M5M5V32R16J,TP-15 --- 15ns(max)
- Low power dissipation Active ----- 297mW(typ)
 Stand by ----- 0.33mW(typ)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by /S
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs
- Separate control of lower and upper bytes by /LB and /UB

APPLICATION

High-speed memory system

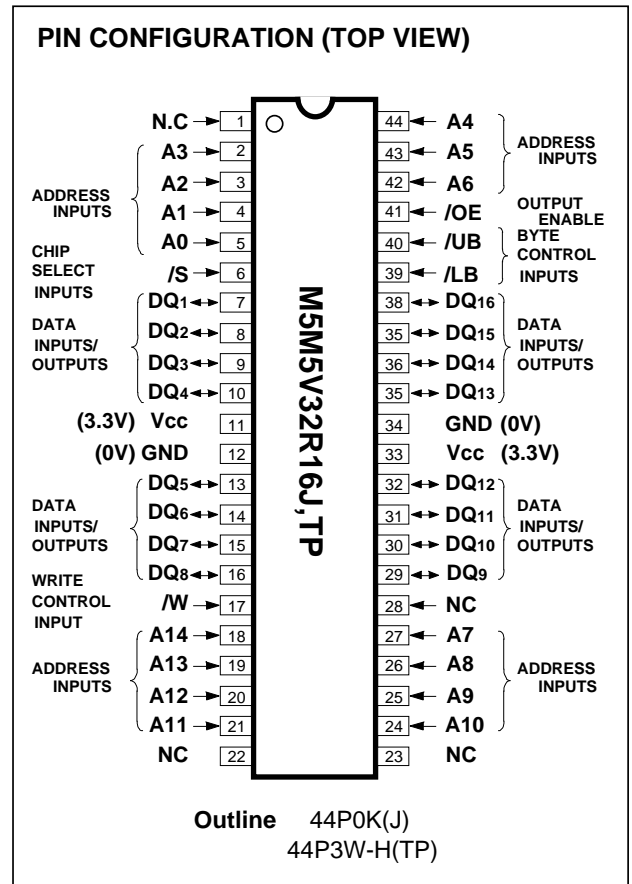
FUNCTION

The operation mode of the M5M5V32R16 is determined by a combination of the device control inputs /S, /W, /OE, /LB, and /UB. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with low level /LB and/or low level /UB and low level /S. The address must be set-up before write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of /W, /LB, /UB or /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting W at a high level and /OE at a low level while /LB and/or /UB and /S are in an active state. (/LB and/or /UB=L, /S=L)



PACKAGE

M5M5V32R16J : 44pin 400mil SOJ
 M5M5V32R16VP: 44pin 400mil TSOP(II)

When setting /LB at a high level and other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enable, and lower-Byte are in a non-selectable mode. And when setting /UB at a high level and other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enable, and upper-Byte are in a non-selectable mode.

When setting /LB and /UB at a high level or /S at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /LB, /UB and /S.

Signal-/S controls the power-down feature. When /S goes high, power dissipation is reduced extremely. The access time from /S is equivalent to the address access time.

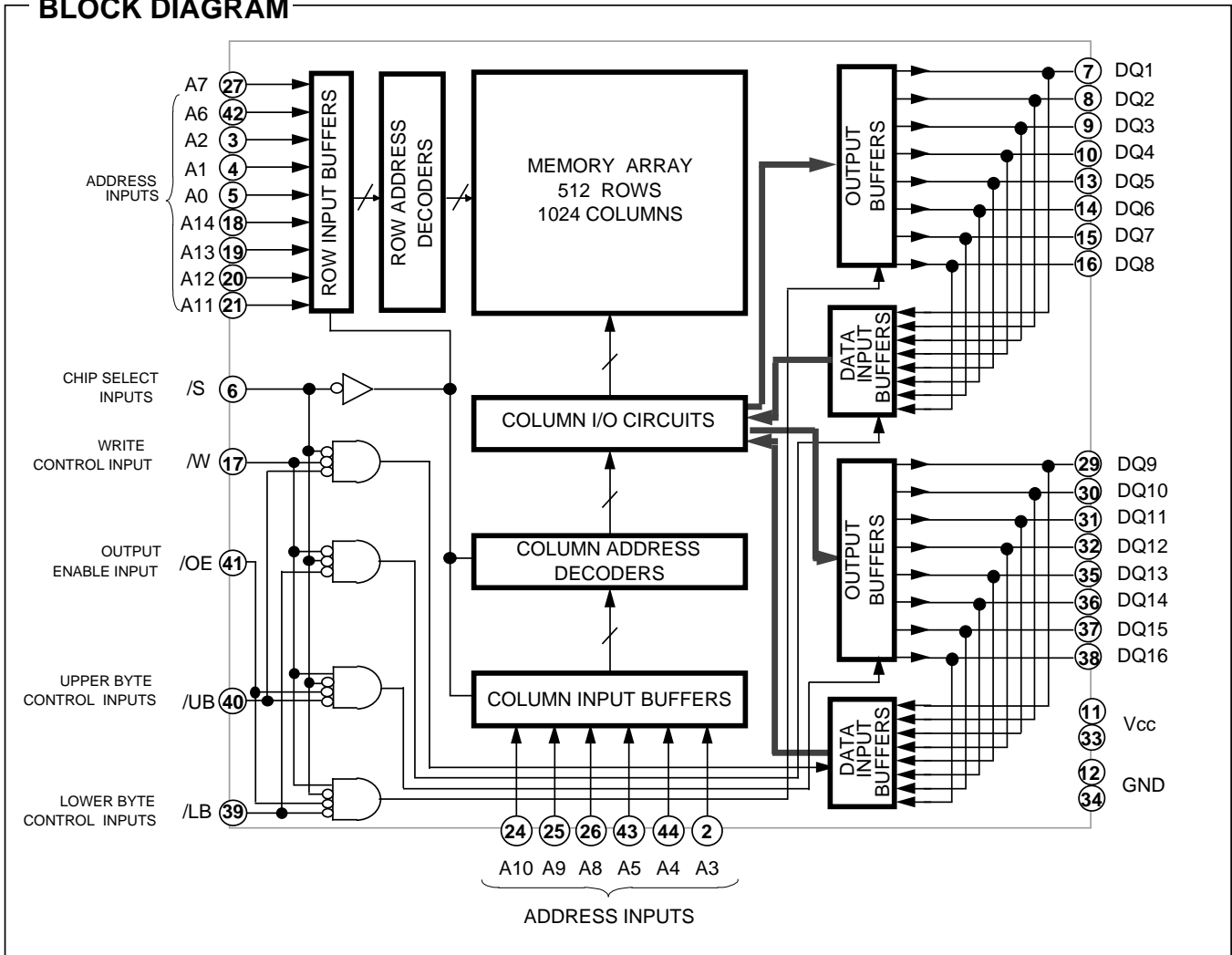
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524288-BIT (32768-WORD BY 16-BIT) CMOS STATIC RAM

FUNCTION TABLE

/S	/W	/OE	/LB	/UB	Mode	DQ1 - 8	DQ9 - 16	Icc
L	H	L	L	L	Read cycle All Bytes	D OUT	D OUT	Active
L	H	L	H	L	Read cycle Upper Bytes	High-impedance	D OUT	Active
L	H	L	L	H	Read cycle Lower Bytes	D OUT	High-impedance	Active
L	L	X	L	L	Write cycle All Bytes	D IN	D IN	Active
L	L	X	H	L	Write cycle Upper Bytes	High-impedance	D IN	Active
L	L	X	L	H	Write cycle Lower Bytes	D IN	High-impedance	Active
L	H	H	X	X	Output disable	High-impedance	High-impedance	Active
L	X	X	H	H				
H	X	X	X	X	Non selection	High-impedance	High-impedance	Stand by

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		-2.0* ~ 4.6	V
V _I	Input voltage	With respect to GND	-2.0* ~ V _{cc} +0.5	V
V _O	Output voltage			
P _d	Power dissipation			
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg(bias)}	Storage temperature(bias)		-10 ~ 85	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

* Pulse width ≤ 20ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{cc}=3.3V^{+10%}_{-5%}, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{cc} +0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = - 4mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0 ~ V _{cc}			2	μA
I _{OZ}	Output current in off-state	V _I (/S)= V _{IH} V _O = 0 ~ V _{cc}			10	μA
I _{CC1}	Active supply current (TTL level)	V _I (/S)= V _{IL} other inputs V _{IH} or V _{IL} Output-open(duty 100%)	AC(10ns cycle)		150	mA
			AC(12ns cycle)		130	
			AC(15ns cycle)		110	
			DC	90	100	
I _{CC2}	Stand-by supply current (TTL level)	V _I (/S)= V _{IH}	AC(10ns cycle)		60	mA
			AC(12ns cycle)		55	
			AC(15ns cycle)		50	
			DC		40	
I _{CC3}	Stand-by current (MOS level)	V _I (/S)= V _{cc} ≥ 0.2V other inputs V _I ≤ 0.2V or V _I ≥ V _{cc} - 0.2V		0.1	1	mA

* Pulse width ≤ 20ns, in case of AC : - 3.0V

CAPACITANCE (T_a=0 ~ 70°C, V_{cc}=3.3V^{+10%}_{-5%}, unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _i =25mVrms, f=1MHz			6	pF
C _O	Output capacitance	V _O =GND, V _o =25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{cc}=3.3V, T_a=25°C

3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{cc}=3.3V^{+10%}_{-5%}, unless otherwise noted)

(1) MEASUREMENT CONDITION

Input pulse levels ----- V_{IH} =3.0V, V_{IL} =0.0V

Input rise and fall time ----- 3ns

Input timing reference levels ----- V_{IH} =1.5V, V_{IL} =1.5V

Output timing reference levels ----- V_{OH} =1.5V, V_{OL} =1.5V

Output loads ----- Fig1, Fig2

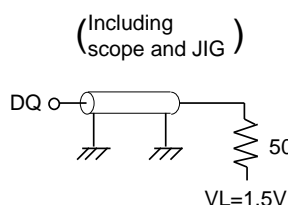


Fig.1 Output load

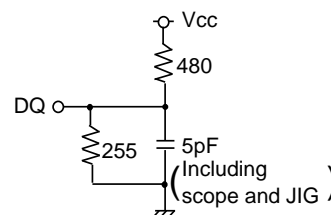


Fig.2 Output load for ten, tdis

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READ CYCLE

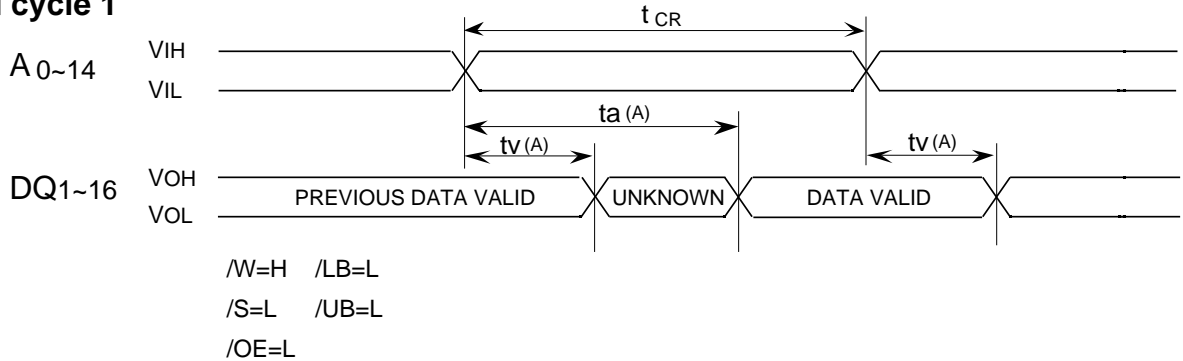
Symbol	Parameter	Limits						Unit
		M5M5V32R16 -10		M5M5V32R16 -12		M5M5V32R16 -15		
		Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	10		12		15		ns
t _{a (A)}	Address access time		10		12		15	ns
t _{a (S)}	Chip select access time		10		12		15	ns
t _{a (OE)}	Output enable access time		5		6		7	ns
t _{a (B)}	/LB,/UB access time		5		6		7	ns
t _{dis (S)}	Output disable time after /S high	0	5	0	6	0	7	ns
t _{dis (OE)}	Output disable time after /OE high	0	5	0	6	0	7	ns
t _{dis (B)}	Output disable time after /LB,/UB high	0	5	0	6	0	7	ns
t _{en (S)}	Output enable time after /S low	4		4		4		ns
t _{en (OE)}	Output enable time after /OE low	3		3		3		ns
t _{en (B)}	Output enable time after /LB,/UB low	3		3		3		ns
t _{v (A)}	Data valid time after address change		4		4		4	ns
t _{PU}	Power-up time after chip selection	0		0		0		ns
t _{PD}	Power down time after chip selection		10		12		15	ns

Write cycle

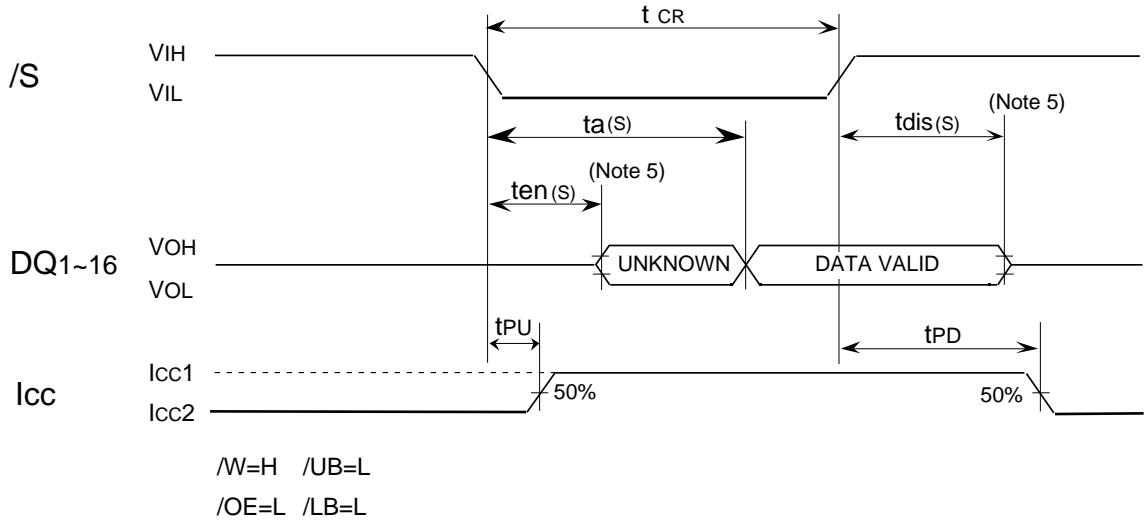
Symbol	Parameter	Limits						Unit
		M5M5V32R16 -10		M5M5V32R16 -12		M5M5V32R16 -15		
		Min	Max	Min	Max	Min	Max	
t _{cw}	Write cycle time	10		12		15		ns
t _{w(W)}	Write pulse width	9		10		12		ns
t _{su(B)}	/LB,/UB setup time	9		10		12		ns
t _{su(A)1}	Address setup time(/W)	0		0		0		ns
t _{su(A)2}	Address setup time(/S)	0		0		0		ns
t _{su(S)}	Chip select setup time	9		10		12		ns
t _{su(D)}	Data setup time	5		6		7		ns
t _{h(D)}	Data hold time	0		0		0		ns
t _{rec(W)}	Write recovery time	0		0		0		ns
t _{dis (W)}	Output disable time after /W low	0	5	0	6	0	7	ns
t _{dis (OE)}	Output disable time after /OE high	0	5	0	6	0	7	ns
t _{en (W)}	Output enable time after /W high	0		0		0		ns
t _{en (OE)}	Output enable time after /OE low	0		0		0		ns
t _{en (B)}	Output enable time after /LB,/UB low	0		0		0		ns
t _{su(A-WH)}	Address to /W High	9		10		12		ns
t _{su(A-SH)}	Address to /S High	9		10		12		ns
t _{su (A-BH)}	Address to /LB,/UB High	9		10		12		ns

(4)TIMING DIAGRAMS

Read cycle 1



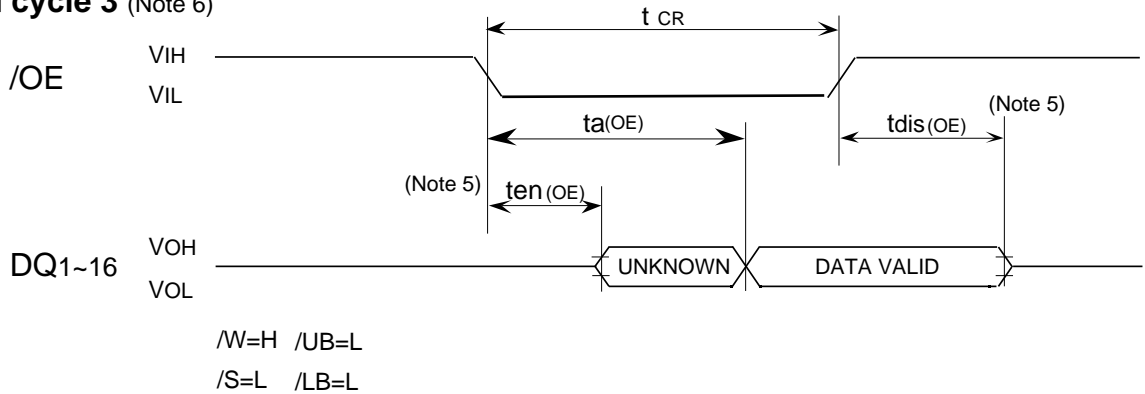
Read cycle 2 (Note 4)



Note 4. Addresses valid prior to or coincident with $/S$ transition low.

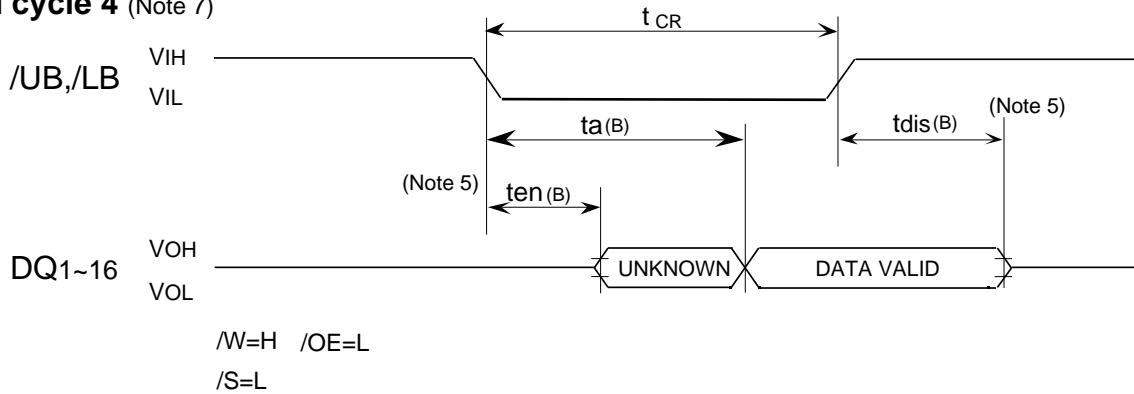
5. Transition is measured $\pm 500\text{mv}$ from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 6)



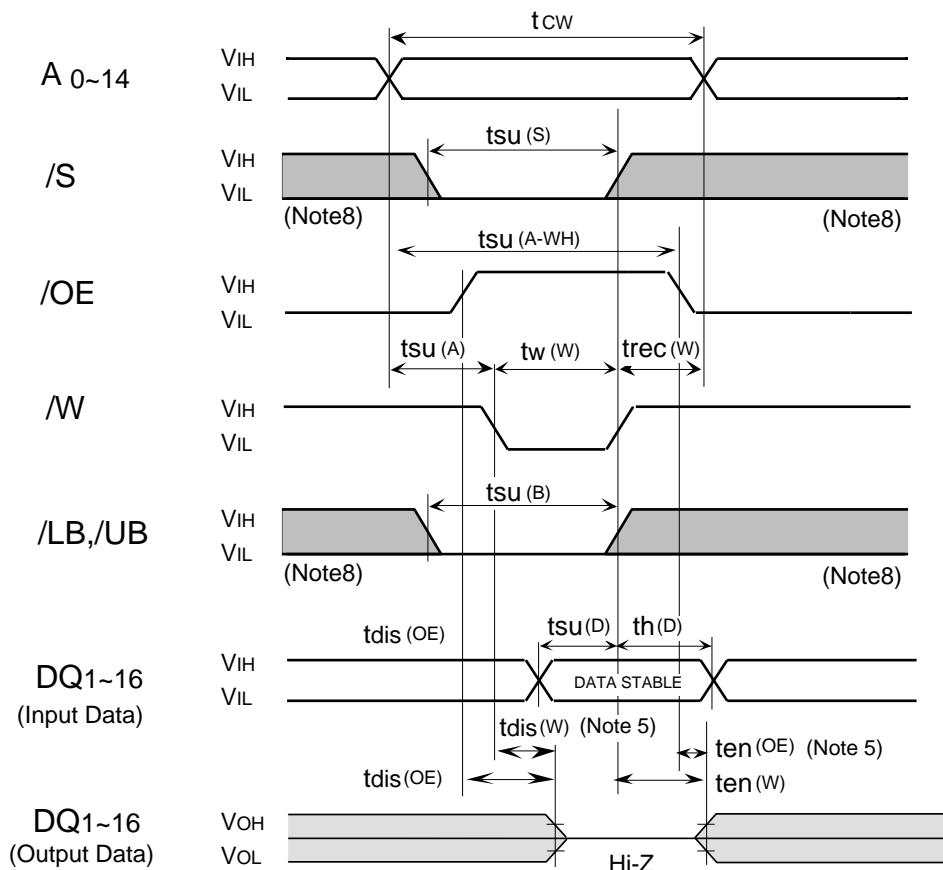
Note 6. Addresses and $/S$ valid prior to $/OE$ transition low by $(t_a(A)-t_a(OE))$, $(t_a(S)-t_a(OE))$

Read cycle 4 (Note 7)



Note 7. Addresses \overline{S} and \overline{OE} valid prior to $\overline{LB}, \overline{UB}$ transition low by $(t_{a(A)}-t_{a(B)})$, $(t_{a(S)}-t_{a(B)})$, $(t_{a(OE)}-t_{a(B)})$.

Write cycle (/W control mode)

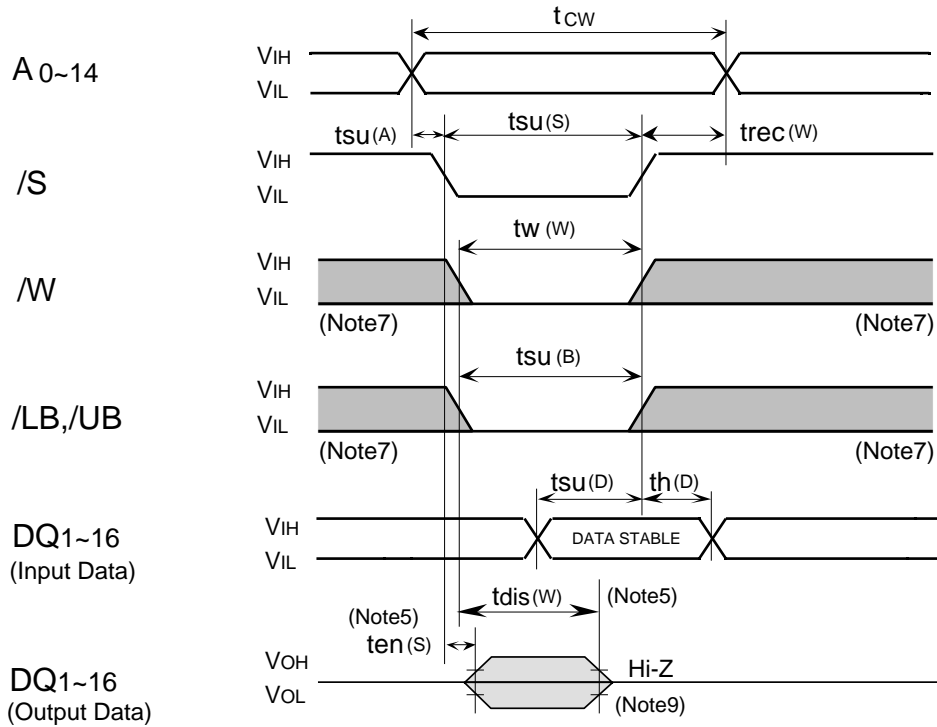


Note 8: Hatching indicates the state is don't care.

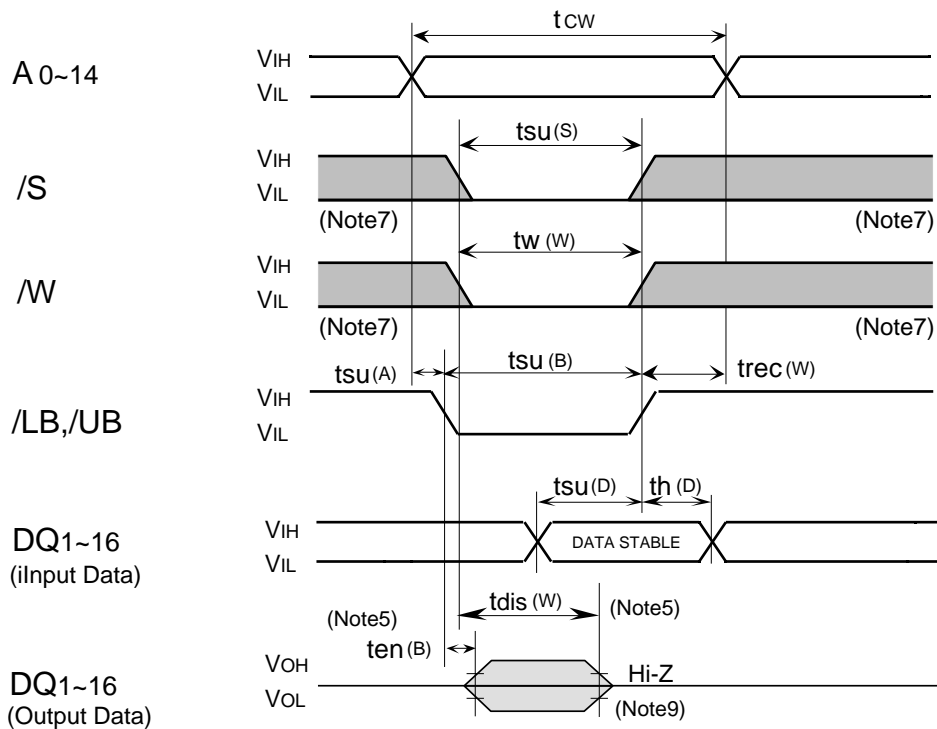
9: When the falling edge of \overline{W} is simultaneous or prior to the falling edge of \overline{S} , the output is maintained in the high impedance.

10: t_{en}, t_{dis} are periodically sampled and are not 100% tested.

Write cycle(/S control)



Write cycle(/LB, /UB control)



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'96.11.20	P3	Vref --> 5.0V	k.kubo
'97.01.22	P3	Output loads=50	k.kubo
'97.02.04	P3	Vref --> Vcc	k.kubo