MicroConverter®, 12- Bit ADC with Embedded 62KB FLASH MCU

Preliminary Technical Data — ADuC831

FEATURES

ANALOG I/O
- 8-Channel, High Accuracy 12-Bit ADC
- High Speed 200 kSPS
- On-Chip, 100 ppm/°C Voltage Reference
- DMA Controller for High-Speed ADC-to-RAM capture
- Two 12-Bit Voltage Output DACs
- Dual Output PWM/ΣΔ DACs

On-Chip Temperature Sensor Function

Memory
- 62Kbytes On-Chip Flash/EE Program Memory
- 4KBytes On-Chip Flash/EE Data Memory
- Flash/EE, 100 Yr Retention, 100 Kcycles Endurance
- 2304 Bytes On-Chip Data RAM

8051 Based Core
- 8051-Compatible Instruction Set (16 MHz Max)
- 12 MHz Nominal Operation (16MHz Max)
- 12 Interrupt Sources, Two Priority Levels
- Dual Data Pointer
- Extended 11-bit Stack Pointer

On-Chip Peripherals
- Time Interval Counter (TIC)
- UART and SPI® Serial I/O
- Watchdog Timer (WDT), Power Supply Monitor (PSM)

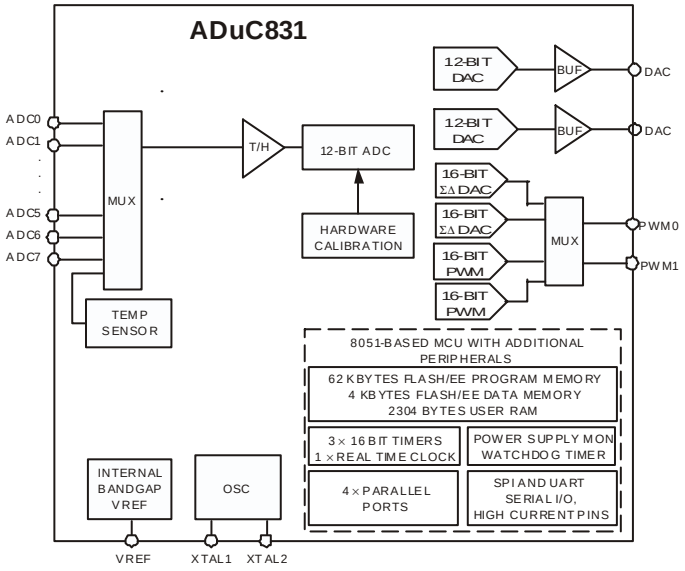
Power
- Specified for 3 V and 5 V Operation
- Normal Idle and Power-down Modes

APPLICATIONS

Intelligent Sensors (IEEE1451.2-Compatible)
Battery Powered Systems (Portable PCs, Instrument Monitors)
Transient Capture Systems
DAS and Communications Systems
Control Loop Monitors(Optical Networks/Basestations)

Pin Compatible Upgrade to existing ADuC812 systems which require additional code or data memory. Runs from 1-16MHz external crystal.

Also available ADuC832, Upgrade to ADuC812 systems. Runs from 32KHz external crystal with on-chip PLL.



GENERAL DESCRIPTION

The ADuC831 is a complete smart transducer front-end, integrating a high-performance self calibrating multichannel ADC, dual DAC and programmable 8-bit MCU on a single chip.

The microcontroller core is an 8052 and therefore 8051-instruction-set-compatible with 12 core clock periods per machine cycle. 62 Kbytes of nonvolatile Flash/EE program memory are provided on-chip. 4 Kbytes of nonvolatile Flash/EE data memory, 256 bytes RAM and 2 KBytes of extended RAM are also integrated on-chip.

The ADuC831 also incorporates additional analog functionality with two 12-bit DACs, power supply monitor, and a bandgap reference. On-chip digital peripherals include two 16-bit ΣΔ DACs, dual output 16-bit PWM, watchdog timer, time interval counter, three timers/counters, Timer 3 for Baud Rate generation and two serial I/O ports (SPI and UART)

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the EA pin. A functional block diagram of the ADuC831 is shown above with a more detailed block diagram shown in figure 1 (page 6).

The part is specified for 3 Vand 5V operation over the industrial temperature range and is available in a 52-lead, plastic quad flatpack package and in a 56-lead, chip scale package.

REV. PrD

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SPECIFICATIONS[1, 2]

(AV_{DD} = DV_{DD} = 3.0 V or 5.0 V 610%, REF_{IN}/REF_{OUT} = 2.5 V Internal Reference, MCLKIN = 11.0592 MHz, f_{SAMPLE} = 200 kHz, DAC V_{OUT} Load to AGND; R_L = 2 kV, C_L = 100 pF. All specifications T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	ADuC831BS V_{DD} = 5 V	ADuC831BS V_{DD} = 3 V	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS				
DC ACCURACY[3, 4]				
Resolution	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	LSB typ	f_{SAMPLE} = 100 kHz
	±1.5	±1.5	LSB max	f_{SAMPLE} = 100 kHz
	±1.5	±1.5	LSB typ	f_{SAMPLE} = 200 kHz
Differential Nonlinearity	±1	±1	LSB typ	f_{SAMPLE} = 100 kHz. Guaranteed No Missing Codes at 5 V
CALIBRATED ENDPOINT ERRORS[5, 6]				
Offset Error	±5	±5	LSB max	
	±1	±1	LSB typ	
Offset Error Match	1	1	LSB typ	
Gain Error	±6	±6	LSB max	
	±1	±1	LSB typ	
Gain Error Match	1.5	1.5	LSB typ	
USER SYSTEM CALIBRATION[7]				
Offset Calibration Range	±5	±5	% of V_{REF} typ	
Gain Calibration Range	±2.5	±2.5	% of V_{REF} typ	
DYNAMIC PERFORMANCE				f_{IN} = 10 kHz Sine Wave f_{SAMPLE} = 100 kHz
Signal-to-Noise Ratio (SNR)[8]	70	70	dB typ	
Total Harmonic Distortion (THD)	–78	–78	dB typ	
Peak Harmonic or Spurious Noise	–78	–78	dB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	
Leakage Current	±1	±1	µA max	
	±0.1	±0.1	µA typ	
Input Capacitance[9]	20	20	pF max	
TEMPERATURE SENSOR[10]				
Voltage Output at 25°C	600	600	mV typ	Can vary significantly (> ±20%)
Voltage TC	–3.0	–3.0	mV/°C typ	from device to device
Acquisition Time Required	1	1	uS typ	
DAC CHANNEL SPECIFICATIONS				
DC ACCURACY[11]				
Resolution	12	12	Bits	
Relative Accuracy	±3	±3	LSB typ	
Differential Nonlinearity	±0.5	±1	LSB typ	Guaranteed 12-Bit Monotonic
Offset Error	±60	±60	mV max	
	±15	±15	mV typ	
Full-Scale Error	±30	±30	mV max	
	±10	±10	mV typ	
Full-Scale Mismatch	±0.5	±0.5	% typ	% of Full-Scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V_{REF}	0 to V_{REF}	V typ	
Voltage Range_1	0 to V_{DD}	0 to V_{DD}	V typ	
Resistive Load	10	10	kΩ typ	
Capacitive Load	100	100	pF typ	
Output Impedance	0.5	0.5	Ω typ	
I_{SINK}	50	50	µA typ	

ADuC831–SPECIFICATIONS[1,2] (continued)

Parameter	ADuC831BS V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
DAC AC CHARACTERISTICS				
Voltage Output Settling Time	15	15	µs typ	Full-Scale Settling Time to Within 1/2 LSB of Final Value
Digital-to-Analog Glitch Energy	10	10	nV sec typ	1 LSB Change at Major Carry
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range[9]	2.3/V_{DD}	2.3/V_{DD}	V min/max	
Input Impedance	150	150	kΩ typ	
REF_{OUT} Output Voltage	2.5 ±2.5%	2.5 ±2.5%	V min/max	Initial Tolerance @ 25°C
	2.5	2.5	V typ	
REF_{OUT} Tempco	100	100	ppm/°C typ	
FLASH/EE MEMORY PERFORMANCE CHARACTERISTICS[12, 13]				
Endurance	100,000	100,000	Cycles min	
Data Retention	100	100	Years min	
WATCHDOG TIMER CHARACTERISTICS				
Oscillator Frequency	32	32	kHz typ	±10% Accurate
TIME INTERVAL COUNTER				
Oscillator Frequency	32	32	kHz typ	±10% Accurate
POWER SUPPLY MONITOR (PSM)				
AV_{DD} Trip Point Selection Range	2.63		Vmin	Four Trip Points Selectable in
	4.63		Vmax	This Range Programmed via TPA 1-0 IN PSMCON
AV_{DD} Power Supply Trip Point Accuracy	±3.5		% max	
DV_{DD} Trip Point Selection Range	2.63		Vmin	Four Trip Points Selectable in
	4.63		Vmax	This Range Programmed via TPD1–0 in PSMCON
DV_{DD} Power Supply Trip Point Accuracy	±3.5		% max	
DIGITAL INPUTS				
Input High Voltage (V_{INH})	2.4		V min	
XTAL1 Input High Voltage (V_{INH}) Only	4		V min	
Input Low Voltage (V_{INL})	0.8		V max	
Input Leakage Current (Port 0, EA)	±10		µA max	V_{IN} = 0 V or V_{DD}
	±1	±1	µA typ	V_{IN} = 0 V or V_{DD}
Logic 1 Input Current (All Digital Inputs)	±10		µA max	V_{IN} = V_{DD}
	±1	±1	µA typ	V_{IN} = V_{DD}
Logic 0 Input Current (Port 1, 2, 3)	–80		µA max	
	–40	–40	µA typ	V_{IL} = 450 mV
Logic 1-0 Transition Current (Port 1, 2, 3)	–700		µA max	V_{IL} = 2 V
	–400	–400	µA typ	V_{IL} = 2 V
Input Capacitance	10	10	pF typ	

Parameter	ADuC831BS V_{DD} = 5 V	ADuC831BS V_{DD} = 3 V	Unit	Test Conditions/Comments
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4		V min	V_{DD} = 4.5 V to 5.5 V I_{SOURCE} = 80 µA
	4.0	2.6	V typ	V_{DD} = 2.7 V to 3.3 V I_{SOURCE} = 20 µA
Output Low Voltage (V_{OL})				
ALE, PSEN, Ports 0 and 2	0.4		V max	I_{SINK} = 1.6 mA
	0.2	0.2	V typ	I_{SINK} = 1.6 mA
Port 3	0.4		V max	I_{SINK} = 8 mA
	0.2	0.2	V typ	I_{SINK} = 8 mA
Floating State Leakage Current	±10		µA max	
	±5	±5	µA typ	
Floating State Output Capacitance	10	10	pF typ	
POWER REQUIREMENTS[14, 15, 16]				
I_{DD} Normal Mode[17]	43		mA max	MCLKIN = 16 MHz
	32	16	mA typ	MCLKIN = 16 MHz
	26	12	mA typ	MCLKIN = 12 MHz
	8	3	mA typ	MCLKIN = 1 MHz
I_{DD} Idle Mode	25		mA max	MCLKIN = 16 MHz
	18	17	mA typ	MCLKIN = 16 MHz
	15	6	mA typ	MCLKIN = 12 MHz
	7	2	mA typ	MCLKIN = 1 MHz
I_{DD} Power-Down Mode[18]	50	50	µA max	
	5	5	µA typ	

NOTES

[1]Specifications apply after calibration.

[2]Temperature range –40°C to +85°C.

[3]Linearity is guaranteed during normal MicroConverter Core operation.

[4]Linearity may degrade when programming or erasing the 640 Byte Flash/EE space during ADC conversion times due to on-chip charge pump activity.

[5]Measured in production at V_{DD} = 5 V after Software Calibration Routine at 25°C only.

[6]User may need to execute Software Calibration Routine to achieve these specifications, which are configuration dependent.

[7]The offset and gain calibration spans are defined as the voltage range of user system offset and gain errors that the ADuC831 can compensate.

[8]SNR calculation includes distortion and noise components.

[9]Specification is not production tested, but is supported by characterization data at initial product release.

[10]The temperature sensor will give a measure of the die temperature directly; air temperature can be inferred from this result.

[11]DAC linearity is calculated using:
reduced code range of 48 to 4095, 0 to V_{REF} range
reduced code range of 48 to 3995, 0 to V_{DD} range
DAC output load = 10 kΩ and 50 pF.

[12]Flash/EE Memory Performance Specifications are qualified as per JEDEC Specification (Data Retention) and JEDEC Draft Specification A117 (Endurance).

[13]Endurance Cycling is evaluated under the following conditions:
Mode = Byte Programming, Page Erase Cycling
Cycle Pattern = 00Hex to FFHex
Erase Time = 20 ms
Program Time = 100 µs

[14]I_{DD} at other MCLKIN frequencies is typically given by:
Normal Mode (V_{DD} = 5 V): I_{DD} = (1.6 nAs x MCLKIN) + 6 mA
Normal Mode (V_{DD} = 3 V): I_{DD} = (0.8 nAs x MCLKIN) + 3 mA
Idle Mode (V_{DD} = 5 V): I_{DD} = (0.75 nAs x MCLKIN) + 6 mA
Idle Mode (V_{DD} = 3 V): I_{DD} = (0.25 nAs x MCLKIN) + 3 mA
Where MCLKIN is the oscillator frequency in MHz and resultant I_{DD} values are in mA.

[15]I_{DD} Currents are expressed as a summation of analog and digital power supply currents during normal MicroConverter operation.

[16]I_{DD} is not measured during Flash/EE program or erase cycles; I_{DD} will typically increase by 10 mA during these cycles.

[17]Analog I_{DD} = 2 mA (typ) in normal operation (internal V_{REF}, ADC and DAC peripherals powered on).

[18]EA = Port0 = DV_{DD}, XTAL1 (Input) tied to DV_{DD}, during this measurement.

Typical specifications are not production tested, but are supported by characterization data at initial product release.

Specifications subject to change without notice.
Please refer to User Guide, Quick Reference Guide, Application Notes, and Silicon Errata Sheet at **www.analog.com/microconverter** for additional information.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

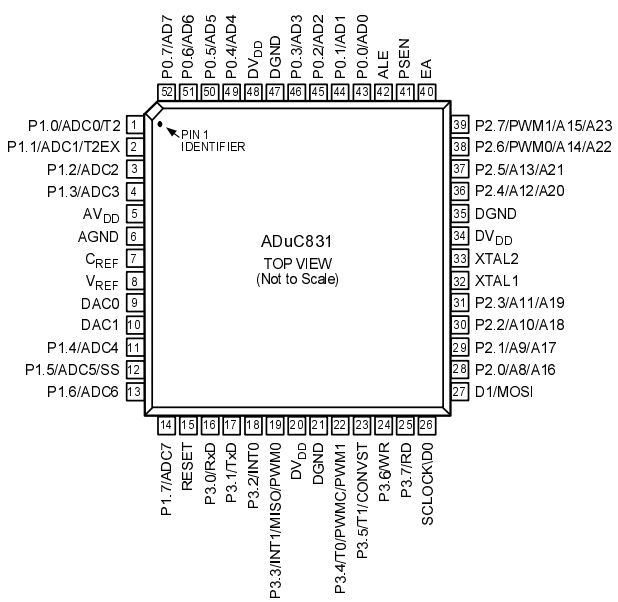
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
AGND to DGND ..... –0.3 V to +0.3 V
DV_{DD} to DGND, AV_{DD} to AGND ..... –0.3 V to +7 V
Digital Input Voltage to DGND ..... –0.3 V, DV_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V, DV_{DD} + 0.3 V
V_{REF} to AGND ..... –0.3 V, AV_{DD} + 0.3 V
Analog Inputs to AGND ..... –0.3 V, AV_{DD} + 0.3 V
Operating Temperature Range Industrial (B Version)
..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
θ_{JA} Thermal Impedance ..... 90°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

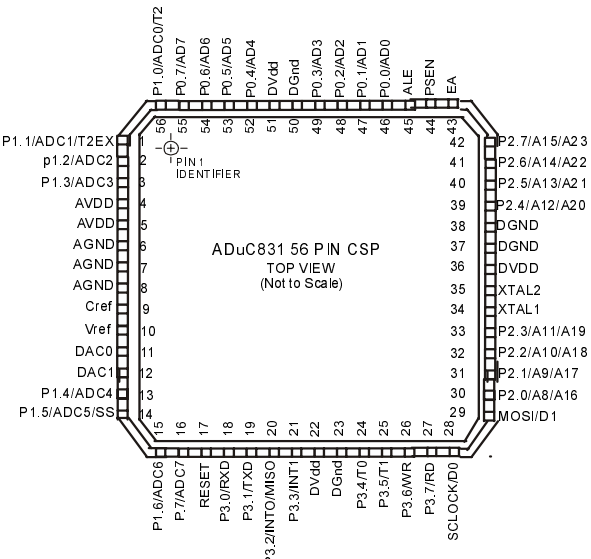
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuC831BS	–40°C to +85°C	52-Lead Plastic Quad Flatpack	S-52
ADuC831BCP	–40°C to +85°C	56-Lead Chip Scale Package	CP-56

PIN CONFIGURATION





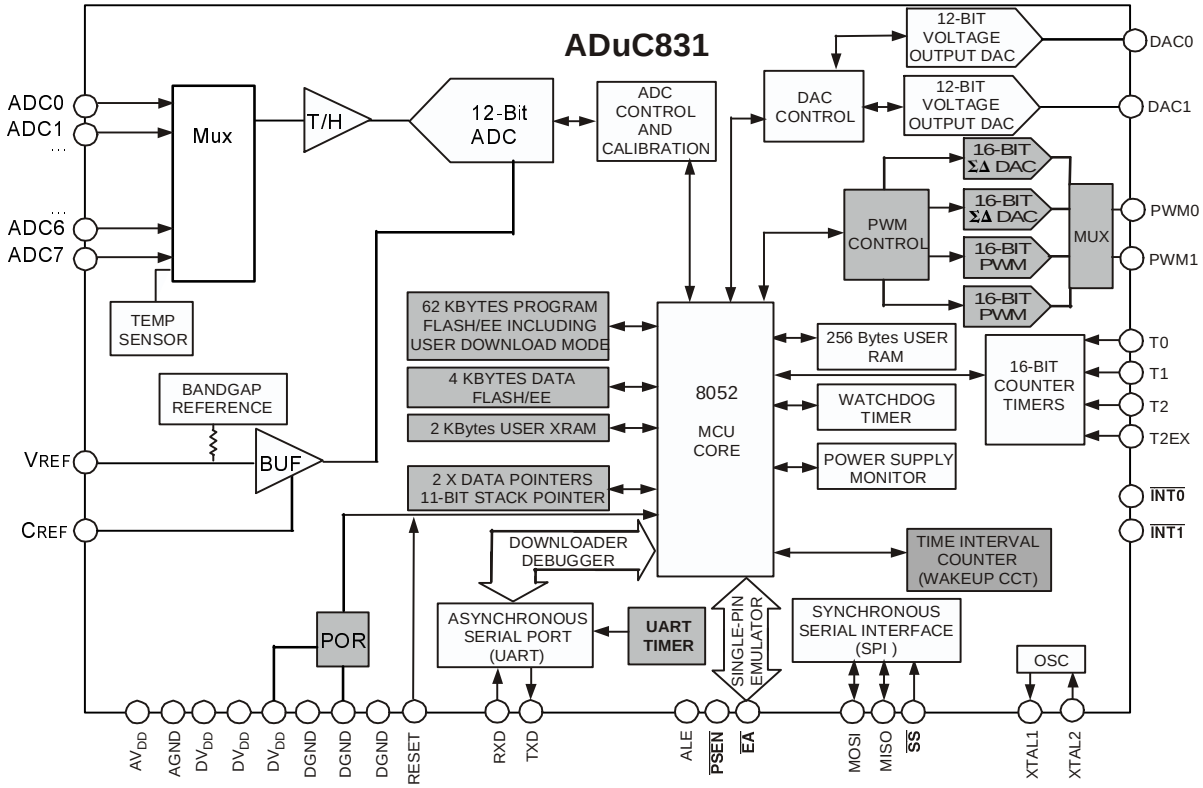


Figure 1 ADuC831 Block Diagram (Shaded areas are features not present on the ADuC812)

PIN FUNCTION DESCRIPTIONS

Mnemonic	Type	Function
DV_{DD}	P	Digital Positive Supply Voltage, 3 V or 5 V Nominal
AV_{DD}	P	Analog Positive Supply Voltage, 3 V or 5 V Nominal
C_{REF}	I	Decoupling Input for On-Chip Reference. Connect 0.1 µF between this pin and AGND.
V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be overdriven by an external reference.
AGND	G	Analog Ground. Ground Reference point for the analog circuitry.
P1.0–P1.7	I	Port 1 is an 8-bit Input Port only. Unlike other Ports, Port 1 defaults to Analog Input Mode, to configure any of these Port Pins as a digital input, write a "0" to the port bit. Port 1 pins are multifunction and share the following functionality.
ADC0–ADC7	I	Analog Inputs. Eight single-ended analog inputs. Channel selection is via ADCCON2 SFR.
T2	I	Timer 2 Digital Input. Input to Timer/Counter 2. When Enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
T2EX	I	Digital Input. Capture/Reload trigger for Counter 2 and also functions as an Up/Down control input for Counter 2.
SS	I	Slave Select Input for the SPI Interface
D1	O	Digital Output Pin
D0	O	Digital Output Pin
SCLOCK	I/O	Serial Clock Pin for Serial Interface Clock
MOSI	I/O	SPI Master Output/Slave Input Data I/O Pin for SPI Interface
MISO	I/O	SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface
DAC0	O	Voltage Output from DAC0
DAC1	O	Voltage Output from DAC1
RESET	I	Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device.
P3.0–P3.7	I/O	Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. Port 3 pins also contain various secondary functions which are described below.
PWMC	I	PWM Clock Input
PWM0	O	PMW0 Voltage Output. PWM outputs can be configured to uses ports 2.6 & 2.7 or 3.3 and 3.4
PWM1	O	PMW1 Voltage Ouput. See CFG831 Register for further Information.
RxD	I/O	Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of Serial (UART) Port
TxD	O	Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of Serial (UART) Port
INT0	I	Interrupt 0, programmable edge or level triggered Interrupt input, which can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
INT1	I	Interrupt 1, programmable edge or level triggered Interrupt input, which can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
T0	I	Timer/Counter 0 Input
T1	I	Timer/Counter 1 Input
CONVST	I	Active low Convert Start Logic input for the ADC block when the external Convert start function is enabled. A low-to-high transition on this input puts the track/hold into its hold mode and starts conversion.
WR	O	Write Control Signal, Logic Output. Latches the data byte from Port 0 into the external data memory.
RD	O	Read Control Signal, Logic Output. Enables the external data memory to Port 0.
XTAL2	O	Output of the Inverting Oscillator Amplifier
XTAL1	I	Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
DGND	G	Digital Ground. Ground reference point for the digital circuitry.
P2.0–P2.7 (A8–A15) (A16–A23)	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the external 24-bit external data memory space.

PIN FUNCTION DESCRIPTION (continued)

Mnemonic	Type	Function
PSEN	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. PSEN can also be used to enable serial download mode when pulled low through a resistor on power-up or RESET.
ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit address space accesses) of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to 1FFFH. When held low this input enables the device to fetch all instructions from external program memory.
P0.7–P0.0 (A0–A7)	I/O	Port 0 is an 8-Bit Open Drain Bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-ups when emitting 1s.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

Gain Error

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV sec.

Full-Scale Error

This is the deviation of the full scale output voltage from the ideal.