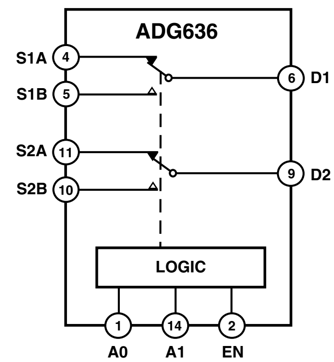
1 pC Charge Injection, 100 pA Leakage CMOS ±5 V/+5 V/+3 V Dual SPDT Switch

ADG636

FEATURES
- 1 pC Charge Injection
- ±2.7 V to ±5.5 V Dual Supply
- +2.7 V to +5.5 V Single Supply
- Automotive Temperature Range: –40°C to +125°C
- 100 pA (Max @ 25°C) Leakage Currents
- 85 Ω Typ On Resistance
- Rail-to-Rail Operation
- Fast Switching Times
- Typical Power Consumption (<0.1 μW)
- TTL/CMOS Compatible Inputs
- 14-Lead TSSOP Package

APPLICATIONS
- Automatic Test Equipment
- Data Acquisition Systems
- Battery-Powered Instruments
- Communication Systems
- Sample-and-Hold Systems
- Remote Powered Equipment
- Audio and Video Signal Routing
- Relay Replacement
- Avionics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG636 is a monolithic device, comprising two independently selectable CMOS SPDT (Single Pole, Double Throw) switches. When on, each switch conducts equally well in both directions.

The ADG636 operates from a dual ±2.7 V to ±5.5 V supply, or from a single supply of +2.7 V to +5.5 V.

This switch offers ultralow charge injection of ±1.5 pC over the entire signal range and leakage current of 10 pA typical at 25°C. It offers on-resistance of 85 Ω typ, which is matched to within 2 Ω between channels. The ADG636 also has low power dissipation yet gives high switching speeds.

The ADG636 exhibits break-before-make switching action and is available in a 14-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Ultralow Charge Injection (Q_{INJ}: ±1.5 pC typ over full signal range)
2. Leakage Current <0.25 nA max @ 85°C
3. Dual ±2.7 V to ±5 V or Single +2.7 V to +5.5 V Supply
4. Automotive Temperature Range: –40°C to +125°C
5. Small 14-Lead TSSOP Package

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700
www.analog.com
Fax: 781/326-8703

ADG636–SPECIFICATIONS

DUAL SUPPLY[1] (V_{DD} = 5 V ± 10%, V_{SS} = –5 V ± 10%, GND = 0 V. All specifications –40°C to +125°C unless noted.)

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
					V_{DD} = +4.5 V, V_{SS} = –4.5 V
On Resistance (R_{ON})	85			Ω typ	V_S = ±3 V, I_S = –1 mA,
	115	140	160	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})	2			Ω typ	V_S = ±3 V, I_S = –1 mA
	4	5.5	6.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	25			Ω typ	V_S = ±3 V, I_S = –1 mA
	40	55	60	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V,
	±0.1	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V,
	±0.1	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = ±4.5 V, Test Circuit 3
	±0.1	±0.25	±6	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time	70			ns typ	V_{S1A} = +3 V, V_{S1B} = –3 V, R_L = 300 Ω,
	100	120	150	ns max	C_L = 35 pF, Test Circuit 4
t_{ON} Enable	100			ns typ	R_L = 300 Ω, C_L = 35 pF
	135	170	190	ns max	V_S = 3 V, Test Circuit 5
t_{OFF} Enable	55			ns typ	R_L = 300 Ω, C_L = 35 pF
	80	90	100	ns max	V_S = 3 V, Test Circuit 5
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	R_L = 300 Ω, C_L = 35 pF,
			10	ns min	V_S = 3 V, Test Circuit 5
Charge Injection	–1.2			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 7
Off Isolation	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 8
Channel-to-Channel Crosstalk	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 10
Bandwidth –3 dB	610			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 9
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)	8			pF typ	f = 1 MHz
C_D, C_S (ON)	8			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = –5.5 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or 5.5 V
			1.0	µA max	
I_{SS}	0.001			µA typ	Digital Inputs = 0 V or 5.5 V
			1.0	µA max	

NOTES
[1]Y Version Temperature Range: –40°C to +125°C
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SINGLE SUPPLY[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications –40°C to +125°C unless otherwise noted.)

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
					V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance (R_{ON})	210			Ω typ	V_S = 3.5 V, I_S = –1 mA,
	290	350	380	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})	3			Ω typ	V_S = 3.5 V, I_S = –1 mA
		12	13	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V,
	±0.1	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V
	±0.1	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = 4.5 V/1 V,
	±0.1	±0.25	±6	nA max	Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time	90			ns typ	V_{S1A} = 3 V, V_{S1B} = 0 V, R_L = 300 Ω,
	150	185	210	ns max	C_L = 35 pF, Test Circuit 4
t_{ON} Enable	135			ns typ	R_L = 300 Ω, C_L = 35 pF
	180	235	275	ns max	V_S = 3 V, Test Circuit 5
t_{OFF} Enable	70			ns typ	R_L = 300 Ω, C_L = 35 pF
	105	120	135	ns max	V_S = 3 V, Test Circuit 5
Break-Before-Make Time Delay, t_{BBM}	30			ns typ	R_L = 300 Ω, C_L = 35 pF,
			10	ns min	V_S = 3 V, Test Circuit 5
Charge Injection	0.3			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 7
Off Isolation	–60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 8
Channel-to-Channel Crosstalk	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 10
Bandwidth –3 dB	530			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 9
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)	8			pF typ	f = 1 MHz
C_D, C_S (ON)	8			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
					Digital Inputs = 0 V or 5.5 V
I_{DD}	0.001			μA typ	
			1.0	μA max	

NOTES
[1]Y Version Temperature Range: –40°C to +125°C
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SINGLE SUPPLY[1] (V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications –40°C to +125°C unless otherwise noted.)

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
					V_{DD} = 2.7 V, V_{SS} = 0 V
On Resistance (R_{ON})	380	420	460	Ω typ	V_S = 1.5 V, I_S = –1 mA, Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})			5	Ω typ	V_S = 1.5 V, I_S = –1 mA
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V,
	±0.1	±0.25	±2	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V,
	±0.1	±0.25	±2	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = 1 V/3 V,
	±0.1	±0.25	±6	nA max	Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time	170			ns typ	V_{S1A} = 2 V, V_{S1B} = 0 V, R_L = 300 Ω,
	320	390	450	ns max	C_L = 35 pF, Test Circuit 4
t_{ON} Enable	250			ns typ	R_L = 300 Ω, C_L = 35 pF
	360	460	530	ns max	V_S = 2 V, Test Circuit 6
t_{OFF} Enable	110			ns typ	R_L = 300 Ω, C_L = 35 pF
	175	205	230	ns max	V_S = 2 V, Test Circuit 6
Break-Before-Make Time Delay, t_{BBM}	80			ns typ	R_L = 300 Ω, C_L = 35 pF,
			10	ns min	V_{S1} = 2 V, Test Circuit 5
Charge Injection	0.6			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 7
Off Isolation	–60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 8
Channel-to-Channel Crosstalk	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Test Circuit 10
Bandwidth –3 dB	530			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 9
C_S (OFF)	5			pF typ	f = 1 MHz
C_D (OFF)	8			pF typ	f = 1 MHz
C_D, C_S (ON)	8			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.3 V
					Digital Inputs = 0 V or 3.3 V
I_{DD}	0.001			µA typ	
		1.0	µA max		

NOTES
[1]Y Version Temperature Range: –40°C to +125°C
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . 13 V
V_{DD} to GND . . . . –0.3 V to +6.5 V
V_{SS} to GND . . . . +0.3 V to –6.5 V
Analog Inputs[2] . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
Digital Inputs[2] . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D
  (Pulsed at 1 ms, 10% Duty Cycle max) . . . . 20 mA
Continuous Current, S or D . . . . 10 mA
Operating Temperature Range
  Automotive (Y Version) . . . . –40°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . 150°C
TSSOP Package
  θ_{JA} Thermal Impedance . . . . 150°C/W
  θ_{JC} Thermal Impedance . . . . 27°C/W
Lead Temperature, Soldering (10 seconds) . . . . 300°C
  IR Reflow, Peak Temperature . . . . 220°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2] Overvoltages at EN, A0, A1, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG636YRU	–40°C to +125°C	Thin Shrink Small Outline (TSSOP)	RU-14

PIN CONFIGURATION

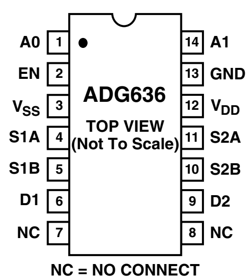


Table I. Truth Table

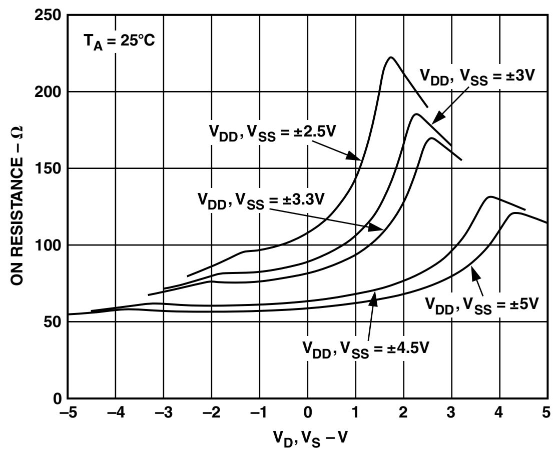
A1	A0	EN	ON Switch
X	X	0	NONE
0	0	1	S1A, S2A
0	1	1	S1B, S2A
1	0	1	S1A, S2B
1	1	1	S1B, S2B

CAUTION

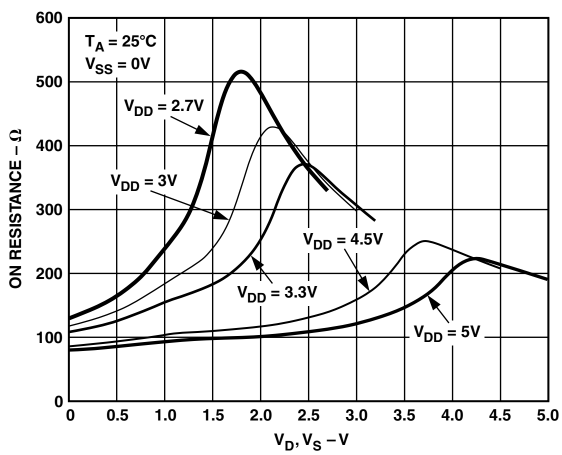
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG636 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

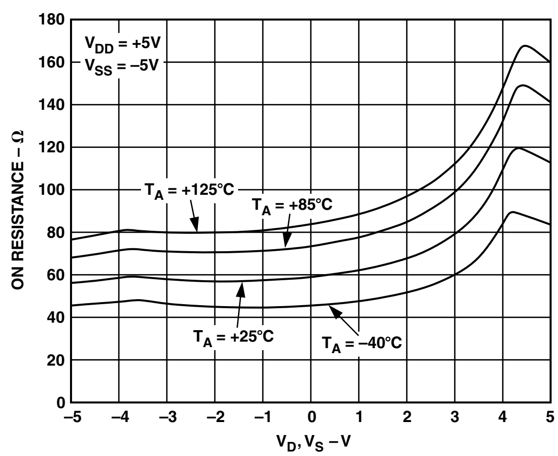
V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance Match between any two channels (i.e., R_{ON} max – R_{ON} min)
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of On Resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF"
I_D (OFF)	Drain Leakage Current with the Switch "OFF"
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON"
V_D , V_S	Analog Voltage on Terminals D, S
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
$I_{INL}(I_{INH})$	Input Current of the Digital Input
C_S (OFF)	Channel Input Capacitance for "OFF" condition.
C_D (OFF)	Channel Output Capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" Switch Capacitance
C_{IN}	Digital Input Capacitance
t_{ON}(EN)	Delay time between the 50% and 90% points of the digital input and Switch "ON" condition
t_{OFF}(EN)	Delay time between the 50% and 90% points of the digital input and Switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital input and Switch "ON" condition when switching from one address state to another.
t_{BBM}	"OFF" time or "ON" time measured between the 80% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the Glitch Impulse transferred from the Digital Input to the Analog Output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Bandwidth	The Frequency Response of the "ON" Switch
Insertion Loss	Loss Due to the On Resistance of the Switch



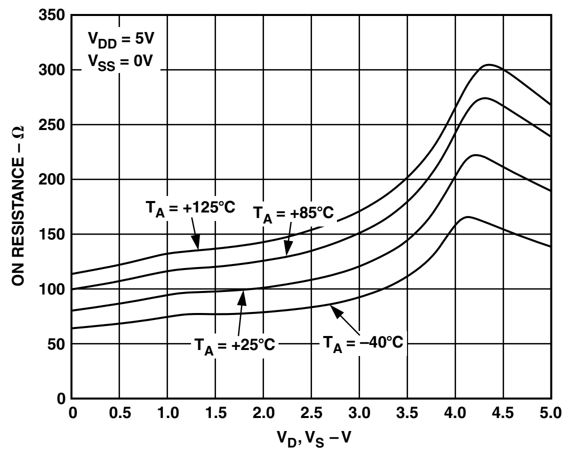
TPC 1. On Resistance vs. V_D (V_S). Dual Supply



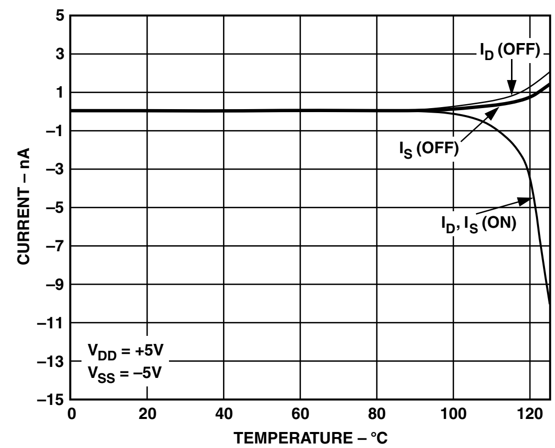
TPC 2. On Resistance vs. V_D (V_S). Single Supply



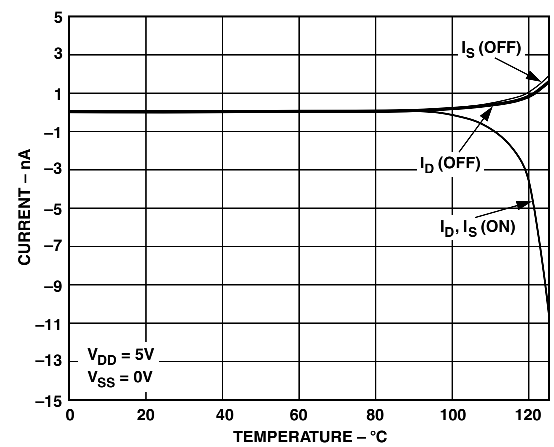
TPC 3. On Resistance vs. V_D (V_S) for Different Temperatures. Dual Supply



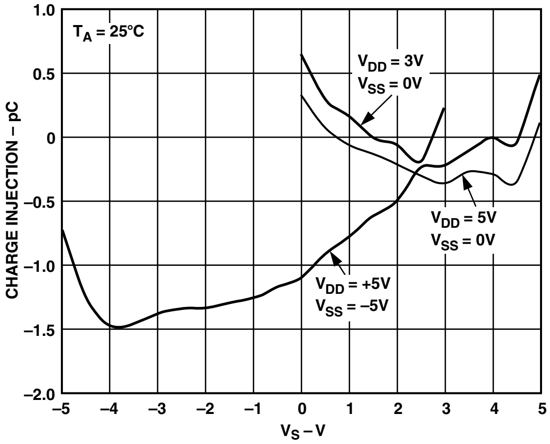
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures. Single Supply



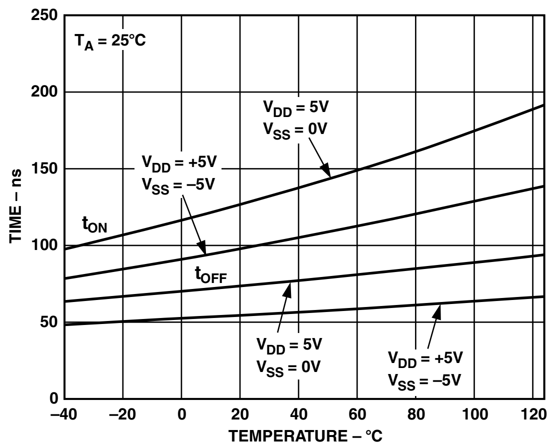
TPC 5. Leakage Currents vs. Temperatures. Dual Supply



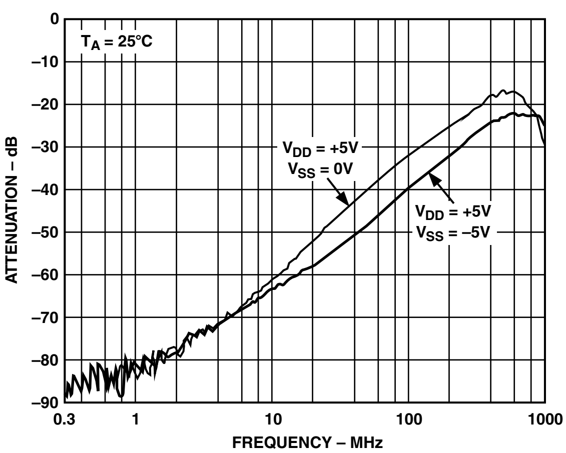
TPC 6. Leakage Currents vs. Temperature. Single Supply



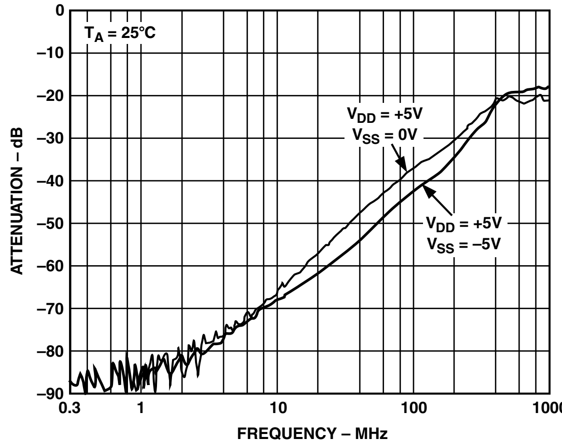
TPC 7. Charge Injection vs. Source Voltage



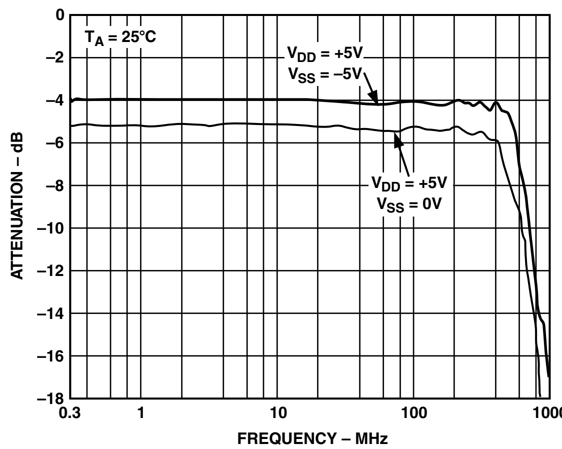
TPC 8. t_{ON}/t_{OFF} Enable Timing vs. Temperature



TPC 9. Off Isolation vs. Frequency

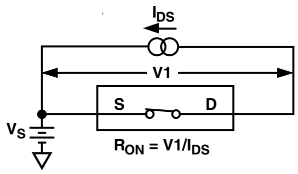


TPC 10. Crosstalk vs. Frequency

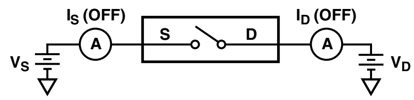


TPC 11. On Response vs. Frequency

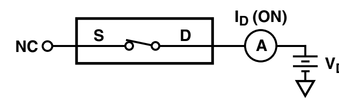
Test Circuits



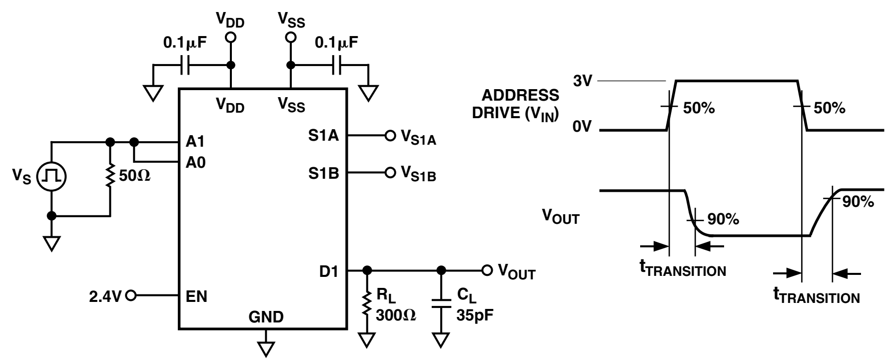
Test Circuit 1. On Resistance



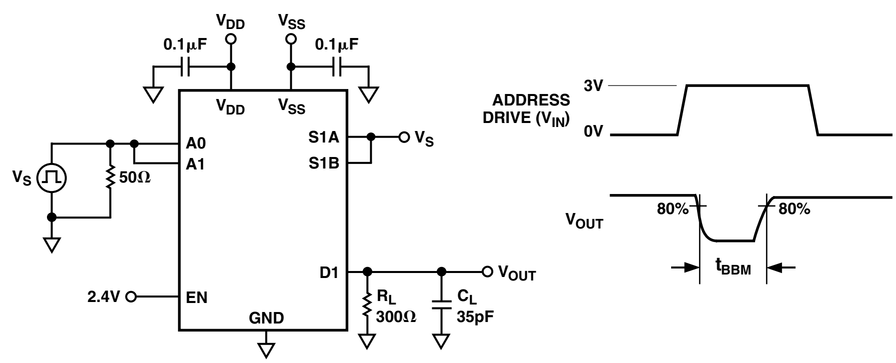
Test Circuit 2. Off Leakage



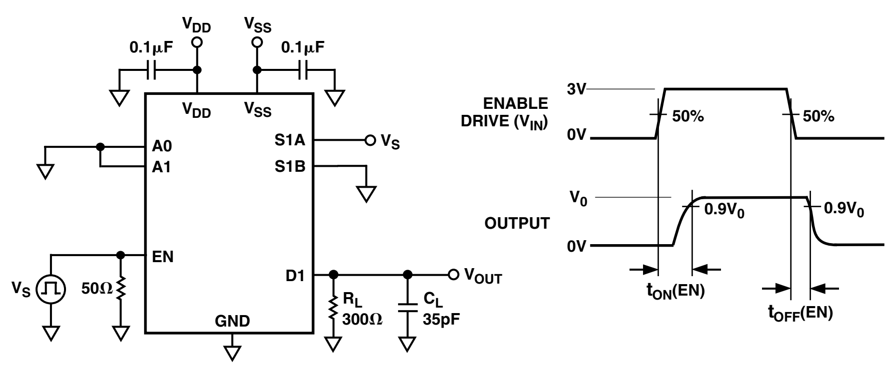
Test Circuit 3. On Leakage



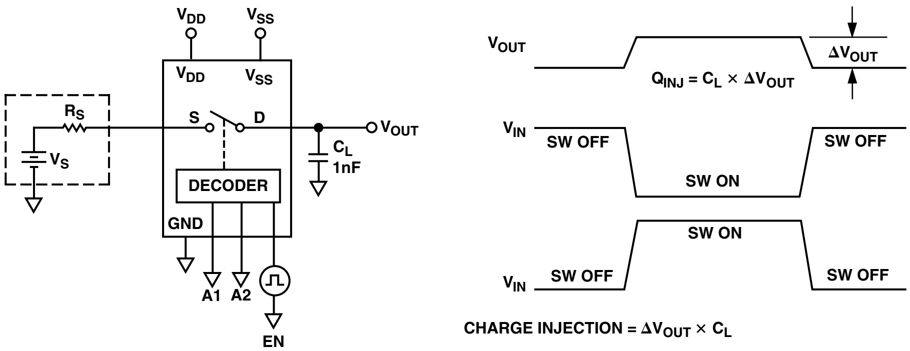
Test Circuit 4. Transition Time, $t_{TRANSITION}$



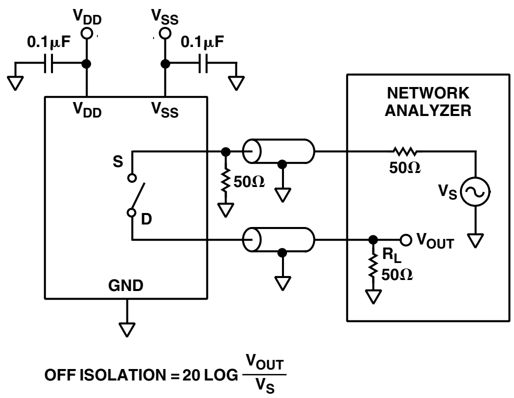
Test Circuit 5. Break-Before-Make Delay, t_{BBM}



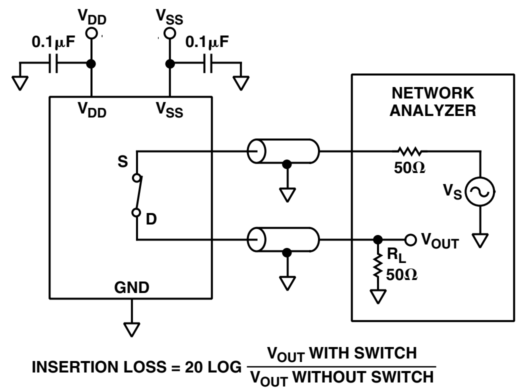
Test Circuit 6. Enable Delay, t_{ON} (EN), t_{OFF} (EN)



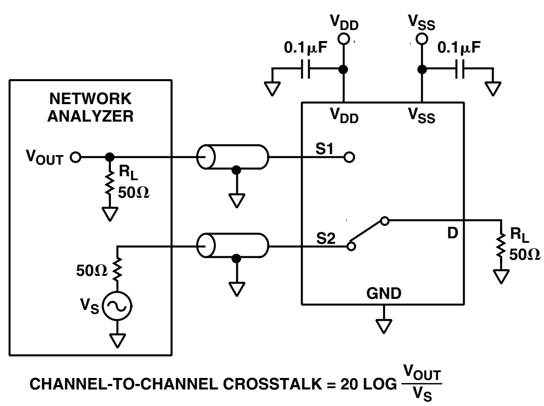
Test Circuit 7. Charge Injection



Test Circuit 8. Off Isolation



Test Circuit 9. Bandwidth

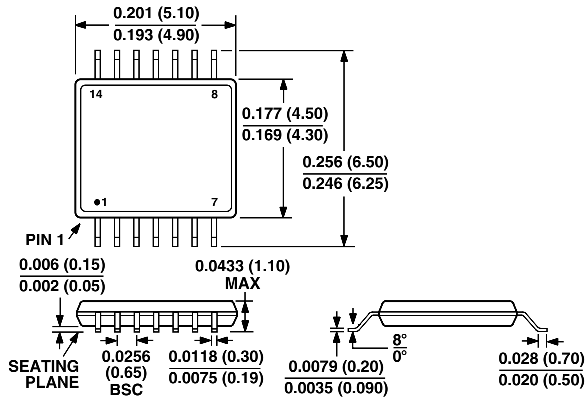


Test Circuit 10. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead TSSOP Package
(RU-14)



C02754-0-1/02(0)

PRINTED IN U.S.A.