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# ICS87946I-01

## LOW SKEW, ÷1, ÷2
## LVPECL-TO-LVCMOS/LVTTL CLOCK GENERATOR

## GENERAL DESCRIPTION

The ICS87946I-01 is a low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87946I-01 has one LVPECL clock input pair. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.
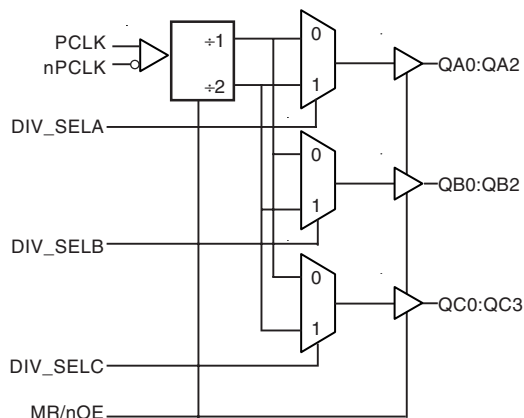
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87946I-01 is characterized at 3.3V core/3.3V output and 3.3V core/2.5V output. Guaranteed bank, output and part-to-part skew characteristics make the ICS87946I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.
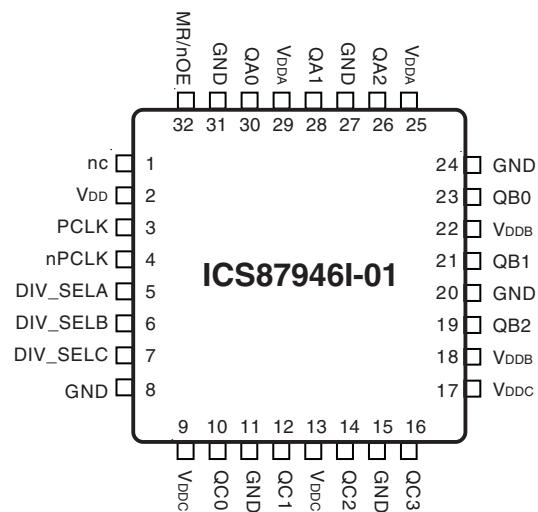
## FEATURES

- 10 single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance

- LVPECL clock input pair

- PCLK, nPCLK supports the following input levels: LVPECL, CML, SSTL

- Maximum input frequency: 250MHz

- Output skew: 120ps (maximum)

- Part-to-part skew: 700ps (maximum)

- Multiple frequency skew: 320ps (maximum)

- 3.3V core, 3.3V or 2.5V output supply modes

- -40°C to 85°C ambient operating temperature

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**32-Lead LQFP**
7mm x 7mm x 1.4mm package body
**Y Package**
Top View

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### TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | nc | Unused | | No connect. |
| 2 | $V_{DD}$ | Power | | Core supply pin. |
| 3 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 4 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 5 | DIV_SELA | Input | Pulldown | Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels. |
| 6 | DIV_SELB | Input | Pulldown | Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels. |
| 7 | DIV_SELC | Input | Pulldown | Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels. |
| 8, 11, 15, 20, 24, 27, 31 | GND | Power | | Power supply ground. |
| 9, 13, 17 | $V_{DDC}$ | Power | | Output supply pins for Bank C outputs. |
| 10, 12, 14, 16 | QC0, QC1, QC2, QC3 | Output | | Bank C outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance. |
| 18, 22 | $V_{DDB}$ | Power | | Output supply pins for Bank B outputs. |
| 19, 21, 23 | QB2, QB1, QB0 | Output | | Bank B outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance. |
| 25, 29 | $V_{DDA}$ | Power | | Output supply pins for Bank A outputs. |
| 26, 28, 30 | QA2, QA1, QA02, | Output | | Bank A outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance. |
| 32 | MR/nOE | Input | Pulldown | Active HIGH Master Reset. Active LOW Output Enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

### TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | KΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | KΩ |
| $C_{PD}$ | Power Dissipation Capacitance (per output); NOTE 1 | $V_{DD}$, $V_{DDx}$ = 3.465V | | | 23 | pF |
| $R_{OUT}$ | Output Impedance | | 5 | 7 | 12 | Ω |

NOTE 1: $V_{DDx}$ denotes $V_{DDA}$, $V_{DDB}$, $V_{DDC}$.

### TABLE 3. FUNCTION TABLE

| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| MR/nOE | DIV_SELA | DIV_SELB | DIV_SELC | QA0:QA2 | QB0:QB2 | QC0:QC3 |
| 1 | X | X | X | Hi Z | Hi Z | Hi Z |
| 0 | 0 | X | X | fIN/1 | Active | Active |
| 0 | 1 | X | X | fIN/2 | Active | Active |
| 0 | X | 0 | X | Active | fIN/1 | Active |
| 0 | X | 1 | X | Active | fIN/2 | Active |
| 0 | X | X | 0 | Active | Active | fIN/1 |
| 0 | X | X | 1 | Active | Active | fIN/2 |

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $V_O$ | -0.5V to $V_{DD}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD}$ = $V_{DDx}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDx}$ | Output Supply Voltage; NOTE 1 | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 54 | mA |
| $I_{DDx}$ | Output Supply Current; NOTE 2 | | | | 23 | mA |

NOTE 1: $V_{DDx}$ denotes $V_{DDA}$, $V_{DDB}$, $V_{DDC}$.
NOTE 2: $I_{DDx}$ denotes $I_{DDA}$, $I_{DDB}$, $I_{DDC}$.

### TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD}$ = 3.3V±5%, $V_{DDx}$ = 3.3V±5% OR 2.5V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | DIV_SELA, DIV_SELB, DIV_SELC, MR/nOE | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | DIV_SELA, DIV_SELB, DIV_SELC, MR/nOE | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1, 2 | | $V_{DDx}$ = 3.465V | 2.6 | | | V |
| | | | $V_{DDx}$ = 2.625V | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1, 2 | | | | | 0.5 | V |
| $I_{OZL}$ | Output Tristate Current Low | | | -5 | | | µA |
| $I_{OZH}$ | Output Tristate Current High | | | | | 5 | µA |

NOTE 1: Outputs terminated with 50Ω to $V_{DDx}$/2. See Paremeter Measurement Section, "3.3V Output Load Test Circuit".
NOTE 2: $V_{DDx}$ denotes $V_{DDA}$, $V_{DDB}$, $V_{DDC}$.

### TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{DD}$ = 3.3V±5%, $V_{DDx}$ = 3.3V±5% OR 2.5V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| | | nPCLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nPCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.3 | | 1 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 1.5 | | $V_{DD}$ | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is $V_{DD}$ + 0.3V.

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,** $V_{DD}$ = 3.3V±5%, $V_{DDx}$ = 2.5V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDx}$ | Output Supply Voltage; NOTE 1 | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | | | | 54 | mA |
| $I_{DDx}$ | Output Supply Current; NOTE 2 | | | | 22 | mA |

NOTE 1: $V_{DDx}$ denotes $V_{DDA}$, $V_{DDB}$, $V_{DDC}$.
NOTE 2: $I_{DDx}$ denotes $I_{DDA}$, $I_{DDB}$, $I_{DDC}$.

**TABLE 5A. AC CHARACTERISTICS,** $V_{DD}$ = $V_{DDx}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$ | Input Frequency | | | | 250 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | f ≤ 250MHz | 2.3 | 3.1 | 3.8 | ns |
| $t$sk(b) | Bank Skew; NOTE 2, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 30 | ps |
| $t$sk(o) | Output Skew; NOTE 3, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 130 | ps |
| $t$sk(w) | Multiple Frequency Skew; NOTE 4, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 320 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 5, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 700 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 400 | | 950 | ps |
| odc | Output Duty Cycle | | 40 | 50 | 60 | % |
| $t_{EN}$ | Output Enable Time; NOTE 6 | f = 10MHz | | | 3 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 6 | f = 10MHz | | | 3 | ns |

NOTE 1: Measured from the differential input crossing point to $V_{DDx}$/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}$/2.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltages and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}$/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.
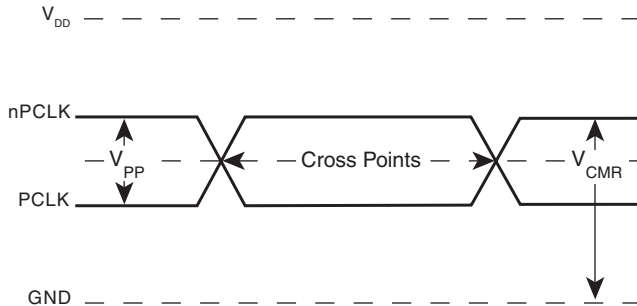
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LVPECL-TO-LVCMOS/LVTTL CLOCK GENERATOR

**TABLE 5B. AC CHARACTERISTICS,** $V_{DD}$ = 3.3V±5%, $V_{DDx}$ = 2.5V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Input Frequency | | | | 250 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | f ≤ 250MHz | 2.5 | 3.2 | 3.8 | ns |
| $t$sk(b) | Bank Skew; NOTE 2, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 35 | ps |
| $t$sk(o) | Output Skew; NOTE 3, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 120 | ps |
| $t$sk(w) | Multiple Frequency Skew; NOTE 4, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 325 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 5, 7 | Measured on rising edge at $V_{DDx}$/2 | | | 700 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 350 | | 800 | ps |
| odc | Output Duty Cycle | | 43 | 50 | 57 | % |
| $t_{EN}$ | Output Enable Time; NOTE 6 | f = 10MHz | | | 3 | ns |
| $t_{DIS}$ | Output Disable Time; NOTE 6 | f = 10MHz | | | 3 | ns |

NOTE 1: Measured from the differential input crossing point to $V_{DDx}$/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
Measured at $V_{DDx}$/2.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltages
and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and
with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}$/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

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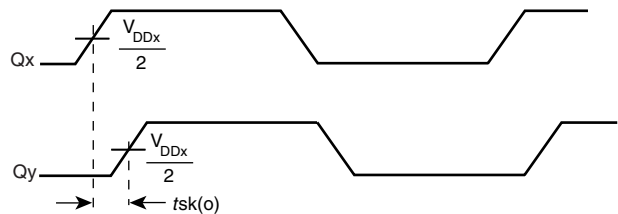
# PARAMETER MEASUREMENT INFORMATION
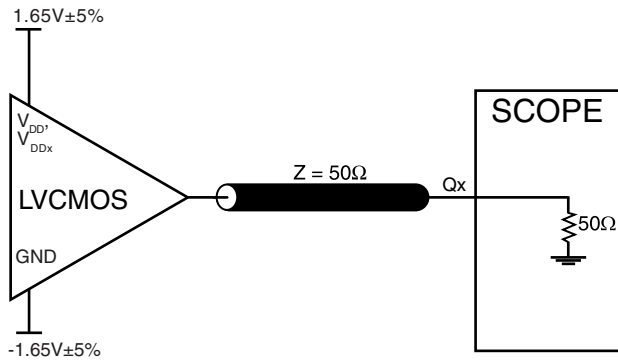
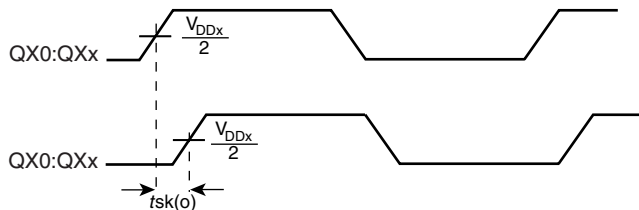**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**
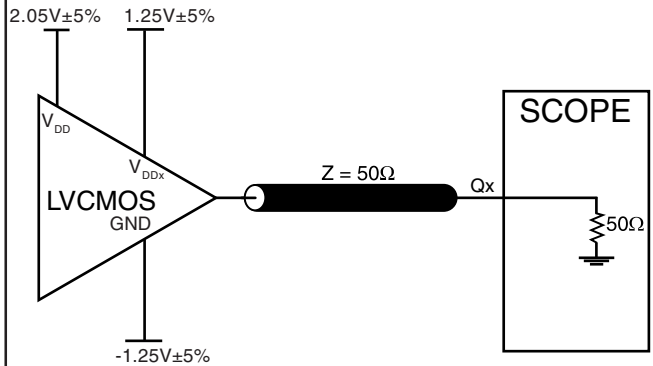
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**

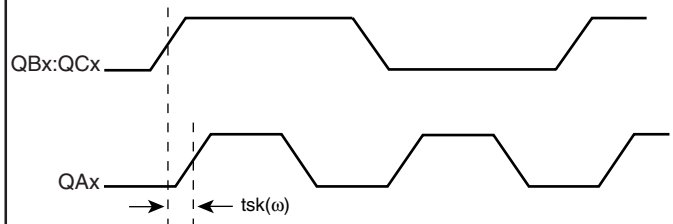**DIFFERENTIAL INPUT LEVEL**

**OUTPUT SKEW**

**BANK SKEW**

**MULTIPLE FREQUENCY SKEW**
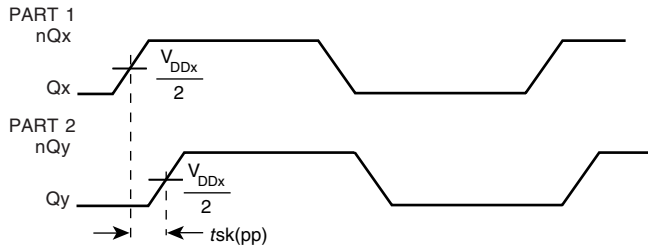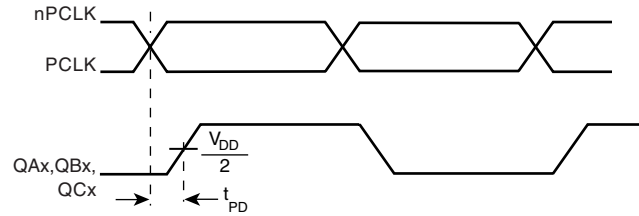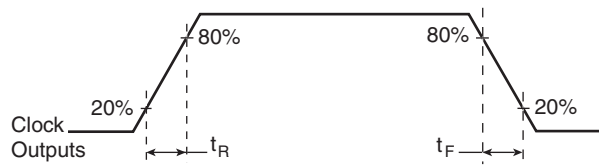
**ICS87946I-01**

Lᴏᴡ Sᴋᴇᴡ, ÷1, ÷2
LVPECL-ᴛᴏ-LVCMOS/LVTTL Cʟᴏᴄᴋ Gᴇɴᴇʀᴀᴛᴏʀ

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PART 1
nQx

Qx — $\dfrac{V_{DDx}}{2}$

PART 2
nQy

Qy — $\dfrac{V_{DDx}}{2}$

$t$sk(pp)

**Pᴀʀᴛ-ᴛᴏ-Pᴀʀᴛ Sᴋᴇᴡ**

nPCLK

PCLK

QAx, QBx,
QCx — $\dfrac{V_{DD}}{2}$

$t_{PD}$

**Pʀᴏᴘᴀɢᴀᴛɪᴏɴ Dᴇʟᴀʏ**

80% 80%

20% 20%

Clock
Outputs

$t_R$    $t_F$

**Oᴜᴛᴘᴜᴛ Rɪsᴇ/Fᴀʟʟ Tɪᴍᴇ**

QAx, QBx,
QCx — $\dfrac{V_{DDx}}{2}$

Pulse Width

$t_{PERIOD}$

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**Oᴜᴘᴜᴛ Dᴜᴛʏ Cʏᴄʟᴇ/Pᴜʟsᴇ Wɪᴅᴛʜ/Pᴇʀɪᴏᴅ**

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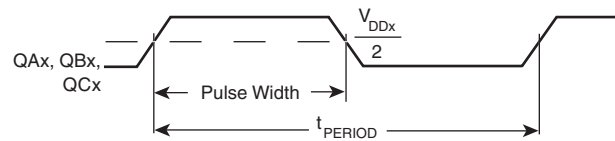
# APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 1* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

**FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT**

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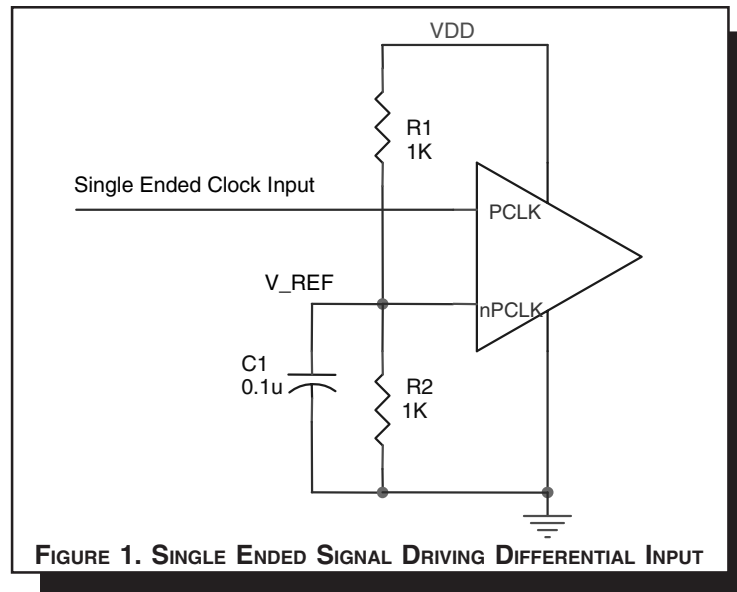
## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.
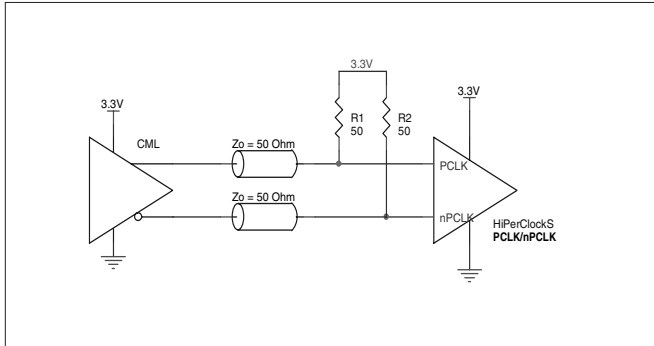


**FIGURE 2A.  HiPerClockS PCLK/nPCLK Input Driven by a CML Driver**
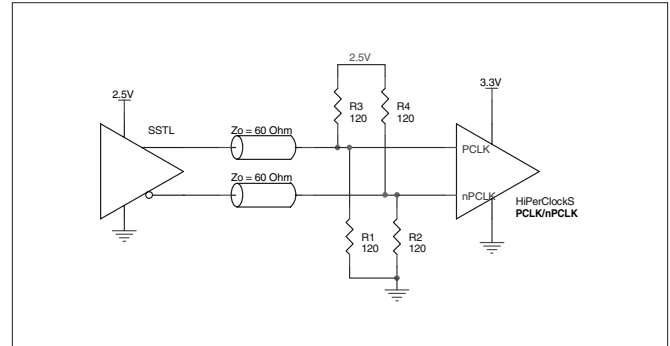


**FIGURE 2B.  HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver**
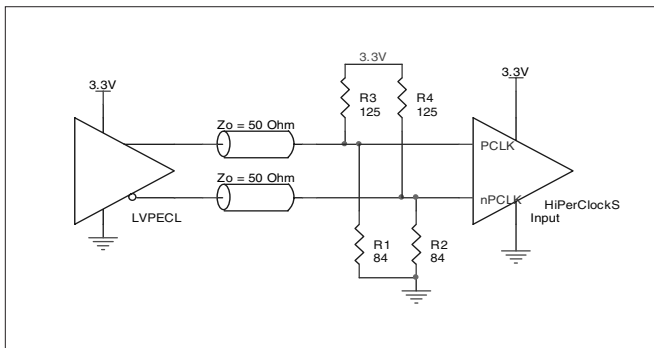


**FIGURE 2C.  HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**
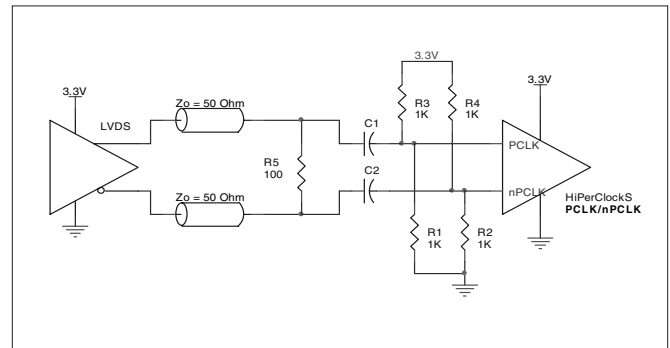


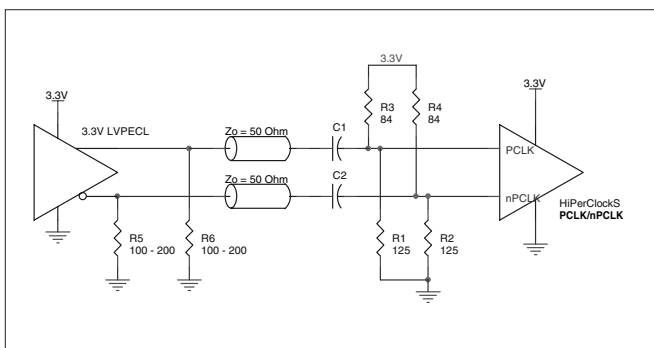**FIGURE 2D.  HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**



**FIGURE 2E.  HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

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# RELIABILITY INFORMATION

TABLE 6. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87946I-01 is: 1204

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**PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP**
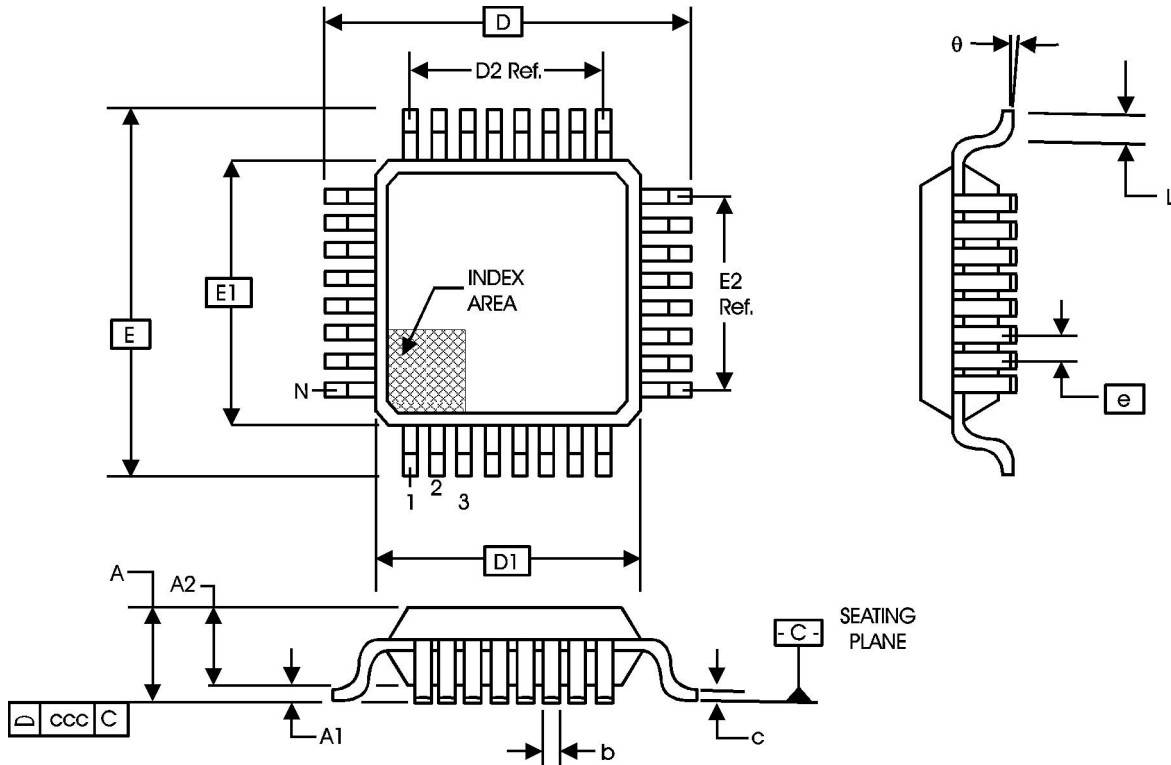


**TABLE 7. PACKAGE DIMENSIONS**

| SYMBOL | JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|
| | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

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**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS87946AYI-01 | ICS87946AYI01 | 32 Lead LQFP | 250 per tray | -40°C to 85°C |
| ICS87946AYI-01T | ICS87946AYI01 | 32 Lead LQFP on Tape and Reel | 1000 | -40°C to 85°C |