

# mos field effect power transistors 2SJ132, 2SJ132-Z

# P-CHANNEL POWER MOS FET FOR SWITCHING

#### **FEATURES**

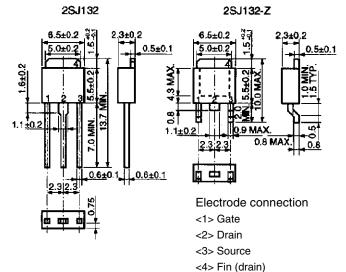
- Gate drive available at logic level (Vgs = -4 V)
- High current control available in small dimension due to low RDS(on) (≅ 0.25 Ω)
- 2SJ132-Z is a lead process product and is deal for mounting a hybrid IC.

### **QUALITY GRADES**

Standard

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

## PACKAGE DRAWING (UNIT: mm)

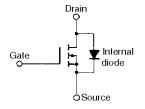


## ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Drain to source voltage	VDSS	V <sub>G</sub> S = 0	-30	V
Gate to source voltage	V <sub>GSS</sub>	V <sub>DS</sub> = 0	∓20	V
Drain current (DC)	I <sub>D(DC)</sub>	Tc = 25°C	∓2.0	Α
Drain current (pulse)	I <sub>D</sub> (pulse)	PW ≤ 300 <i>μ</i> s duty cycle ≤ 10 %	∓8.0	Α
Total power dissipation	Рт	Tc = 25°C	20	W
Total power dissipation	Рт	T <sub>a</sub> = 25°C	1.0*, 2.0**	W
Channel temperature	Tch		150	°C
Storage temperature	$T_{\text{stg}}$		-55 to +150	°C

## \* Printing board mounted

## INTERNAL EQUIVALENT CIRCUIT



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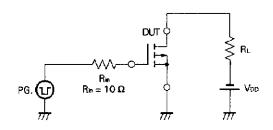
<sup>\*\* 7.5</sup> cm<sup>2</sup> × 0.7 mm ceramic board mounted

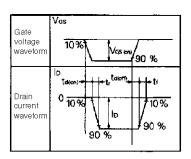


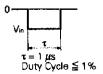
## **ELECTRICAL CHARACTERISTICS (Ta = 25°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain cutoff current	IDSS	$V_{DS} = -30 \text{ V}, V_{GS} = 0$			-10	μΑ
Gate cutoff current	Igss	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0$			∓100	nA
Gate cutoff voltage	V <sub>GS(off)</sub>	$V_{DS} = -10 \text{ V}, I_{D} = -1.0 \text{ mA}$	-1.0	-2.0	-3.0	V
Forward transfer admittance	yts	$V_{DS} = -10 \text{ V}, I_{D} = -1.0 \text{ A}$	1.0	1.8		S
Drain to source on-state resistance	RDS(on)1	Vgs = -10 V, ID = -1.0 A		0.25	0.4	Ω
Drain to source on-state resistance	RDS(on)2	Vgs = -4 V, ID = -0.8 A		0.4	0.6	Ω
Input capacitance	Ciss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}$		730		pF
Output capacitance	Coss	f = 1 MHz		180		pF
Reverse transfer capacitance	Crss			45		pF
Turn-on delay time	t <sub>d(on)</sub>	$I_D = -1.0 \text{ A}, V_{GS(on)} = -10 \text{ V}$		30		ns
Rise time	t <sub>t</sub>	$V_{DD} \cong -15 \text{ V}, \text{ RL} = 50 \Omega,$ $R_{in} = 10 \Omega$		30		ns
Turn-off delay time	t <sub>d(off)</sub>	1 1 1 1 1 2 2		110		ns
Fall time	tf			40		ns

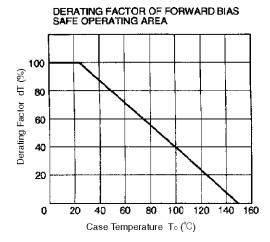
## SWITCHING TIME TEST CIRCUIT, TEST CONDITION (RESISTANCE LOAD)

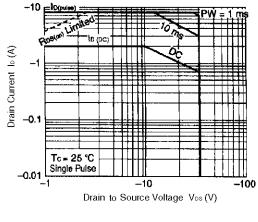




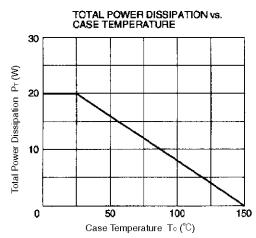


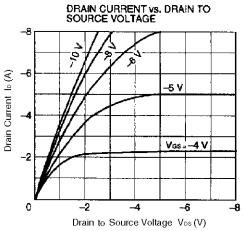
## TYPICAL CHARACTERISTICS (Ta = 25°C)

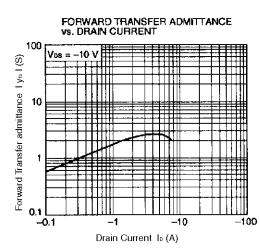


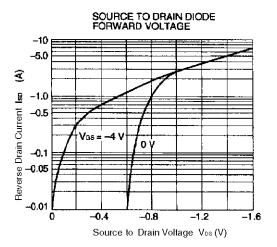


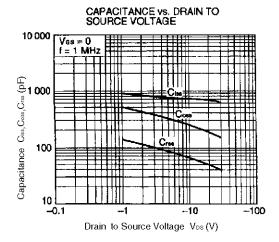
FORWARD BIAS SAFE OPERATING AREA

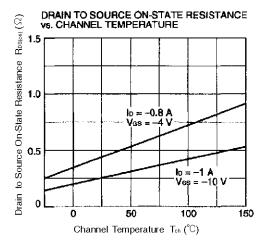


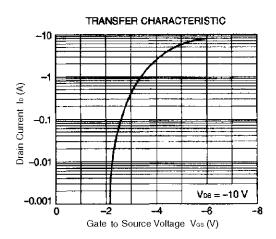


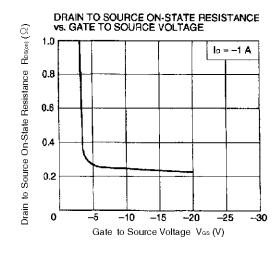


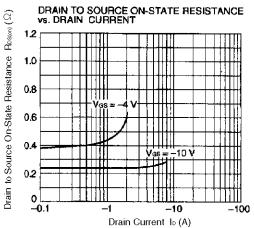


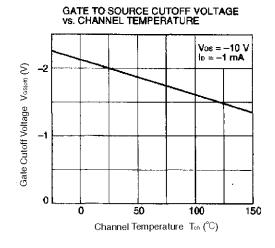


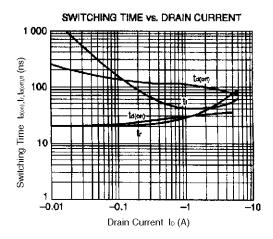


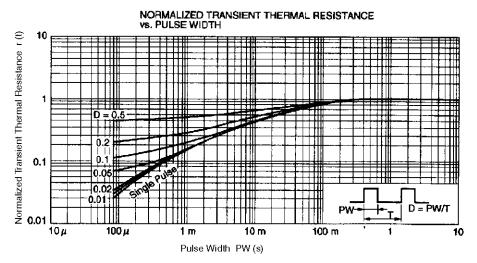












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