SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

DESCRIPTION

The M56769SP/FP is a semiconductor integrated circuit, an oxide-film separated ECL/I²L PLL frequency synthesizer. The prescaler and PLL, with a maximum operating frequency of 1.0 GHz, are housed on a single chip.

FEATURES

- Built-in prescaler with input amplifier (fmax=1.0GHz)
- Low power dissipation (Icc=30mA at Vcc=5V)
- Fine tuning capability (50.00kHz/step)
- PLL lock/unlock status display output
- Serial data input (2 or 3 data transfer lines)
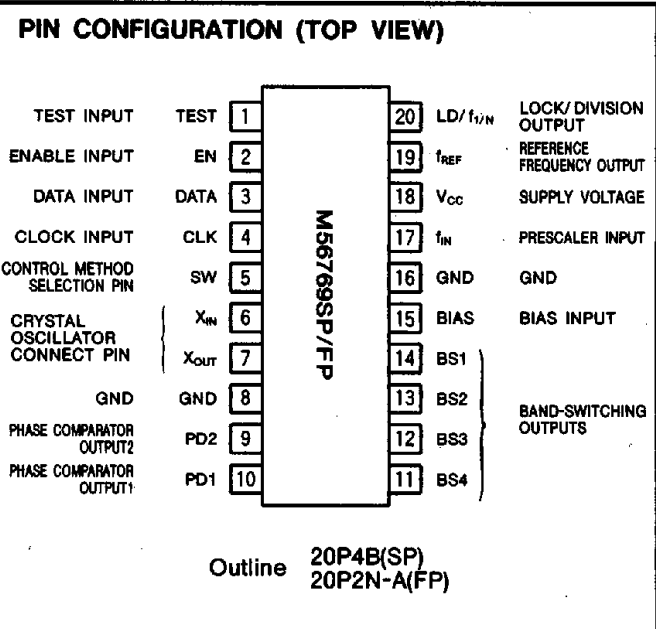
APPLICATION

TV and VCR tuners

RECOMMENDED OPERATING CONDITION

Supply voltage range...4.5~5.5V
Operating frequency(1)...4MHz(Typ)
(Crystal oscillator circuit)
Operating frequency(2)........................80~1000MHz(fIN input)
Output low-level current........................2mA(Max)(Pin ⑲.⑳)
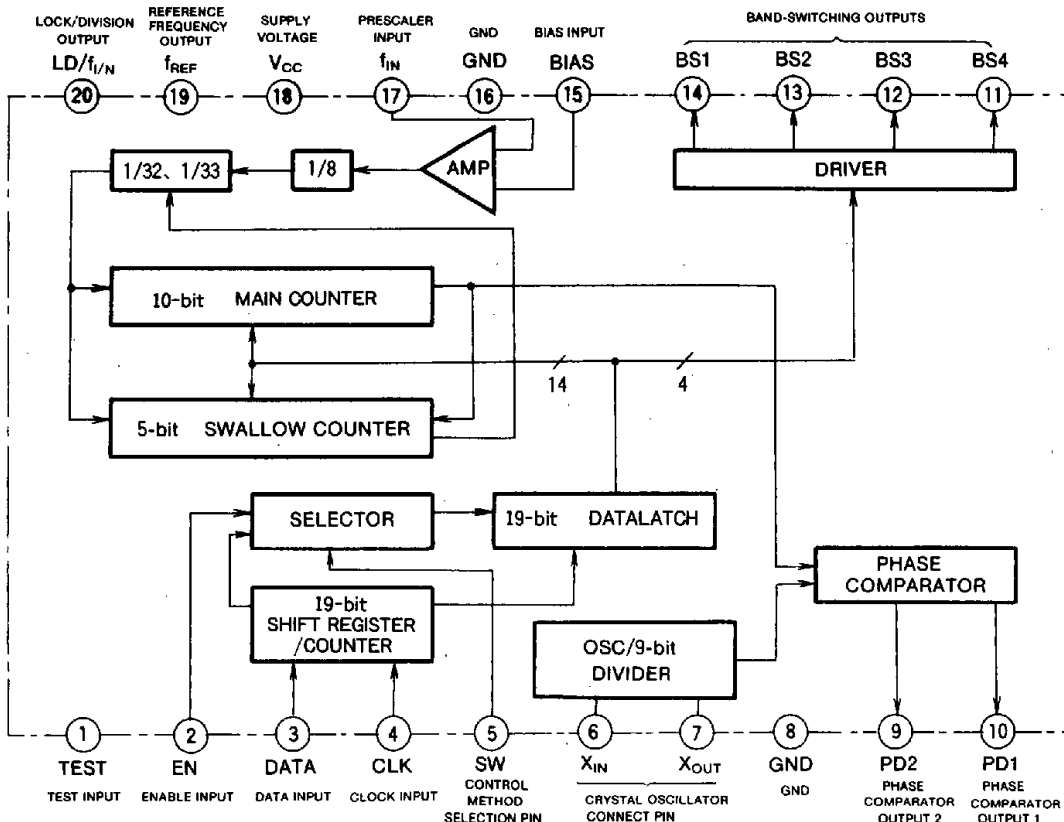Band output low-level current ⋯⋯1mA(Max)(Pin ⑪.⑫.⑬.⑭)

FUNCTION

The M56769SP/FP is a PLL frequency synthesizer IC for TVS and VCRS. The prescaler is realized in emitter-coupled logic and the PLL in integrated injection logic. The maximum oper-

PIN CONFIGURATION (TOP VIEW)

	Pin		Pin	
TEST INPUT	TEST 1		20 LD/f₁/N	LOCK/ DIVISION OUTPUT
ENABLE INPUT	EN 2		19 fREF	REFERENCE FREQUENCY OUTPUT
DATA INPUT	DATA 3		18 Vcc	SUPPLY VOLTAGE
CLOCK INPUT	CLK 4		17 fIN	PRESCALER INPUT
CONTROL METHOD SELECTION PIN	SW 5	M56769SP/FP	16 GND	GND
CRYSTAL OSCILLATOR CONNECT PIN	XIN 6		15 BIAS	BIAS INPUT
	XOUT 7		14 BS1	
GND	GND 8		13 BS2	BAND-SWITCHING OUTPUTS
PHASE COMPARATOR OUTPUT2	PD2 9		12 BS3	
PHASE COMPARATOR OUTPUT1	PD1 10		11 BS4	

Outline   20P4B(SP)
          20P2N-A(FP)

ating frequency of the prescaler is 1.0 GHz. The first stage consists of a fixed 1/8 prescaler and the second stage of a 1/32 1/33 dual-modulus prescaler. The PLL consists of a 3.2MHz crystal oscillator, a 9-bit reference frequency divider, a programmable divider(a 10-bit M counter and a 5-bit S counter), a phase comparator,and a lock detector. Four band-switching circuits are also provided.

BLOCK DIAGRAM

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings		Unit
		Min.	Max.	
Vcc	supply voltage	−0.5	6.5	V
Vi	Input voltage	−0.5	6.5	V
Vo1	Output voltage (1)　PD output	−0.5	5.5	V
Vo2	Output voltage (2)　Other than above	−0.5	6.5	V
Vв0	Output withstanding voltage		13	V
Pd	Power dissipation		550	mW
Topr	Operating temperature	−20	75	℃
Tstg	Storage temperature	−40	125	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
VIH	High-level input voltage		1, 2, 3, 4, 5		2.0		Vcc+0.3	V
VIL	Low-level input voltage		1, 2, 3, 4, 5				0.7	V
IIH1	High-level input current 1		1, 3, 4, 5, 2	Vcc=5.5V, VI=2.7V			50	μA
IIL1	Low-level input current 1		1, 3, 4, 5, 2	Vcc=5.5V, VI=0.4V		−100	−200	μA
VIC	Input clamp voltage		1, 2, 3, 4,	Vcc=4.5V, IIC=−1.0mA		−1.3	−1.8	V
VOL	Low-level output voltage		19, 20	Vcc=4.5V, IOL=2mA		0.3	0.5	V
IOLK1	Output leak current	PD output	10	Vcc=5.5V, Vo=0.5~4.8V	−1.0		1.0	μA
IOLK2		BS output	11~14	Vcc=4.5V, Vo=12V			10	μA
IOLK3		Other than above	19, 20	Vcc=5.5V, Vo=5.5V			10	μA
Icc	Supply current		18	Vcc=5.5V		33	55	mA

Typical values are at Vcc=5.0V, Ta=25℃.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test pin	Test conditions		Limits			Unit
					Min.	Typ.	Max.	
fopr	Prescaler operating frequency	17	Vcc=4.5~5.5V VIN=VINmin~VINmax		80		1000	MHz
VIN	Operating input voltage	17	Vcc=4.5~5.5V	80~100MHz	−24		4	dBm
				100~1000MHz	−27		4	
tpwc	Clock pulse width	4			1			μs
tsu (D)	Data setup time	3			2			μs
tH (D)	Data hold time	3			1			μs
tsu (E)	Enable setup time	2	Vcc=4.5~5.5V		3			μs
tH (E)	Enable hold time	2			3			μs
tINT	Enable data interval time	2, 3			1			μs
tr	Rising time	2, 3, 4					1	μs
tf	Falling time	2, 3, 4					1	μs

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

TEST CIRCUIT

* Setting dividing ratio of main counter and swallow counter

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY

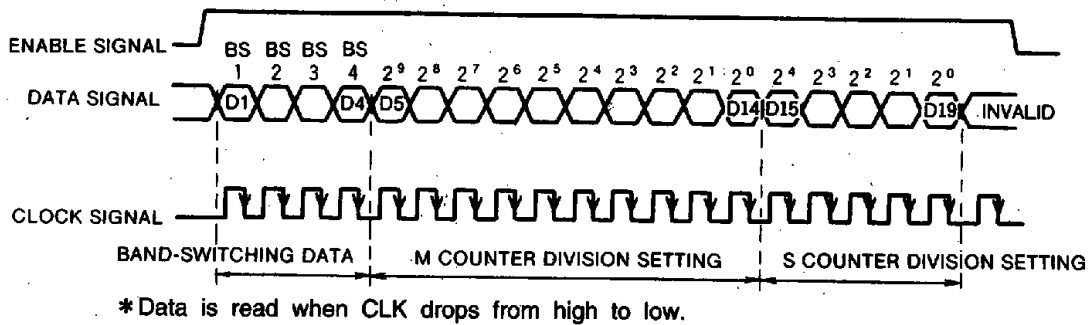

$V_{CC} = 5.0$ (V)
$T_a = 25$ (°C)

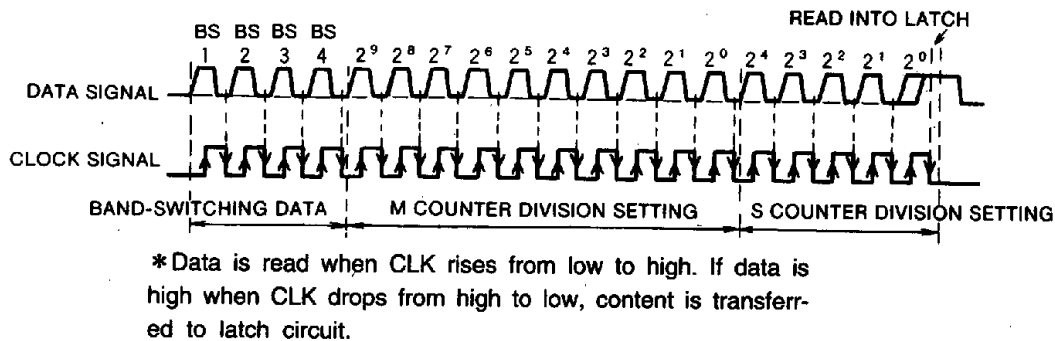INPUT AMPLITUDE V_{IN} (dBm)

INPUT FREQUENCY f_{IN} (MHz)

HOW TO SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER AND BAND-SWITCHING OUTPUT

(1) When the control method selection pin SW is set to Vcc or OPEN, the division ratio of the programmable divider and band-switching output is set as shown below.
When set high, the data and clock signals are read, and the data is read into the latch at the falling edge of the 19th clock signal pulse. The clock signal then becomes invalid.

* Data is read when CLK drops from high to low.

(2) When the control method selection pin SW is set to GND, the division ratio of the programmable divider and band-switching output is as shown below.

* Data is read when CLK rises from low to high. If data is high when CLK drops from high to low, content is transferred to latch circuit.

Total division N is given by the following formulas, in addition to the prescaler used in the previous stage.

$$N=8(32M+S)$$

M : 10-bit Main Counter Division
S : 5-bit Swallow Counter Division

The M and S counters are binary and the possible division ranges are as follows

$$32 \leq M \leq 1023$$
$$0 \leq S \leq 31$$

Therefore, the range of division N is 8,192~262,136.
The tuning frequency $f_{v.c.o.}$ is given by the following expressions.

$$f_{v.c.o.} = f_{REF} \times N$$
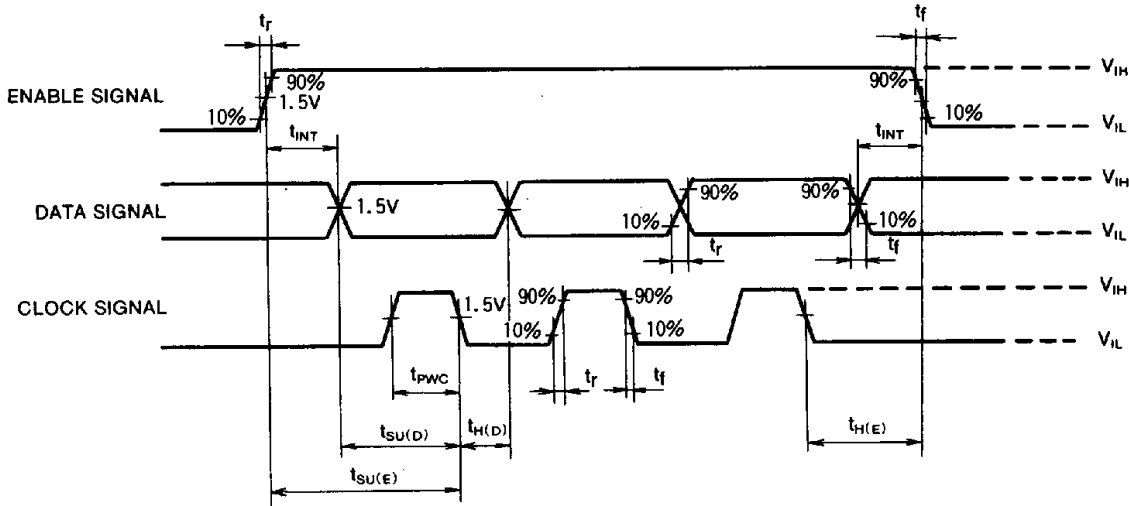$$= 6.250 \times 8 \cdot (32M+S)$$
$$= 50.0(32M+S)[kHz]$$

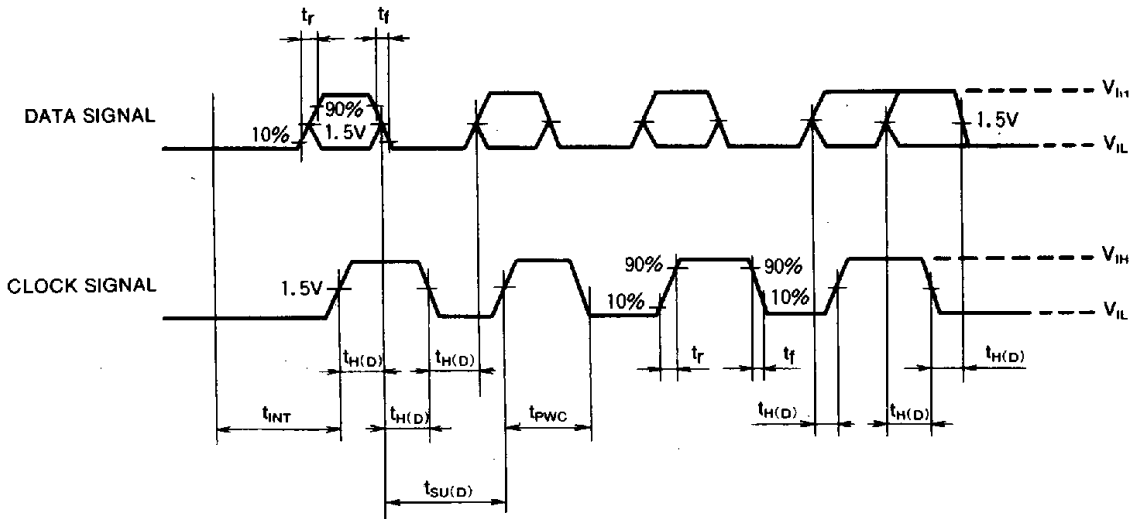Therefore, the tuning frequency range is 51.2MHz~1,000MHz.

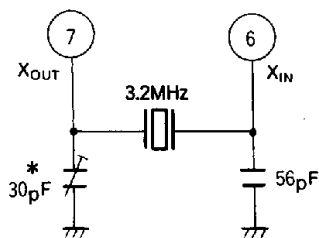### SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

TIMING DIAGRAM

(1) When the control method selection pin SW is set to Vcc(V)

(2) When the control method selection pin SW is set to GND

CRYSTAL OSCILLATATOR CONNECTION DIAGRAM
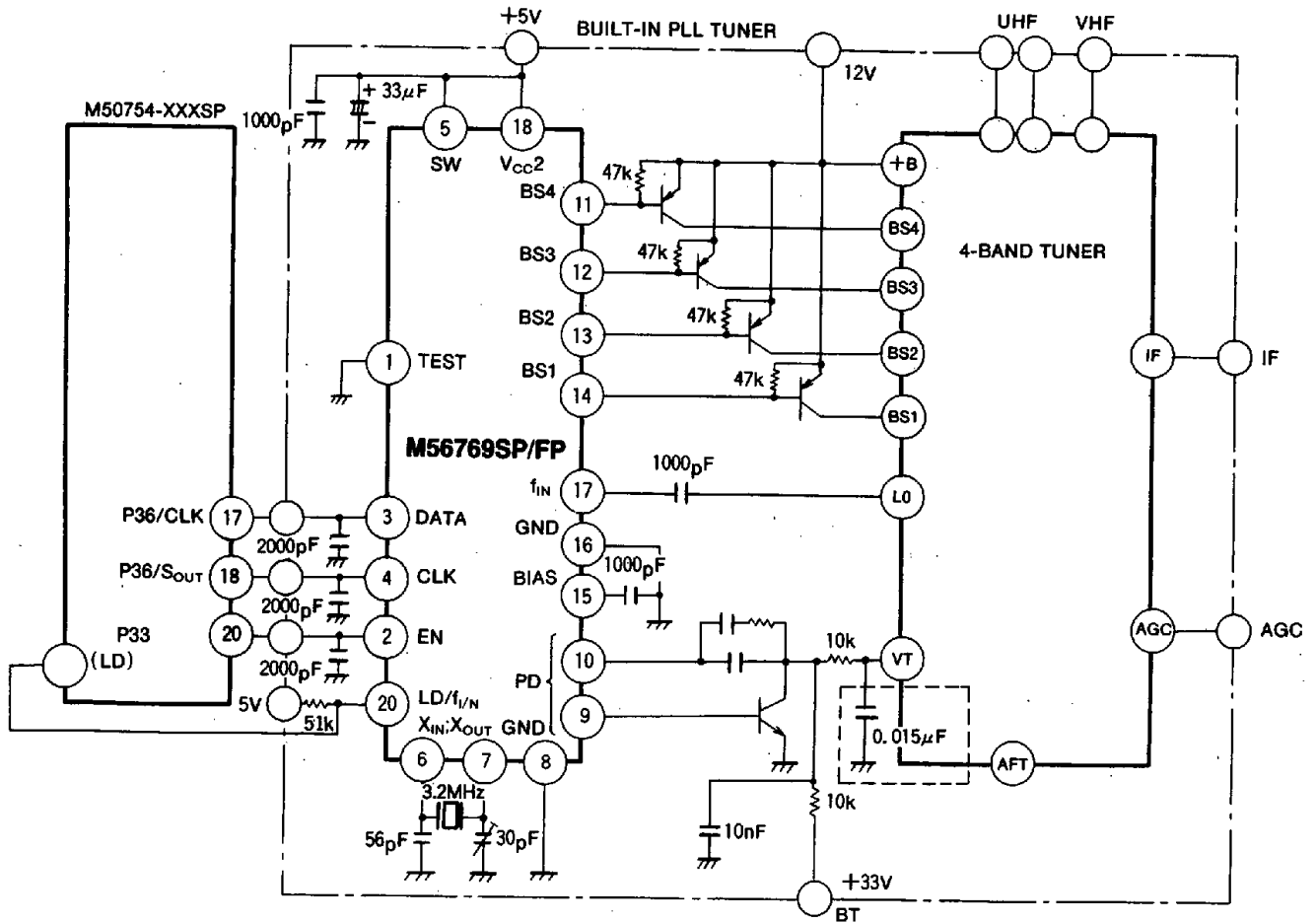

CRYSTAL OSCILLATOR CHARACTERISTICS
Actual resistance:less than 100Ω
Load capacitance:20pF
*This trimmer is used to compensate for frequency variations of around $\pm20\sim30$ ppm due to the crystal oscillator characteristics and oscillator circuit capacitance.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

APPLICATION EXAMPLE

Unit Resistance : Ω
      Capacitance : F

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VCR

DESCRIPTION OF PIN

No.	Pin	Name	Description of function
①	TEST	Test input	Pin is used for testing, and is normally set low, in which case LD is selected and f_{REF} is set low. When set high, f_{REF} and $f_{I/N}$ outputs are selected and phase comparator output enters high impedance state.
②	EN	Enable input	Pin is normally set low. When set high, data and clock signals are read, and data is read into latch at falling edge of 19th clock signals pulse. Clock signal then becoms invalid.
③	DATA	Data input	Programmble divider division set input
④	CLK	Clock input	When SW pin is set to Vcc or OPEN, data is read into shift register when clock signal drops from high to low. When SW pin is set to GND, data is read into shift register when clock signal rises from low to high.
⑤	SW	Control method selection pin	When SW pin is set to Vcc or OPEN, division ratio of programmable divider is set for enable input, data input and clock input pins. When SW pin is set to GND, division ratio of programmable divider is set for data and clock input pins only.
⑥ ⑦	XIN XOUT	Crystal oscillator connect pin	3.2MHz crystal oscillator is connected.
⑧	GND1	GND1	Connect to 0V.
⑨ ⑩	PD2 PD1	Phase comparator output 2 Phase comparator output 1	When phase programmable divider division output ($f_{I/N}$) is advanced with respect to reference frequency (f_{REF}), this output becomes high, and when programmable divider division output is delayed, it becomes low. When the two are in sync, output enters high-impedance state.
⑪ ⑫ ⑬ ⑭	BS4 BS3 BS2 BS1	Band-switching outputs pin	Open-collector band-switching outpus When band-switching data is high, output goes ON, when low, it goes OFF.
⑮	BIAS	Bias input	Prescaler bias pin. Capacitance of 1000pF is inserted between GND and this pin.
⑯	GND2	GND2	Connect to 0V.
⑰	fIN	Prescaler input pin	Prescaler input pin, to which V. C. O. frequency is applied.
⑱	Vcc	Supply voltage	Supply voltage pin, 5.0±0.5V is applied.
⑲	fREF	Reference frequency output	When TEST input is low, theres is a constant low-level output. When high , reference frequency output (f_{REF}) is selected. Reference frequency is 6.250kHz with open-collector output.
⑳	LD/fI/N	Lock detector/ division output	When TEST input is low, lock detector output (LD) is selected. When high, programmable divider division output ($f_{I/N}$) is selected. Open-colleector output. When PLL is locked, lock detector output (LD) becomes low.when PLL is unlocked, it becomes high.