Document Title

Multi-Chip Package MEMORY

32M Bit (4Mx8/2Mx16) Dual Bank NOR Flash Memory / 8M(1Mx8/512Kx16) Full CMOS SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	August 28, 2001	Preliminary
1.0	Final Specification	November 13, 2001	Final

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FEATURES

- Power Supply voltage : 2.7V to 3.3V
- Organization
  - Flash : 4,194,304 x 8 / 2,097,152 x 16 bit
  - SRAM : 1,048,576 x 8 / 524,288 x 16 bit
- Access Time (@2.7V)
  - Flash : 80 ns, SRAM : 55 ns
- Power Consumption (typical value)
  - Flash Read Current : 14 mA (@5MHz)
    Program/Erase Current : 15 mA
    Standby mode/Autosleep mode : 0.2 µA
    Read while Program or Read while Erase : 25 mA
  - SRAM Operating Current : 22 mA
    Standby Current : 0.5 µA
- Secode(Security Code) Block : Extra 64KB Block (Flash)
- Support Common Flash Memory Interface
- Block Group Protection / Unprotection (Flash)
- Flash Bank Size : 8Mb / 24Mb , 16Mb / 16Mb
- Flash Endurance : 100,000 Program/Erase Cycles Minimum
- SRAM Data Retention : 1.5 V (min.)
- Industrial Temperature : -40°C ~ 85°C
- Package : 69-ball TBGA Type - 8 x 11mm, 0.8 mm pitch
  1.2mm(max.) Thickness

GENERAL DESCRIPTION

The K5A3x80YT(B)A featuring single 3.0V power supply is a Multi Chip Package Memory which combines 32Mbit Dual Bank Flash and 8Mbit fCMOS SRAM.

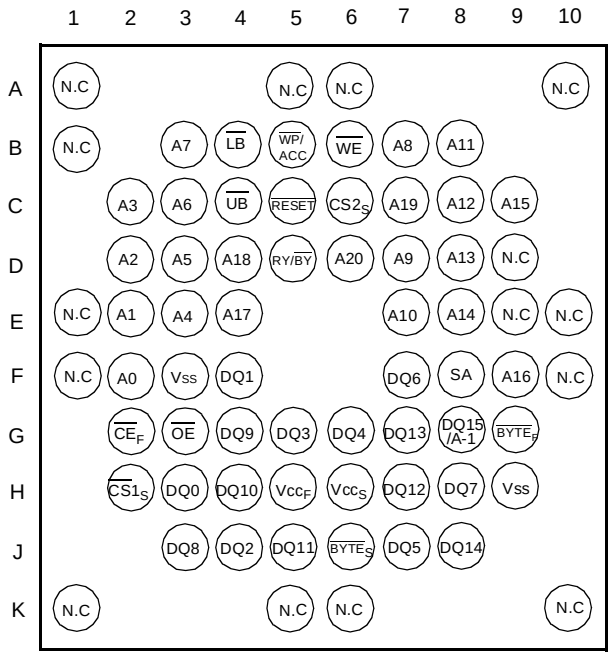
The 32Mbit Flash memory is organized as 4M x8 or 2M x16 bit and 8Mbit SRAM is organized as 1M x8 or 512K x16 bit. The memory architecture of flash memory is designed to divide its memory arrays into 71 blocks and this provides highly flexible erase and program capability. This device is capable of reading data from one bank while programming or erasing in the other bank with dual bank organization.

The Flash memory performs a program operation in units of 8 bits (Byte) or 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed for typically 0.7sec.

The 8Mbit SRAM supports low data retention voltage for battery backup operation with low data retention current.

The K5A3x80YT(B)A is suitable for the memory of mobile communication system to reduce mount area. This device is available in 69-ball TBGA Type package.

BALL CONFIGURATION



69 Ball TBGA , 0.8mm Pitch

Top View (Ball Down)

BALL DESCRIPTION

Ball Name	Description
A_0 to A_{18}	Address Input Balls (Common)
A-1, A_{19} to A_{20}	Address Input Balls (Flash Memory)
DQ_0 to DQ_{15}	Data Input/Output Balls (Common)
$\overline{RESET}$	Hardware Reset (Flash Memory)
$\overline{WP}$/ACC	Write Protection / Acceleration Program (Flash Memory)
Vcc_S	Power Supply (SRAM)
Vcc_F	Power Supply (Flash Memory)
Vss	Ground (Common)
$\overline{UB}$	Upper Byte Enable (SRAM)
$\overline{LB}$	Lower Byte Enable (SRAM)
$\overline{BYTE}_S$	$\overline{BYTE}_S$ Control (SRAM)
$\overline{BYTE}_F$	$\overline{BYTE}_F$ Control (Flash Memory)
SA	Address Inputs (SRAM)
$\overline{CE}_F$	Chip Enable (Flash Memory)
$\overline{CS1}_S$	Chip Enable (SRAM Low Active)
$CS2_S$	Chip Enable (SRAM High Active)
$\overline{WE}$	Write Enable (Common)
$\overline{OE}$	Output Enable (Common)
RY/$\overline{BY}$	Ready/Busy (Flash memory)
N.C	No Connection

ORDERING INFORMATION

K 5 A 3 x 8 0 Y T A - T 8 5 5

Samsung MCP Memory

Device Type
Dual Bank Boot Block NOR + fCMOS SRAM

NOR Flash Density (Bank Size), (Organization)
32 : 32Mbit, (8Mb, 24Mb) (x8/x16 Selectable)
33 : 32Mbit, (16Mb, 16Mb) (x8/x16 Selectable)

SRAM Density , Organization
8Mbit, x8/x16 Selectable

Operating Voltage Range
2.7V to 3.3V

SRAM Access Time
55 = 55 ns

Flash Access Time
8 = 80 ns
3 = 85 ns
9 = 90 ns

Package
T = 69 TBGA

Version
A = 2nd Generation

Block Architecture
T = Top Boot Block
B = Bottom Boot Block

Figure 1. FUNCTIONAL BLOCK DIAGRAM

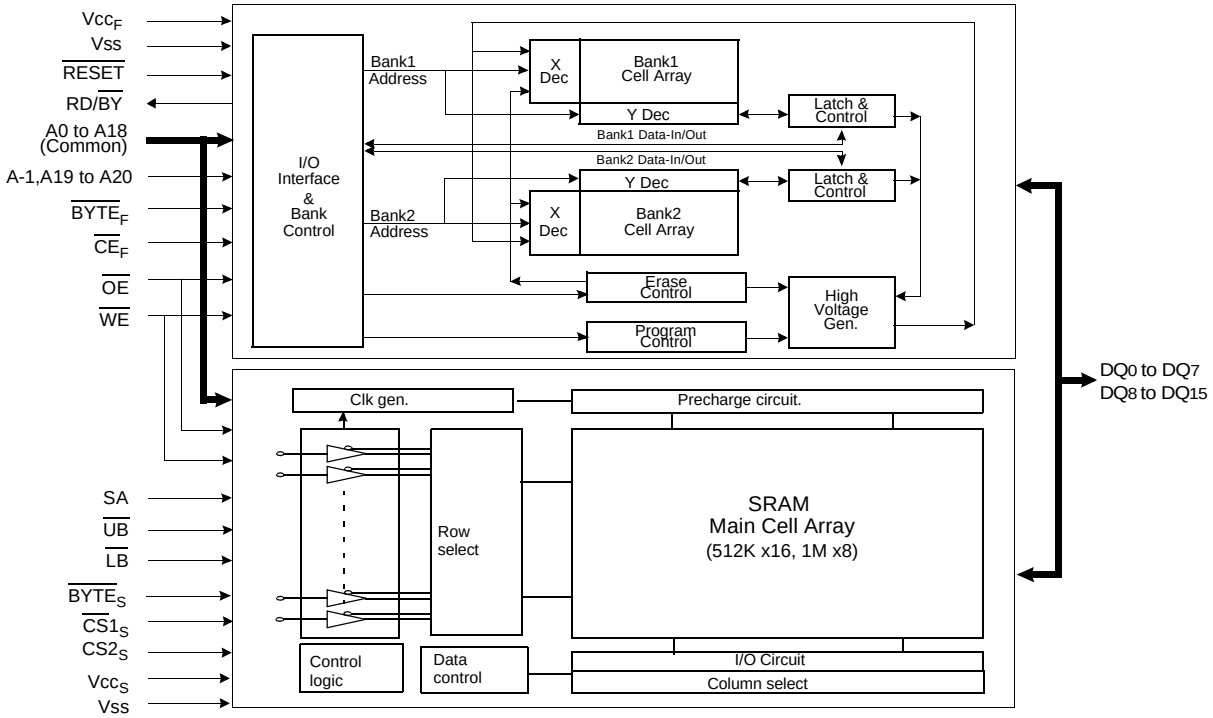


Table 1. Flash Memory Top Boot Block Address (K5A3280YT/K5A3380YT)

K5 A3280 YT	K5 A3380 YT	Block	Block Address									Block Size (KB/KW)	Address Range	
			A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank1	Bank1	BA70	1	1	1	1	1	1	1	1	1	8/4	3FE000H-3FFFFFH	1FF000H-1FFFFFH
		BA69	1	1	1	1	1	1	1	1	0	8/4	3FC000H-3FDFFFH	1FE000H-1FEFFFH
		BA68	1	1	1	1	1	1	1	0	1	8/4	3FA000H-3FBFFFH	1FD000H-1FDFFFH
		BA67	1	1	1	1	1	1	1	0	0	8/4	3F8000H-3F9FFFH	1FC000H-1FCFFFH
		BA66	1	1	1	1	1	1	0	1	1	8/4	3F6000H-3F7FFFH	1FB000H-1FBFFFH
		BA65	1	1	1	1	1	1	0	1	0	8/4	3F4000H-3F5FFFH	1FA000H-1FAFFFH
		BA64	1	1	1	1	1	1	0	0	1	8/4	3F2000H-3F3FFFH	1F9000H-1F9FFFH
		BA63	1	1	1	1	1	1	0	0	0	8/4	3F0000H-3F1FFFH	1F8000H-1F8FFFH
		BA62	1	1	1	1	1	0	X	X	X	64/32	3E0000H-3EFFFFH	1F0000H-1F7FFFH
		BA61	1	1	1	1	0	1	X	X	X	64/32	3D0000H-3DFFFFH	1E8000H-1EFFFFH
		BA60	1	1	1	1	0	0	X	X	X	64/32	3C0000H-3CFFFFH	1E0000H-1E7FFFH
		BA59	1	1	1	0	1	1	X	X	X	64/32	3B0000H-3BFFFFH	1D8000H-1DFFFFH
		BA58	1	1	1	0	1	0	X	X	X	64/32	3A0000H-3AFFFFH	1D0000H-1D7FFFH
		BA57	1	1	1	0	0	1	X	X	X	64/32	390000H-39FFFFH	1C8000H-1CFFFFH
		BA56	1	1	1	0	0	0	X	X	X	64/32	380000H-38FFFFH	1C0000H-1C7FFFH
		BA55	1	1	0	1	1	1	X	X	X	64/32	370000H-37FFFFH	1B8000H-1BFFFFH
		BA54	1	1	0	1	1	0	X	X	X	64/32	360000H-36FFFFH	1B0000H-1B7FFFH
		BA53	1	1	0	1	0	1	X	X	X	64/32	350000H-35FFFFH	1A8000H-1AFFFFH
		BA52	1	1	0	1	0	0	X	X	X	64/32	340000H-34FFFFH	1A0000H-1A7FFFH
		BA51	1	1	0	0	1	1	X	X	X	64/32	330000H-33FFFFH	198000H-19FFFFH
		BA50	1	1	0	0	1	0	X	X	X	64/32	320000H-32FFFFH	190000H-197FFFH
		BA49	1	1	0	0	0	1	X	X	X	64/32	310000H-31FFFFH	188000H-18FFFFH
		BA48	1	1	0	0	0	0	X	X	X	64/32	300000H-30FFFFH	180000H-187FFFH
Bank2		BA47	1	0	1	1	1	1	X	X	X	64/32	2F0000H-2FFFFFH	178000H-17FFFFH
		BA46	1	0	1	1	1	0	X	X	X	64/32	2E0000H-2EFFFFH	170000H-177FFFH
		BA45	1	0	1	1	0	1	X	X	X	64/32	2D0000H-2DFFFFH	168000H-16FFFFH
		BA44	1	0	1	1	0	0	X	X	X	64/32	2C0000H-2CFFFFH	160000H-167FFFH
		BA43	1	0	1	0	1	1	X	X	X	64/32	2B0000H-2BFFFFH	158000H-15FFFFH
		BA42	1	0	1	0	1	0	X	X	X	64/32	2A0000H-2AFFFFH	150000H-157FFFH
		BA41	1	0	1	0	0	1	X	X	X	64/32	290000H-29FFFFH	148000H-14FFFFH
		BA40	1	0	1	0	0	0	X	X	X	64/32	280000H-28FFFFH	140000H-147FFFH
		BA39	1	0	0	1	1	1	X	X	X	64/32	270000H-27FFFFH	138000H-13FFFFH
		BA38	1	0	0	1	1	0	X	X	X	64/32	260000H-26FFFFH	130000H-137FFFH
		BA37	1	0	0	1	0	1	X	X	X	64/32	250000H-25FFFFH	128000H-12FFFFH
		BA36	1	0	0	1	0	0	X	X	X	64/32	240000H-24FFFFH	120000H-127FFFH
		BA35	1	0	0	0	1	1	X	X	X	64/32	230000H-23FFFFH	118000H-11FFFFH

Table 1. Flash Memory Top Boot Block Address (K5A3280YT/K5A3380YT)

K5 A3280 YT	K5 A3380 YT	Block	Block Address									Block Size (KB/KW)	Address Range	
			A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	Bank1	BA34	1	0	0	0	1	0	X	X	X	64/32	220000H-22FFFFH	110000H-117FFFH
		BA33	1	0	0	0	0	1	X	X	X	64/32	210000H-21FFFFH	108000H-10FFFFH
		BA32	1	0	0	0	0	0	X	X	X	64/32	200000H-20FFFFH	100000H-107FFFH
	Bank2	BA31	0	1	1	1	1	1	X	X	X	64/32	1F0000H-1FFFFFH	0F8000H-0FFFFFH
		BA30	0	1	1	1	1	0	X	X	X	64/32	1E0000H-1EFFFFH	0F0000H-0F7FFFH
		BA29	0	1	1	1	0	1	X	X	X	64/32	1D0000H-1DFFFFH	0E8000H-0EFFFFH
		BA28	0	1	1	1	0	0	X	X	X	64/32	1C0000H-1CFFFFH	0E0000H-0E7FFFH
		BA27	0	1	1	0	1	1	X	X	X	64/32	1B0000H-1BFFFFH	0D8000H-0DFFFFH
		BA26	0	1	1	0	1	0	X	X	X	64/32	1A0000H-1AFFFFH	0D0000H-0D7FFFH
		BA25	0	1	1	0	0	1	X	X	X	64/32	190000H-19FFFFH	0C8000H-0CFFFFH
		BA24	0	1	1	0	0	0	X	X	X	64/32	180000H-18FFFFH	0C0000H-0C7FFFH
		BA23	0	1	0	1	1	1	X	X	X	64/32	170000H-17FFFFH	0B8000H-0BFFFFH
		BA22	0	1	0	1	1	0	X	X	X	64/32	160000H-16FFFFH	0B0000H-0B7FFFH
		BA21	0	1	0	1	0	1	X	X	X	64/32	150000H-15FFFFH	0A8000H-0AFFFFH
		BA20	0	1	0	1	0	0	X	X	X	64/32	140000H-14FFFFH	0A0000H-0A7FFFH
		BA19	0	1	0	0	1	1	X	X	X	64/32	130000H-13FFFFH	098000H-09FFFFH
		BA18	0	1	0	0	1	0	X	X	X	64/32	120000H-12FFFFH	090000H-097FFFH
		BA17	0	1	0	0	0	1	X	X	X	64/32	110000H-11FFFFH	088000H-08FFFFH
		BA16	0	1	0	0	0	0	X	X	X	64/32	100000H-10FFFFH	080000H-087FFFH
		BA15	0	0	1	1	1	1	X	X	X	64/32	0F0000H-0FFFFFH	078000H-07FFFFH
		BA14	0	0	1	1	1	0	X	X	X	64/32	0E0000H-0EFFFFH	070000H-077FFFH
		BA13	0	0	1	1	0	1	X	X	X	64/32	0D0000H-0DFFFFH	068000H-06FFFFH
		BA12	0	0	1	1	0	0	X	X	X	64/32	0C0000H-0CFFFFH	060000H-067FFFH
		BA11	0	0	1	0	1	1	X	X	X	64/32	0B0000H-0BFFFFH	058000H-05FFFFH
		BA10	0	0	1	0	1	0	X	X	X	64/32	0A0000H-0AFFFFH	050000H-057FFFH
		BA9	0	0	1	0	0	1	X	X	X	64/32	090000H-09FFFFH	048000H-04FFFFH
		BA8	0	0	1	0	0	0	X	X	X	64/32	080000H-08FFFFH	040000H-047FFFH
		BA7	0	0	0	1	1	1	X	X	X	64/32	070000H-07FFFFH	038000H-03FFFFH
		BA6	0	0	0	1	1	0	X	X	X	64/32	060000H-06FFFFH	030000H-037FFFH
		BA5	0	0	0	1	0	1	X	X	X	64/32	050000H-05FFFFH	028000H-02FFFFH
		BA4	0	0	0	1	0	0	X	X	X	64/32	040000H-04FFFFH	020000H-027FFFH
		BA3	0	0	0	0	1	1	X	X	X	64/32	030000H-03FFFFH	018000H-01FFFFH
		BA2	0	0	0	0	1	0	X	X	X	64/32	020000H-02FFFFH	010000H-017FFFH
		BA1	0	0	0	0	0	1	X	X	X	64/32	010000H-01FFFFH	008000H-00FFFFH
		BA0	0	0	0	0	0	0	X	X	X	64/32	000000H-00FFFFH	000000H-007FFFH

Note : The address range is A20 ~ A-1 in the byte mode ($\overline{BYTE}_F$ = V_{IL}) or A20 ~ A0 in the word mode ($\overline{BYTE}_F$ = V_{IH}).
The bank address bits is A20 ~ A19 for K5A3280YT, A20 for K5A3380YT.

Table 2. Secode Block Addresses for Top Boot Devices

Device	Block Address A20-A12	Block Size	(X8) Address Range	(X16) Address Range
K5A3280YT/K5A3380YT	111111xxx	64/32	3F0000H-3FFFFFH	1F8000H-1FFFFFH

Table 3. Flash Memory Bottom Boot Block Address (K5A3280YB/K5A3380YB)

K5 A3280 YB	K5 A3380 YB	Block	Block Address									Block Size (KB/KW)	Address Range	
			A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	Bank2	BA70	1	1	1	1	1	1	X	X	X	64/32	3F0000H-3FFFFFH	1F8000H-1FFFFFH
		BA69	1	1	1	1	1	0	X	X	X	64/32	3E0000H-3EFFFFH	1F0000H-1F7FFFH
		BA68	1	1	1	1	0	1	X	X	X	64/32	3D0000H-3DFFFFH	1E8000H-1EFFFFH
		BA67	1	1	1	1	0	0	X	X	X	64/32	3C0000H-3CFFFFH	1E0000H-1E7FFFH
		BA66	1	1	1	0	1	1	X	X	X	64/32	3B0000H-3BFFFFH	1D8000H-1DFFFFH
		BA65	1	1	1	0	1	0	X	X	X	64/32	3A0000H-3AFFFFH	1D0000H-1D7FFFH
		BA64	1	1	1	0	0	1	X	X	X	64/32	390000H-39FFFFH	1C8000H-1CFFFFH
		BA63	1	1	1	0	0	0	X	X	X	64/32	380000H-38FFFFH	1C0000H-1C7FFFH
		BA62	1	1	0	1	1	1	X	X	X	64/32	370000H-37FFFFH	1B8000H-1BFFFFH
		BA61	1	1	0	1	1	0	X	X	X	64/32	360000H-36FFFFH	1B0000H-1B7FFFH
		BA60	1	1	0	1	0	1	X	X	X	64/32	350000H-35FFFFH	1A8000H-1AFFFFH
		BA59	1	1	0	1	0	0	X	X	X	64/32	340000H-34FFFFH	1A0000H-1A7FFFH
		BA58	1	1	0	0	1	1	X	X	X	64/32	330000H-33FFFFH	198000H-19FFFFH
		BA57	1	1	0	0	1	0	X	X	X	64/32	320000H-32FFFFH	190000H-197FFFH
		BA56	1	1	0	0	0	1	X	X	X	64/32	310000H-31FFFFH	188000H-18FFFFH
		BA55	1	1	0	0	0	0	X	X	X	64/32	300000H-30FFFFH	180000H-187FFFH
		BA54	1	0	1	1	1	1	X	X	X	64/32	2F0000H-2F1FFFH	178000H-17FFFFH
		BA53	1	0	1	1	1	0	X	X	X	64/32	2E0000H-2EFFFFH	170000H-177FFFH
		BA52	1	0	1	1	0	1	X	X	X	64/32	2D0000H-2DFFFFH	168000H-16FFFFH
		BA51	1	0	1	1	0	0	X	X	X	64/32	2C0000H-2CFFFFH	160000H-167FFFH
		BA50	1	0	1	0	1	1	X	X	X	64/32	2B0000H-2BFFFFH	158000H-15FFFFH
		BA49	1	0	1	0	1	0	X	X	X	64/32	2A0000H-2AFFFFH	150000H-157FFFH
		BA48	1	0	1	0	0	1	X	X	X	64/32	290000H-29FFFFH	148000H-14FFFFH
		BA47	1	0	1	0	0	0	X	X	X	64/32	280000H-28FFFFH	140000H-147FFFH
		BA46	1	0	0	1	1	1	X	X	X	64/32	270000H-27FFFFH	138000H-13FFFFH
		BA45	1	0	0	1	1	0	X	X	X	64/32	260000H-26FFFFH	130000H-137FFFH
		BA44	1	0	0	1	0	1	X	X	X	64/32	250000H-25FFFFH	128000H-12FFFFH
		BA43	1	0	0	1	0	0	X	X	X	64/32	240000H-24FFFFH	120000H-127FFFH
		BA42	1	0	0	0	1	1	X	X	X	64/32	230000H-23FFFFH	118000H-11FFFFH
		BA41	1	0	0	0	1	0	X	X	X	64/32	220000H-22FFFFH	110000H-117FFFH
		BA40	1	0	0	0	0	1	X	X	X	64/32	210000H-21FFFFH	108000H-10FFFFH
		BA39	1	0	0	0	0	0	X	X	X	64/32	200000H-20FFFFH	100000H-107FFFH
		BA38	0	1	1	1	1	1	X	X	X	64/32	1F0000H-1FFFFFH	0F8000H-0FFFFFH
		BA37	0	1	1	1	1	0	X	X	X	64/32	1E0000H-1EFFFFH	0F0000H-0F7FFFH
		BA36	0	1	1	1	0	1	X	X	X	64/32	1D0000H-1DFFFFH	0E8000H-0EFFFFH
		BA35	0	1	1	1	0	0	X	X	X	64/32	1C0000H-1CFFFFH	0E0000H-0E7FFFH

Table 3. Flash Memory Bottom Boot Block Address (K5A3280YB/K5A3380YB)

K5 A3280 YB	K5 A3380 YB	Block	Block Address									Block Size (KB/KW)	Address Range	
			A20	A19	A18	A17	A16	A15	A14	A13	A12		Byte Mode	Word Mode
Bank2	Bank1	BA34	0	1	1	0	1	1	X	X	X	64/32	1B0000H-1BFFFFH	0D8000H-0DFFFFH
		BA33	0	1	1	0	1	0	X	X	X	64/32	1A0000H-1AFFFFH	0D0000H-0D7FFFH
		BA32	0	1	1	0	0	1	X	X	X	64/32	190000H-19FFFFH	0C8000H-0CFFFFH
		BA31	0	1	1	0	0	0	X	X	X	64/32	180000H-18FFFFH	0C0000H-0C7FFFH
		BA30	0	1	0	1	1	1	X	X	X	64/32	170000H-17FFFFH	0B8000H-0BFFFFH
		BA29	0	1	0	1	1	0	X	X	X	64/32	160000H-16FFFFH	0B0000H-0B7FFFH
		BA28	0	1	0	1	0	1	X	X	X	64/32	150000H-15FFFFH	0A8000H-0AFFFFH
		BA27	0	1	0	1	0	0	X	X	X	64/32	140000H-14FFFFH	0A0000H-0A7FFFH
		BA26	0	1	0	0	1	1	X	X	X	64/32	130000H-13FFFFH	098000H-09FFFFH
		BA25	0	1	0	0	1	0	X	X	X	64/32	120000H-12FFFFH	090000H-097FFFH
		BA24	0	1	0	0	0	1	X	X	X	64/32	110000H-11FFFFH	088000H-08FFFFH
		BA23	0	1	0	0	0	0	X	X	X	64/32	100000H-10FFFFH	080000H-087FFFH
Bank1		BA22	0	0	1	1	1	1	X	X	X	64/32	0F0000H-0FFFFFH	078000H-07FFFFH
		BA21	0	0	1	1	1	0	X	X	X	64/32	0E0000H-0EFFFFH	070000H-077FFFH
		BA20	0	0	1	1	0	1	X	X	X	64/32	0D0000H-0DFFFFH	068000H-06FFFFH
		BA19	0	0	1	1	0	0	X	X	X	64/32	0C0000H-0CFFFFH	060000H-067FFFH
		BA18	0	0	1	0	1	1	X	X	X	64/32	0B0000H-0BFFFFH	058000H-05FFFFH
		BA17	0	0	1	0	1	0	X	X	X	64/32	0A0000H-0AFFFFH	050000H-057FFFH
		BA16	0	0	1	0	0	1	X	X	X	64/32	090000H-09FFFFH	048000H-04FFFFH
		BA15	0	0	1	0	0	0	X	X	X	64/32	080000H-08FFFFH	040000H-047FFFH
		BA14	0	0	0	1	1	1	X	X	X	64/32	070000H-07FFFFH	038000H-03FFFFH
		BA13	0	0	0	1	1	0	X	X	X	64/32	060000H-06FFFFH	030000H-037FFFH
		BA12	0	0	0	1	0	1	X	X	X	64/32	050000H-05FFFFH	028000H-02FFFFH
		BA11	0	0	0	1	0	0	X	X	X	64/32	040000H-04FFFFH	020000H-027FFFH
		BA10	0	0	0	0	1	1	X	X	X	64/32	030000H-03FFFFH	018000H-01FFFFH
		BA9	0	0	0	0	1	0	X	X	X	64/32	020000H-02FFFFH	010000H-017FFFH
		BA8	0	0	0	0	0	1	X	X	X	64/32	010000H-01FFFFH	008000H-00FFFFH
		BA7	0	0	0	0	0	0	1	1	1	8/4	00E000H-00FFFFH	007000H-007FFFH
		BA6	0	0	0	0	0	0	1	1	0	8/4	00C000H-00DFFFH	006000H-006FFFH
		BA5	0	0	0	0	0	0	1	0	1	8/4	00A000H-00BFFFH	005000H-005FFFH
		BA4	0	0	0	0	0	0	1	0	0	8/4	008000H-009FFFH	004000H-004FFFH
		BA3	0	0	0	0	0	0	0	1	1	8/4	006000H-007FFFH	003000H-003FFFH
		BA2	0	0	0	0	0	0	0	1	0	8/4	004000H-005FFFH	002000H-002FFFH
		BA1	0	0	0	0	0	0	0	0	1	8/4	002000H-003FFFH	001000H-001FFFH
		BA0	0	0	0	0	0	0	0	0	0	8/4	000000H-001FFFH	000000H-000FFFH

Note : The address range is A20 ~ A-1 in the byte mode ($\overline{BYTE}_F$ = V_{IL}) or A20 ~ A0 in the word mode ($\overline{BYTE}_F$ = V_{IH}).
The bank address bits is A20 ~ A19 for K5A3280YB, A20 for K5A3380YB.

Table 4. Secode Block Addresses for Bottom Boot Devices

Device	Block Address A20-A12	Block Size	(X8) Address Range	(X16) Address Range
K5A3280YB/K5A3380YB	000000xxx	64/32	000000H-00FFFFH	000000H-007FFFH

Flash MEMORY COMMAND DEFINITIONS

Flash memory operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 5. Note that Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Block Erase Operation is in progress.

Table 5. Command Sequences

Command Sequence		Cycle	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
			Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
Read	Addr	1	RA											
	Data		RD											
Reset	Addr	1	XXXH											
	Data		F0H											
Autoselect Manufacturer ID (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA/ X00H	DA/ X00H				
	Data		AAH		55H		90H		ECH					
Autoselect Device Code (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA/ X01H	DA/ X02H				
	Data		AAH		55H		90H		(See Table 6)					
Autoselect Block Group Protect Verify (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	BA / X02H	BA/ X04H				
	Data		AAH		55H		90H		(See Table 6)					
Auto Select Secode Block Factory Protect Verify (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA / X03H	DA/ X06H				
	Data		AAH		55H		90H		(See Table 6)					
Enter Secode Block Region	Addr	3	555H	AAAH	2AAH	555H	555H	AAAH						
	Data		AAH		55H		88H							
Exit Secode Block Region	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	XXXH					
	Data		AAH		55H		90H		00H					
Program	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	PA					
	Data		AAH		55H		A0H		PD					
Unlock Bypass	Addr	3	555H	AAAH	2AAH	555H	555H	AAAH						
	Data		AAH		55H		20H							
Unlock Bypass Program	Addr	2	XXXH		PA									
	Data		A0H		PD									
Unlock Bypass Reset	Addr	2	XXXH		XXXH									
	Data		90H		00H									
Chip Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	555H	AAAH
	Data		AAH		55H		80H		AAH		55H		10H	
Block Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	BA	
	Data		AAH		55H		80H		AAH		55H		30H	
Block Erase Suspend (4, 5)	Addr	1	XXXH											
	Data		B0H											
Block Erase Resume	Addr	1	XXXH											
	Data		30H											
CFI Query (6)	Addr	1	55H	AAH										
	Data		98H											

Notes : 1. RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data
DA : Dual Bank Address (A19 - A20), BA : Block Address (A12 - A20), X = Don't care .
2. To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
3. The 4th cycle data of Autoselect mode is output data.
The 3rd and 4th cycle bank addresses of Autoselect mode must be same.
4. The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
5. The Erase Suspend command is applicable only to the Block Erase operation.
6. Command is valid when the device is in read mode or Autoselect mode.
7. DQ8 - DQ15 are don't care in command sequence, except for RD and PD.
8. A11 - A20 are also don't care, except for the case of special notice.

Table 6. Flash Memory Autoselect Codes

Description	DQ8 to DQ15		DQ7 to DQ0
	$\overline{BYTE}_F = V_{IH}$	$\overline{BYTE}_F = V_{IL}$	
Manufacturer ID	X	X	ECH
Device Code K5A3280YT (Top Boot Block)	22H	X	B8H
Device Code K5A3280YB (Bottom Boot Block)	22H	X	30H
Device Code K5A3380YT (Top Boot Block)	22H	X	BBH
Device Code K5A3380YB (Bottom Boot Block)	22H	X	3EH
Block Protection Verification	X	X	01H (Protected), 00H (Unprotected)
Secode Block Indicator Bit (DQ7)	X	X	80H (Factory locked), 00H (Not factory locked)

Table 7-1. Device Bus Operations - Flash Word Mode, $\overline{BYTE}_F$ = V_{IH}; SRAM Word Mode, $\overline{BYTE}_S$ = Vcc_S

Operation (Notes 1, 2)	$\overline{CE}_F$	$\overline{CS1}_S$	$CS2_S$	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	$\overline{RESET}$	$\overline{WP}$/ACC (Note 3)	DQ0-DQ7	DQ8-DQ15
Read from Flash	L	H	X	L	H	X	X	X	H	L/H	D_{OUT}	D_{OUT}
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	H	(Note 3)	D_{IN}	D_{IN}
		X	L									
Standby	Vcc_F ± 0.3V	H	X	X	X	X	X	X	Vcc_F ± 0.3V	H	High-Z	High-Z
		X	L									
Output Disable	H	L	H	H	H	X	L	X	H	L/H	High-Z	High-Z
				H	H	X	X	L				
	L	H	X	H	H	X	X	X				
		X	L									
Flash Hardware Reset	X	H	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L									
Block Protect (Note 4)	L	H	X	H	L	X	X	X	V_{ID}	L/H	D_{IN}	X
		X	L									
Block Unprotect (Note 4)	L	H	X	H	L	X	X	X	V_{ID}	(Note 5)	D_{IN}	X
		X	L									
Temporary Block Group Unprotect	X	H	X	X	X	X	X	X	V_{ID}	(Note 5)	X	X
		X	L									
Read from SRAM	H	L	H	L	H	X	L	L	H	X	D_{OUT}	D_{OUT}
							H	L			High-Z	D_{OUT}
							L	H			D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	X	L	L	H	X	D_{IN}	D_{IN}
							H	L			High-Z	D_{IN}
							L	H			D_{IN}	High-Z

Notes: L = Logic Low = V_{IL}, H = Logic High =V_{IH}, V_{ID} = 8.5V~12.5V, V_{HH} = 8.5V~12.5V, X = Don't Care, SA = LSB Address for SRAM in Byte Mode, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{CE}_F$ = V_{IL}, $\overline{CS1}_S$ = V_{IL} and $CS2_S$ =V_{IH} at the same time.
3. If $\overline{WP}$/ACC =V_{IL}, the boot blocks will be protected. If WP/ACC = V_{IH} the boot blocks protection will be removed.
4. The block protect and block unprotect functions may also be implemented via programming equipment. Refer to the "Block Group Protection and Unprotection".
5. If $\overline{WP}$/ACC=V_{IL}, the two outermost boot blocks remain protected. If $\overline{WP}$/ACC=V_{IH}, the two outermost boot block protection depends on whether they were last protected or unprotected using the method described in "Block GroupProtection and Unprotection". If $\overline{WP}$/ACC=V_{HH}, all blocks will be unprotected.

Table 7-2. Device Bus Operations - Flash Word Mode, $\overline{BYTE_F}$ = V_{IH}; SRAM Byte Mode, $\overline{BYTE_S}$ = V_{SS}

Operation (Notes 1, 2)	$\overline{CE_F}$	$\overline{CS1_S}$	$CS2_S$	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$ (Note 3)	$\overline{UB}$ (Note 3)	$\overline{RESET}$	$\overline{WP}$/ACC (Note 4)	DQ0-DQ7	DQ8-DQ15
Read from Flash	L	H	X	L	H	X	X	X	H	L/H	D_{OUT}	D_{OUT}
		X	L									
Write to Flash	L	H	X	H	L	L	X	X	H	(Note 3)	D_{IN}	D_{IN}
		X	L									
Standby	Vcc_F ± 0.3V	H	X	X	X	X	X	X	Vcc_F ± 0.3V	H	High-Z	High-Z
		X	L									
Output Disable	H	L	H	H	H	X	L	X	H	L/H	High-Z	High-Z
				H	H	X	X	L				
	L	H	X	H	H	X	X	X				
		X	L									
Flash Hardware Reset	X	H	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L									
Block Protect (Note 5)	L	H	X	H	L	X	X	X	V_{ID}	L/H	D_{IN}	X
		X	L									
Block Unprotect (Note 5)	L	H	X	H	L	X	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L									
Temporary Block Group Unprotect	X	H	X	X	X	X	X	X	V_{ID}	(Note 6)	X	X
		X	L									
Read from SRAM	H	L	H	L	H	SA	X	X	H	X	D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	SA	X	X	H	X	D_{IN}	High-Z

Notes: L = Logic Low = V_{IL}, H = Logic High =V_{IH}, V_{ID} = 8.5V~12.5V, V_{HH} = 8.5V~12.5V, X = Don't Care, SA = LSB Address for SRAM in Byte Mode, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{CE_F}$ = V_{IL}, $\overline{CS1_S}$ = V_{IL} and $CS2_S$ =V_{IH} at the same time.
3. Don't care or open $\overline{LB}$ or $\overline{UB}$.
4. If $\overline{WP}$/ACC =V_{IL}, the boot blocks will be protected. If $\overline{WP}$/ACC = V_{IH} the boot blocks protection will be removed.
5. The block protect and block unprotect functions may also be implemented via programming equipment. Refer to the "Block Group Protection and Unprotection".
6. If $\overline{WP}$/ACC=V_{IL}, the two outermost boot blocks remain protected. If $\overline{WP}$/ACC=V_{IH}, the two outermost boot block protection depends on whether they were last protected or unprotected using the method described in "Block Group Protection and Unprotection". If $\overline{WP}$/ACC=V_{HH}, all blocks will be unprotected.

Table 8. Device Bus Operations - Flash Byte Mode, $\overline{BYTE_F}$ = V_{IL}; SRAM Byte Mode, $\overline{BYTE_S}$ = V_{SS}

Operation (Notes 1, 2)	$\overline{CE_F}$	$\overline{CS1_S}$	$CS2_S$	DQ15/ A-1	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$ (Note 3)	$\overline{UB}$ (Note 3)	$\overline{RESET}$	$\overline{WP}$/ACC (Note 4)	DQ0-DQ7	DQ8-DQ15
Read from Flash	L	H	X	A-1	L	H	X	X	X	H	L/H	D_{OUT}	High-Z
		X	L										
Write to Flash	L	H	X	A-1	H	L	X	X	X	H	(Note 3)	D_{IN}	High-Z
		X	L										
Standby	$Vcc_F \pm 0.3V$	H	X	High-Z	X	X	X	X	X	$Vcc_F \pm 0.3V$	H	High-Z	High-Z
		X	L										
Output Disable	H	L	H	X	H	H	X	L	X	H	L/H	High-Z	High-Z
				H	H	X	X	X	L				
	L	H	X	A-1	H	H	X	X	X				
		X	L										
Flash Hardware Reset	X	H	X	High-Z	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Block Protect (Note 5)	L	H	X	X	H	L	X	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Block Unprotect (Note 5)	L	H	X	X	H	L	X	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Block Group Unprotect	X	H	X	X	X	X	X	X	X	V_{ID}	(Note 6)	X	X
		X	L										
Read from SRAM	H	L	H	X	L	H	SA	X	X	H	X	D_{OUT}	High-Z
Write to SRAM	H	L	H	X	X	L	SA	X	X	H	X	D_{IN}	High-Z

Notes: L = Logic Low = V_{IL}, H = Logic High =V_{IH}, V_{ID} = 8.5V~12.5V, V_{HH} = 8.5V~12.5V, X = Don't Care, SA = LSB Address for SRAM in Byte Mode, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{CE_F}$ = V_{IL}, $\overline{CS1_S}$ = V_{IL} and $CS2_S$ =V_{IH} at the same time.
3. Don't care or open $\overline{LB}$ or $\overline{UB}$.
4. If $\overline{WP}$/ACC =V_{IL}, the boot blocks will be protected. If $\overline{WP}$/ACC = V_{IH} the boot blocks protection will be removed.
5. The block protect and block unprotect functions may also be implemented via programming equipment. Refer to the "Block GroupProtection and Unprotection".
6. If $\overline{WP}$/ACC=V_{IL}, the two outermost boot blocks remain protected. If $\overline{WP}$/ACC=V_{IH}, the two outermost boot block protection depends on whether they were last protected or unprotected using the method described in "Block Group Protection and Unprotection". If $\overline{WP}$/ACC=V_{HH}, all blocks will be unprotected.

Flash DEVICE OPERATION

Byte/Word Mode

If the $\overline{BYTE}_F$ ball is set at logical "1" , the device is in word mode, DQ0-DQ15 are active. Otherwise the $\overline{BYTE}_F$ ball is set at logical "0" , the device is in byte mode, DQ0-DQ7 are active. DQ8-DQ14 are in the High-Z state and DQ15 ball is used as an input for the LSB (A-1) address ball.

Read Mode

Flash memory is controlled by Chip Enable ($\overline{CE}_F$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$). When $\overline{CE}_F$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE}_F$ or $\overline{OE}$ is high.

Standby Mode

Flash memory features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is either unselected or deselected by making $\overline{CE}_F$ high ($\overline{CE}_F = V_{IH}$). Refer to the DC characteristics for more details on stand-by modes.

Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE} = V_{IH}$). The output balls are in high impedance state.

Automatic Sleep Mode

Flash memory features Automatic Sleep Mode to minimize the device power consumption. Since the device typically draws 200nA of current in Automatic Sleep Mode, this feature plays an extremely important role in battery-powered applications. When addresses remain steady for t_{AA}+50ns, the device automatically activates the Automatic Sleep Mode. In the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

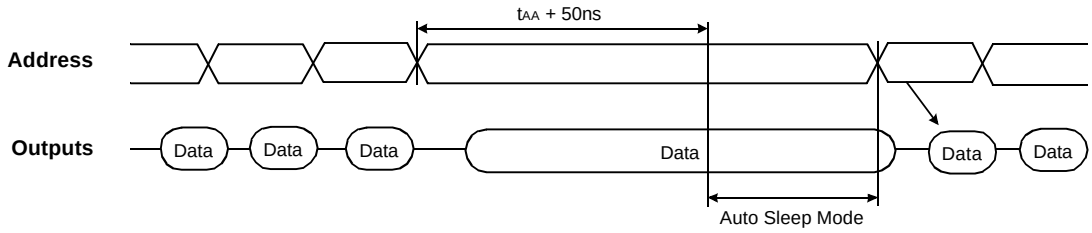
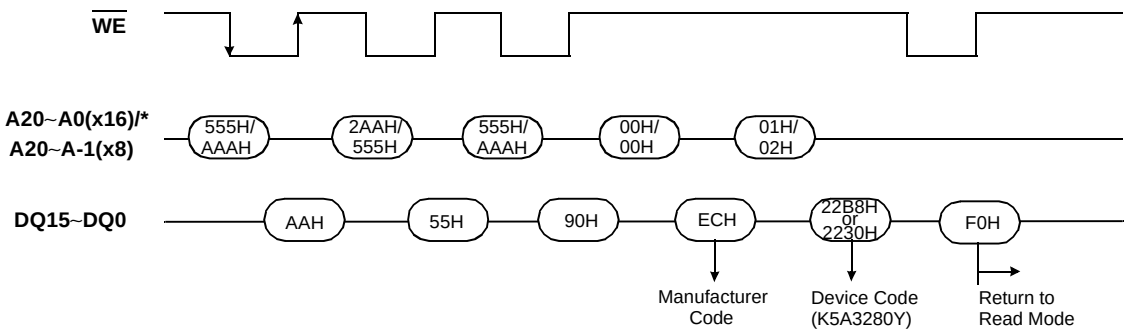


Figure 2. Auto Sleep Mode Operation

Autoselect Mode

Flash memory offers the Autoselect Mode to identify manufacturer and device type by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. In addition, this mode allows the verification of the status of write protected blocks. The manufacturer and device code can be read via the command register. The Command Sequence is shown in Table 5 and Figure 3. The autoselect operation of block protect verification is initiated by first writing two unlock cycle. The third cycle must contain the bank address and autoselect command (90H). If Block address while (A6, A1, A0) = (0,1,0) is finally asserted on the address ball, it will produce a logical "1" at the device output DQ0 to indicate a write protected block or a logical "0" at the device output DQ0 to indicate a write unprotected block. To terminate the autoselect operation, write Reset command (F0H) into the command register.



Note : The 3rd Cycle and 4th Cycle address must include the same bank address. Please refer to Table 6 for device code.

Figure 3. Autoselect Operation

Write (Program/Erase) Mode

Flash memory executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}_F$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses are latched on the falling edge of $\overline{CE}_F$ or $\overline{WE}$ (whichever occurs last) and the data are latched on the rising edge of $\overline{CE}_F$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

Program

Flash memory can be programmed in units of a word or a byte. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

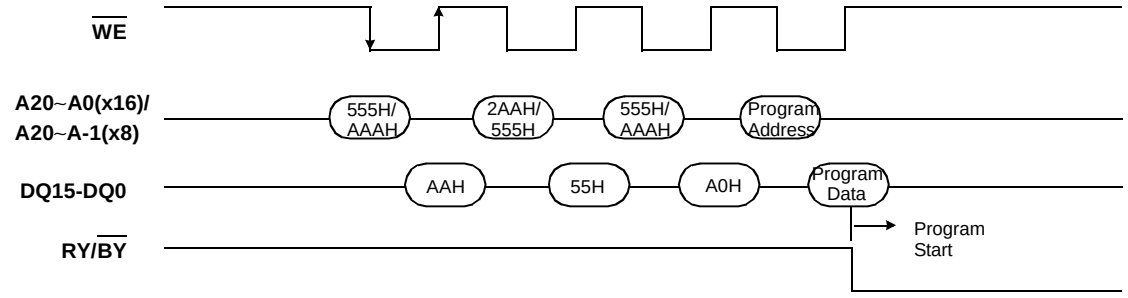


Figure 4. Program Command Sequence

Unlock Bypass

Flash memory provides the unlock bypass mode to save its program time. The mode is invoked by the unlock bypass command sequence. Unlike the standard program command sequence that contains four bus cycles, the unlock bypass program command sequence comprises only two bus cycles.
The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program command sequence is necessary to program in this mode. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode.
The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode

Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}_F$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

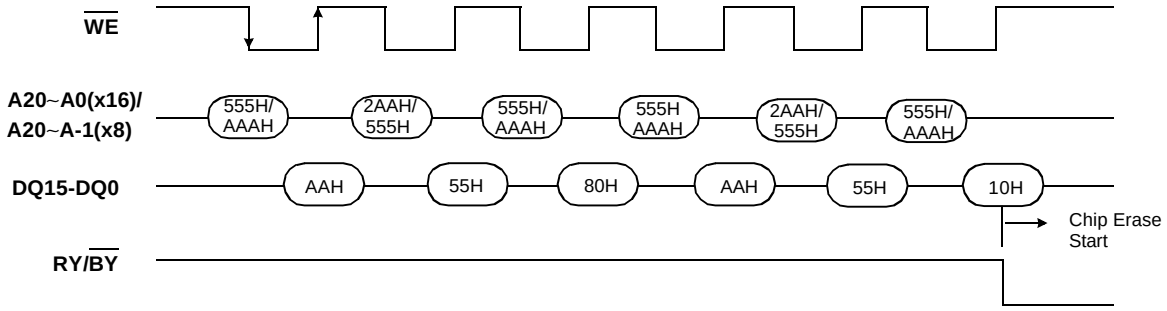


Figure 5. Chip Erase Command Sequence

Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 5. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}_F$, while the Block Erase command is latched on the rising edge of $\overline{WE}$ or $\overline{CE}_F$.
Multiple blocks can be erased sequentially by writing the six bus-cycle operation in Fig 6. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command.

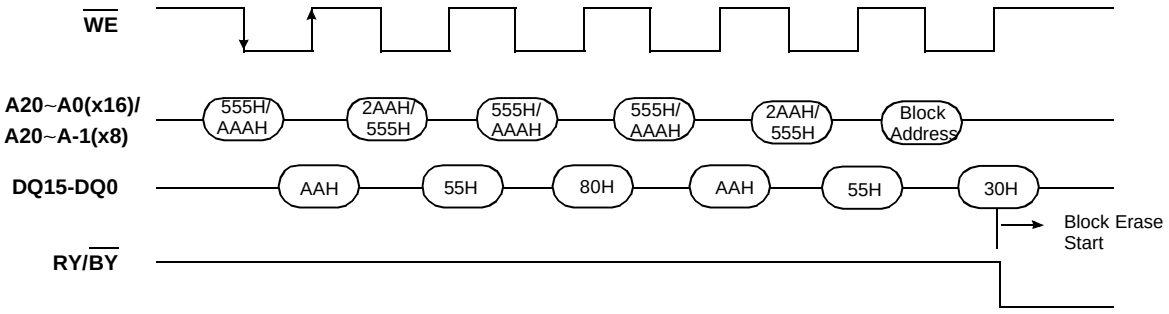


Figure 6. Block Erase Command Sequence

Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50 us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running.
When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20 us to suspend the erase operation. But, when the Erase Suspend command is written during the block erase time window (50 us) , the device immediately terminates the block erase time window and suspends the erase operation.
After the erase operation has been suspended, the device is availble for reading or programming data in a block that is not being erased. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode.
When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in Don't Care state.

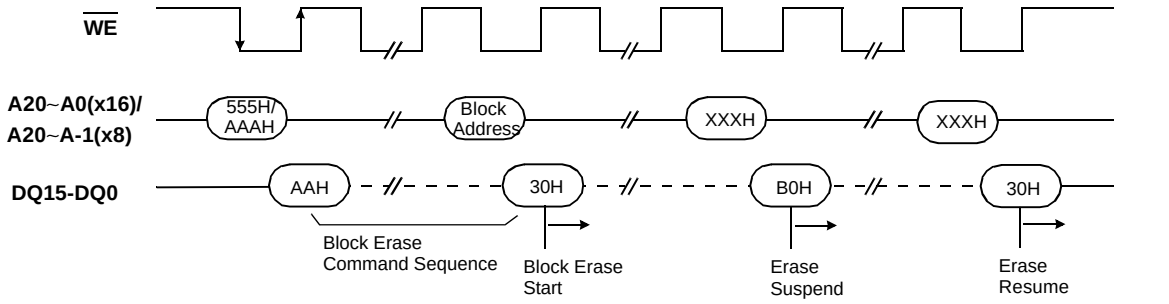


Figure 7. Erase Suspend/Resume Command Sequence

Read While Write

Flash memory provides dual bank memory architecture that divides the memory array into two banks. The device is capable of reading data from one bank and writing data to the other bank simultaneously. This is so called the Read While Write operation with dual bank architecture; this feature provides the capability of executing the read operation during Program/Erase or Erase-Suspend-Program operation.
The Read While Write operation is prohibited during the chip erase operation. It is also allowed during erase operation when either single block or multiple blocks from same bank are loaded to be erased. It means that the Read While Write operation is prohibited when blocks from Bank1 and another blocks from Bank2 are loaded all together for the multi-block erase operation.

Block Group Protection & Unprotection

Flash memory feature hardware block group protection. This feature will disable both program and erase operations in any combination of twenty five block groups of memory. Please refer to Tables 10 and 11. The block group protection feature is enabled using programming equipment at the user's site. The device is shipped with all block groups unprotected.
This feature can be hardware protected or unprotected. If a block is protected, program or erase command in the protected block will be ignored by the device. The protected block can only be read. This is useful method to preserve an important program data. The block group unprotection allows the protected blocks to be erased or programed. All blocks must be protected before unprotect operation is executing. The block protection and unprotection can be implemented by the following method.

Table 9. Block Group Protection & Unprotection

Operation	$\overline{CE}_F$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}_F$	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{RESET}$
Block Group Protect	L	H	L	X	X	L	H	L	X	X	D_{IN}	V_{ID}
Block Group Unprotect	L	H	L	X	X	H	H	L	X	X	D_{IN}	V_{ID}

Address must be inputted to the block group address (A12~A20) during block group protection operation. Please refer to Figure 9 (Algorithm) and Switching Waveforms of Block Group Protect & Unprotect Operations.

Temporary Block Group Unprotect

The protected blocks of the Flash memory can be temporarily unprotected by applying high voltage (V_{ID} = 8.5V~12.5V) to the $\overline{RESET}$ ball. In this mode, previously protected blocks can be programmed or erased with the program or erase command routines. When the $\overline{RESET}$ ball goes high ($\overline{RESET}$ = V_{IH}), all the previously protected blocks will be protected again. If the $\overline{WP}$/ACC ball is asserted at V_{IL}, the two outermost boot blocks remain protected.

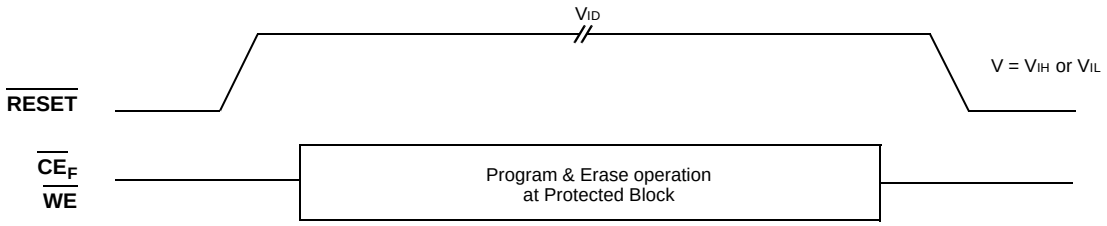
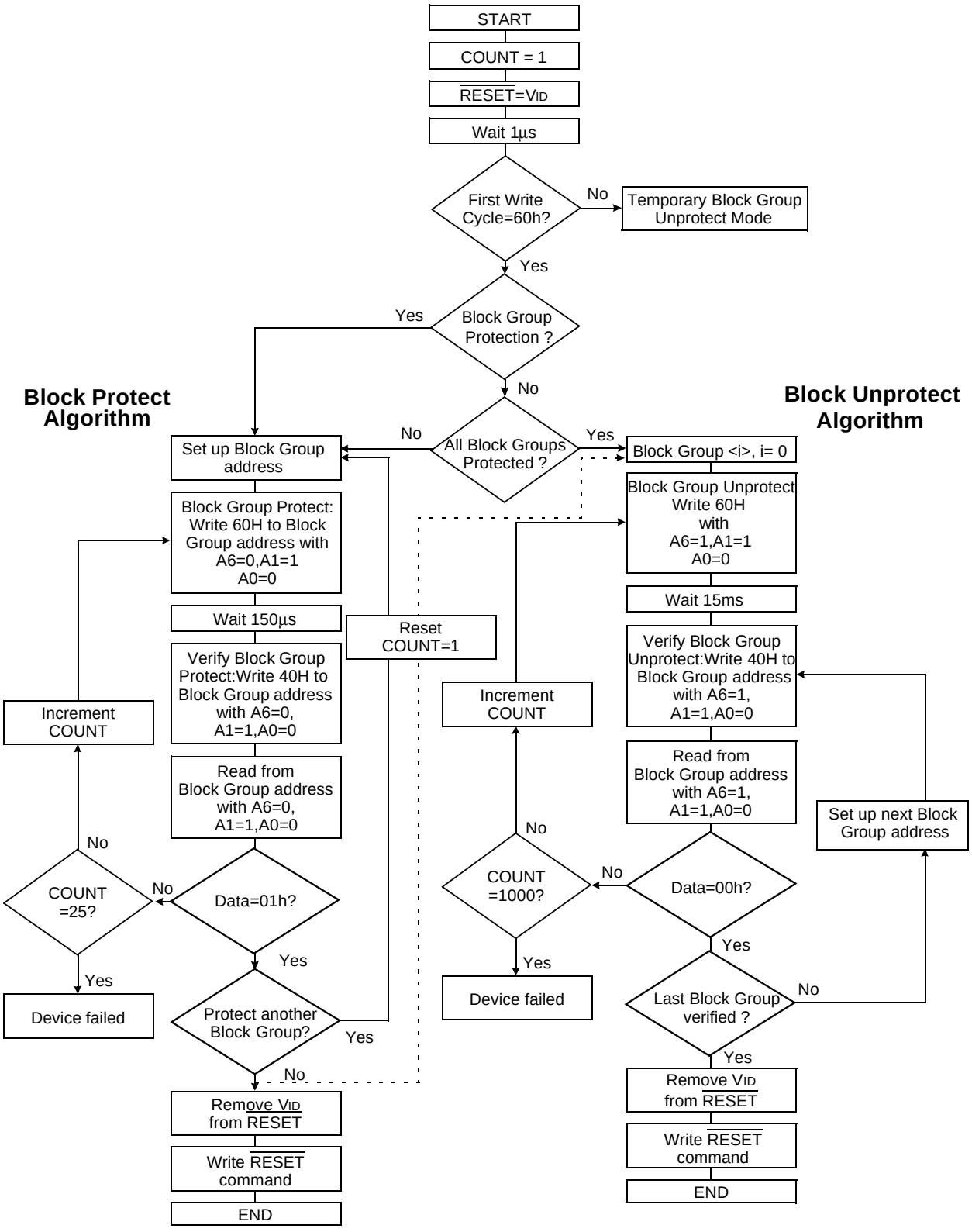


Figure 8. Temporary Block Group Unprotect Sequence



Note : All blocks must be protected before unprotect operation is executing.

Figure 9. Block Group Protection & Unprotection Algorithms

Table 10. Flash Memory Block Group Address (Top Boot Block)

Block Group	Block Address									Block
	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BGA0	0	0	0	0	0	0	X	X	X	BA0
BGA1	0	0	0	0	0	1	X	X	X	BA1 to BA3
					1	0				
					1	1				
BGA2	0	0	0	1	X	X	X	X	X	BA4 to BA7
BGA3	0	0	1	0	X	X	X	X	X	BA8 to BA11
BGA4	0	0	1	1	X	X	X	X	X	BA12 to BA15
BGA5	0	1	0	0	X	X	X	X	X	BA16 to BA19
BGA6	0	1	0	1	X	X	X	X	X	BA20 to BA23
BGA7	0	1	1	0	X	X	X	X	X	BA24 to BA27
BGA8	0	1	1	1	X	X	X	X	X	BA28 to BA31
BGA9	1	0	0	0	X	X	X	X	X	BA32 to BA35
BGA10	1	0	0	1	X	X	X	X	X	BA36 to BA39
BGA11	1	0	1	0	X	X	X	X	X	BA40 to BA43
BGA12	1	0	1	1	X	X	X	X	X	BA44 to BA47
BGA13	1	1	0	0	X	X	X	X	X	BA48 to BA51
BGA14	1	1	0	1	X	X	X	X	X	BA52 to BA55
BGA15	1	1	1	0	X	X	X	X	X	BA56 to BA59
BGA16	1	1	1	1	0	0	X	X	X	BA60 to BA62
					0	1				
					1	0				
BGA17	1	1	1	1	1	1	0	0	0	BA63
BGA18	1	1	1	1	1	1	0	0	1	BA64
BGA19	1	1	1	1	1	1	0	1	0	BA65
BGA20	1	1	1	1	1	1	0	1	1	BA66
BGA21	1	1	1	1	1	1	1	0	0	BA67
BGA22	1	1	1	1	1	1	1	0	1	BA68
BGA23	1	1	1	1	1	1	1	1	0	BA69
BGA24	1	1	1	1	1	1	1	1	1	BA70

Table 11. Flash Memory Block Group Address (Bottom Boot Block)

Block Group	Block Address									Block
	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BGA0	0	0	0	0	0	0	0	0	0	BA0
BGA1	0	0	0	0	0	0	0	0	1	BA1
BGA2	0	0	0	0	0	0	0	1	0	BA2
BGA3	0	0	0	0	0	0	0	1	1	BA3
BGA4	0	0	0	0	0	0	1	0	0	BA4
BGA5	0	0	0	0	0	0	1	0	1	BA5
BGA6	0	0	0	0	0	0	1	1	0	BA6
BGA7	0	0	0	0	0	0	1	1	1	BA7
BGA8	0	0	0	0	0	1	X	X	X	BA8 to BA10
					1	0				
					1	1				
BGA9	0	0	0	1	X	X	X	X	X	BA11 to BA14
BGA10	0	0	1	0	X	X	X	X	X	BA15 to BA18
BGA11	0	0	1	1	X	X	X	X	X	BA19 to BA22
BGA12	0	1	0	0	X	X	X	X	X	BA23 to BA26
BGA13	0	1	0	1	X	X	X	X	X	BA27 to BA30
BGA14	0	1	1	0	X	X	X	X	X	BA31 to BA34
BGA15	0	1	1	1	X	X	X	X	X	BA35 to BA38
BGA16	1	0	0	0	X	X	X	X	X	BA39 to BA42
BGA17	1	0	0	1	X	X	X	X	X	BA43 to BA46
BGA18	1	0	1	0	X	X	X	X	X	BA47 to BA50
BGA19	1	0	1	1	X	X	X	X	X	BA51 to BA54
BGA20	1	1	0	0	X	X	X	X	X	BA55 to BA58
BGA21	1	1	0	1	X	X	X	X	X	BA59 to BA62
BGA22	1	1	1	0	X	X	X	X	X	BA63 to BA66
BGA23	1	1	1	1	0	0	X	X	X	BA67 to BA69
					0	1				
					1	0				
BGA24	1	1	1	1	1	1	X	X	X	BA70

Write Protect ($\overline{WP}$)

The $\overline{WP}$/ACC ball has two useful functions. The one is that certain boot block is protected by the hardware method not to use V_{ID}. The other is that program operation is accelerated to reduce the program time (Refer to Accelerated program Operation Paragraph).
When the $\overline{WP}$/ACC ball is asserted at V_{IL}, the device can not perform program and erase operation in the two "outermost" 8K byte boot blocks independently of whether those blocks were protected or unprotected using the method described in "Block Group protection/Unprotection".
The write protected blocks can only be read. This is useful method to preserve an important program data.
The two outermost 8K byte boot blocks are the two blocks containing the lowest addresses in a bottom-boot-configured device, or the two blocks containing the highest addresses in a top-boot-congfigured device.
(K5A3280YT/K5A3380YT : BA69 and BA70, K5A3280YB/K5A3380YB : BA0 and BA1)
When the $\overline{WP}$/ACC ball is asserted at V_{IH}, the device reverts to whether the two outermost 8K byte boot blocks were last set to be protected or unprotected. That is, block protection or unprotection for these two blocks depends on whether they were last protected or unprotected using the method described in "Block Group protection/unprotection".
Recommend that the $\overline{WP}$/ACC ball must not be in the state of floating or unconnected, or the device may be led to malfunction.

Secode(Security Code) Block Region

The Secode Block feature provides a Flash memory region to be stored unique and permanent identification code, that is, Electronic Serial Number (ESN), customer code and so on. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Secode Block region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.
The Secode Block is factory locked or customer lockable. Before the device is shipped, the factory locked Secode Block is written on the special code and it is protected. The Secode Indicator bit (DQ7) is permanently fixed at "1" and it is not changed. The customer lockable Secode Block is unprotected, therefore it is programmed and erased. The Secode Indicator bit (DQ7) of it is permanently fixed at "0" and it is not changed. But once it is protected, there is no procedure to unprotect and modify the Secode Block.
The Secode Block region is 64K bytes in length and is accessed through a new command sequence (see Table 5). After the system has written the Enter Secode Block command sequence, the system may read the Secode Block region by using the same addresses of the boot blocks (8KBx8). The K5A3280YT/K5A3380YT occupies the address of the byte mode 3F0000H to 3FFFFFH (word mode 1F8000H to 1FFFFFH) and the K5A3280YB/K5A3380YB type occupies the address of the byte mode 000000H to 00FFFFH (word mode 000000H to 007FFFH). This mode of operation continues until the system issues the Exit Secode Block command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to read mode.

Accelerated Program Operation

Accelerated program operation reduces the program time through the ACC function. This is one of two functions provided by the $\overline{WP}$/ACC ball. When the $\overline{WP}$/ACC ball is asserted as V_{HH}, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotecting any protected blocks, and reduces the program operation time. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the $\overline{WP}$/ACC ball returns the device to normal operation. **Recommend that the WP/ACC ball must not be asserted at V_{HH} except accelerated program operation, or the device may be damaged. In addition, the WP/ACC ball must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.**

Software Reset

The reset command provides that the device is reseted to read mode or erase-suspend-read mode. The addresses are in Don't Care state. The reset command is vaild between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. This resets the bank in which was operating to read mode. if the device is be erasing or programming, the reset command is invalid until the operation is completed. Also, the reset command is valid between the sequence cycles in an autoselect command sequence. In the autoselect mode, the reset command returns the bank to read mode. If a bank entered the autoselect mode in the Erase Suspend mode, the reset command returns the bank to erase-suspend-read mode. If DQ5 is high on erase or program operation, the reset command return the bank to read mode or erase-suspend-read mode if the bank was in the Erase Suspend state.

Hardware Reset

Flash memory offers a reset feature by driving the $\overline{RESET}$ ball to V_{IL}. The $\overline{RESET}$ ball must be kept low (V_{IL}) for at least 500ns. When the $\overline{RESET}$ ball is driven low, any operation in progress will be terminated and the internal state machine will be reset to the standby mode after 20us. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ ball is taken high, the device requires 50ns of wake-up time until outputs are valid for read access. Also, note that all the data output balls are tri-stated for the duration of the $\overline{RESET}$ pulse.
The $\overline{RESET}$ ball may be tied to the system reset ball. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

Power-up Protection

To avoid initiation of a write cycle during Vcc_F Power-up, $\overline{RESET}$ low must be asserted during power-up. After $\overline{RESET}$ goes high, the device is reset to the read mode.

Low Vcc_F Write Inhibit

To avoid initiation of a write cycle during Vcc_F power-up and power-down, a write cycle is locked out for Vcc_F less than 1.8V. If Vcc_F < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc_F level is greater than V_{LKO}. It is the user′s responsibility to ensure that the control balls are logically correct to prevent unintentional writes when Vcc_F is above 1.8V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{CE}_F$, $\overline{OE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{OE}$ = V_{IL}, $\overline{CE}_F$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write, $\overline{CE}_F$ and $\overline{WE}$ must be "0", while $\overline{OE}$ is "1".

Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size, byte/word configuration, and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H in word mode(or address AAH in byte mode), the device enters the CFI mode. And then if the system writes the address shown in Table 12, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

Table 12. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	20H 22H 24H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	26H 28H	0002H 0000H
Address for Primary Extended Table	15H 16H	2AH 2CH	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	2EH 30H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	32H 34H	0000H 0000H
Vcc_F Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	36H	0027H
Vcc_F Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	38H	0036H
Vpp Min. voltage(00H = no Vpp ball present)	1DH	3AH	0000H
Vpp Max. voltage(00H = no Vpp ball present)	1EH	3CH	0000H
Typical timeout per single byte/word write 2^N us	1FH	3EH	0004H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	40H	0000H
Typical timeout per individual block erase 2^N ms	21H	42H	000AH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	44H	0000H
Max. timeout for byte/word write 2^N times typical	23H	46H	0005H
Max. timeout for buffer write 2^N times typical	24H	48H	0000H
Max. timeout per individual block erase 2^N times typical	25H	4AH	0004H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	4CH	0000H
Device Size = 2^N byte	27H	4EH	0016H
Flash Device Interface description	28H 29H	50H 52H	0002H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	54H 56H	0000H 0000H
Number of Erase Block Regions within device	2CH	58H	0002H
Erase Block Region 1 Information	2DH 2EH 2FH 30H	5AH 5CH 5EH 60H	0007H 0000H 0020H 0000H
Erase Block Region 2 Information	31H 32H 33H 34H	62H 64H 66H 68H	003EH 0000H 0000H 0001H
Erase Block Region 3 Information	35H 36H 37H 38H	6AH 6CH 6EH 70H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	72H 74H 76H 78H	0000H 0000H 0000H 0000H

Table 12. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query-unique ASCII string "PRI"	40H 41H 42H	80H 82H 84H	0050H 0052H 0049H
Major version number, ASCII	43H	86H	0031H
Minor version number, ASCII	44H	88H	0031H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	8AH	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	8CH	0002H
Block Protect 0 = Not Supported, 1 = Number of blocks in per group	47H	8EH	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	90H	0001H
Block Protect/Unprotect scheme 04 = K8D1x16U Mode	49H	92H	0004H
Simultaneous Operation (1) 00 = Not Supported, XX = Number of Blocks in Bank2	4AH	94H	00XXH
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	96H	0000H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page 02 = 8 Word Page	4CH	98H	0000H
ACC(Acceleration) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4DH	9AH	0085H
ACC(Acceleration) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4EH	9CH	00C5H
Top/Bottom Boot Block Flag 02H = Bottom Boot Device, 03H = Top Boot Device	4FH	9EH	000XH

Note :
1. The number of blocks in Bank2 is device dependent.
   K5A3280Y(8Mb/24Mb) = 30h (48blocks)
   K5A3380Y(16Mb/16Mb) = 20h (32blocks)

DEVICE STATUS FLAGS

Flash memory has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being excuted internal routine operation. The status is indicated by raising the device status flag via corresponding DQ balls or the RY/ $\overline{BY}$ ball. The corresponding DQ balls are DQ7, DQ6, DQ5, DQ3 and DQ2. The status is as follows :

Table 13. Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle (Note 1)	1
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0

Notes :
1. DQ2 will toggle when the device performs successive read operations from the erase suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the device during the Erase operation, DQ7 will be low. If the device is placed in the Erase Suspend Mode, the status can be detected via the DQ7 ball. If the system tries to read an address which belongs to a block that is being erased, DQ7 will be high. If a non-erased block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase Suspend Mode, an attempt to read an address that belongs to a block that is being erased will produce a high output of DQ6. If an address belongs to a block that is not being erased, toggling is halted and valid data is produced at DQ6.
If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

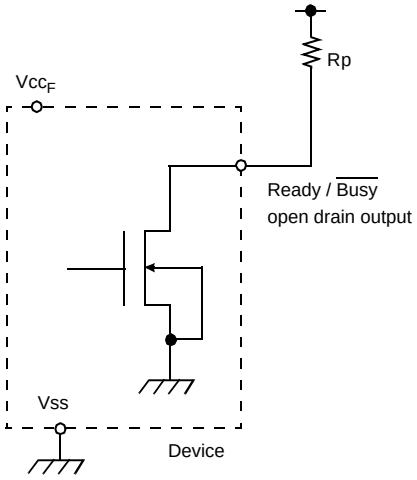
The status of the multi-block erase operation can be detected via the DQ3 ball. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase Suspend mode, DQ2 toggles only if an address in the erasing block is read. If a non-erasing block address is read during the Erase Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode. Combination of the status in DQ6 and DQ2 can be used to distinguish the erase operation from the program operation.

RY/$\overline{BY}$: Ready/$\overline{Busy}$

Flash memory has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ ball is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If Flash memory is placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be High. For programming, the RY/ $\overline{BY}$ is valid (RY/ $\overline{BY}$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, RY/ $\overline{BY}$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, RY/ $\overline{BY}$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.
The ball is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor is required for proper operation.



$$Rp = \frac{Vcc_F\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{2.9\ V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ ball.

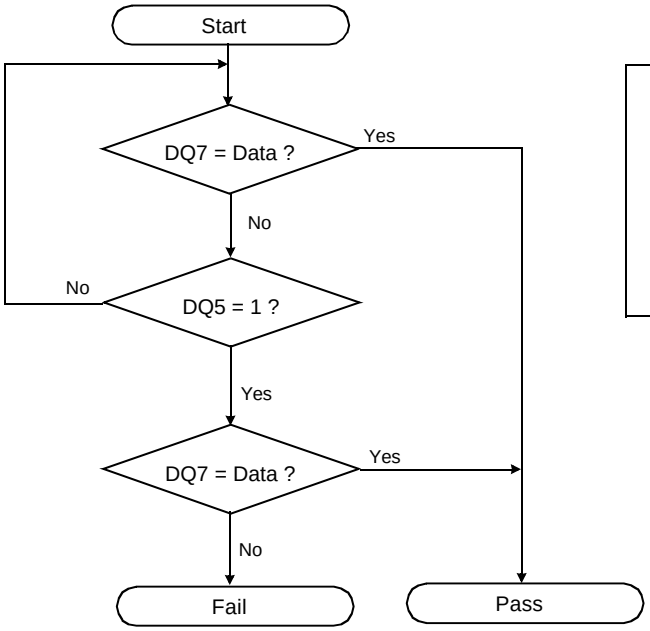


Figure 10. Data Polling Algorithms

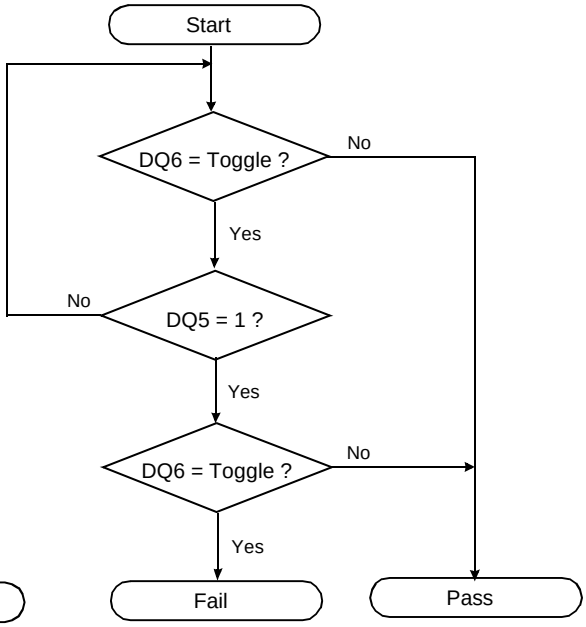
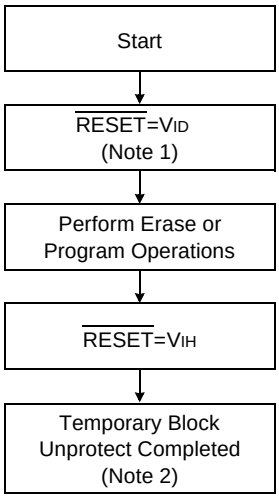


Figure 11. Toggle Bit Algorithms



Notes :
1. All protected block groups are unprotected.
   (If $\overline{WP}$/ACC = V_{IL}, the two outermost boot blocks remain protected)
2. All previously protected block groups are protected once again.

Figure 12. Temporary Block Group Unprotect Routine

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any ball relative to Vss	Vcc	Vcc_F , Vcc_S	-0.3 to +3.6	V
	$\overline{RESET}$	V_{IN}	-0.3 to +12.5	
	$\overline{WP}$/ACC		-0.3 to +12.5	
	All Other Balls		-0.3 to Vcc+0.3V(Max.3.6V)	
Temperature Under Bias		T_{bias}	-40 to +125	°C
Storage Temperature		T_{stg}	-65 to +150	°C
Operating Temperature		T_A	-40 to +85	°C

Notes :

1. Minimum DC voltage is -0.3V on Input/ Output balls. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output balls is Vcc+0.3V(Max. 3.6V) which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Minimum DC voltage is -0.3V on RESET and WP/ACC balls. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on RESET and WP/ACC balls are 12.5V which, during transitions, may overshoot to 14.0V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc_F , Vcc_S	2.7	3.0	3.3	V
Supply Voltage	Vss	0	0	0	V

DC CHARACTERISTICS

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Com-mon	Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc, Vcc=Vcc_{max}		-1.0	-	1.0	µA
	Output Leakage Current	I_{LO}	V_{OUT}=Vss to Vcc, Vcc=Vcc_{max}, $\overline{OE}$=V_{IH}		-1.0	-	1.0	µA
	Input Low Level	V_{IL}			-0.3	-	0.6	V
	Input High Level	V_{IH}			2.2	-	Vcc +0.3	V
	Output Low Level	V_{OL}	I_{OL}= 2.1mA, Vcc = Vcc_{min}		-	-	0.4	V
	Output High Level	V_{OH}	I_{OH}= -1.0mA, Vcc = Vcc_{min}		2.4	-	-	V
Flash	$\overline{RESET}$ Input Leakage Current	I_{LIT}	Vcc_F=Vcc_{max}, $\overline{RESET}$=12.5V		-	-	35	µA
	$\overline{WP}$/ACC Input Leakage Current	I_{LIW}	Vcc_F=Vcc_{max}, $\overline{WP}$/ACC=12.5V		-	-	35	µA
	Active Read Current (1)	I_{CC1}	$\overline{CE}_F$=V_{IL}, $\overline{OE}$=V_{IH}	5MHz	-	14	20	mA
				1MHz	-	3	6	
	Active Write Current (2)	I_{CC2}	$\overline{CE}_F$=V_{IL}, $\overline{OE}$=V_{IH}		-	15	30	mA
	Read While Program Current (3)	I_{CC3}	$\overline{CE}_F$=V_{IL}, $\overline{OE}$=V_{IH}		-	25	50	mA
	Read While Erase Current (3)	I_{CC4}	$\overline{CE}_F$=V_{IL}, $\overline{OE}$=V_{IH}		-	25	50	mA
	Program While Erase Suspend Current	I_{CC5}	$\overline{CE}_F$=V_{IL}, $\overline{OE}$=V_{IH}		-	15	35	mA
	ACC Accelerated Program Current	I_{ACC}	$\overline{CE}_F$=V_{IL}, $\overline{OE}$=V_{IH}	ACC Ball	-	5	10	mA
				Vcc_F Ball	-	15	30	
	Standby Current	I_{SB1}	Vcc_F=Vcc_Fmax, $\overline{CE}_F$=Vcc_F± 0.3V, $\overline{RESET}$=Vcc_F± 0.3V, $\overline{WP}$/ACC=Vcc_F± 0.3V or Vss± 0.3V		-	0.2	10	µA
	Standby Curren During Reset	I_{SB2}	Vcc_F=Vcc_{Fmax}, $\overline{RESET}$=Vss±0.3V, $\overline{WP}$/ACC=Vcc_F± 0.3V or Vss± 0.3V		-	0.2	10	µA

DC CHARACTERISTICS (Continued)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Flash	Automatic Sleep Mode	$I_{SB}3$	$V_{IH}=Vcc_F\pm0.3V$, $V_{IL}=V_{SS}\pm0.3V$, $\overline{OE}=V_{IL}$, $I_{OL}=I_{OH}=0$	-	0.2	10	µA
	Voltage for $\overline{WP}$/ACC Block Temporarily Unprotect and Program Acceleration (4)	V_{HH}	Vcc_F = 3.0V ± 0.3V	8.5	-	12.5	V
	Voltage for Autoselect and Block Protect (4)	V_{ID}	Vcc_F = 3.0V ± 0.3V	8.5	-	12.5	V
	Low Vcc_F Lock-out Voltage (5)	V_{LKO}		1.8	-	-	V
SRAM	Operating Current	$I_{CC}1$	Cycle time=1µs, 100% duty, $\overline{CS1}_S\leq0.2V$, $CS2_S\geq Vcc_S-0.2V$, $\overline{LB}\leq0.2V$ and/or $\overline{UB}\leq0.2V$ All outputs open, $V_{IN}\leq0.2V$ or $V_{IN}\geq Vcc_S-0.2V$, $\overline{BYTE}_S=Vcc_S\pm0.3V$ or Vss± 0.3V	-	-	3	mA
		$I_{CC}2$	Cycle time=Min, 100% duty, $\overline{CS1}_S=V_{IL}$, $CS2_S=V_{IH}$, $\overline{LB}=V_{IL}$ and/or $\overline{UB}=V_{IL}$, All outputs open, $V_{IN}=V_{IL}$ or V_{IH}, $\overline{BYTE}_S=Vcc_S\pm0.3V$ or Vss± 0.3V	-	22	28	mA
	Standby Current	I_{SB}	$\overline{CS1}_S\geq Vcc_S-0.2V$, $CS2_S\geq Vcc_S-0.2V$ ($\overline{CS1}_S$ controlled) or $CS2_S\leq0.2V$ ($CS2_S$ controlled), $\overline{BYTE}_S=Vcc_S\pm0.3V$ or Vss± 0.3V, Other input =0~Vcc_S	-	0.5	15	µA

Notes :
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component(at 5 MHz).
   The read current is typically 14 mA (@ Vcc_F=3.0V , $\overline{OE}$ at V_{IH}.)
2. I_{CC} active during Internal Routine(program or erase) is in progress.
3. I_{CC} active during Read while Write is in progress.
4. The high voltage (V_{HH} or V_{ID}) must be used in the range of Vcc_F = 3.0V ± 0.3V
5. Not 100% tested.
6. Typical values are measured at Vcc_F = Vcc_S = 3.0V, Ta=25°C , not 100% tested.

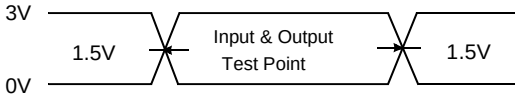
CAPACITANCE(T_A = 25 °C, Vcc_F = Vcc_S = 3.3V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	18	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	20	pF
Control Ball Capacitance	C_{IN2}	V_{IN}=0V	-	18	pF

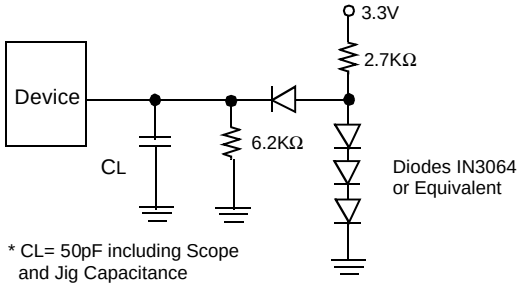
Note : Capacitance is periodically sampled and not 100% tested.

AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL and C_L = 50pF



Input Pulse and Test Point



Output Load

Flash AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{WE}$ Controlled Write

Parameter		Symbol	80ns		85ns		90ns		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	80	-	85	-	90	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
		t_{ASO}	55	-	55	-	55	-	ns
Address Hold Time		t_{AH}	45	-	45	-	45	-	ns
		t_{AHT}	0	-	0	-	0	-	ns
Data Setup Time		t_{DS}	35	-	45	-	45	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	t_{OEH1}	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	t_{OEH2}	10	-	10	-	10	-	ns
$\overline{CE}_F$ Setup Time		t_{CS}	0	-	0	-	0	-	ns
$\overline{CE}_F$ Hold Time		t_{CH}	0	-	0	-	0	-	ns
Write Pulse Width		t_{WP}	35	-	45	-	45	-	ns
Write Pulse Width High		t_{WPH}	25	-	30	-	30	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Accelerated Programming Operation	Word	t_{ACCPGM}	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		5(typ.)		5(typ.)		5(typ.)		µs
Block Erase Operation (2)		t_{BERS}	0.7(typ.)		0.7(typ.)		0.7(typ.)		sec
Vcc_F Set Up Time		t_{VCS}	50	-	50	-	50	-	µs
Write Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	0	-	0	-	ns
$\overline{RESET}$ High Time Before Read		t_{RH}	50	-	50	-	50	-	ns
$\overline{RESET}$ to Power Down Time		t_{RPD}	20	-	20	-	20	-	µs
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}	90	-	90	-	90	-	ns
V_{ID} Rising and Falling Time		t_{VID}	500	-	500	-	500	-	ns
$\overline{RESET}$ Pulse Width		t_{RP}	500	-	500	-	500	-	ns
$\overline{RESET}$ Low to RY/BY High		t_{RRB}	-	20	-	20	-	20	µs
$\overline{RESET}$ Setup Time for Temporary Unprotect		t_{RSP}	1	-	1	-	1	-	µs
$\overline{RESET}$ Low Setup Time		t_{RSTS}	500	-	500	-	500	-	ns
$\overline{RESET}$ High to Address Valid		t_{RSTW}	200	-	200	-	200	-	ns
Read Recovery Time Before Write		t_{GHWL}	0	-	0	-	0	-	ns
$\overline{CE}_F$ High during toggling bit polling		t_{CEPH}	20	-	20	-	20	-	ns
$\overline{OE}$ High during toggling bit polling		t_{OEPH}	20	-	20	-	20	-	ns

Notes : 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

Flash AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{CE}_F$ Controlled Writes

Parameter		Symbol	80ns		85ns		90ns		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	80	-	85	-	90	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
Address Hold Time		t_{AH}	45	-	45	-	45	-	ns
Data Setup Time		t_{DS}	35	-	45	-	45	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	t_{OEH1}	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	t_{OEH2}	10	-	10	-	10	-	ns
$\overline{WE}$ Setup Time		t_{WS}	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		t_{WH}	0	-	0	-	0	-	ns
$\overline{CE}_F$ Pulse Width		t_{CP}	35	-	45	-	45	-	ns
$\overline{CE}_F$ Pulse Width High		t_{CPH}	25	-	30	-	30	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Accelerated Program-ming Operation	Word	t_{ACCPGM}	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		5(typ.)		5(typ.)		5(typ.)		µs
Block Erase Operation (2)		t_{BERS}	0.7(typ.)		0.7(typ.)		0.7(typ.)		sec
$\overline{BYTE}_F$ Switching Low to Output HIGH-Z		t_{FLQZ}	25	-	30	-	30	-	ns

Notes : 1. Not 100% tested.
2.This does not include the preprogramming time.

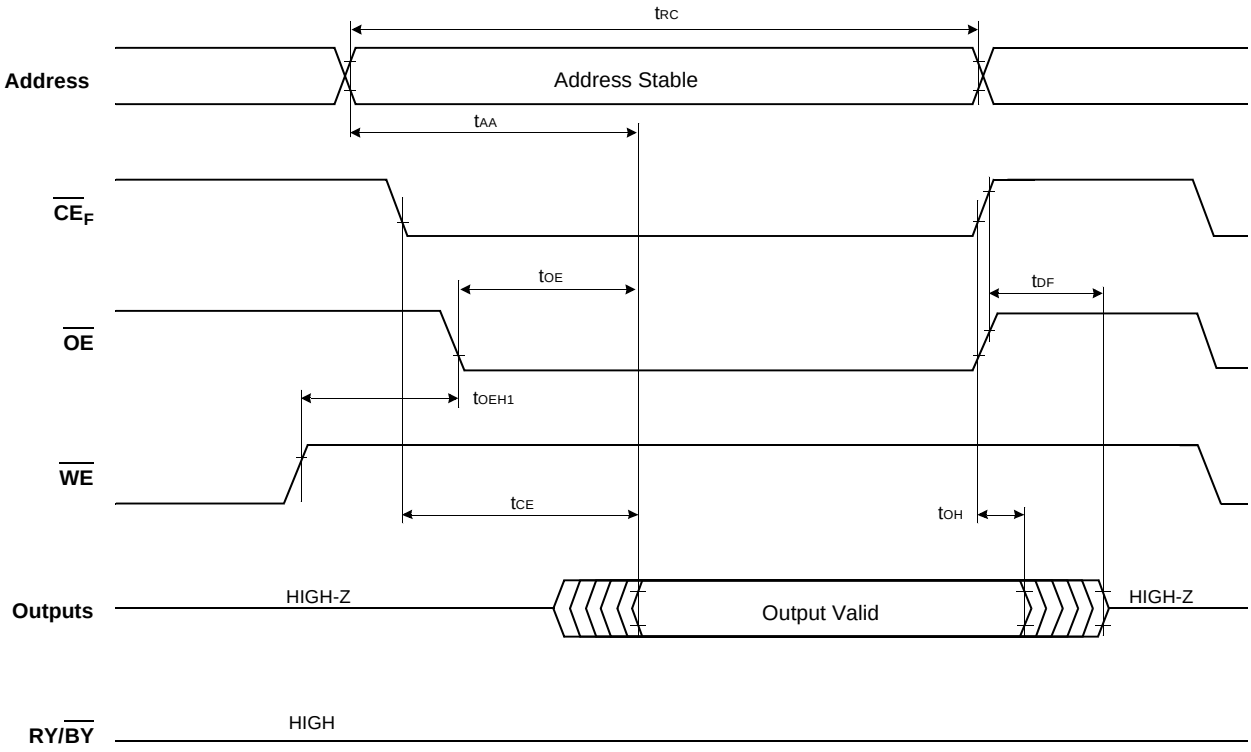
Flash ERASE AND PROGRAM PERFORMANCE

Parameter		Limits			Unit	Comments
		Min	Typ	Max		
Block Erase Time		-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		-	49	-	sec	
Word Programming Time		-	11	330	µs	Excludes system-level overhead
Byte Programming Time		-	7	210	µs	Excludes system-level overhead
Accelerated Byte/Word Program Time	Word Mode	-	9	210	µs	Excludes system-level overhead
	Byte Mode	-	5	150	µs	Excludes system-level overhead
Chip Programming Time	Word Mode	-	22	66	sec	Excludes system-level overhead
	Byte Mode	-	28	84	sec	
Erase/Program Endurance		100,000	-	-	cycles	Minimum 100,000 cycles guaran-teed

Notes : 1. 25 °C, Vcc_F = 3.0 V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Internal Erase Routine, all bytes are programmed to 00H before erasure.

Flash SWITCHING WAVEFORMS

Read Operations

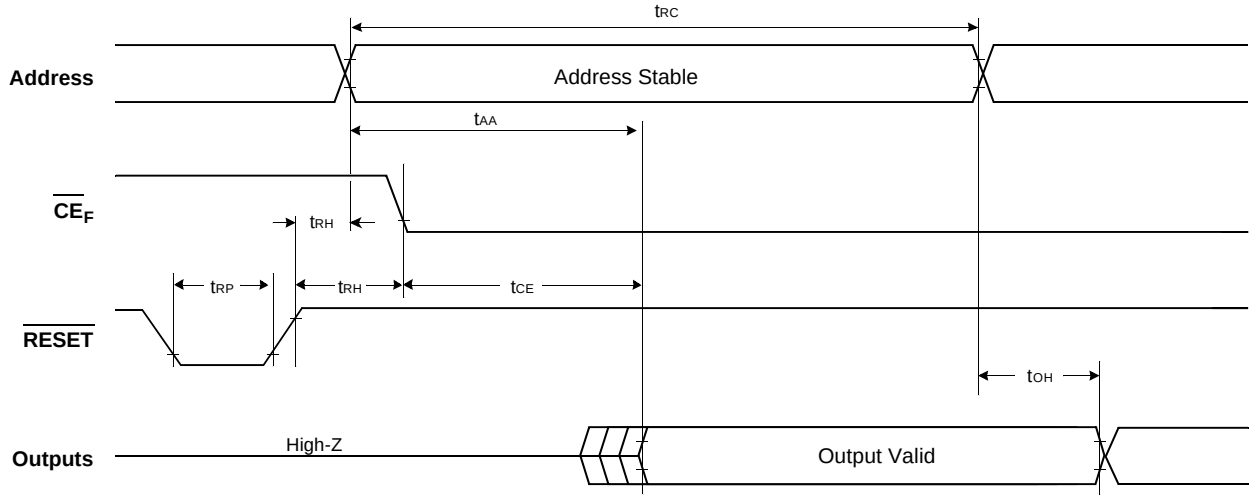


Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80	-	85	-	90	-	ns
Address Access Time	t_{AA}	-	80	-	85	-	90	ns
Chip Enable Access Time	t_{CE}	-	80	-	85	-	90	ns
Output Enable Time	t_{OE}	-	25	-	35	-	35	ns
$\overline{CE}_F$ & $\overline{OE}$ Disable Time (1)	t_{DF}	-	25	-	30	-	30	ns
Output Hold Time from Address, $\overline{CE}_F$ or $\overline{OE}$	t_{OH}	0	-	0	-	0	-	ns
$\overline{OE}$ Hold Time	t_{OEH1}	0	-	0	-	0	-	ns

Note : 1. Not 100% tested.

Flash SWITCHING WAVEFORMS

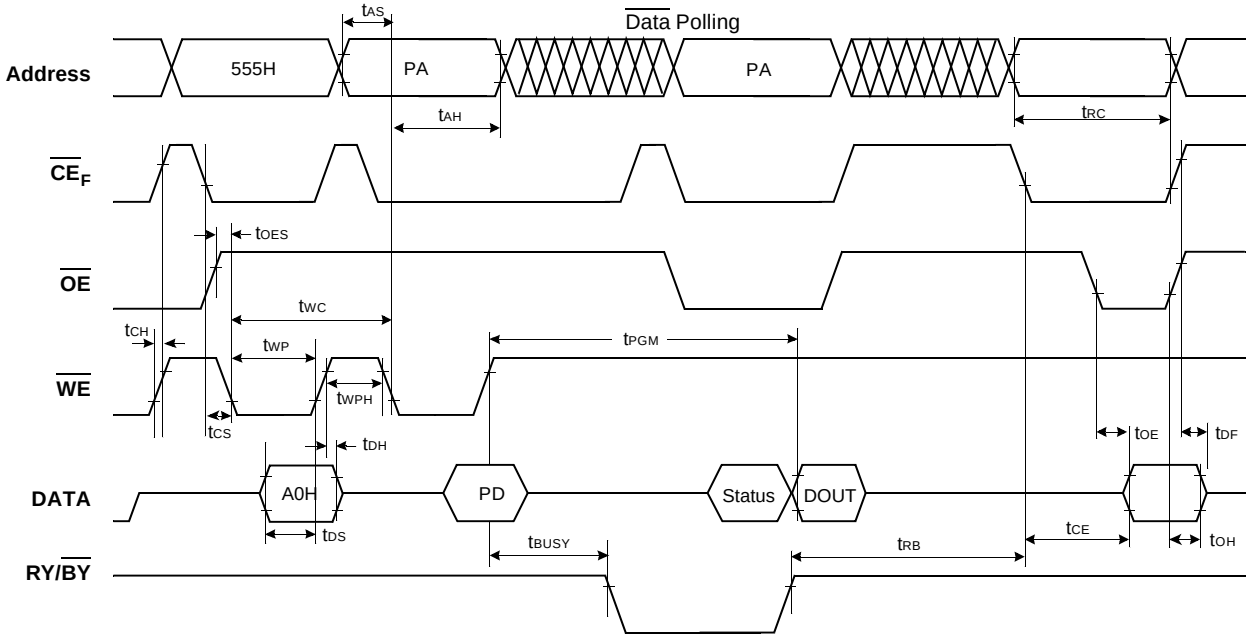
Hardware Reset/Read Operations



Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	80	-	85	-	90	-	ns
Address Access Time	t_{AA}	-	80	-	85	-	90	ns
Chip Enable Access Time	t_{CE}	-	80	-	85	-	90	ns
Output Hold Time from Address, $\overline{CE}_F$ or $\overline{OE}$	t_{OH}	0	-	0	-	0	-	ns
$\overline{RESET}$ Pulse Width	t_{RP}	500	-	500	-	500	-	ns
$\overline{RESET}$ High Time Before Read	t_{RH}	50	-	50	-	50	-	ns

Flash SWITCHING WAVEFORMS

Alternate $\overline{WE}$ Controlled Program Operations

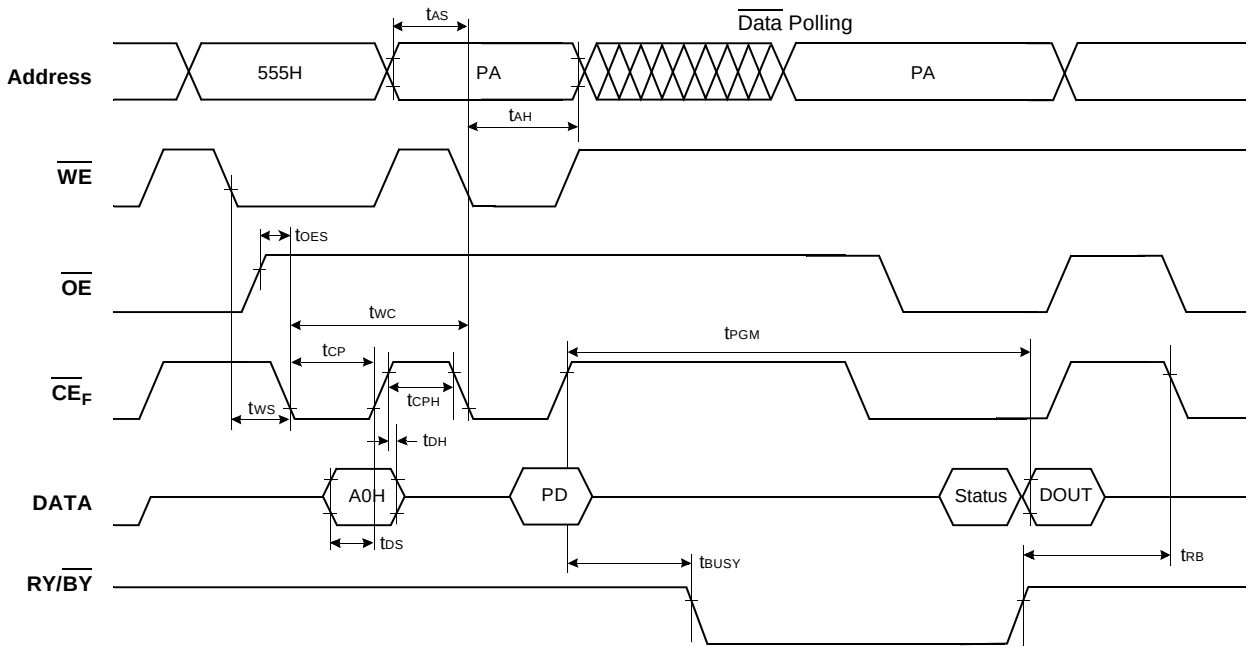


Notes : 1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Parameter		Symbol	80ns		85ns		90ns		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time		t_{WC}	80	-	85	-	90	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
Address Hold Time		t_{AH}	45	-	45	-	45	-	ns
Data Setup Time		t_{DS}	35	-	45	-	45	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
$\overline{CE}_F$ Setup Time		t_{CS}	0	-	0	-	0	-	ns
$\overline{CE}_F$ Hold Time		t_{CH}	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time		t_{OES}	0	-	0	-	0	-	ns
Write Pulse Width		t_{WP}	35	-	45	-	45	-	ns
Write Pulse Width High		t_{WPH}	25	-	30	-	30	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		us
	Byte		7(typ.)		7(typ.)		7(typ.)		us
Accelerated Programming Operation	Word	t_{ACCPGM}	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		5(typ.)		5(typ.)		5(typ.)		µs
Read Cycle Time		t_{RC}	80	-	85	-	90	-	ns
Chip Enable Access Time		t_{CE}	-	80	-	85	-	90	ns
Output Enable Time		t_{OE}	-	25	-	35	-	35	ns
$\overline{CE}_F$ & $\overline{OE}$ Disable Time		t_{DF}	-	25	-	30	-	30	ns
Output Hold Time from Address, $\overline{CE}_F$ or $\overline{OE}$		t_{OH}	0	-	0	-	0	-	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}	90	-	90	-	90	-	ns
Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	0	-	0	-	ns

Flash SWITCHING WAVEFORMS

Alternate $\overline{CE}_F$ Controlled Program Operations

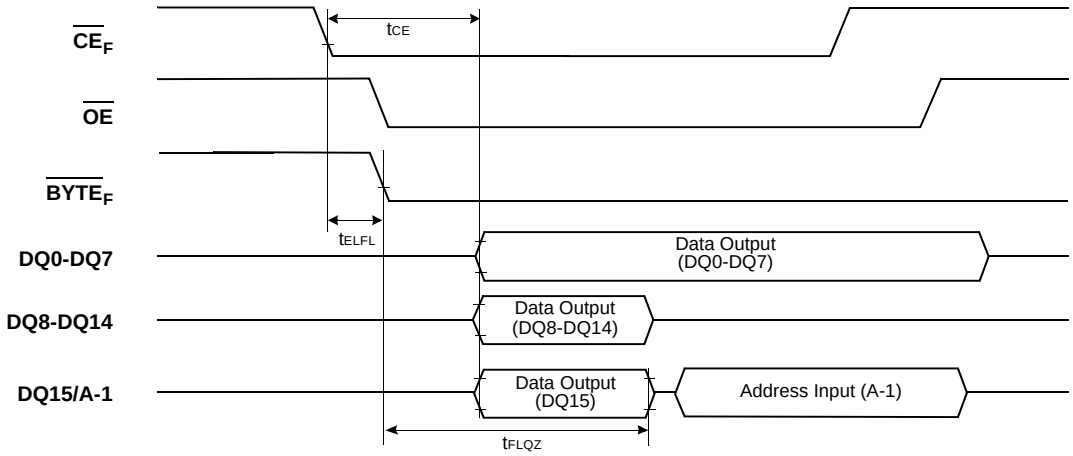


Notes :
1. DQ7 is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

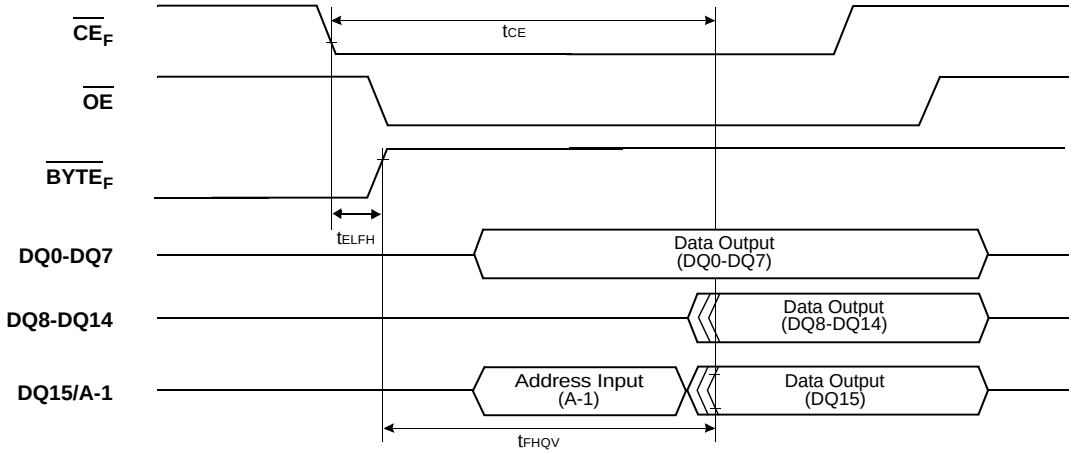
Parameter		Symbol	80ns		85ns		90ns		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time		t_{WC}	80	-	85	-	90	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
Address Hold Time		t_{AH}	45	-	45	-	45	-	ns
Data Setup Time		t_{DS}	35	-	45	-	45	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time		t_{OES}	0	-	0	-	0	-	ns
$\overline{WE}$ Setup Time		t_{WS}	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		t_{WH}	0	-	0	-	0	-	ns
$\overline{CE}_F$ Pulse Width		t_{CP}	35	-	45	-	45	-	ns
$\overline{CE}_F$ Pulse Width High		t_{CPH}	25	-	30	-	30	-	ns
Programming Operation	Word	t_{PGM}	11(typ.)		11(typ.)		11(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Accelerated Programming Operation	Word	t_{ACCPGM}	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		5(typ.)		5(typ.)		5(typ.)		µs
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}	90	-	90	-	90	-	ns
Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	0	-	0	-	ns

Flash SWITCHING WAVEFORMS

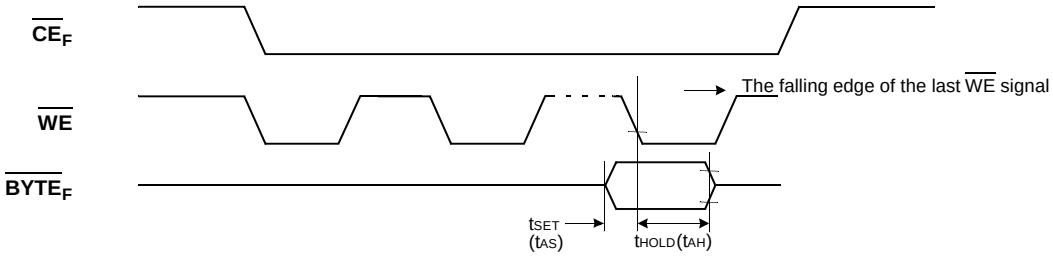
Word to Byte Timing Diagram for Read Operation



Byte to Word Timing Diagram for Read Operation

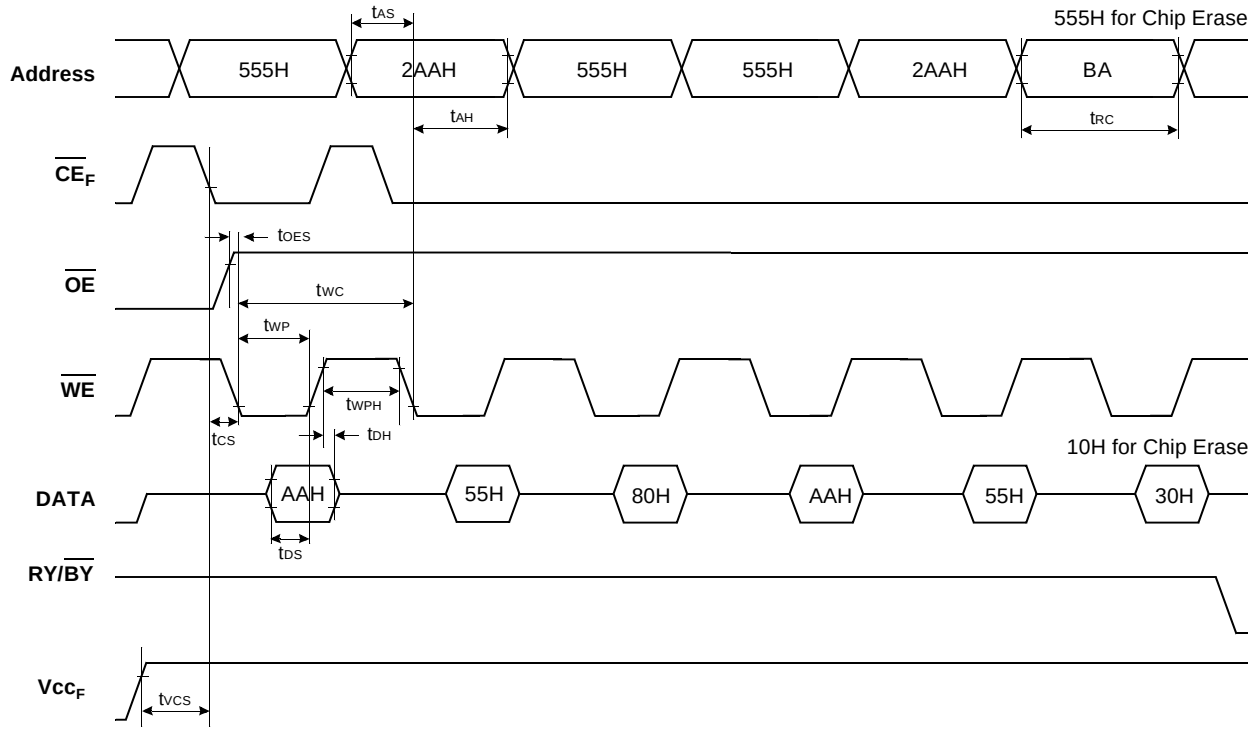


$\overline{BYTE}_F$ Timing Diagram for Write Operation



Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Chip Enable Access Time	tCE	-	80	-	85	-	90	ns
$\overline{CE}_F$ to $\overline{BYTE}_F$ Switching Low or High	tELFL/tELFH	-	5	-	5	-	5	ns
$\overline{BYTE}_F$ Switching Low to Output HIGH-Z	tFLQZ	-	25	-	30	-	30	ns
$\overline{BYTE}_F$ Switching High to Output Active	tFHQV	-	25	-	35	-	35	ns

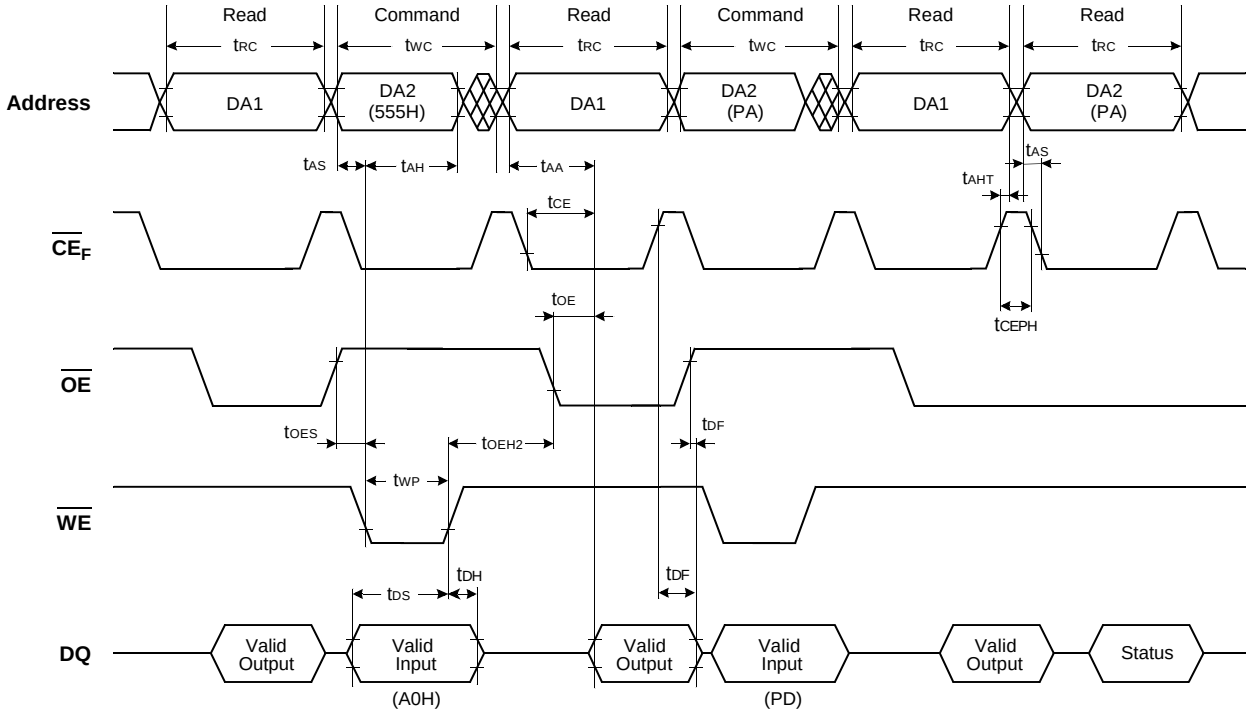
Flash SWITCHING WAVEFORMS
Chip/Block Erase Operations



Note : BA : Block Address

Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80	-	85	-	90	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	45	-	45	-	45	-	ns
Data Setup Time	t_{DS}	35	-	45	-	45	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time	t_{OES}	0	-	0	-	0	-	ns
$\overline{CE}_F$ Setup Time	t_{CS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	45	-	45	-	ns
Write Pulse Width High	t_{WPH}	25	-	30	-	30	-	ns
Read Cycle Time	t_{RC}	80	-	85	-	90	-	ns
Vcc_F Set Up Time	t_{VCS}	50	-	50	-	50	-	µs

Flash SWITCHING WAVEFORMS
Read While Write Operations

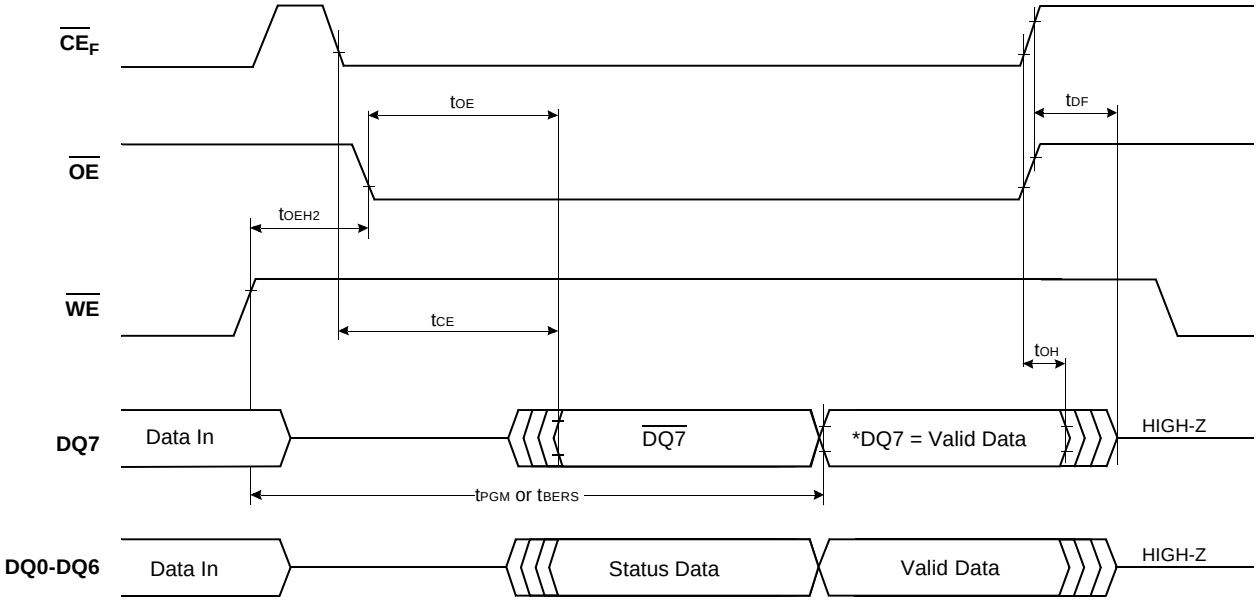


Note : This is an example in the program-case of the Read While Write function.
DA1 : Address of Bank1, DA2 : Address of Bank 2
PA = Program Address at one bank , RA = Read Address at the other bank, PD = Program Data In , RD = Read Data Out

Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	80	-	85	-	90	-	ns
Write Pulse Width	t_{WP}	35	-	45	-	45	-	ns
Write Pulse Width High	t_{WPH}	25	-	30	-	30	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	45	-	45	-	45	-	ns
Data Setup Time	t_{DS}	35	-	45	-	45	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	ns
Read Cycle Time	t_{RC}	80	-	85	-	90	-	ns
Chip Enable Access Time	t_{CE}	-	80	-	85	-	90	ns
Address Access Time	t_{AA}	-	80	-	85	-	90	ns
Output Enable Access Time	t_{OE}	-	25	-	35	-	35	ns
$\overline{OE}$ Setup Time	t_{OES}	0	-	0	-	0	-	ns
$\overline{OE}$ Hold Time	t_{OEH2}	10	-	10	-	10	-	ns
$\overline{CE}_F$ & $\overline{OE}$ Disable Time	t_{DF}	-	25	-	30	-	30	ns
Address Hold Time	t_{AHT}	0	-	0	-	0	-	ns
$\overline{CE}_F$ High during toggle bit polling	t_{CEPH}	20	-	20	-	20	-	ns

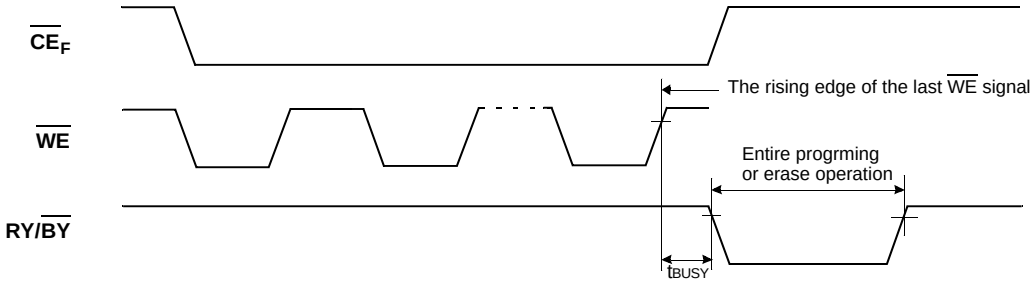
Flash SWITCHING WAVEFORMS

Data Polling During Internal Routine Operation



Note : *DQ7=Vaild Data (The device has completed the internal operation).

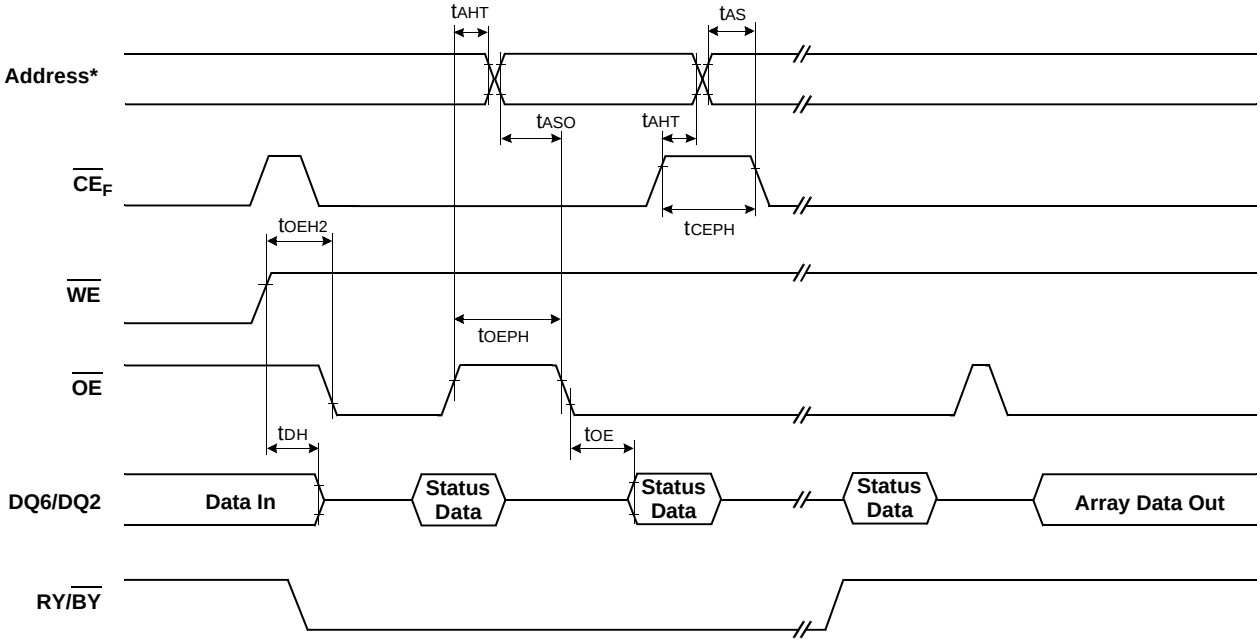
RY/BY Timing Diagram During Program/Erase Operation



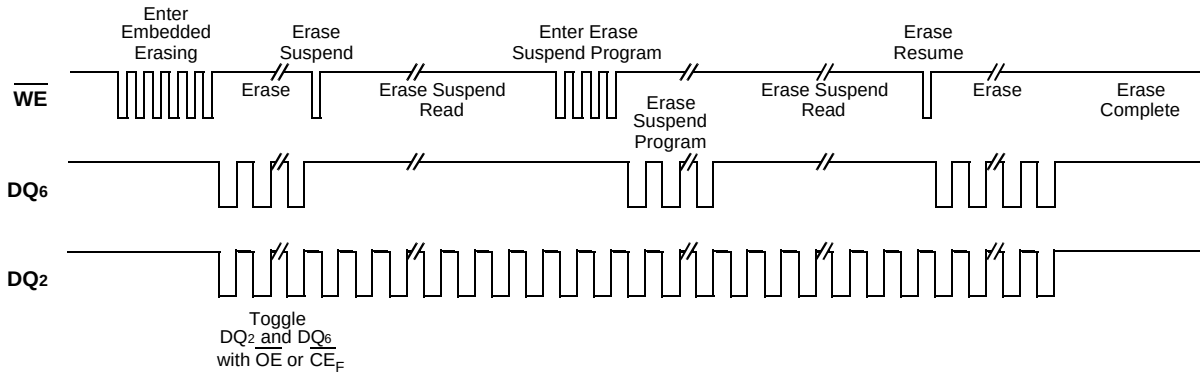
Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Program/Erase Valid to RY/BY Delay	tBUSY	90	-	90	-	90	-	ns
Chip Enable Access Time	tCE	-	80	-	85	-	90	ns
Output Enable Time	tOE	-	25	-	35	-	35	ns
CEF & OE Disable Time	tDF	-	25	-	30	-	30	ns
Output Hold Time from Address, CEF or OE	tOH	0	-	0	-	0	-	ns
OE Hold Time	tOEH2	10	-	10	-	10	-	ns

SWITCHING WAVEFORMS

Toggle Bit During an Internal Routine Operation



Note : Address for the write operation must include a bank address (A18~A20) where the data is written.

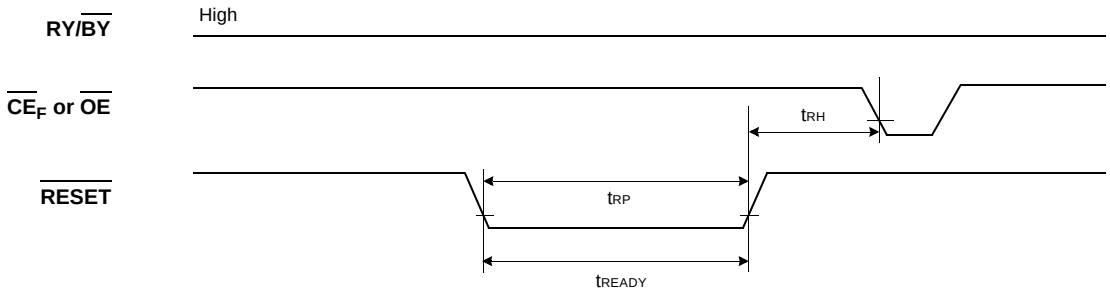


Note : DQ2 is read from the erase-suspended block.

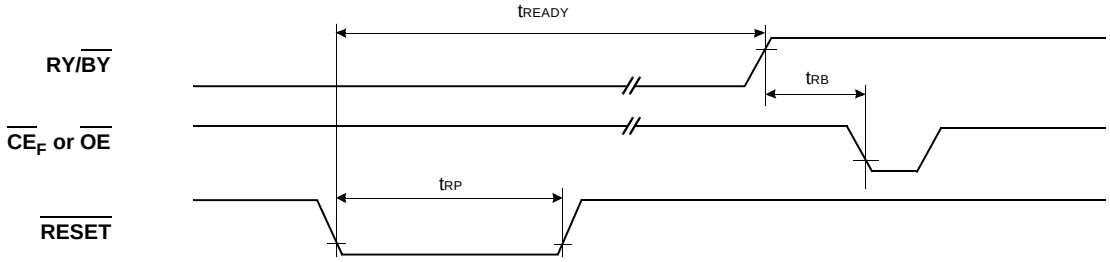
Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
Output Enable Access Time	tOE	-	25	-	35	-	35	ns
OE Hold Time	tOEH2	10	-	10	-	10	-	ns
Address Hold Time	tAHT	0	-	0	-	0	-	ns
Address Setup	tASO	55	-	55	-	55	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	ns
CEF High during toggle bit polling	tCEPH	20	-	20	-	20	-	ns
OE High during toggle bit polling	tOEPH	20	-	20	-	20	-	ns

Flash SWITCHING WAVEFORMS

$\overline{\text{RESET}}$ Timing Diagram

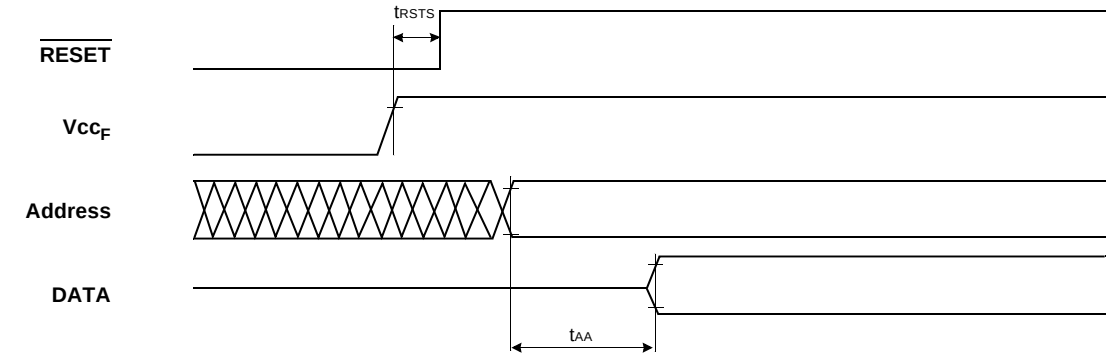


Reset Timings NOT during Internal Routine



Reset Timings during Internal Routine

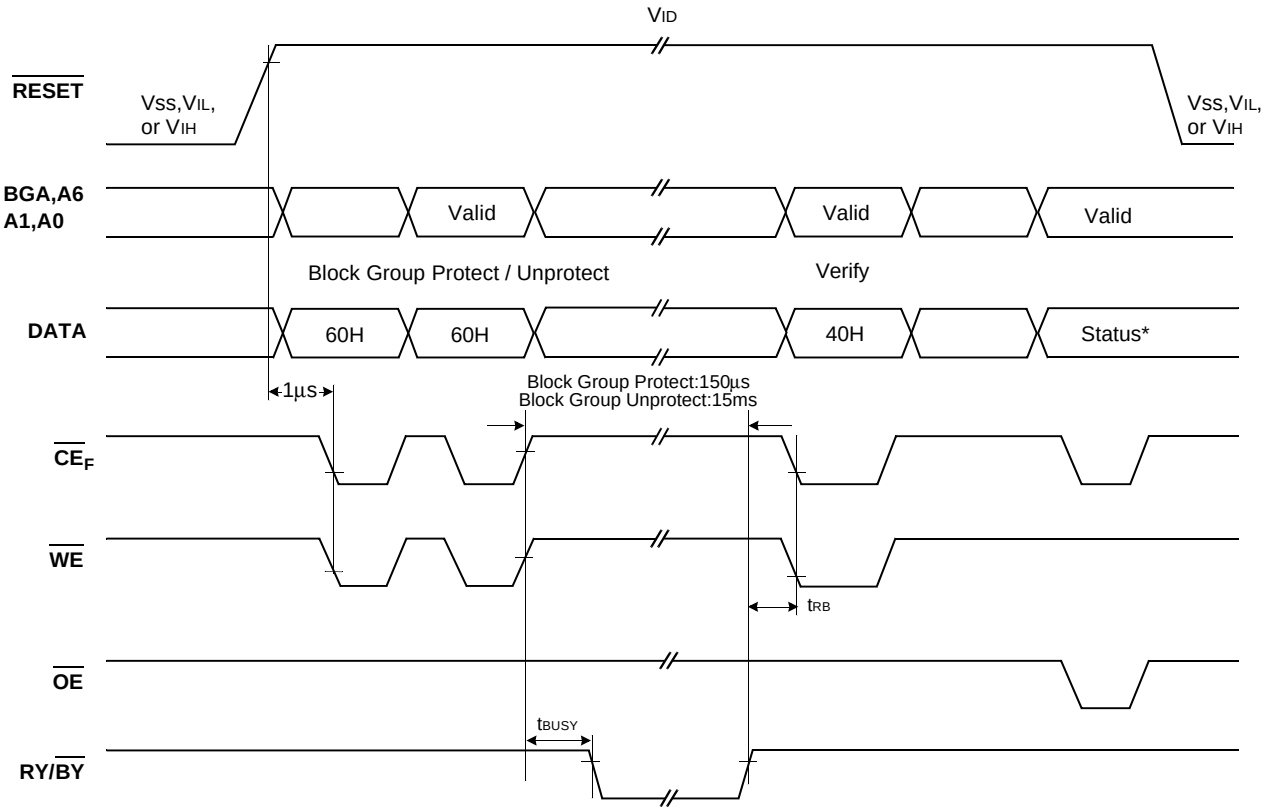
Power-up and $\overline{\text{RESET}}$ Timing Diagram



Parameter	Symbol	80ns		85ns		90ns		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{RESET}}$ Pulse Width	t_{RP}	500	-	500	-	500	-	ns
$\overline{\text{RESET}}$ Low to Valid Data (During Internal Routine)	t_{READY}	-	20	-	20	-	20	µs
$\overline{\text{RESET}}$ Low to Valid Data (Not during Internal Routine)	t_{READY}	-	500	-	500	-	500	ns
$\overline{\text{RESET}}$ High Time Before Read	t_{RH}	50	-	50	-	50	-	ns
RY/$\overline{\text{BY}}$ Recovery Time	t_{RB}	0	-	0	-	0	-	ns
$\overline{\text{RESET}}$ High to Address Valid	t_{RSTW}	200	-	200	-	200	-	ns
$\overline{\text{RESET}}$ Low Set-up Time	t_{RSTS}	500	-	500	-	500	-	ns

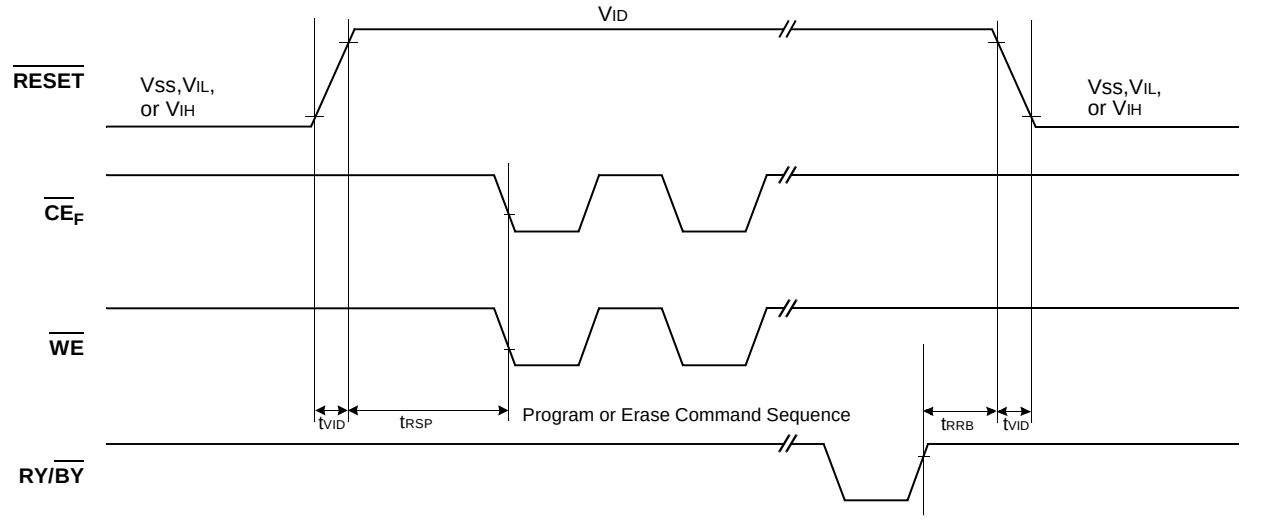
Flash SWITCHING WAVEFORMS

Block Group Protect & Unprotect Operations



Notes : Block Group Protect (A6=V_{IL} , A1=V_{IH} , A0=V_{IL}) , Status=01H
Block Group Unprotect (A6=V_{IH} , A1=V_{IH}, A0=V_{IL}) , Status=00H
BGA = Block Group Address (A12 ~ A20)

Temporary Block Group Unprotect



SRAM AC CHARACTERISTICS

Parameter List		Symbol	55ns		Units
			Min	Max	
Read	Read cycle time	t_{RC}	55	-	ns
	Address access time	t_{AA}	-	55	ns
	Chip select to output	t_{CO1}, t_{CO2}	-	55	ns
	Output enable to valid output	t_{OE}	-	30	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	55	ns
	Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	ns
	$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	ns
	Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	20	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	0	20	ns
	Output disable to high-Z output	t_{OHZ}	0	20	ns
	Output hold from address change	t_{OH}	10	-	ns
Write	Write cycle time	t_{WC}	55	-	ns
	Chip select to end of write	t_{CW}	45	-	ns
	Address set-up time	t_{AS}	0	-	ns
	Address valid to end of write	t_{AW}	45	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	45	-	ns
	Write pulse width	t_{WP}	40	-	ns
	Write recovery time	t_{WR}	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	ns
	Data to write time overlap	t_{DW}	20	-	ns
	Data hold from write time	t_{DH}	0	-	ns
	End write to output low-Z	t_{OW}	5	-	ns

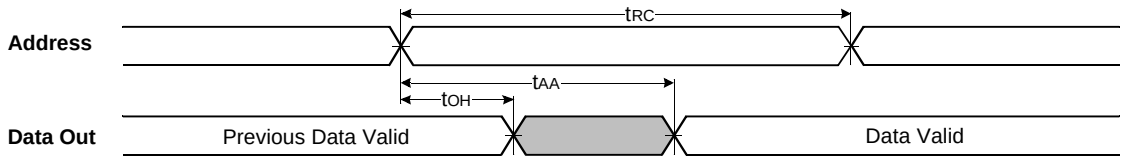
SRAM DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC_S} for data retention	V_{DR}	$\overline{CS1}_S \geq V_{CC_S}$-0.2V	1.5	-	3.3	V
Data retention current	I_{DR}	V_{CC_S}=3.0V, $\overline{CS1}_S \geq V_{CC_S}$-0.2V	-	0.5	15	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		tRC	-	-	

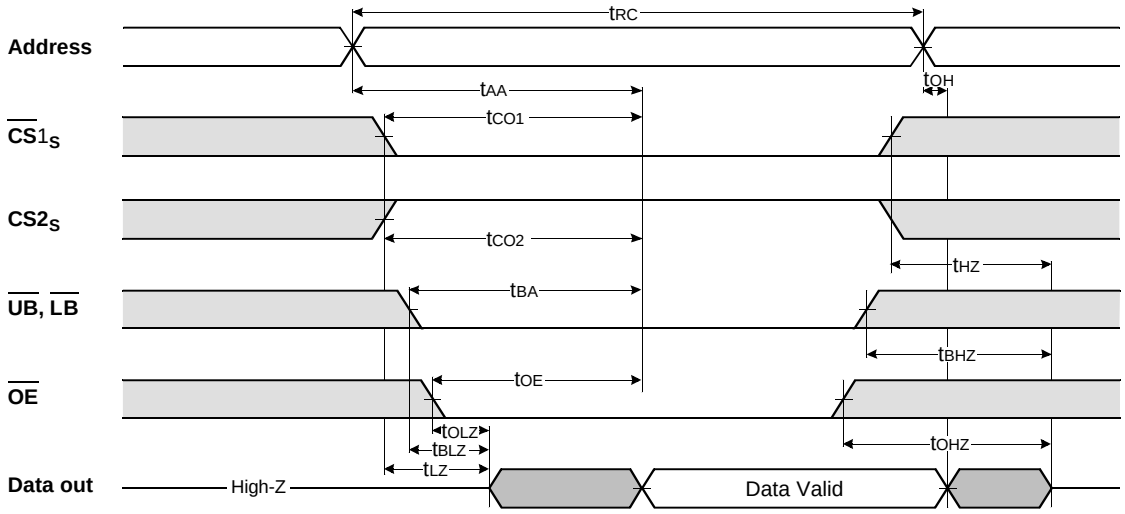
1. $\overline{CS1}_S \geq V_{CC_S}$-0.2V, $CS2_S \geq V_{CC_S}$-0.2V($\overline{CS1}_S$ controlled) or $CS2_S \leq$0.2V($CS2_S$ controlled)
2. Typical values are measured at Vcc=3.0V, Ta=25°C , not 100% tested.

SRAM TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}_S$=$\overline{OE}$=V_{IL}, $CS2_S$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})

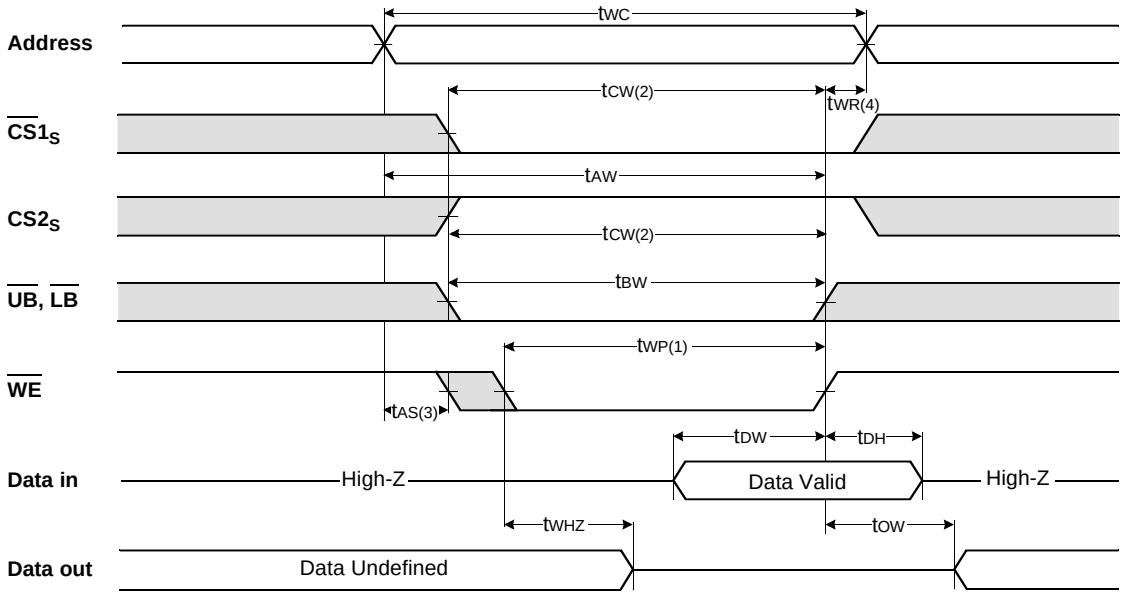


NOTES (READ CYCLE)

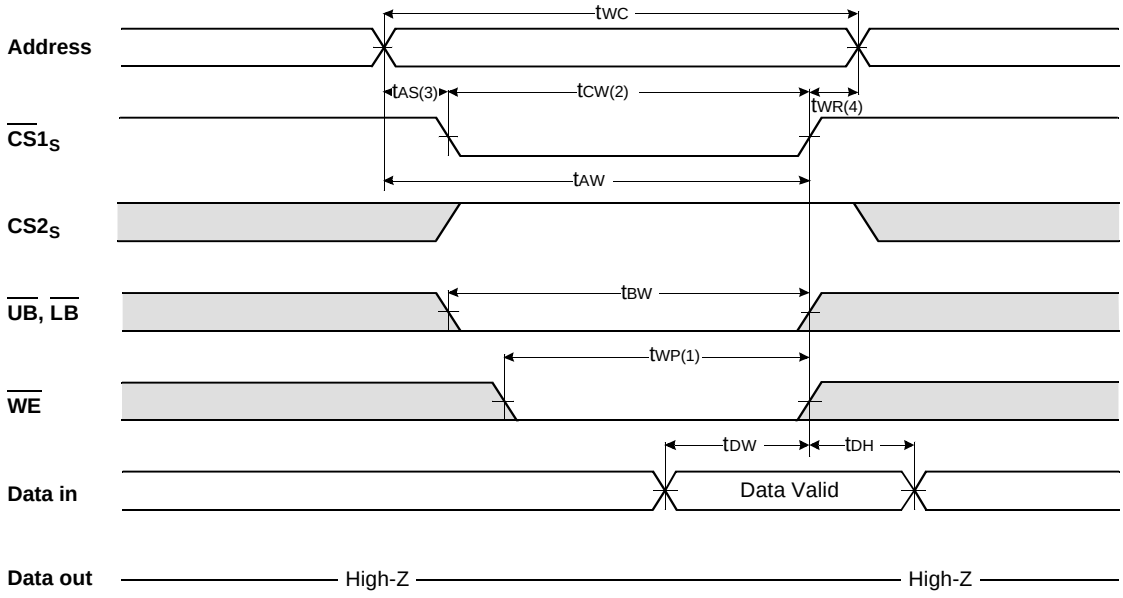
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

SRAM TIMING DIAGRAMS

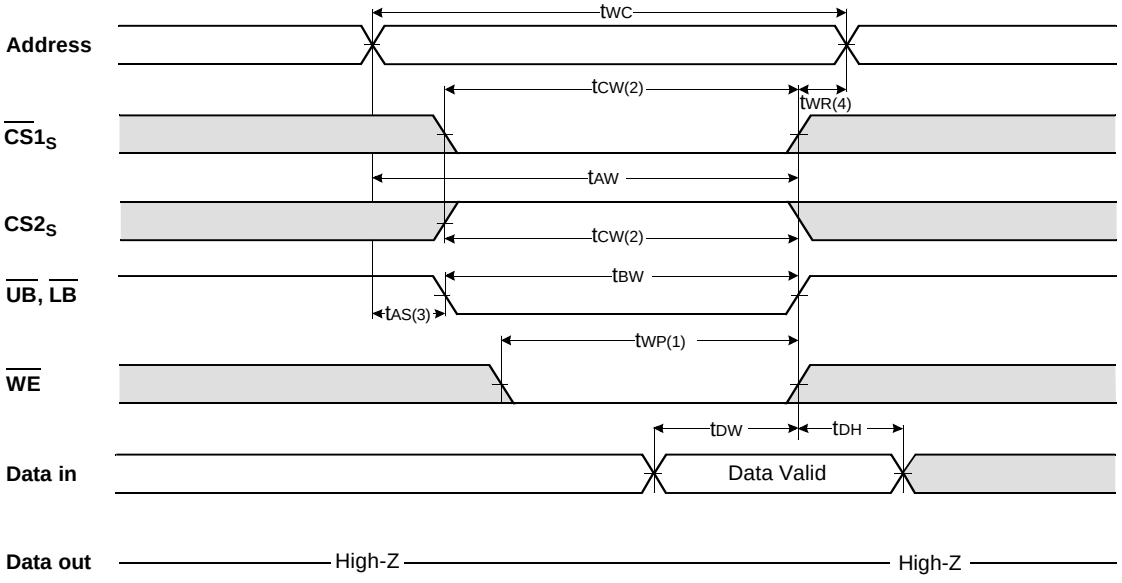
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}_S$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

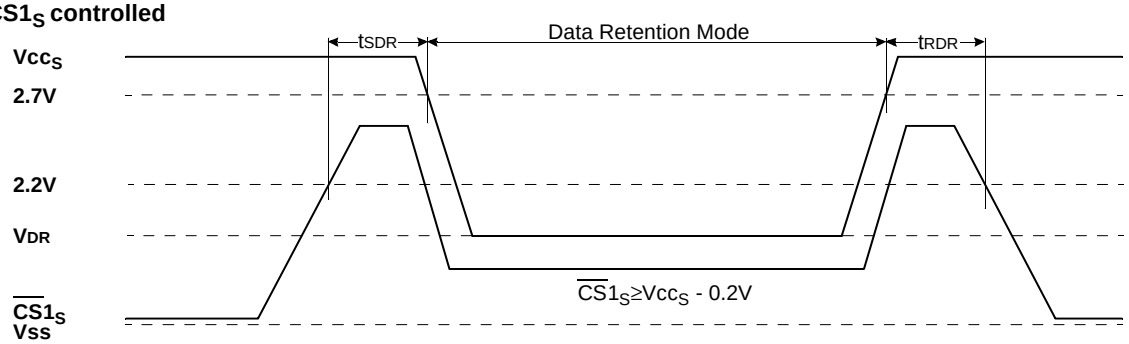


NOTES (WRITE CYCLE)

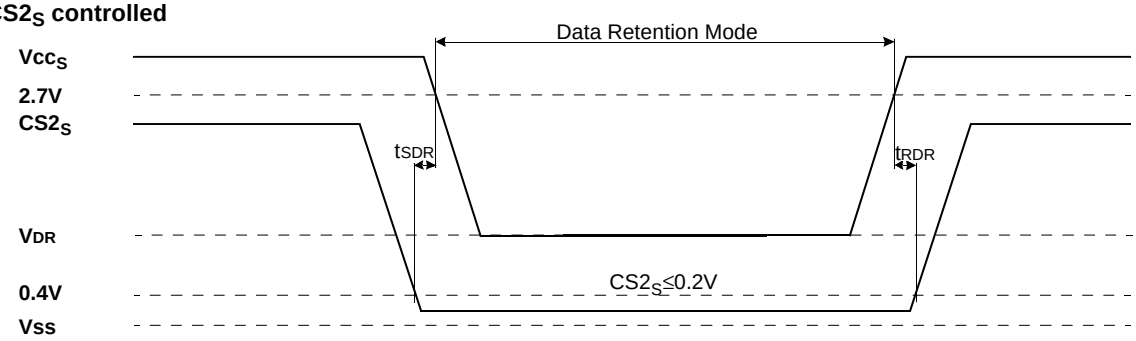
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}_S$ and low $\overline{WE}$. A write begins when $\overline{CS1}_S$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS1}_S$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}_S$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}_S$ or $\overline{WE}$ going high.

SRAM DATA RETENTION WAVE FORM

$\overline{CS1}_S$ controlled



$CS2_S$ controlled



PACKAGE DIMENSION

69-Ball Tape Ball Grid Array Package (measured in millimeters)