intersil

HS-6617RH

**Radiation Hardened
2K x 8 CMOS PROM**

August 1995

Features

- **Total Dose 1 x 10^5 RAD (Si)**
- **Latch-Up Free >1 x 10^{12} RAD (Si)/s**
- **Field Programmable**
- **Functionally Equivalent to HM-6617**
- **Pin Compatible with Intel 2716**
- **Low Standby Power 1.1mW Max**
- **Low Operating Power 137.5mW/MHz Max**
- **Fast Access Time 100ns Max**
- **TTL Compatible Inputs/Outputs**
- **Synchronous Operation**
- **On Chip Address Latches**
- **Three-State Outputs**
- **Nicrome Fuse Links**
- **Easy Microprocessor Interfacing**
- **Military Temperature Range -55°C to +125°C**

Description

The Intersil HS-6617RH is a radiation hardened 16K CMOS PROM, organized in a 2K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and is designed to be functionally equivalent to the HM-6617. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structure, such as the HS-80C85RH or HS-80C86RH. The output enable control ($\overline{G}$) simplifies microprocessor system interfacing by allowing output data bus control, in addition to, the chip enable control. Synchronous operation of the HS-6617RH is ideal for high speed pipe-lined architecture systems and also in synchronous logic replacement functions.
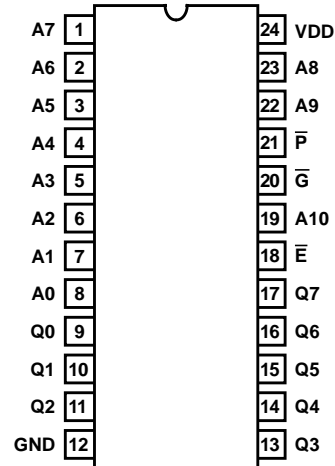
Applications for the HS-6617RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.
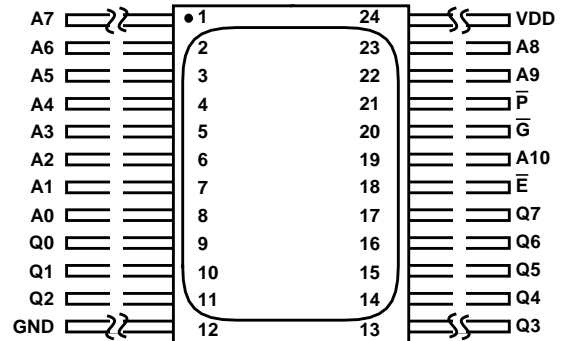
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-6617RH-Q	-55°C to +125°C	24 Lead SBDIP
HS1-6617RH-8	-55°C to +125°C	24 Lead SBDIP
HS1-6617RH/SAMPLE	25°C	24 Lead SBDIP
HS1-6617RH/PROTO	-55°C to +125°C	24 Lead SBDIP
HS9-6617RH-Q	-55°C to +125°C	24 Lead Flatpack
HS9-6617RH-8	-55°C to +125°C	24 Lead Flatpack
HS9-6617RH/Sample	25°C	24 Lead Flatpack
HS9-6617RH/PROTO	-55°C to +125°C	24 Lead Flatpack

Pinouts

**24 LEAD CERAMIC DUAL-IN-LINE
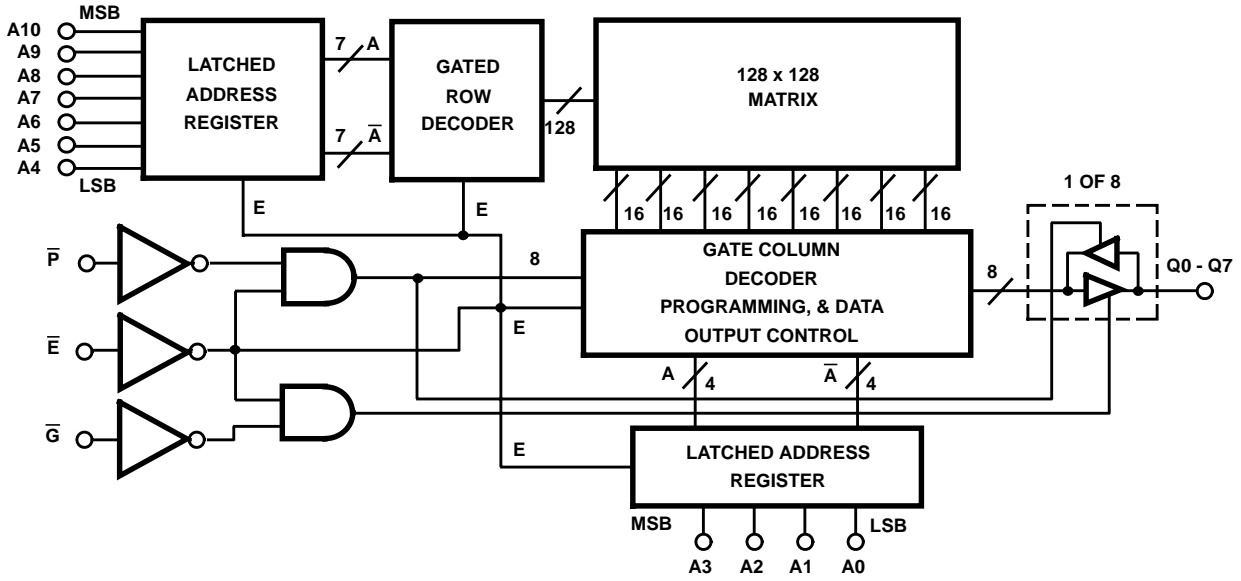METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T24**
TOP VIEW

A7	1	24 VDD
A6	2	23 A8
A5	3	22 A9
A4	4	21 $\overline{P}$
A3	5	20 $\overline{G}$
A2	6	19 A10
A1	7	18 $\overline{E}$
A0	8	17 Q7
Q0	9	16 Q6
Q1	10	15 Q5
Q2	11	14 Q4
GND	12	13 Q3

**24 LEAD CERAMIC METAL SEAL FLATPACK
PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F24**
TOP VIEW

A7	1	24 VDD
A6	2	23 A8
A5	3	22 A9
A4	4	21 $\overline{P}$
A3	5	20 $\overline{G}$
A2	6	19 A10
A1	7	18 $\overline{E}$
A0	8	17 Q7
Q0	9	16 Q6
Q1	10	15 Q5
Q2	11	14 Q4
GND	12	13 Q3

PIN	DESCRIPTION
A	Address Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program Enable ($\overline{P}$ Hardwired to VDD, except during programming)

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Spec Number **518742**

File Number **3033.3**

Functional Diagram

ALL LINES POSITIVE LOGIC:
ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH $\longrightarrow$ OUTPUT ACTIVE

ADDRESS LATCHES & GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{G}$
$\overline{P}$ = HARDWIRED TO VDD EXCEPT DURING PROGRAMMING

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) . . . . +7.0V
Input or Output Voltage
Applied for All Grades. . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature . . . . +175°C
Lead Temperature (Soldering 10s) . . . . +300°C
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Sidebraze DIP Package	40°C/W	6°C/W
Ceramic Flatpack Package	60°C/W	4°C/W

Maximum Package Power Dissipation at +125°C
Sidebraze DIP Package 1.251W
Ceramic Flatpack Package 0.83W
If device power exceeds package dissipation capability, provide heat
sinking or derate linearly at the following rate:
Sidebraze DIP Package 25.0mW/C
Ceramic Flatpack Package 16.7mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . .0V to +0.8V
Input High Voltage (VIH) . . . . +2.4V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS
Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 4.8mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	25	mA
Functional Test	FT	VDD = 4.5V (Note 4)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTES:

1. All voltages referenced to device GND.

2. All tests performed with $\overline{P}$ hardwired to VDD.

3. Typical derating = 20mA/MHz increase in IDDOP.

4. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS
Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Access Time	TAVQV	VDD = 4.5V and 5.5V (Note 4)	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	ns
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	100	ns
Address Setup Time	TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Hold Time	TELAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	ns
Chip Enable Low Width	TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	120	-	ns
Chip Enable High Width	TEHEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Read Cycle Time	TELEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	160	-	ns

NOTES:

1. All voltages referenced to device GND.

2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF.

3. All tests performed with $\overline{P}$ hardwired to VDD.

4. TAVQV = TELQV + TAVEL.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 2) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 3	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	1, 3	$T_A = +25^oC$	-	12	pF
Chip Enable Time	TELQX	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable Time	TGLQX	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Disable Time	TEHQZ	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Disable Time	TGHQZ	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output High Voltage	VOH2	VDD = 4.5V, IO = 100μA	3	$-55^oC \leq T_A \leq +125^oC$	VDD-0.5V	-	V

NOTES:

1. All measurements referenced to device GND.

2. All tests performed with $\overline{P}$ hardwired to VDD.

3. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.

TABLE 4. POST 100K RAD AC AND DC ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: All AC and DC parameters are tested at the $+25^oC$ pre-irradiation limits.

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TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	$\pm10\mu$A
Input Leakage Current	IOZ	$\pm 1\mu$A
	II	±100nA
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)	-	
Subgroup B6	Sample 5005	1, 7, 9	-	-	
Group C	Sample 5005	-	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.

2. Table 5 parameters only

Intersil Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007
   (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach (Note 1)

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

CSI and/or GSI Pre-Cap (Note 8)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 2)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

Sample - Group B, Method 5005 (Notes 5 and 6)

Sample - Group D, Method 5005 (Notes 6 and 7)

100% Data Package Generation (Note 9)

CSI and/or GSI Final (Note 8)

NOTES:

1. Epoxy or Silver glass die attach shall be permitted.

2. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.

3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.

4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.

5. QCI Subgroup B5 samples are programmed with a checkerboard pattern before life test and pattern tested after life test. Therefore, the Subgroup B5 samples must be considered destruct samples and cannot be shipped as flight quantity.

6. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group Samples, Group D Test and Group D Samples.

7. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.

8. CSI and/or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI Final Inspection, GSI PreCap inspection, and/or GSI Final Inspection.

9. Data Package Contents:

   • Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).

   • Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.

   • GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.

   • X-Ray report and film. Includes penetrometer measurements.

   • Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).

   • Lot Serial Number Sheet (Good units serial number and lot number).

   • Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.

   • Group B and D attributes and/or Generic data is included when required by the P.O.

   • The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Intersil Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach (Note 1)

Periodic- Wire Bond Pull Monitor, Method 2011

Periodic- Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

CSI and/or GSI Pre-Cap (Note 7)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 5)

Sample - Group C, Method 5005 (Notes 4, 5 and 6)

Sample - Group D, Method 5005 (Notes 5 and 6)

100% Data Package Generation (Note 8)

CSI and/or GSI Final (Note 7)

NOTES:

1. Epoxy or Silver glass die attach shall be permitted.

2. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5%.

3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.

4. QCI Group C samples are programmed with a checkerboard pattern before life test and pattern tested after life test. Therefore, the Group C samples must be considered destruct samples and cannot be shipped as flight quantity.

5. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.

6. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.

7. CSI and/or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI Final Inspection, GSI PreCap inspection, and/or GSI Final Inspection.

8. Data Package Contents:

   • Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).

   • GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.

   • Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).

   • Group B, C and D attributes and/or Generic data is included when required by the P.O.

   • The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.
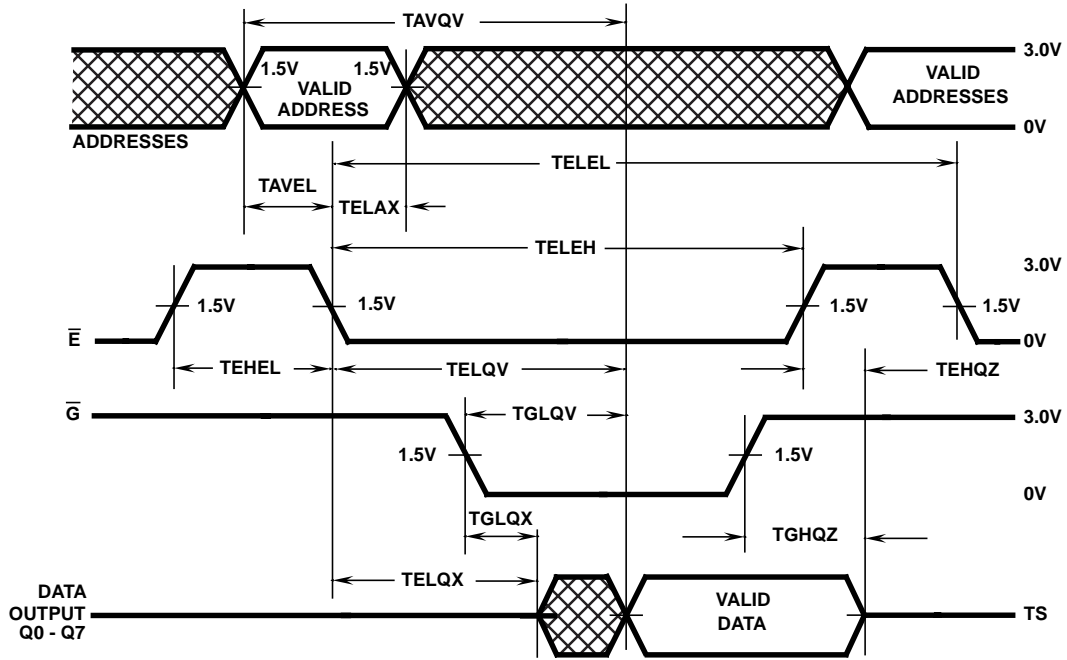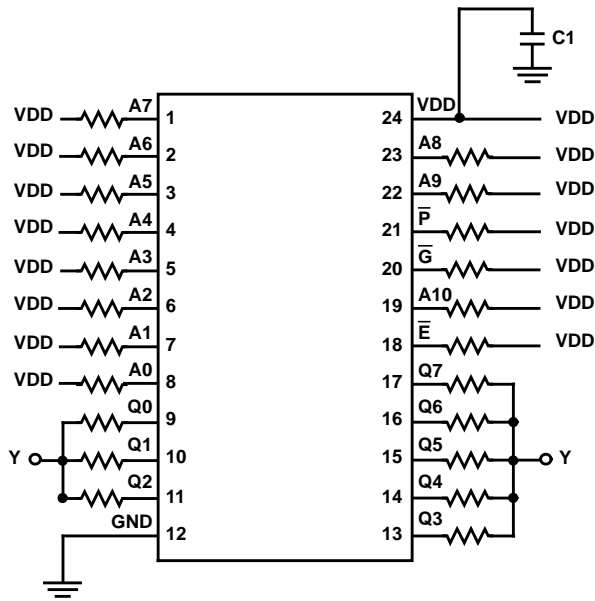
Spec Number **518742**

Timing Waveform

FIGURE 1. READ CYCLE

Burn-In Circuits

HS-6617RH 24 LEAD SBDIP AND FLATPACK

STATIC CONFIGURATION

NOTES:

1. VDD = 6.0V $\pm$ 0.5V
2. C1 = 0.01μF (Min)
3. All Resistors = 47kΩ $\pm$ 5%
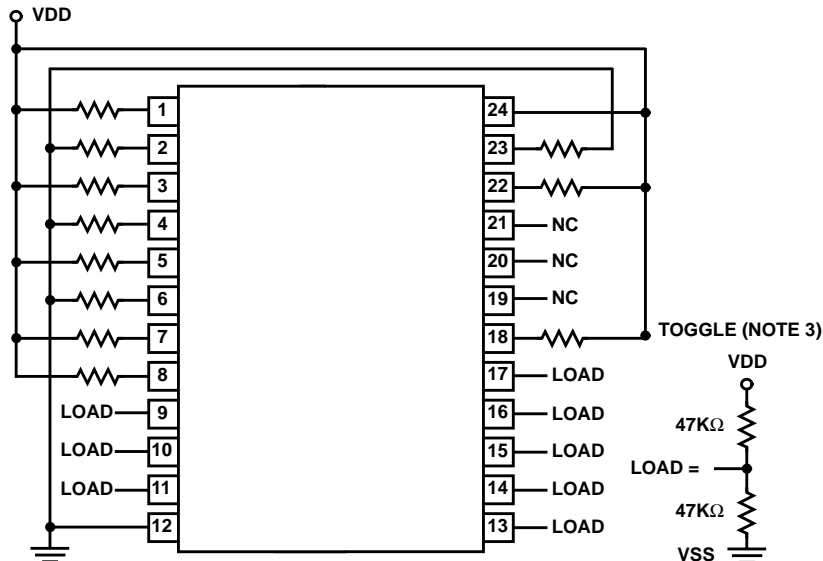4. Y = 2.7V $\pm$ 10%

HS-6617RH 24 LEAD SBDIP AND FLATPACK
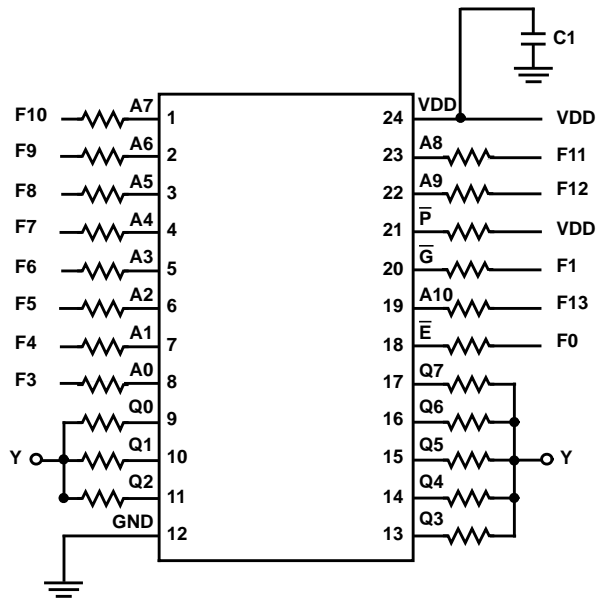
DYNAMIC CONFIGURATION

NOTES:

1. VDD = 6.0V $\pm$ 0.5V
2. VIH = 4.5V$\pm$ 10%
3. VIL = 0.8V (Max)
4. C1 = 0.01μF (Min)
5. All Resistors = 47kΩ $\pm$ 5%
6. F0 = 100KHz $\pm$ 10%, 40 - 60% duty cycle
7. F1 = F0/2 . . . F13 = F12/2
8. Y = 2.7V $\pm$ 10%

Irradiation Circuit

HS-6617RH 24 LEAD FLATPACK

NOTES:

1. Power Supply: VDD = 5.5V
2. All Registors = 47KΩ
3. Pin 18 is toggled from VSS to VDD then back to VSS and held at VSS during irradiation.

Spec Number **518742**

Metallization Topology

DIE DIMENSIONS:
 164 x 250 x 19 ±1mils

METALLIZATION:
 Type: Silicon-Aluminum
 Thickness: 13kÅ ± 2kÅ

GLASSIVATION:
 Type: SiO_2
 Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
 1×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6617RH
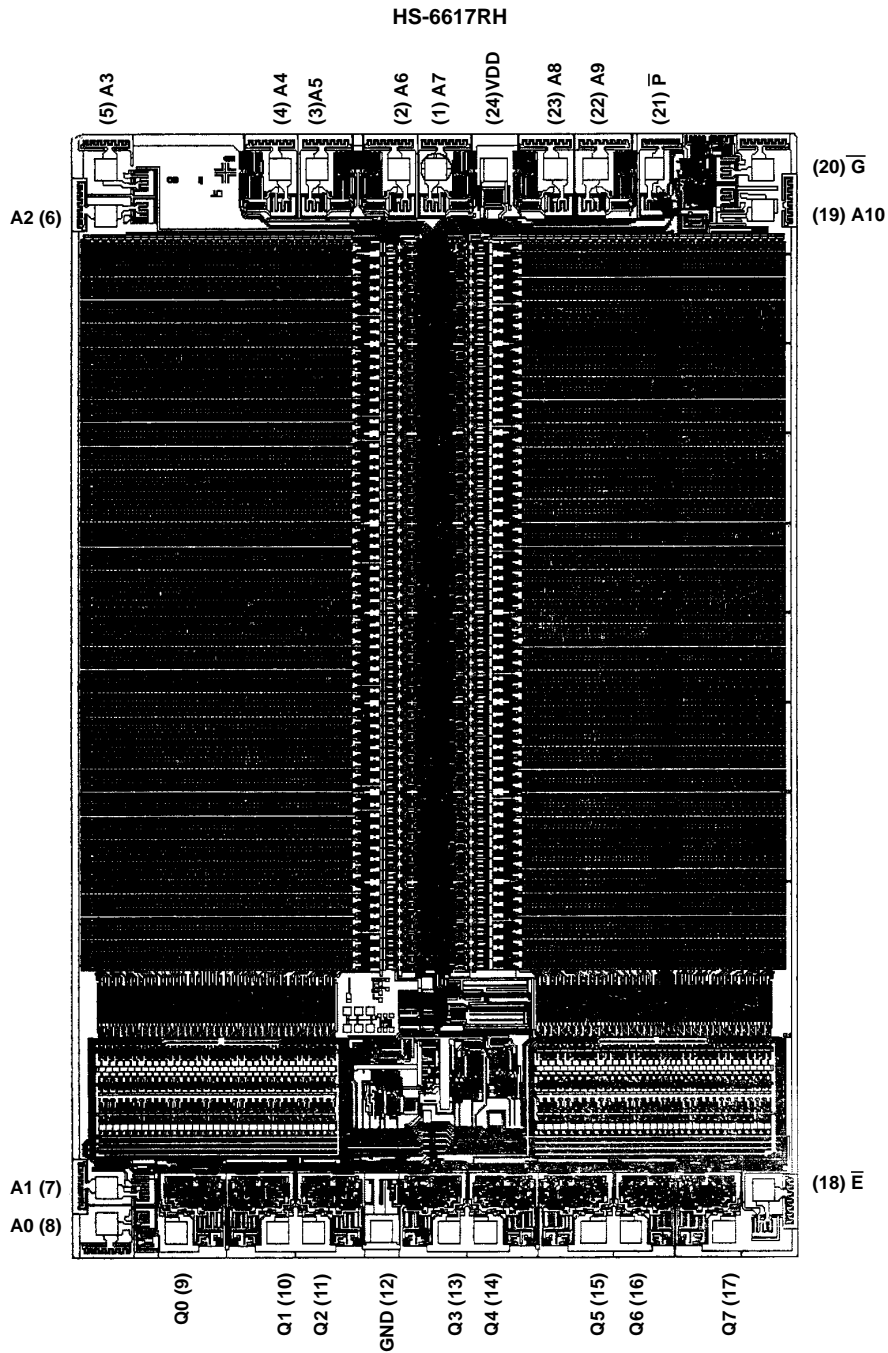
DESIGN INFORMATION

July 1995

2K x 8 CMOS PROM

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information HS-6617RH Programming

PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input "0"	VIL	0.0	0.2	0.8	V	
Voltage "1"	VIH	VDD-2	VDD	VDD+0.3	V	6
Programming VDD	VDDPROG	10.0	10.0	10.0	V	2
Operating VDD	VDD1	4.5	5.5	5.5	V	
Special Verify	VDD2	4.0	-	6.0	V	3
Delay Time	td	1.0	1.0	-	μs	
Rise Time	tr	1.0	10.0	10.0	μs	
Fall Time	tf	1.0	10.0	10.0	μs	
Chip Enable Pulse Width	TEHEL	50	-	-	ns	
Address Valid to Chip Enable Low Time	TAVEL	20	-	-	ns	
Chip Enable Low to Output Valid Time	TELQV	-	-	120	ns	
Programming Pulse Width	tpw	90	100	110	μs	4
Input Leakage at VDD = VDDPROG	tIP	-10	+1.0	10	μA	
Data Output Current at VDD = VDDPROG	IOP	-	-5.0	-10	mA	
Output Pull-Up Resistor	Rn	5	10	15	kΩ	5
Ambient Temperature	T_A	-	25	-	°C	

NOTES:

1. All inputs must track VDD (pin 24) within these limits.

2. VDDPROG must be capable of supplying 500mA. VDDPROG Power Supply tolerence ±3% (Max.)

3. See Steps 22 through 29 of the Programming Algorithm.

4. See Step 11 of the Programming Algorithm.

5. All outputs should be pulled up to VDD through a resistor of value Rn.

6. Except during programming (See Programming Cycle Waveforms).

Spec Number **518742**

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information Programming

The HS-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or use of an approved commercial programmer is recommended.

Programming Sequence of Events

1. Apply a voltage of VDD1 to VDD of the PROM.

2. Read all fuse locations to verify that the PROM is blank (output low).

3. Place the PROM in the initial state for programming: $\overline{E}$ = VIH, $\overline{P}$ = VIH, $\overline{G}$ = VIL.

4. Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.

5. After a delay of td, apply voltage of VIL to $\overline{E}$ (pin 18) to access the addressed word.

6. The address may be held through the cycle, but must be held valid at least for a time equal to td after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.

7. After a delay of td, disable the outputs by applying a voltage of VIH to $\overline{G}$ (pin 20).

8. After a delay of td, apply voltage of VIL to $\overline{P}$ (pin 21).

9. After delay of td, raise VDD (pin 24) to VDDPROG with a rise time of tr. All outputs at VIH should track VDD within VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resistors of value Rn.

10. After a delay of td, pull the output which corresponds to the bit to be programmed to VIL. Only one bit should be programmed at a time.

11. After a delay of tpw, allow the output to be pulled to VIH through pull-up resistor Rn.

12. After a delay of td, reduce VDD (pin 24) to VDD1 with a fall time of tf. All outputs at VIH should track VDD with VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resis- tors of value Rn.

13. Apply a voltage of VIH to $\overline{P}$ (pin 21).

14. After a delay of td, apply a voltage of VIL to $\overline{G}$ (pin 20).

15. After a delay of td, examine the outputs for correct data. If any location verifies incorrectly, it should be considered a programming reject.

16. Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

Post-Programming Verification

17. Place the PROM in the post-programming verification mode: $\overline{E}$ = VIH, $\overline{G}$ = VIL, $\overline{P}$ = VIH, VDD (pin 24) = VDD1.

18. Apply the correct binary address of the word to be verified to the PROM.

19. After a delay of td, apply a voltage of VIL to $\overline{E}$ (pin 18).

20. After a delay of td, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.

21. Repeat steps 17 through 20 for all possible programming locations.

Post-Programming Read

22. Apply a voltage of VDD2 = 4.0V to VDD (pin 24).

23. After a delay of td, apply a voltage of VIH to $\overline{E}$ (pin 18).

24. Apply the correct binary address of the word to be read.

25. After a delay of TAVEL, apply a voltage of VIL to $\overline{E}$ (pin 18).

26. After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.

27. Repeat steps 23 through 26 for all address locations.

28. Apply a voltage of VDD2 = 6.0V to VDD (pin 24).

29. Repeat steps 23 through 26 for all address locations.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.
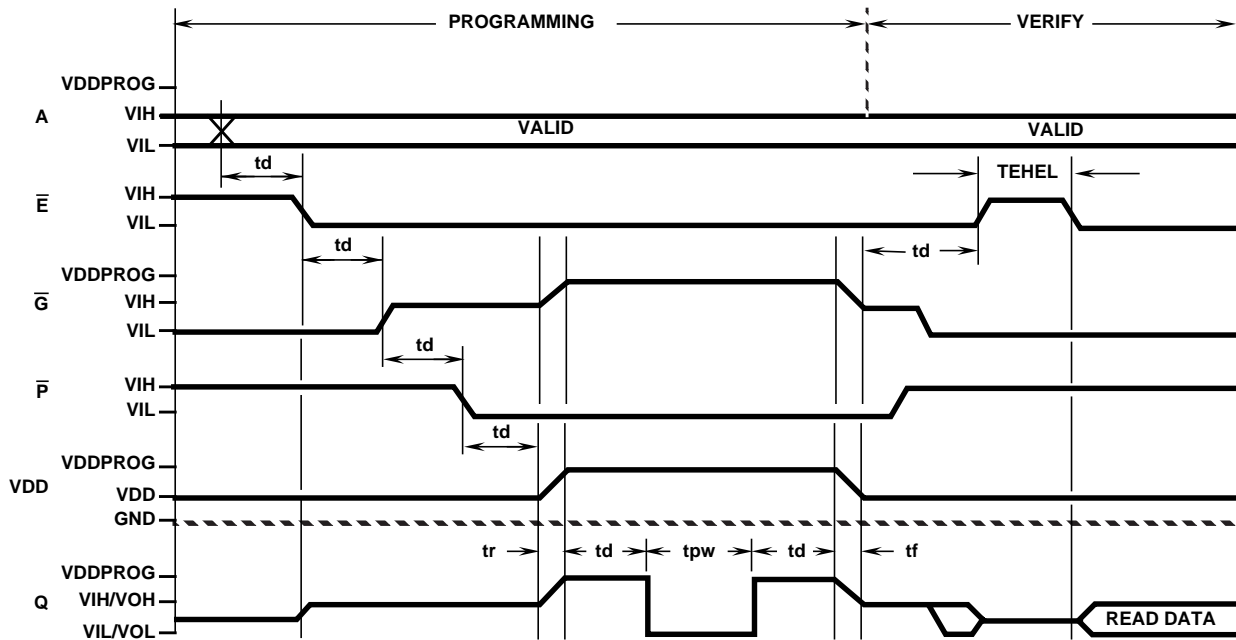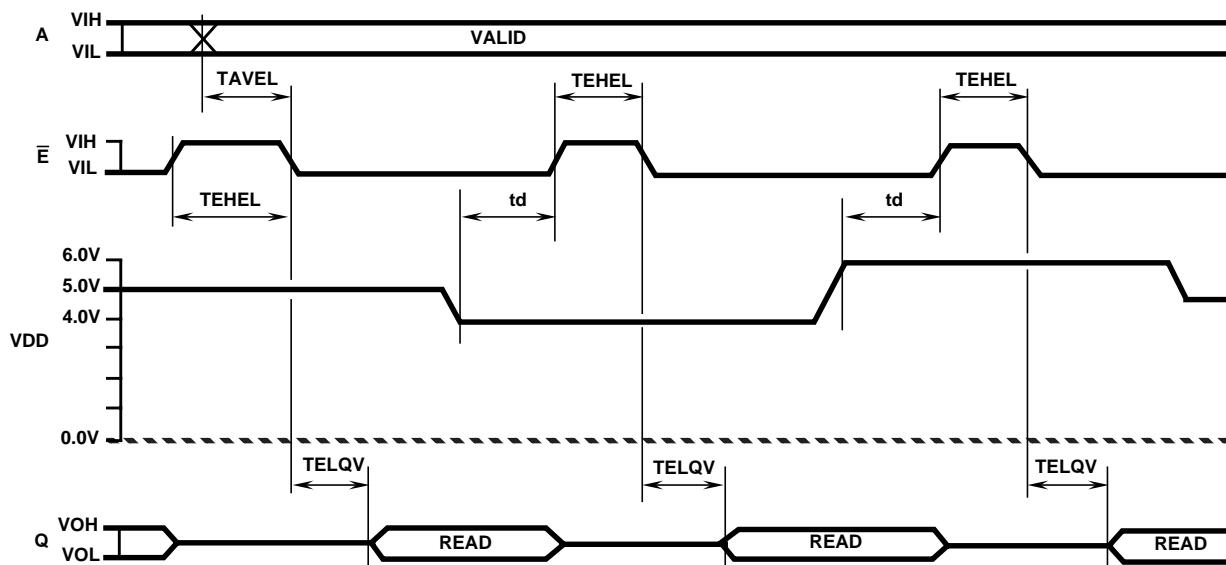

FIGURE 2. HS-6617RH PROGRAMMING CYCLE

FIGURE 3. HS-6617RH POST PROGRAMMING VERIFY CYCLE

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