



CMOS Color Digital Video Camera

Features

- 352 x 288 active pixel array with color filters, 1/3 inch lens format ¥
- Programmable formats CIF 352x288, QCIF 176x144, CCIR601 704x288
- Digital output CCIR601 4:2:2 (8-bit or 16-bit)
- Multidimensional automatic shutter control
- Below 5 LUX sensitivity
- Programmable I²C Serial bus control:
 - Frame rate: 30fps-1fps in eight steps
 - Gamma correction
 - Shutterspeed
 - Analog gain
 - 16 backlight compensation zones
 - Black clamp level
 - White balance adjustment
 - Power down modes
- Stand-alone 25fps PAL operation with all automatic features
- Single crystal operation: Video timing on-chip
- Single 5V power supply
- Less than 0.5 watt power dissipation

¥ Patent number x,xxx,xxx patents pending

Description

The CH5001 is a single chip active pixel CMOS color video camera with digital video output in several formats. Using sophisticated noise correction circuitry to minimize fixed pattern noise and dark current effects, the CH5001 provides a superb quality picture in a low cost device.

The CH5001 uses a proprietary autos shutter algorithm to dynamically control the shutter time, analog gain, and black clamp level, providing optimum picture and contrast under all lighting conditions. The CH5001 also incorporates extensive on-chip programmable digital signal processing to maximize the usefulness of the device in processor driven applications. This includes 16 programmable zones for backlight compensation, allowing the user to adjust the image to their unique lighting environment.

Additionally, at power-up the backlight compensation zone, power-up condition, and direct A/D output modes are selectable without IIC control by using the PUD pins.

Requiring a minimum of parts for operation, the CH5001 provides a low cost camera for the next generation video conferencing, videophone, and surveillance products.

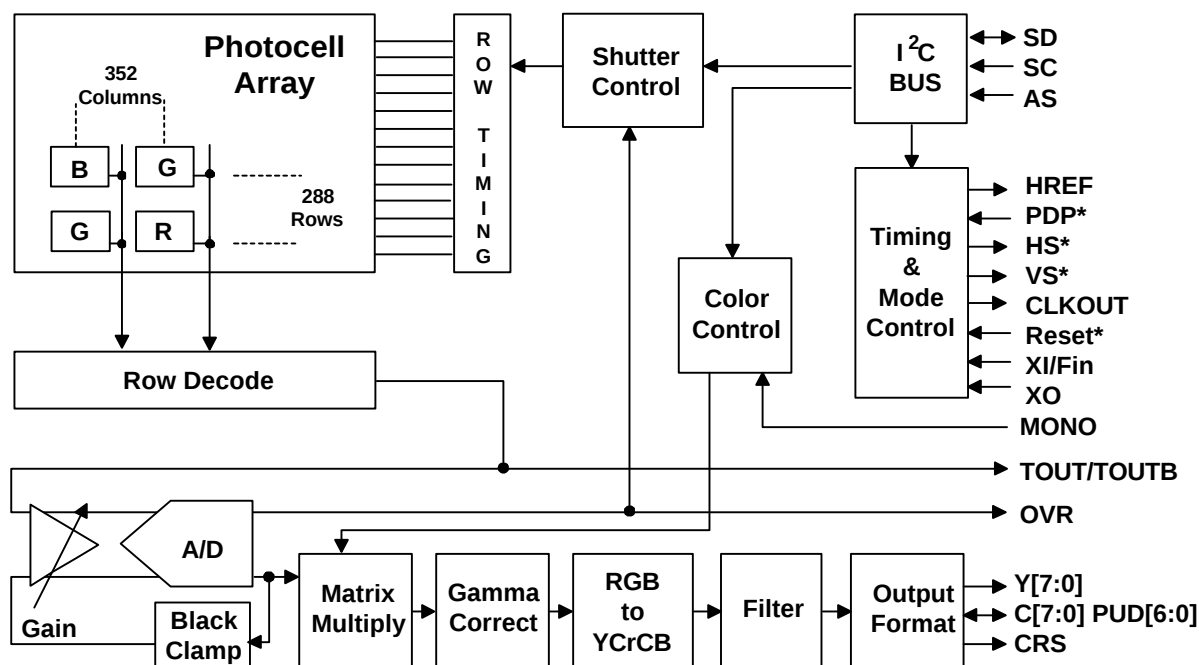


Figure 1: Block Diagram

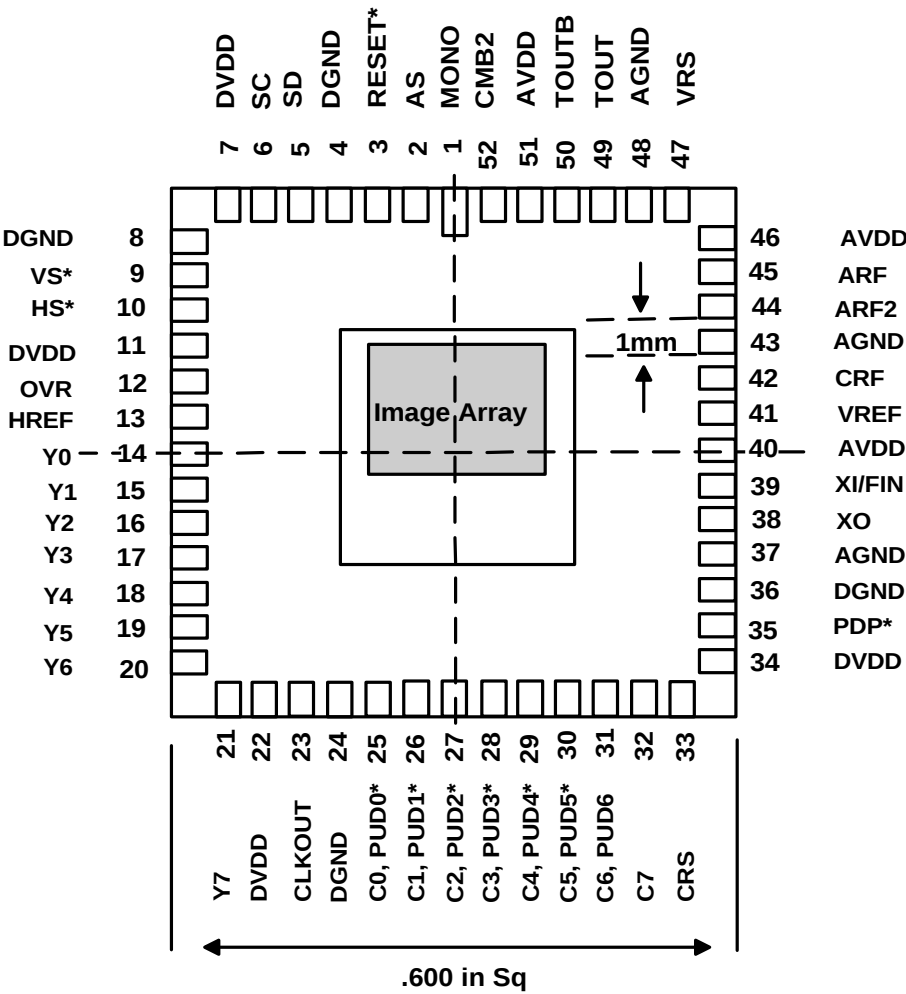


Figure 2: 52 Contact Ceramic LCC (Top View)

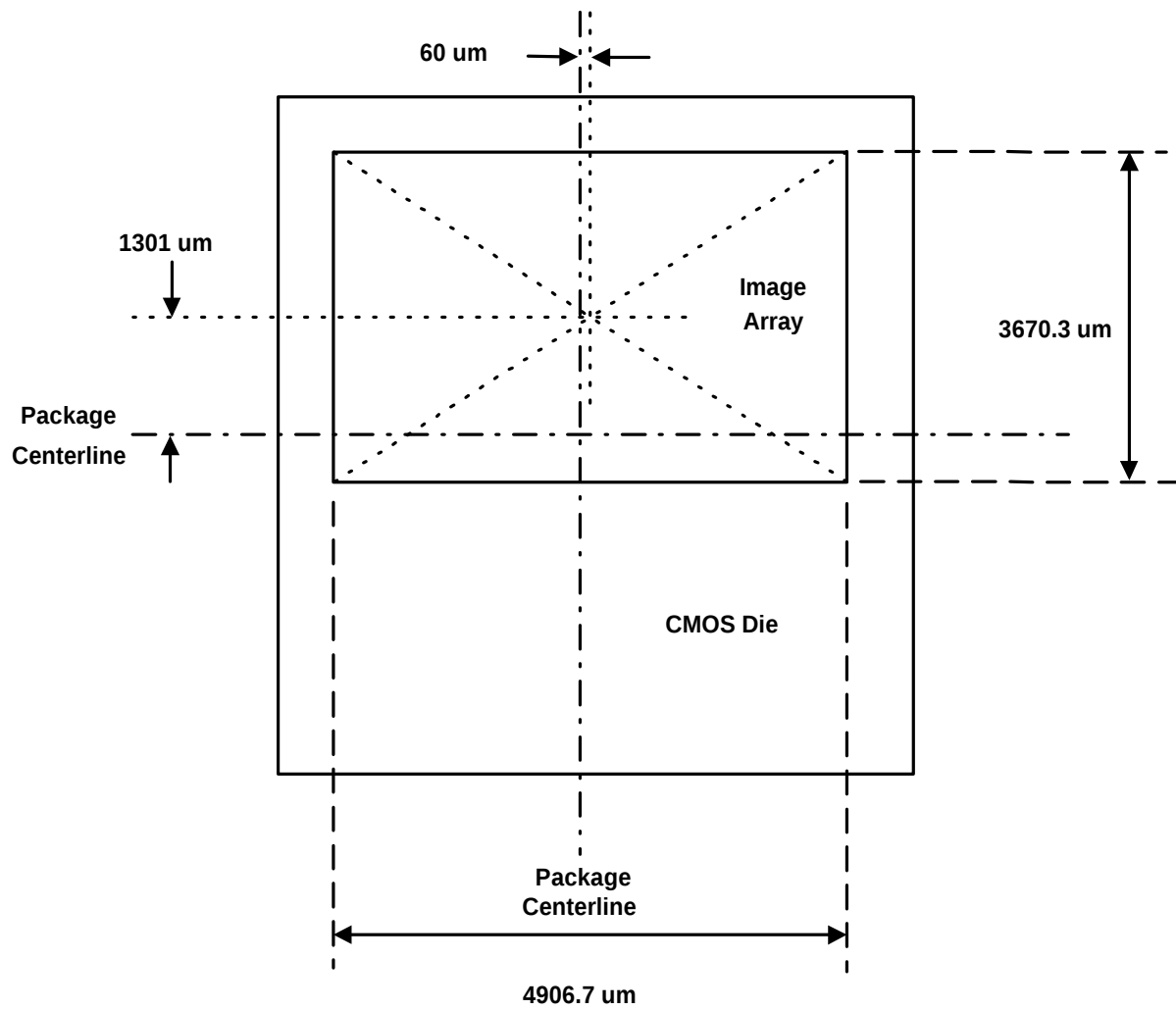


Figure 3: CH5001 Array Image Offset

Table 1. Pin Descriptions

Pin	Type	Symbol	Description
21-14	Out	Y[7:0]	Video Output Provides the luminance data of the digital video output.
7, 11, 22, 34	Power	DVDD	Digital Supply Voltage These pins supply the 5V power to the digital section of CH5001.
4, 8, 24, 36	Power	DGND	Digital Ground Provides the ground reference for the digital section of CH5001. These pins MUST be connected to the system ground.
32-25	Out	C[7:0]	Video Output Chrominance data of the digital video output are provided by these pins.
33	Out	CRS	Cr Select CRS specifies the CrCb data sequence. CRS is an alternating signal. CRS=1 indicates that C[7:0] carry the Cr data. CRS=0 indicates C[7:0] carry the Cb data.
23	Out	CLKOUT	Video Pixel Clock Output This pin outputs a buffered clock signal which can be used to latch data output by pins Y[7:0] and C[7:0].
9	Out	VS*	Vertical Sync Output (active low) Outputs a vertical sync pulse.
10	Out	HS*	Horizontal Sync Output (active low) Outputs a horizontal sync pulse.
12	Out	OVR	Over Range This pin is high when the A/D converter input is beyond the full scale range of the A/D.
13	Out	HREF	Horizontal Reference Active video timing signal. This output is high when active data is being output from the device, and low otherwise.
6	In	SC	Serial Clock IIC clock input pin.
5	In/Out	SD	Serial Data IIC data input/output pin.
2	In	AS	Chip Address Select (internal pullup) This pin selects the IIC address for the device. AS = 1 Address = 100 0101 AS = 0 Address = 100 0110
3	In	RESET*	Chip Reset (active low, internal pullup) Puts all registers into power-on default states. The state at pin SD must be HIGH during reset for proper initialization.
38	In/Out	XO	Crystal Output A 27 MHz (± 50 ppm, parallel resonance) crystal may be attached between XO and XI/FIN.
39	In	XI/FIN	Crystal Input or External input A 27 MHz (± 50 ppm, parallel resonance) crystal should be attached between XO and XI/FIN. An external CMOS compatible clock can be connected to XI/FIN as an alternative.

Table 1. Pin Descriptions

Pin	Type	Symbol	Description
40, 46, 51	Power	AVDD	Analog Supply Voltage Supplies the 5V power to the analog section of the CH5001.
41	Out	VREF	Voltage Reference VREF provides a 1.235V reference. A 0.01 μ F decoupling capacitor should be connected between VREF and AGND.
37, 43, 48	Power	AGND	Analog Ground These pins provide the ground reference for the analog section of CH5001. Pins must be connected to the system ground to prevent latchup.
42	Out	CRF	Column Filter CRF provides a 2.5 V reference. A 0.1 μ F decoupling capacitor should be connected between CRF and AGND.
49, 50	In/Out	TOUT, TOUTB	Test Mode I/O Pins For test purposes only. Should be NC.
44, 45	Out	ARF2, ARF	Array Filters A 0.1 μ F decoupling capacitors should be connected between each of the pins and AGND.
47	Out	VRS	Array Bias Filter VRS provides a 2.1V reference. A 0.1 μ F decoupling capacitor should be connected between VRS and AGND.
1	In	MONO	Monochrome (active high, internal pulldown) Digital pin to select Color / Monochrome operation. 1= Monochrome 0=Color
35	In	PDP*	Power Down Pin (active low, internal pullup) 0 = power down
52	Out	CMB2	Bias Filter A 0.1 μ F decoupling capacitor should be connected between CMB2 and AGND.
31-25	In	PUD[5:0]* PUD[6]	Power Up Detect (internal pull-up) These pins are shared with the C[6:0] chrominance output function. At power-up they are inputs controlling the default value of IIC register bits M0, ADDO, PD, ASW[3:0]. Attach 100K Ohms to DGND to pull low. NOTE: PUD[5:0]* are logically inverted

Functional Description

The CH5001 accepts a light input to a photosensitive array, and produces a digital video stream in response. Each photodiode in the array is covered with a red, green or blue filter whose spectral response is designed to provide a proper color picture when displayed on a standard monitor/TV. The internal functions performed are:

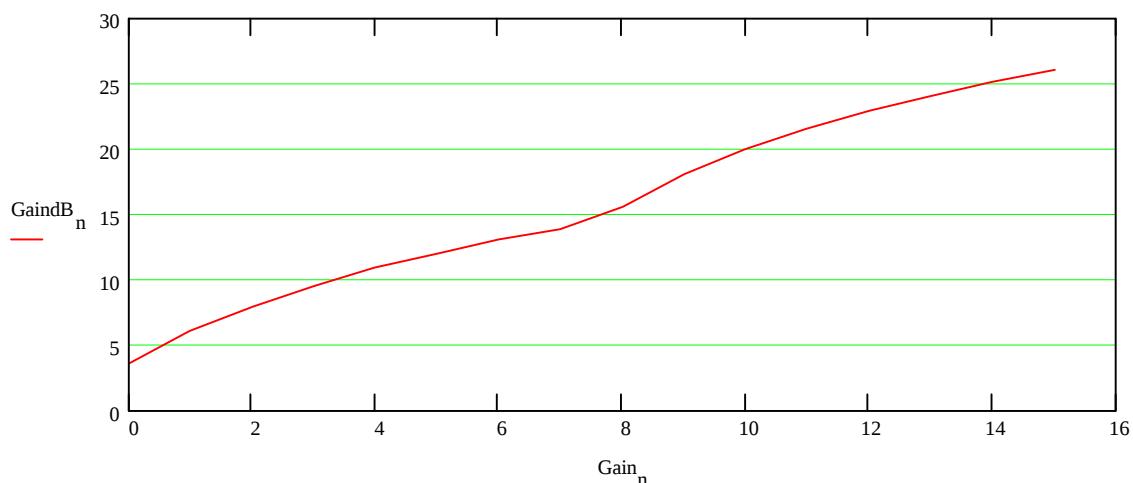
- Scanning of the photodiode array into a serial data stream.
- Programmable gain sample and hold with programmable offset.
- Digitization of data stream.
- Transform the data from the color filter domain to RGB domain.
- Programmable gamma correction and RGB offset.
- Conversion from RGB to YCrCb domain.
- Interpolate/Decimate data to desired resolution
- Formatting of the data stream for the desired type of output.
- Automatic Shutter, Gain and Black Setting.
- Timing signal generation.
- Bus control.
- Power up control of key register bits

Scanning of the photodiode array:

The CH5001 serializes the data captured in the photo array, and outputs one pixel of data each clock period. The first row is output a programmable number of lines after the leading edge of the vertical sync output. After the entire row has been output, the next row will be addressed and output. Correlated double sampling techniques are used during readout to reduce fixed pattern noise. After this transfer is complete, pixel data is serially sent to the programmable gain amplifier and then to an A/D converter.

Programmable gain sample and hold:

The programmable gain is divided into two sections. The first gain block is controlled by PGSH[2:0] and the second by the ADFS control. ADFS can be treated as the MSB of the gain control, and a plot of gain versus control setting is shown below. The programmable gain section also provides a bias adjustment, under the control of the an chip DAC. When the ASBE bit is a one (default) this DAC value is determined automatically, via a feedback loop which monitors the A/D output signal. When the ASBE bit is a zero, the DAC can be controlled via BCLMP[7:0].



A/D Conversion:

The data out of the programmable sample and hold is input to an 8-bit A/D. The output of the A/D is sent to the datapath section, and can alternatively be sent directly to the Y[7:0] pins. The A/D has an over-range output which is available as an external pin.

Transformation to RGB domain:

Each pixel output from the A/D has been exposed to light which was filtered by one of three types of colored filter, red, green or blue. To create RGB values for each pixel, four neighboring pixels are combined in different strengths in a matrix multiplier. The gains used in the matrix multiplier are programmable via the CSCXX[7:0] registers.

Programmable Gamma correction of RGB signals:

The RGB signals are next applied to a gamma correction block with selectable gamma settings of 1.0, 1.6 and 2.2, controlled via GAM[1:0]. Following gamma correction, a programmable offset is added to each term, via controls ROS[4:0], GOS[4:0] and BOS[4:0].

Convert to the YCrCb domain:

A color space conversion is then applied to the gamma corrected RGB signals to convert to the Y, Cr, Cb domain. The Cr and Cb gain can be independently adjusted in this block with the CRG and CBG controls.

Interpolate/Decimate data to desired resolution:

The output resolution is determined by the mode register bits M[2:0].

When a CCIR601 mode is selected (M[2:0] = 4,5), a signal compatible with Chrontel's CH7202 input will be generated. This entails interpolating the luminance signal by a factor of two, time multiplexing the CrCb signals, delay matching the CrCb signal to the filtered Y signal, and selecting the 8-bit output mode (register 00h, bit 0).

When a CIF output is selected (M[2:0] = 1), the Cr,Cb resolution will be decimated by a factor of two in both horizontal and vertical directions. This entails band-limiting the CrCb data, decimating in the horizontal direction, storing one line of decimated CrCb data and averaging the delayed line with the current line. This will position the chrominance samples according to H.261 standards, and is register controlled (CVL, CHL). When CIF2 is selected, the chrominance data is decimated in the horizontal direction only.

When QCIF output is selected (M[2:0] = 3), the Y resolution will be decimated by a factor of two in both horizontal and vertical directions and the CrCb data will be decimated by a factor of four in both the horizontal and vertical directions. This requires bandlimiting the Y and CrCb data, decimating in the horizontal direction. The Y data is not be decimated in the vertical direction (since two lines have already been averaged in the matrix multiplier section) but the CrCb data will generated a four line average in the vertical direction. When CIF2 is selected, the chrominance data is decimated by four in the horizontal direction, and by two in the vertical direction.

Format the data stream for the desired type of output:

In addition to the selection of CCIR601 or the different CIF and QCIF modes, the output format can be selected between 16-bit data (8-bit Y and 8-bit time multiplexed CrCb), and 8-bit data (time multiplexed Cb,Y,Cr,Y data at twice the rate).

Automatic Shutter, Gain and Black Setting:

The CH5001 contains circuitry to automatically adjust the shutter (ESLE, ESLH and ESLL), programmable gain (PGSH[2:0]) and black level (BCLMP[7:0]). These feedback loops are independently controlled by the three control bits Auto-Shutter Shutter Enable (ASSE), Auto-Shutter Gain Enable (ASGE) and Auto-Shutter Black Enable (ASBE). When each of these loops is enabled (default), a read to the corresponding shutter, gain or black level register will result in a readout of the control signal the algorithm has determined to be correct. Data can continue to be written to the control registers, but will not have an effect until the automatic feedback control is disabled. The feedback loops will attempt to force a percentage of the image (controlled by ASBC[4:0] and ASBT[2:0]) to black, and a certain percentage of the image (controlled by ASWC[7:0]) inside the selectable window to white. This will create an output image which maximizes the dynamic range of the signal, without creating overflow or underflow problems within the A/D or the datapath.

Timing signal generation:

The CH5001 generates all required internal and external timing signals. The following timing signals are output by the CH5001:

- Clock out (CLKOUT) - This output is used to latch the outputs of the Y[7:0], C[7:0], CRS, HS*, VS* and HREF.
- Cr Select (CRS) - The Cr Select signal determines whether the chroma sample being output is a Cr or Cb data.
- Horizontal Sync (HS*) - The horizontal sync output is used to determine the start of a new line. Polarity is selectable via control bit HSP.
- Vertical Sync (VS*) - The vertical sync output is used to determine the start of a new frame. Polarity is selectable via control bit VSP.
- Horizontal Reference (HREF) - The horizontal reference is high when active data is output from the CH5001.

The following timing parameters are programmable:

- Shutter - This control is divided among three registers, Electronic Shutter Length Extended (ESLE), Electronic Shutter Length High (ESLH) and Electronic Shutter Length Low (ESLL). The control range is from ~1 μ S, to just under the frame duration.
- Frame rate - In non-CCIR601 modes, the frame rate is selectable via the FR register. The CH5001 has two methods for adjusting the frame rate of the device.
- Horizontal start - In non-CCIR601 modes, the delay between the HS* output and the output of active data from the CH5001 is programmable via the HS register. The polarity of this output is programmable.
- Vertical start - In non-CCIR601 modes, the delay between the VS* output and the output of active data from the CH5001 is programmable via the VS register. The polarity of this output is programmable.
- Frame rate adjustment method — The CH5001 has two methods for adjusting the frame rate of the device. The first method is to add additional black lines to each frame after reading out the active data. The second method is to have each frame remain a constant number of lines long, and have each line contain a variable number of blank pixels after reading out the active data. In this mode, all clock signals are 1/2 of the normal rate.
- Auto shutter speed — The auto-shutter loop speed can be controlled via ASSPD[2:0].

Bus control:

The CH5001 is controlled via a 2 pin serial interface. The description of this interface, and all registers accessible via the interface is described later in the data sheet.

Power up control:

Seven bits within the CH5001 register map can have their default value determined at the time of power-up, or when the Reset pin is exercised. This is accomplished by using a high valued pull-down resistor on the C[6:0] pins. At power-up, the output buffers on these pins are tri-stated, and the pin is pulled high by an internal high impedance pull-up device. This pull-up can be overridden by connecting a 100K ohm resistor externally to ground. After three frames, the level at the C[6:0] pins is latched, and seven register bits are set or cleared depending upon the corresponding pin's level. The C[6:0] pins functions are then returned to outputs of the chroma data. The power-up control affects the following register bits:

Table 2. Power Up Default Control

Pin	Register	Bit	Function
C5 (PUD5*)	22h	3	ADDO The A/D Direct Output mode can be selected at power up. This may be desirable for applications which want to use raw data. Logically inverted input No pull-down resistor - Datapath processing Pull-down resistor - A/D direct output
C4 (PUD4*)	19h	4	PD The power down bit can be enabled at power up. This may be desirable in USB cameras which have power limitations at power up. Logically inverted input No pull-down resistor - Normal power-up Pull-down resistor - Power-up in low-power mode
C6 (PUD6)	00h	1	M0 The Mode[0] bit can be used to select between NTSC or PAL output at power up. No pull-down resistor - PAL operation Pull-down resistor - NTSC operation
C[3:0] (PUD[3:0]*)	1Eh	3:0	ASW[3:0] The auto-shutter window can be selected at power up. See the register description for corresponding window selection. Logically inverted inputs No pull-down resistors gives window "0", Center location

I²C Port Operation

The CH5001 contains a standard I²C control port, through which the control registers can be written and read. This port is comprised of a two-wire serial interface, pins SD (bidirectional) and SC, which can be connected directly to the SDB and SCB buses as shown in **Figure 4**.

The Serial Clock line (SC) is input only and is driven by the output buffer of the master device. The CH5001 acts as a slave and generation of clock signals on the bus is always the responsibility of the master device. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the bus can be transferred up to 400kbit/s according to I²C specifications. However, in direct connections to the bus master device, the CH5001 can operate at transfer rates up to 5 MHz.

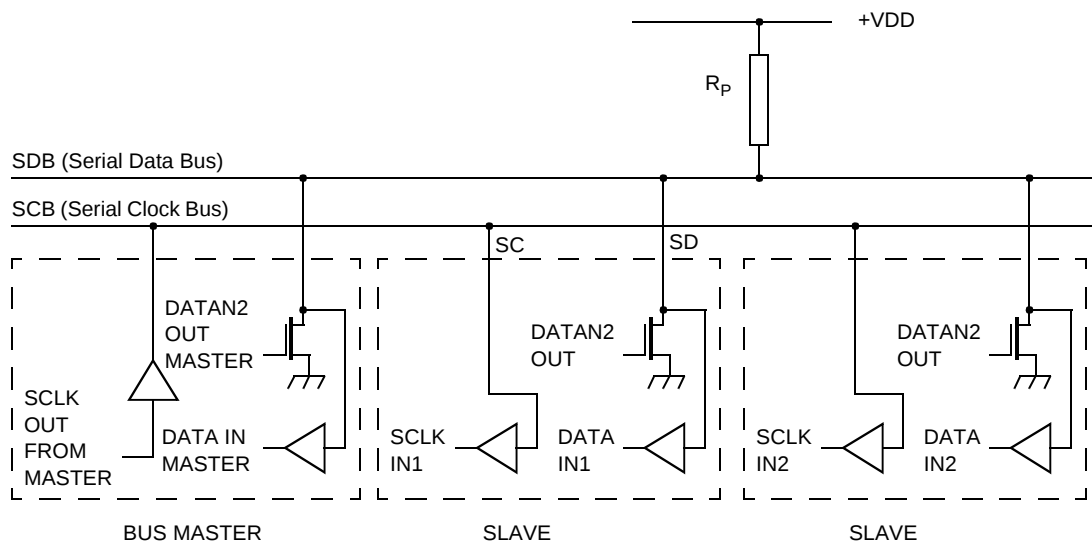


Figure 4: Connection of Devices to the Bus

Electrical Characteristics for Bus Devices

The electrical specifications of the bus devices' inputs and outputs and the characteristics of the bus lines connected to them are shown in **Figure 4**. A pullup resistor (R_P) must be connected to a $5V \pm 10\%$ supply. The CH5001 is a device with input levels related to V_{DD} .

Maximum and minimum values of pullup resistor (R_P)

The value of R_P depends on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices connected (input current + leakage current = I_{input})

The supply voltage limits the minimum value of resistor R_P due to the specified minimum sink current of 3mA at $VOL_{max} = 0.4 V$ for the output stages:

$$R_P \geq (V_{DD} - 0.4) / 3 \quad (R_P \text{ in } k\Omega)$$

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_P due to the specified rise time. The equation for R_P is shown below:

$$R_P \geq 10^3 / C \quad (\text{where: } R_P \text{ is in } k\Omega \text{ and } C, \text{ the total capacitance, is in pF})$$

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μA .

Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_P . The R_P limit depends on V_{DD} and is shown below:

$$R_P \geq (100 \times V_{DD}) / I_{input} \quad (\text{where: } R_P \text{ is in } k\Omega \text{ and } I_{input} \text{ is in } \mu A) \text{ Transfer Protocol}$$

Both read and write cycles can be executed in Alternating and Auto-increment modes. Alternating mode expects a register address prior to each read or write from that location (i.e., transfers alternate between address and data). Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access (i.e., transfers will be address, data, data, data...). A basic serial port transfer protocol is shown in **Figure 5** and described below.

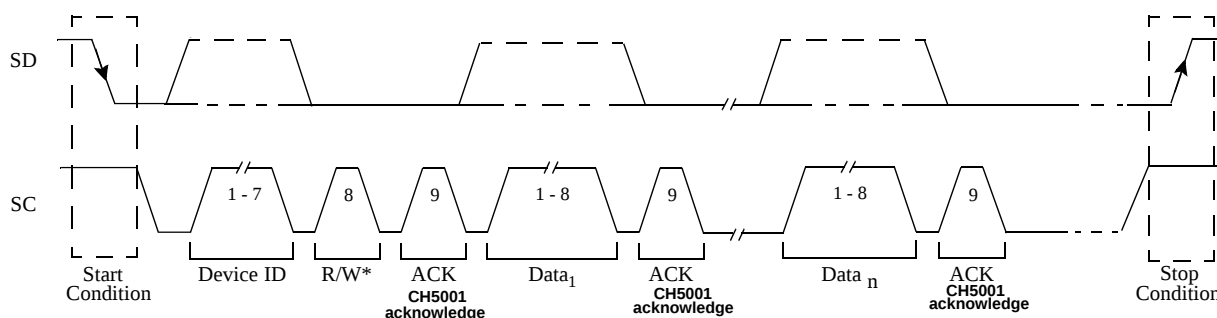


Figure 5: Serial Port Transfer Protocol

1. The transfer sequence is initiated when a high-to-low transition of SD occurs while SC is high; this is the START condition. Transitions of address and data bits can only occur while SC is low.
2. The transfer sequence is terminated when a low-to-high transition of SD occurs while SC is high; this is the STOP condition.
3. Upon receiving the first START condition, the CH5001 expects a Device Address Byte (DAB) from the master device. The value of the device address is shown in the DAB data format below. Note that B[2:1] is determined by the state of the AS pin (see **Table 1** for details).

Table 3. Device Address Byte (DAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	1	AS*	AS	R/W

4. After the DAB is received, the CH5001 expects a Register Address Byte (RAB) from the master. The format of the RAB is shown in the RAB data format below (note that B7 is not used).

R/W

Read/Write Indicator

- 0: Master device will write to the CH5001 at the register location specified by the address AR[5:0]
- 1: Master device will read from the CH5001 at the register location specified by the address AR[5:0]. AutoInc Register Address Auto-Increment - to facilitate sequential R/W of registers 1: Auto-Increment enabled (auto-increment mode).

Table 4. Register Address Byte (RAB)

B7	B6	B5	B4	B3	B2	B1	B0
X	AutoInc	AR[5]	AR[4]	AR[3]	AR[2]	AR[1]	AR[0]

Write: After writing data into a register, the address register will automatically be incremented by one.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the address register will automatically be incremented by one. However, for the first read after an RAB, the address register will not be changed.

0: Auto-increment disabled (alternating mode).

Write: After writing data into a register, the address register will remain unchanged until a new RAB is written.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the address register will remain unchanged.

AR[5:0]

Specifies the Address of the Register to be Accessed.

This register address is loaded into the address register of the CH5001. The R/W* access, which follows, is directed to the register specified by the content stored in the address register.

The following two sections describe the operation of the serial interface for the four combinations of R/W* = 0,1 and AutoInc = 0,1.

CH5001 Write Cycle Protocols (R/W* = 0)

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the mastertransmitter. The mastertransmitter releases the SD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SD line, during the acknowledge clock pulse, so that it remains stable LOW during the HIGH period of the clock pulse. The CH5001 always acknowledges for writes (see **Figure 6**). Note that the resultant state on SD is the wired-AND of data outputs from the transmitter and receiver

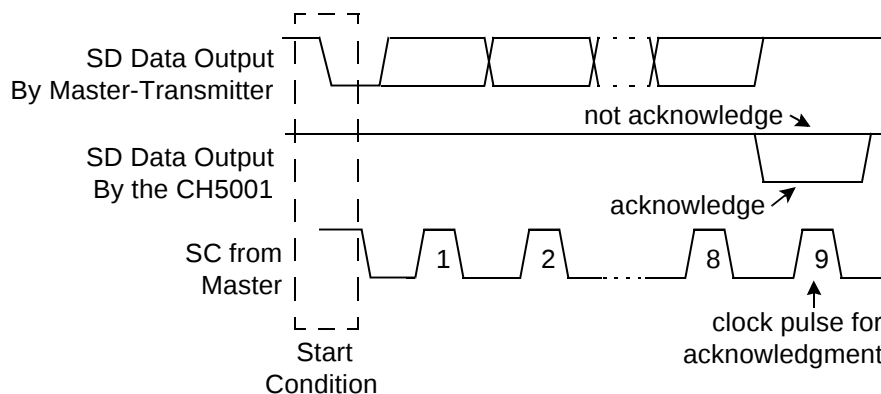


Figure 6: Acknowledge on the Bus

Figure 7 shows two consecutive alternating write cycles for AutoInc = 0 and R/W* = 0. The byte of information following the Register Address Byte (RAB) is the data to be written into the register specified by AR[5:0]. If autoInc = 0, then another RAB is expected from the master device followed by another data byte, and so on.

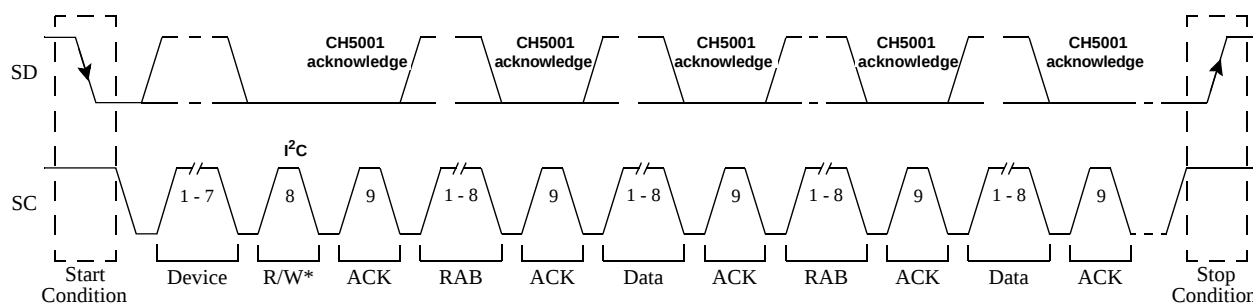


Figure 7: Alternating Write Cycles

Note: The acknowledge is from the CH5001 (slave).

If AutoInc = 1, then the register address pointer will be incremented automatically and subsequent data bytes will be written into successive registers without providing an RAB between each data byte. An auto-increment write cycle is shown in **Figure 8**.

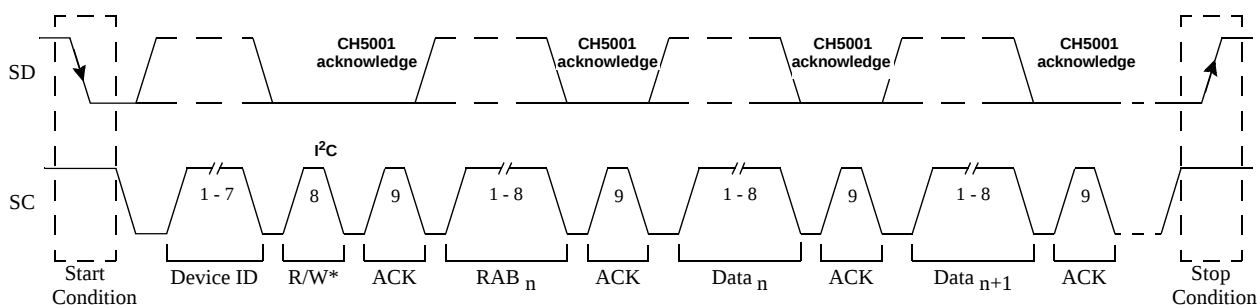


Figure 8: Auto-Increment Write Cycle

Note: The acknowledge is from the CH5001 (slave).

When the auto-increment mode is enabled (AutoInc is set to 1), the register address pointer continues to increment for each write cycle until AR[5:0] = 26 (26 is the address of the address register). The next byte of information represents a new auto-sequencing starting address which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new starting address. The auto-increment sequence can be terminated any time by either a STOP or RESTART condition. The write operation can be terminated with a STOP condition.

CH5001 Read Cycle Protocols (R/W = 1)

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH5001 releases the data line to allow the master to generate the STOP condition or the RESTART condition.

To read the content of the registers, the master device starts by issuing a START condition (or a RESTART condition). The first byte of data, after the START condition, is a DAB with R/W = 0. The second byte is the RAB with AR[5:0] containing the address of the register that the master device intends to read from in AR[5:0]. The master device should then issue a RESTART condition (RESTART = START, without a previous STOP condition). The first byte of data, after this RESTART condition, is another DAB with R/W*=1, indicating the master's intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). If AutoInc = 0, then another RESTART condition, followed by another DAB with R/W* = 0 and RAB, is expected from the master device. The master device then issues another RESTART, followed by another DAB. After

that, the master may read another data byte and so on. In summary, a RESTART condition, followed by a DAB, must be produced by the master before each of the RAB and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 9**.

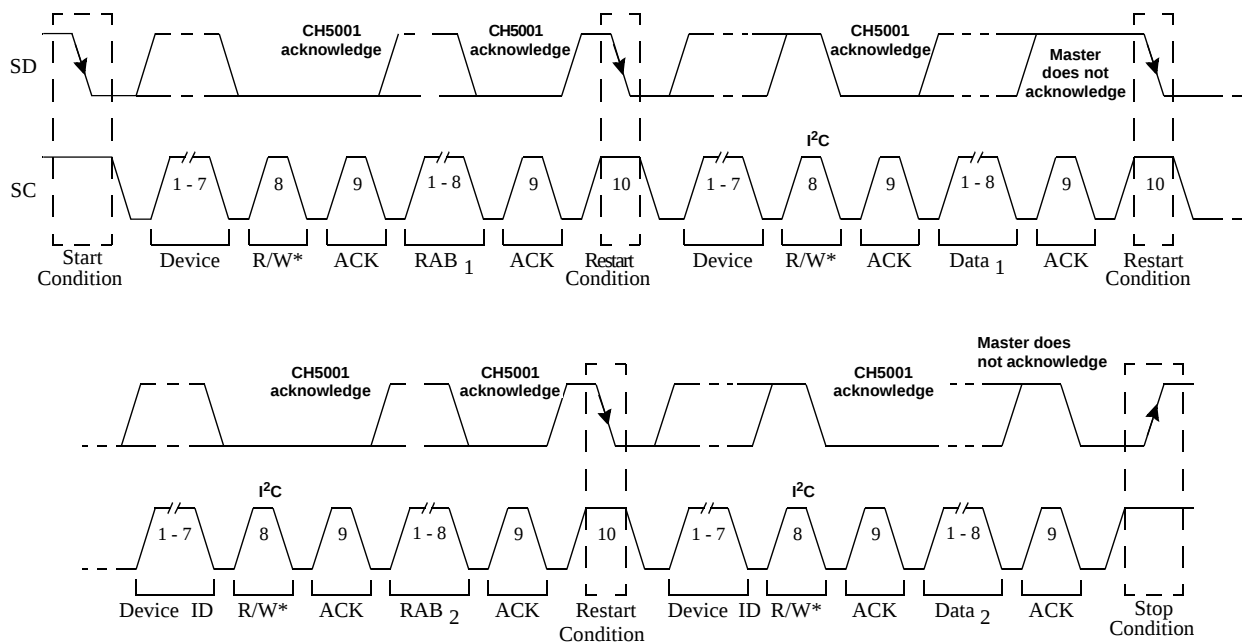


Figure 9: Alternating Read Cycle

If AutoInc = 1, then the address register will be incremented automatically and subsequent data bytes can be read from successive registers, without providing a second RAB

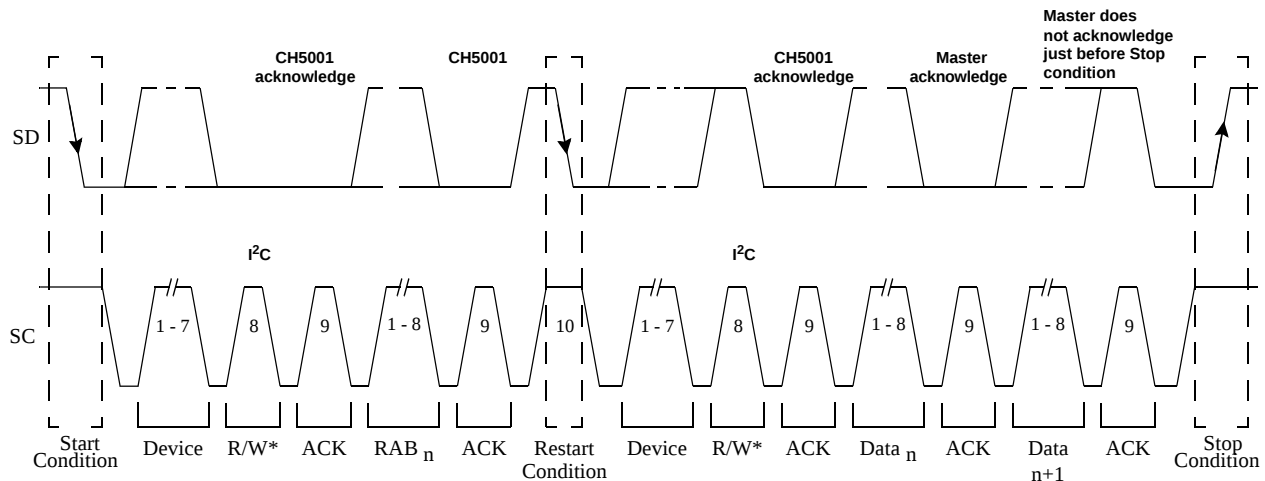


Figure 10: Auto-increment Read Cycle

When the auto-increment mode is enabled (AutoInc is set to 1), the address register will continue incrementing for each read cycle. When the content of the Address Register reaches 2A, it will wrap around and start from 00h again. The auto increment sequence can be terminated by either a STOP or RESTART condition. The read operation can be terminated with a "STOP" condition. **Figure 10** shows an auto-increment read cycle terminated by a STOP or RESTART condition. The CH5001 contains 38 control registers each with a maximum of 8 usable bits to provide access to basic video attribute control functions. These registers are accessible via the 2-bit serial bus (SD & SC). The following sections describe the functions and the controls available through these registers.

Table 5. Register Descriptions

Register	Symbol	Address (Hex)	Default Value	Description
Mode/Output Format	MOF	00	0000 1011	Selects the mode (CCIR601, CIF, or QCIF) and output format.
Frame Rate	FR	01	0010 x000	Sets the frame rate of the output signal. The four MSBs contain the revision number.
Horizontal Start	HS	02	xx11 1101	Sets the horizontal start position of the active output pixel in relationship to the HSYNC signal.
Vertical Start	VS	03	x0x1 0101	Used to set the vertical start position of the active output pixel in relationship to the VSYNC signal.
Electronic Shutter Length High Byte	ESLH	04	1111 0000	Used in conjunction with ESLP register to specify the duration of the electronic shutter.
Electronic Shutter Length Low Byte	ESLL	05	0000 0000	Used in conjunction with ESLL register to specify the duration of the electronic shutter.
Matrix Coefficient 11	CSC11	06	1111 1011	Color Space Converter matrix coefficient for row 1, column 1.
Matrix Coefficient 12	CSC12	07	1100 1100	Color Space Converter matrix coefficient for row 1, column 2.
Matrix Coefficient 13	CSC13	08	1100 1100	Color Space Converter matrix coefficient for row 1, column 3
Matrix Coefficient 14	CSC14	09	1100 0000	Color Space Converter matrix coefficient for row 1, column 4.
Matrix Coefficient 21	CSC21	0A	1100 0000	Color Space Converter matrix coefficient for row 2, column 1.
Matrix Coefficient 22	CSC22	0B	1110 0000	Color Space Converter matrix coefficient for row 2, column 2.
Matrix Coefficient 23	CSC23	0C	1110 0000	Color Space Converter matrix coefficient for row 2, column 3.
Matrix Coefficient 24	CSC24	0D	1100 0000	Color Space Converter matrix coefficient for row 2, column 4.
Matrix Coefficient 31	CSC31	0E	1100 0000	Color Space Converter matrix coefficient for row 3, column 1.
Matrix Coefficient 32	CSC32	0F	1100 0000	Color Space Converter matrix coefficient for row 3, column 2.
Matrix Coefficient 33	CSC33	10	1100 0000	Color Space Converter matrix coefficient for row 3, column 3.
Matrix Coefficient 34	CSC34	11	0010 1000	Color Space Converter matrix coefficient for row 3, column 4.
Red Offset	ROS	12	xxx0 0000	Black balance offset for Red channel.
Green Offset	GOS	13	xxx0 0000	Black balance offset for Green channel.
Blue Offset	BOS	14	xxx0 0000	Black balance offset for Blue channel.

Table 5. Register Descriptions

Register	Symbol	Address (Hex)	Default Value	Description
Cr Gain	CRG	15	1011 1010	Gain applied to the Cr color difference signal.
Cb Gain	CBG	16	1001 0011	Gain applied to the Cb color difference signal.
PSH Gain Gamma	PSHG	17	0001 1001	0-2: Selects the gain of the programmable sample and hold. 4,5: Selects Gamma correction value
Clamp Level	BCLMP	18	1000 0000	Selects the level that the black level clamp adjusts to during dark pixel.
Miscellaneous	MISC	19	1000 1000	7,6,5: Reserved 4: Power Down 3: V Sync. Polarity 2: H Sync. Polarity 1,0: Border Color
Device ID	DID	1A	0010 0000	The four MSBs hold the device ID. The four LSBs hold the version ID.
Test Register	TST	1B	0000 0000	Test Register
Test Memory	TM	1C	0000 0000	Test Register
Auto-Shutter Enable	ASE	1D	1110 0100	Enables and controls the following autoshutter algorithm parameters: 7: Enables the AS to control the shutter 6: Enables the AS to control black level 5: Enables the AS to control programmable gain. 4,3: Reserved 2-0: Determines the threshold of the shutter gain setting to enable black level changes.
Auto-Shutter Window and Input Control Bits	ASW	1E	x100 PUD[3:0]	Used to select the autoshutter window, display window, and select input data to algorithm: 6: Autosshutter max input enable 5: Autosshutter A/D or CSC select 4: Window Display 3-0: Window Select
Auto-Shutter Black Count Threshold Value	ASBC	1F	1111 1001	Determines the threshold that compares the Black Sense value.
Auto-Shutter White Count Threshold Value	ASWC	20	1000 0000	Determines the threshold that compares the White Sense value.
Extended Shutter Bits	ESLE	21	xxx0 0000	ESLE (MSB) along with ESLH and ESLL form the overall Shutter Length Control Register.
Miscellaneous 2	MISC2	22	0001 1001	Determines Master clock frequency, CLKOUT control, and A/D Direct Output mode
Miscellaneous 3	MISC3	23	0011 1001	Determines internal clock delay and A/D full scale value
Power Down Register	PD	24	xxx1 0000	4: ResetB provides software reset 3-0: Reserved.
Address Register	AR	26	0000 0000	Holds the address of the IIC register being accessed

Table 6. Register Map

BIT:	7	6	5	4	3	2	1	0
00	CIF2	ELFA	CVL	CHL	M2	M1	M0	OF
01	RNUM3	RNUM2	RNUM1	RNUM0		FR2	FR1	FR0
02			HS5	HS4	HS3	HS2	HS1	HS0
03		YDEL		VS4	VS3	VS2	VS1	VS0
04	ESLH7	ESLH6	ESLH5	ESLH4	ESLH3	ESLH2	ESLH1	ESLH0
05	ESLL7	ESLL6	ESLL5	ESLL4	ESLL3	ESLL2	ESLL1	ESLL0
06	CSC117	CSC116	CSC115	CSC114	CSC113	CSC112	CSC111	CSC110
07	CSC127	CSC126	CSC125	CSC124	CSC123	CSC122	CSC121	CSC120
08	CSC137	CSC136	CSC135	CSC134	CSC133	CSC132	CSC131	CSC130
09	CSC147	CSC146	CSC145	CSC144	CSC143	CSC142	CSC141	CSC140
0A	CSC217	CSC216	CSC215	CSC214	CSC213	CSC212	CSC211	CSC210
0B	CSC227	CSC226	CSC225	CSC224	CSC223	CSC222	CSC221	CSC220
0C	CSC237	CSC236	CSC235	CSC234	CSC233	CSC232	CSC231	CSC230
0D	CSC247	CSC246	CSC245	CSC244	CSC243	CSC242	CSC241	CSC240
0E	CSC317	CSC316	CSC315	CSC314	CSC313	CSC312	CSC311	CSC310
0F	CSC327	CSC326	CSC325	CSC324	CSC323	CSC322	CSC321	CSC320
10	CSC337	CSC336	CSC335	CSC334	CSC333	CSC332	CSC331	CSC330
11	CSC347	CSC346	CSC345	CSC344	CSC343	CSC342	CSC341	CSC340
12				ROS4	ROS3	ROS2	ROS1	ROS0
13				GOS4	GOS3	GOS2	GOS1	GOS0
14				BOS4	BOS3	BOS2	BOS1	BOS0
15	CRG7	CRG6	CRG5	CRG4	CRG3	CRG2	CRG1	CRG0
16	CBG7	CBG6	CBG5	CBG4	CBG3	CBG2	CBG1	CBG0
17	Reserved	Reserved	GAM1	GAM0	Reserved	PSHG2	PSHG1	PSHG0
18	BCLMP7	BCLMP6	BCLMP5	BCLMP4	BCLMP3	BCLMP2	BCLMP1	BCLMP0
19	Reserved	Reserved	DVDD	PD	VSP	HSP	BDR1	BDR0
1A	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
1B								
1C								
1D	ASSE	ASBE	ASGE	Reserved	Reserved	ASSPD2	ASSPD1	ASSPD0
1E		ASME	ASCSC	ASWD	ASW3	ASW2	ASW1	ASW0
1F	ASBC4	ASBC3	ASBC2	ASBC1	ASBC0	ASBT2	ASBT1	ASBT0
20	ASWC7	ASWC6	ASWC5	ASWC4	ASWC3	ASWC2	ASWC1	ASWC0
21				ESLE4	ESLE3	ESLE2	ESLE1	ESLE0
22	RENB	Reserved	Reserved	Reserved	ADDO	CLKOUTP	DVC	MCF
23	ADFSR	Reserved	Reserved	Reserved	CLKDLY3	CLKDLY2	CLKDLY1	CLKDLY0
24				ResetB	Reserved	PD2	PD1	PD0
26	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Mode / Output Format Register

Symbol: MOF

Address: 00h

Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CIF2	ELFA	CVL	CHL	M2	M1	M0	OF
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	PUD6	1

Register MOF determines the operating mode of the IC, output data format and the chrominance sample location. When bit 0 of register OF is low, data will be output in 16-bit mode. When OF is high, data will be time multiplexed and output on the 8-bit bus Y[7:0]. In the tables below, Y0 is the first pixel generated from the array on a given line, Y1 is the second pixel on that line, etc. In CCIR modes, Y0i, Y1i data are the pixels interpolated between the Y0 and Y1, and Y1 and Y2 samples. For each of the possible modes, the format of the output data is shown below. The total amount of time shown for each table is 24 cycles of MCLK when ELFA=0 and 48 cycles of MCLK when ELFA=1. The line number in each table refers to which active video line is being output.

M[2:0] = 0 or 1, OF = 0, CIF2 = 0 (2 line pattern, CLKOUT = 6.75MHz (ELFA=0) or 3.375MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6
1	Y[7:0]	Y0	Y1	Y2	Y3	Y4	Y5
1	C[7:0]	128	128	128	128	128	128
2	Y[7:0]	Y0	Y1	Y2	Y3	Y4	Y5
2	C[7:0]	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4

M[2:0] = 0 or 1, OF = 1, CIF2 = 0 (2 line pattern, CLKOUT = 13.5 MHz (ELFA=0) or 6.75MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12
1	Y[7:0]	128	Y0	128	Y1	128	Y2	128	Y3	128	Y4	128	Y5
2	Y[7:0]	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cb4	Y4	Cr4	Y5

M[2:0] = 0 or 1, OF = 0, CIF2 = 1 (1 line pattern, CLKOUT = 6.75MHz (ELFA=0) or 3.375MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6
1	Y[7:0]	Y0	Y1	Y2	Y3	Y4	Y5
1	C[7:0]	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
2	Y[7:0]	Y0	Y1	Y2	Y3	Y4	Y5
2	C[7:0]	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4

M[2:0] = 0 or 1, OF = 1, CIF2 = 1 (1 line pattern, CLKOUT = 13.5 MHz (ELFA=0) or 6.75MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12
1	Y[7:0]	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cb4	Y4	Cr4	Y5
2	Y[7:0]	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cb4	Y4	Cr4	Y5

M[2:0]2 or 3, OF = 0 CIF2 = 0 (4 line pattern, CLKOUT = 6.75MHz (ELFA=0) or 3.375MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6
1	Y[7:0]	Y0	Y0	Y2	Y2	Y4	Y4
1	C[7:0]	128	128	128	128	128	128
2	Y[7:0]	16	16	16	16	16	16
2	C[7:0]	128	128	128	128	128	128
3	Y[7:0]	Y0	Y0	Y2	Y2	Y4	Y4
3	C[7:0]	Cb0	Cb0	Cr0	Cr0	Cb4	Cb4
4	Y[7:0]	16	16	16	16	16	16
4	C[7:0]	128	128	128	128	128	128

M[2:0] = 2 or 3, OF = 1 CIF2 = 0 (4 line pattern, CLKOUT = 13.5 MHz (ELFA=0) or 6.75MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12
1	Y[7:0]	128	128	Y0	Y0	128	128	Y2	Y2	128	128	Y4	Y4
2	Y[7:0]	128	128	16	16	128	128	16	16	128	128	16	16
3	Y[7:0]	Cb0	Cb0	Y0	Y0	Cr0	Cr0	Y2	Y2	Cb4	Cb4	Y4	Y4
4	Y[7:0]	128	128	16	16	128	128	16	16	128	128	16	16

M[2:0] = 2 or 3, OF = 0 CIF2 = 1 (2 line pattern, CLKOUT = 6.75MHz (ELFA=0) or 3.375MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12
1	Y[7:0]	Y0	Y0	Y2	Y2	Y4	Y4						
1	C[7:0]	Cb0	Cb0	Cr0	Cr0	Cb4	Cb4						
2	Y[7:0]	16	16	16	16	16	16						
2	C[7:0]	128	128	128	128	128	128						
3	Y[7:0]	Y0	Y0	Y2	Y2	Y4	Y4						
3	C[7:0]	Cb0	Cb0	Cr0	Cr0	Cb4	Cb4						
4	Y[7:0]	16	16	16	16	16	16						
4	C[7:0]	128	128	128	128	128	128						

M[2:0] = 2 or 3, OF = 1 CIF2 = 1 (2 line pattern, CLKOUT = 13.5 MHz (ELFA=0) or 6.75MHz (ELFA=1))

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12
1	Y[7:0]	Cb0	Cb0	Y0	Y0	Cr0	Cr0	Y2	Y2	Cb4	Cb4	Y4	Y4
2	Y[7:0]	128	128	16	16	128	128	16	16	128	128	16	16
3	Y[7:0]	Cb0	Cb0	Y0	Y0	Cr0	Cr0	Y2	Y2	Cb4	Cb4	Y4	Y4
4	Y[7:0]	128	128	16	16	128	128	16	16	128	128	16	16

M[2:0] = 4 or 5, OF = 0 (repeats pattern every line, CLKOUT =13.5 MHz)

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12
1	Y[7:0]	Y0	Y0i	Y1	Y1i	Y2	Y2i	Y3	Y3i	Y4	Y4i	Y5	Y5i
1	C[7:0]	Cb0	Cr0	Cb1	Cr1	Cb2	Cr2	Cb3	Cr3	Cb4	Cr4	Cb5	Cr5

M[2:0] = 4 or 5, OF = 1 (repeats pattern every line, CLKOUT = 27MHz)

Line	CLKOUT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	Y[7:0]	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y	C	Y
		b	0	r	0	b	1	r	1	b	2	r	2	b	3	r	3	b	4	r	4	b	5	r	5
		0		0	i	1		1	i	2		2	i	3		3	i	4		4	i	5		5	i

Bits 1 through 3 of the MOF register along with ELFA, bit 6 select the mode that the IC operates according to the table below. A listing of 'FR' in a column indicates that the frame rate is adjusted through varying this parameter, and the table under the Frame Rate register should be used to determine this value. When modes 4 or 5 are selected, the value of the FR register is ignored, and the IC will output a frame rate compatible with the field rate of PAL or NTSC. An integer number of lines will be output in each frame, with the odd frames having one line more than the even frames.

Table 7. Operating Modes

ELFA	M2	M1	M0	Operating Mode	Y Active Pixels /Line	Y Active Lines	CrCb Active Pixels /Line	CrCb Active Lines	Total MCLK / Line	Total Lines/ Frame	Functional Description
0	0	0	1	CIF	352	288	176	144	1716	FR	CIF Progressive scan
0	0	1	1	QCIF	176	144	88	72	1716	FR	QCIF Progressive scan
x	1	0	0	CCIR601	704	240	352	240	1716	263/ 262	525 Line scan 4:2:2
x	1	0	1	CCIR601	704	288	352	288	1728	313/ 312	625 Line scan 4:2:2
x	1	1	0	Reserved							
x	1	1	1	Reserved							
1	0	0	1	CIF 2	352	288	176	144	FR	289	CIF-289 Progressive scan
1	0	1	1	QCIF 2	176	144	88	72	FR	289	QCIF-298 Progressive scan

Bits 4, 5 and 7 'CHL' 'CVL' 'CIF2' of the MOF register specify the chrominance sample location with respect to the luminance samples in the horizontal and vertical directions respectfully. When CHL is 0, chrominance samples are located between the luminance samples in the horizontal direction. When CHL is 1, chrominance samples are aligned with alternate luminance samples. When CIF2 is 0 and CVL is 0, chrominance samples are located between the luminance samples in the vertical direction. When CIF2 is 0 and CVL is 1, chrominance samples are aligned with alternate luminance samples. When M[2:0] is set to mode 5, the CHL and CVL bits are ignored. When the CIF2 bit is high, the CVL bit is ignored, and the chrominance signal is output on every line that has luminance.

Frame Rate Register

Symbol:FR
Address:01h
Bits:3

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	RNUM3	RNUM2	RNUM1	RNUM0		FR2	FR1	FR0
TYPE:	R	R	R	R		R/W	R/W	R/W
DEFAULT:	0	0	1	0		0	0	0

Register FR determines the frame rate. The frame rate is adjusted by increasing the number of blank lines after reading the entire array, or by inserting extra blank pixels at the end of each line readout. The method of frame rate control is determined by bit ELFA in register MOF. When ELFA = 0, the amount of delay between the completion of reading one frame and the start of reading the next frame is varied. There are eight frame rates that can be selected in this mode, each one a fixed integer number of lines long. When ELFA = 1, the amount of delay between the completion of reading one line, and the start of reading the next line is varied. There are seven frame rates that can be selected in this mode, each one 289 lines.

In modes M[2:0] equal to 0-3, the device can operate with a 24MHz MCLK or a 27MHz MCLK. Descriptions of some of the key parameters are shown in **Table 8** and **Table 9**.

Table 8. Operating Modes For 27 MHz MCLK

ELFA	M [2:0]	FR [2:0]	Total Lines	Blank Lines / Frame	MCLK / Line	Blank MCLK / Line	Frame Rate (Hz)	Max Shutter Length (register value)	Max Shutter Time (mS)
0	1,3	0 0 0	525	236	1716	308	30	112,398	33
0	1,3	0 0 1	656	367	1716	308	24	140,497	42
0	1,3	0 1 0	787	498	1716	308	20	168,597	50
0	1,3	0 1 1	1049	760	1716	308	15	224,796	67
0	1,3	1 0 0	1312	1023	1716	308	12	281,209	83
0	1,3	1 0 1	1967	1678	1716	308	8	421,707	125
0	1,3	1 1 0	3934	3645	1716	308	4	843,628	250
0	1,3	1 1 1	15735	15446	1716	308	1	2,097,151	621
x	4	x	263 / 262	23 / 22	1716		60	55,984	17
x	5	x	313 / 312	25 / 24	1728		50	67,176	20
1	1,3	0 0 1	289		3896	1080	24	140,256	42
1	1,3	0 1 0	289		4672	1856	20	168,192	50
1	1,3	0 1 1	289		6232	3416	15	224,352	66
1	1,3	1 0 0	289		7784	4968	12	280,224	83
1	1,3	1 0 1	289		11680	8864	8	420,480	125
1	1,3	1 1 0	289		23360	20544	4	840,960	249
1	1,3	1 1 1	289		93424	90608	1	2,097,151	621

Table 9. Operating modes for 24 MHz MCLK

ELFA	M [2:0]	FR [2:0]	Total Lines	Blank Lines / Frame	MCLK / Line	Blank MCLK / Line	Frame Rate (Hz)	Max Shutter Length (register value)	Max Shutter Time (mS)
0	1,3	0 0 0	467	178	1716	308	30	99,957	33
0	1,3	0 0 1	583	294	1716	308	24	124,839	42
0	1,3	0 1 0	700	411	1716	308	20	149,935	50
0	1,3	0 1 1	933	644	1716	308	15	199,914	67
0	1,3	1 0 0	1166	877	1716	308	12	249,892	83
0	1,3	1 0 1	1749	1460	1716	308	8	374,946	125
0	1,3	1 1 0	3497	3208	1716	308	4	749,892	250
0	1,3	1 1 1	13987	13698	1716	308	1	2,097,151	699
1	1,3	0 0 1	289		3464	648	24	124,704	42
1	1,3	0 1 0	289		4152	1336	20	149,472	50
1	1,3	0 1 1	289		5536	2720	15	199,296	66
1	1,3	1 0 0	289		6920	4104	12	249,120	83
1	1,3	1 0 1	289		10384	7568	8	373,824	125
1	1,3	1 1 0	289		20760	17944	4	747,360	249
1	1,3	1 1 1	289		83048	80232	1	2,097,151	699

Bits 7-4 (RNUM#) of the FR register contain the revision number of the CH5001 device. These bits are read only. When using ELFA=1, if 30 Hz frame rate is desired a 30MHz crystal should be used, and the 24MHz MCLK control (MCE=0) should be selected. All frame rates will be scaled by the value of 30/24.

Horizontal Start Register

Symbol: HS
Address:02h
Bits:6

BIT:	7	6	5	4	3	2	1	0
SYMBOL:			HS5	HS4	HS3	HS2	HS1	HS0
TYPE:			R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:			1	1	1	1	0	1

Register HS determines the number of pixels between the leading edge of H Sync and the first active pixel to be output on the Y[7:0] and C[7:0] pins. The number is in units of pixels; the range is from 0 to 63 CLKOUT and must be limited to 38 when ELFA=1. When M[2:0] = 4 or 5, this register is ignored and the timing below is followed assuming 16-bit output mode. Values are doubled for 8-bit output mode

M[2:0]	Leading Edge of -> H Sync	H Delay (CLKOUT)	Border (CLKOUT)	Active (CLKOUT)	Border (CLKOUT)	Blank (CLKOUT)	Total (CLKOUT)
4 - NTSC		122	8	704	8	16	858
5 - PAL		132	8	704	8	12	864

Vertical Start Register

Symbol:VS
Address:03h
Bits:6

BIT:	7	6	5	4	3	2	1	0
SYMBOL:		YDEL		VS4	VS3	VS2	VS1	VS0
TYPE:		R/W		R/W	R/W	R/W	R/W	R/W
DEFAULT:		0		1	0	1	0	1

Register VS determines the number of lines between the leading edge of V Sync and the first active line to be output on the Y[7:0] and C[7:0] pins. The number is in units of lines; the range is 0 to 31 lines. When ELFA = 1, this register is ignored, and there is always a one line delay between the leading edge of vertical sync and the first line with active video.

The YDEL (bit 6) controls the delay in the luma processing path. The value should match the setting of CHL.

Electronic Shutter Length High Byte

Symbol:ESLH
Address:04h
Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	ESLH7	ESLH6	ESLH5	ESLH4	ESLH3	ESLH2	ESLH1	ESLH0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	0	0	0	0

The ESLH register, combined with the ESLE and ESLL registers determine the length of the electronic shutter.

Electronic Shutter Length Low Byte

Symbol:ESLL
Address:05h
Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	ESLL7	ESLL6	ESLL5	ESLL4	ESLL3	ESLL2	ESLL1	ESLL0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Registers ESLE, ESLH and ESLL specify the duration of the electronic shutter. These 21 bits are concatenated into a single 21-bit word ({ESLE,ESLH,ESLL}) whose value is multiplied by 8. The shutter is enabled for this number of MCLKs. The duration of the shutter can, therefore, be determined from the equation $(8 \cdot (65536 \cdot \text{ESLE} + 256 \cdot \text{ESLH} + \text{ESLL})) / \text{MCLK}$. The range is from 0mS to 699mS, but is limited to a lower value in some frame rates (see Frame Rate Register description). When the autoshutter algorithm is controlling the shutter value and this register is read out, the autoshutter generated value is read instead of the actual IIC register content.

Matrix Coefficient Registers

Symbol:CSC11-CSC34

Address:06h-11h

Bits:8 each

BITS:	7	6	5	4	3	2	1	0
SYMBOL:	CSC##7	CSC##6	CSC##5	CSC##4	CSC##3	CSC##2	CSC##1	CSC##0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:								

Registers CSC11, CSC12, CSC13, CSC14, CSC21, CSC22, CSC23, CSC24, CSC31, CSC32, CSC33 and CSC34 specify the color space conversion matrix values used to convert from the color space of the filters to the RGB domain dictated by television phosphors. The values are 2's complement and 64 will be added to each value internally to make the range of possible values -64 to +191. There is a second set of fixed matrix multiplier coefficient values that can be multiplexed with the register values under the control of the MONO pin. The matrix multiplication equation, default register values and second set of register values are shown below:

Output		Matrix Coefficient Register					Input
R		06H	07H	08H	09H		Pr
G	=	0AH	0BH	0CH	0DH	*	Pg1
B		0EH	0FH	10H	11H		Pg2 Pb

Table 10. Register Values for Color Space Conversion Matrix

Register (H)	Default Value		'MONO' Multiplexed Value	
	Decimal	Binary	Decimal	Binary
06	-5	1111 1011	-48	1101 0000
07	-52	1100 1100	-48	1101 0000
08	-52	1100 1100	-48	1101 0000
09	-64	1100 0000	-48	1101 0000
0A	-64	1100 0000	-48	1101 0000
0B	-32	1110 0000	-48	1101 0000
0C	-32	1110 0000	-48	1101 0000
0D	-64	1100 0000	-48	1101 0000
0E	-64	1100 0000	-48	1101 0000
0F	-64	1100 0000	-48	1101 0000
10	-64	1100 0000	-48	1101 0000
11	40	0010 1000	-48	1101 0000

Red Offset Register

Symbol:ROS

Address:12h

Bits:5

BITS:	7	6	5	4	3	2	1	0
SYMBOL:				ROS4	ROS3	ROS2	ROS1	ROS0
TYPE:				R/W	R/W	R/W	R/W	R/W
DEFAULT:				0	0	0	0	0

Register ROS specifies the offset given to the red channel after color space conversion. The value is a 2's complement number in the range of -16 to +15. After adjustments to the matrix multiplier coefficients have been made, this value can be used to perform a black balance adjustment.

Green Offset Register**Symbol:GOS****Address:13h****Bits:5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:				GOS4	GOS3	GOS2	GOS1	GOS0
TYPE:				R/W	R/W	R/W	R/W	R/W
DEFAULT:				0	0	0	0	0

Register GOS specifies the offset given to the green channel after color space conversion. The value is a 2's complement number in the range of -16 to +15. After adjustments to the matrix multiplier coefficients have been made, this value can be used to perform a black balance adjustment.

Blue Offset Register**Symbolist****Address:14h****Bits:5**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:				BOS4	BOS3	BOS2	BOS1	BOS0
TYPE:				R/W	R/W	R/W	R/W	R/W
DEFAULT:				0	0	0	0	0

Register BOS specifies the offset given to the blue channel after color space conversion. The value is a 2's complement number in the range of -16 to +15. After adjustments to the matrix multiplier coefficients have been made, this value can be used to perform a black balance adjustment.

Cr Gain Register**Symbol:CRG****Address:15h****Bits:8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CRG7	CRG6	CRG5	CRG4	CRG3	CRG2	CRG1	CRG0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	1	1	0	1	0

Register CRG specifies the gain given to the Cr channel after color space conversion. The nominal value is 186.

Cb Gain Register**Symbol:CBG****Address:16h****Bits:8**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CBG7	CBG6	CBG5	CBG4	CBG3	CBG2	CBG1	CBG0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	1	0	0	1	1

Register CBG specifies the gain given to the Cb channel after color space conversion. The nominal gain is 147.

Programmable Sample and Hold Gain Register

Symbol: PSHG

Address: 17h

Bits: 8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	GAM1	GAM0	Reserved	PSHG2	PSHG1	PSHG0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	0	0	1

Register PSHG specifies the gain of the programmable sample and hold before A/D conversion. There are eight gain settings ranging from a gain of 1.5x to a gain of 5.0x. When the autoshutter algorithm is controlling the gain value and this register is read out, the autoshutter generated gain value is read instead of the actual IIC register content.

Bits 5 and 4 (GAM[1:0]) control the gamma correction used, according to **Table 11**.

Table 11. Gamma Correction

GAM1	GAM0	Gamma
0	0	1.0
0	1	1.6
1	0	2.2
1	1	2.2

Clamp Level Register

Symbol: BCLMP

Address: 18h

Bits: 5

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BCLMP7	BCLMP6	BCLMP5	BCLMP4	BCLMP3	BCLMP2	BCLMP1	BCLMP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

Register BCLMP specifies the offset level used in the black level clamp block.

A value of 0 in register BCLMP will nominally cause the A/D to output a value of zero for a dark cell input. The register value is 2's complement and ranges from -128 at maximum brightness to +127 at minimum brightness. This register has no effect when the ASBE bit is HIGH (default).

Miscellaneous Register

Symbol: MISC

Address: 19h

Bits: 7

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	PD	VSP	HSP	BDR1	BDR0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	PUD4*	0	0	0	0

Bits 0 and 1 of the MISC register control the border color that is output on each line containing active video for eight 13.5MHz clocks before the start of active video and eight 13.5MHz clocks after active video. This is only done when the IC is placed into display modes four or five (M[2:0] = 4,5). In these modes, the luminance data has been interpolated to a pixel rate of 13.5MHz. Therefore, 8 pixels equals 592.5nS. The border colors are described in **Table 12**.

Table 12. Border Colors

BDR 1	BDR 0	Color	Y Value	CR Value	CB Value
0	0	Black	16	128	128
0	1	Blue	40	110	240
1	0	Green	144	33	53
1	1	White	235	128	128

Bits 2 and 3 (HSP and VSP) of the MISC register control the polarity of the H and V sync signals.

Bit 4 (PD) of the MISC register places the IC in a power down mode. When PD=0, clocks to all digital circuitry are disabled and analog circuitry bias currents are shut down. When PD=1, the IC is placed in its normal operating mode according to the user inputs. The default value of this bit is set using the PUD4 input.

Device ID Register

Symbol:DID
Address:1Ah
Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	1	0	0	0	0	0

Register DID is a read only register which holds the device ID number of the CH5001.

Test Register

Symbol:TST
Address:1Bh
Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	LM Done	LS Select	LM Test	IOC1	IOC0	CSH2	CSH1	CSH0
TYPE:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

TST is a test register.

Test Memory Register

Symbol:TM
Address:1Ch
Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

TM is a test register.

Auto-Shutter Enable

Symbol:ASE

Address:1Dh

Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	ASSE	ASBE	ASGE	Reserved	Reserved	ASSPD2	ASSPD1	ASSPD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	1	0	0

Bits 0-2 of the ASE register control the speed of the auto-shutter loop. Values of 0-4 are valid.

Bits 3-4 of the ASE register are reserved, and should be left at their default value.

Bit 5 of the ASE register enables the autoshutter algorithm to adjust the gain of the programmable sample and hold. A 1 in this location allows the autoshutter algorithm to control this gain. A zero in this location disables the autoshutter algorithm from controlling this value, and allows bits 2-0 of register PSHG (17H) to control the gain.

Bit 6 of the ASE register enables the autoshutter algorithm to adjust the black level (bias) of the readout signal prior to A/D conversion. A 1 in this location allows the autoshutter algorithm to control the black level. A 0 in this location disables the autoshutter algorithm from controlling this value and allows bits 7-0 of register BCLMP (18H) to control the black level.

Bit 7 of the ASE register enables the autoshutter algorithm to adjust the shutter duration. A 1 in this location allows the autoshutter algorithm to control the shutter. A zero in this location disables the autoshutter algorithm from controlling this value and allows registers ESLE, ESLH and ESLL to control the shutter duration.

Auto-Shutter Window / Input Control

Symbol:ASW

Address:1Eh

Bits:7

BIT:	7	6	5	4	3	2	1	0
SYMBOL:		ASME	ASCSC	ASWD	ASW3	ASW2	ASW1	ASW0
TYPE:		R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:		1	0	0	PUD3*	PUD2*	PUD1*	PUD0*

Bits 0, 1, 2 and 3 of the ASW register determine the active window that is used to operate the autoshutter algorithm. There are 16 possible windows, which are shown in **Figure 11**. The default value of these bits can be set using the PUD [3:0] inputs. This allows the backlight compensation window to be set without using IIC control.

Bit 4 of the ASW register enables the selected window to be highlighted in the image which is output from the CH5001. All image outside of the window will be reduced in amplitude.

Bits 5 and 6 of the ASW register determine which data is input to the autoshutter algorithm, according to **Table 13**.

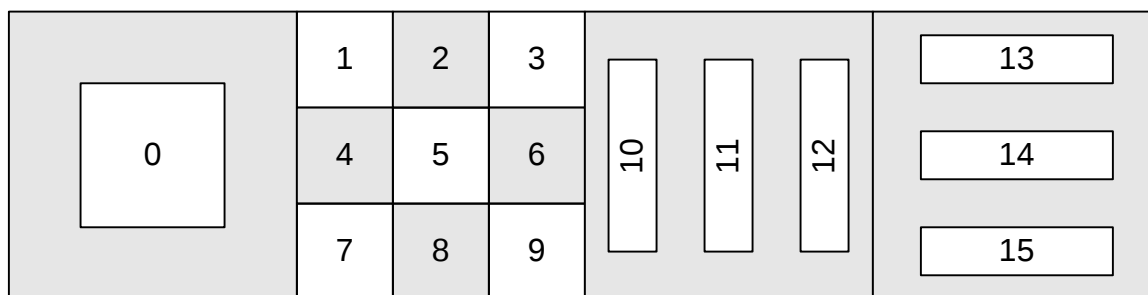


Figure 11: ASW Register Possible Windows

Table 13. Autoshutter Algorithm Input

ASME	ASCSC	Input to Autoshutter Algorithm
0	0	'Y[7:0]' output of color space conversion
0	1	A/D output
1	x	MAX (A/D, Y[7:0])

Auto-Shutter Black Count Threshold

Symbol:ASBC
Address:1Fh
Bits:8

BITS:	7	6	5	4	3	2	1	0
SYMBOL:	ASBC4	ASBC3	ASBC2	ASBC1	ASBC0	ASBT2	ASBT1	ASBT0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	1	0	0	1

Bits 2-0 of register ASBC determine the black threshold used by the auto-shutter algorithm. The value used is $8 \cdot \text{ASBT} + 3$. Bits 7-3 of register ASBC determine the number of pixels below the ASBT level. When the number of pixels is less than this value, the autoshutter algorithm will adjust the black level downwards. When the number of pixels is greater than this value, the black level will be adjusted upwards.

Auto-Shutter White Count Threshold

Symbol:ASWC
Address:20h
Bits:8

BITS:	7	6	5	4	3	2	1	0
SYMBOL:	ASWC7	ASWC6	ASWC5	ASWC4	ASWC3	ASWC2	ASWC1	ASWC0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

The number of pixels above the white level is compared to the ASWC value to determine the direction that the shutter value should be changed.

Electronic Shutter Length Extended Value

Symbol: ESLE
Address:21h
Bits:5

BITS:	7	6	5	4	3	2	1	0
SYMBOL:				ESLE4	ESLE3	ESLE2	ESLE1	ESLE0
TYPE:				R/W	R/W	R/W	R/W	R/W
DEFAULT:				0	0	0	0	0

The ESLE register, combined with the ESLH and ESLL registers, determine the length of the electronic shutter.

Miscellaneous Register 2**Symbol:**MISC2**Address:**22h**Bits:**7

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	RENB	Reserved	Reserved	Reserved	ADDO	CLKOUTP	DVC	MCF
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	PUD5*	0	0	1

Bit 0 (Master Clock Frequency) of register MISC2 refers to the CH5001 the master clock (XO) frequency. A 0 should be written to this location when the master clock is 24MHz. A 1 should be written to this location when the master clock is 27MHz. When modes four or five are selected (M[2:0] =4,5), the master clock must be 27MHz.

Bit 1 (Data Valid Control) of register MISC2 selects whether or not the CLKOUT signal is gated. When this bit is a 0, the CLKOUT pin will produce a continuous clock output signal. When bit DVC is a 1, the CLKOUT will be gated, and will be active when active data is being output from the CH5001, and inactive when non-active data is present at the outputs.

Bit 2 (CLKOUT Polarity) of register MISC2 selects the polarity of the CLKOUT signal. A 0 in this location means output data has been latched with the positive edge of the CLKOUT signal. A 1 in this location means output data has been latched with the negative edge of the CLKOUT signal.

Bit 3 (A/D Direct Output) of register MISC2 selects whether the output signal is directly from the A/D converter or after the datapath postprocessing. In both cases, the relationship between the Hsync, Vsync and active video will remain the same. When a 1 is written to this location, the Y[7:0] and C[7:0] will output luma and chroma data from the datapath circuitry. When a 0 is written to this location, the Y[7:0] pins will contain the A/D data directly. With no postprocessing and the C[7:0] outputs will be set to 128. If 8-bit output mode is selected, the A/D output will be multiplexed with the decimal value 128 to enable connection to an 8-bit video encoder resulting in a black and white image.

Bits 4-6 of Register MISC2 are reserved.

Bit 7 (Refresh Enable) enables memory refresh.

Miscellaneous Register 3**Symbol:**MISC3**Address:**23h**Bits:**6

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	ADFSR	Reserved	Reserved	Reserved	CKDLY3	CKDLY2	CKDLY1	CKDLY0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	1	0	0	1

Bits 0-3 (Clock Delay) of register MISC3 determine the clock delay between internal clock signals. The recommended value is 9.

Bit 7 (A/D Full Scale Range) of register MISC3 changes the full scale range of the A/D converter. A 0 in this location sets the A/D full scale range at ± 1 volt. A 1 in this location sets the A/D full scale range at ± 0.25 volt. This bit can be combined with the PSHG[2:0] to form a 4-bit control.

Power Down Register

Symbol:PD
Address:24h
Bits:3

BIT:	7	6	5	4	3	2	1	0
SYMBOL:				ResetB	Reserved	Reserved	Reserved	Reserved
TYPE:				R/W	R/W	R/W	R/W	R/W
DEFAULT:				1	0	0	0	0

Bits 3-0 of register PD are reserved.

Bit 4 of register PD is used to perform a software reset on the device. It is logically AND'd with the power on reset signal. The output of this AND'ing will be used to reset all circuitry in the CH5001, except for the ResetB bit itself and the IIC state machines. ResetB and the IIC state machines are reset by the power on reset signal only.

Address Register

Symbol:AR
Address:26h
Bits:8

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

Register AR is the CH5001 address register, which holds the address of the register currently being accessed.

Electrical Specifications**Table 14. Absolute Maximum Ratings**

Symbol	Description	Min	Typ	Max	Units
	V _{DD} relative to GND	- 0.5		7.0	V
	Input voltage of all digital pins ¹	GND - 0.5		V _{DD} + 0.5	V
T _{STOR}	Storage temperature	- 65		100	° C
T _J	Junction temperature			150	° C
T _{VPS}	Vapor phase soldering (one minute)			220	° C

Notes:

- 1 Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2 The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latch.

Table 15. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
DV _{DD}	Digital supply voltage	4.75	5.00	5.25	V
AV _{DD}	Analog supply voltage	4.75	5.00	5.25	V
T _A	Ambient operating temperature	0	25	40	C

Table 16. Digital Inputs/Outputs

Symbol	Description	Test Condition @TA= 25° C	Min	Typ	Max	Unit
V _{oh}	Output high voltage	I _{oh} = .400 mA	2.8			V
V _{ol}	Output low voltage	I _{ol} = 3.2 mA			0.4	V
V _{ih}	Input high voltage		3.4		V _{DD}	V
V _{il}	Input low voltage		GND		0.8	V
I _{lk}	Input leakage current		-10		10	μA

Table 17. Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
t _{VSW}	Vertical sync pulse width		2		Lines
t _{HSW}	Horizontal sync pulse width		64		MCLK
t _{HD}	Horizontal and vertical sync delay from clock	2		10	nS
t _P	CLKOUT period (varies with mode and output format)	37		148.2	nS
t _{PH}	CLKOUT high time	14.8		89	nS
t _{PL}	CLKOUT low time	14.8		89	nS
t _{SP}	CLKOUT to pixel data setup time	2			ns
t _{HP}	CLKOUT to pixel data hold time	2			ns

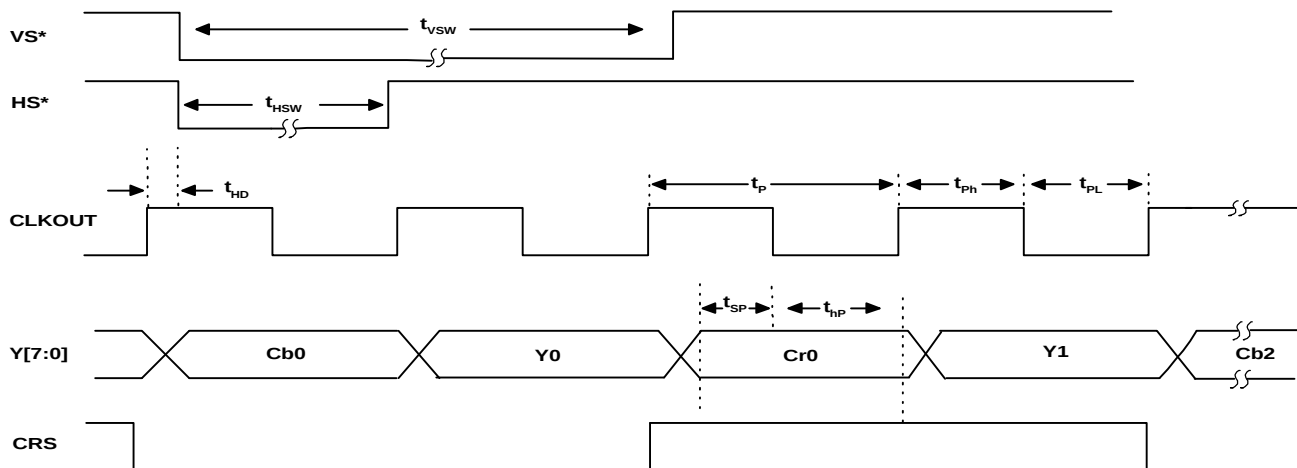


Figure 12: Timing Diagram (M[2:0] = 1, OF = 1, H Start = 0)

Note: The output pixel Cb0 will be delayed by 2 times the value of the HStart register CLKOUT cycles, if HStart is non-zero.

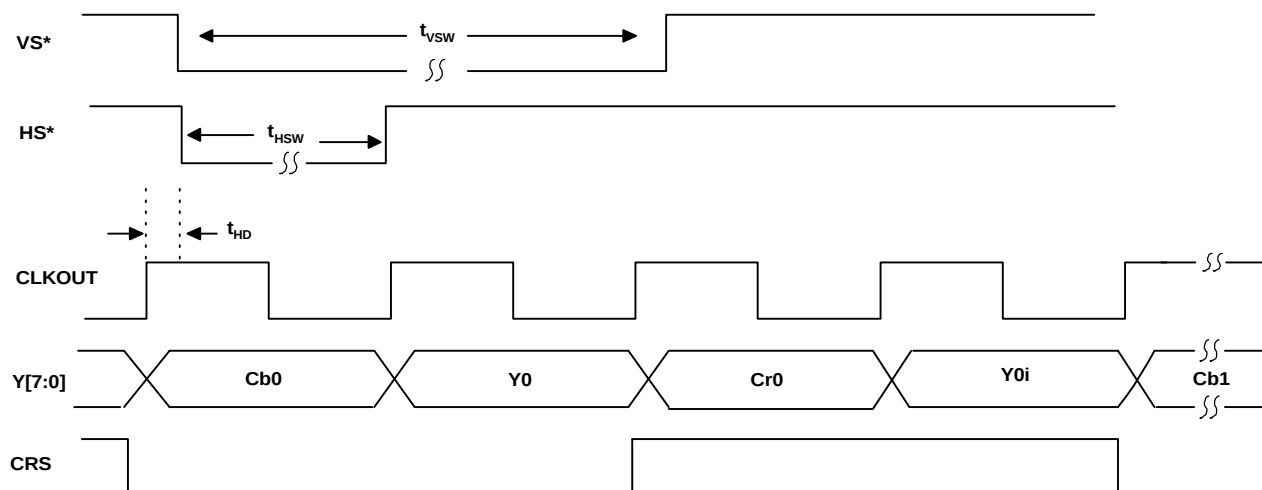


Figure 13: Timing Diagrams ($M[2:0] = 1$, $OF = 0$, $HStart = 0$)

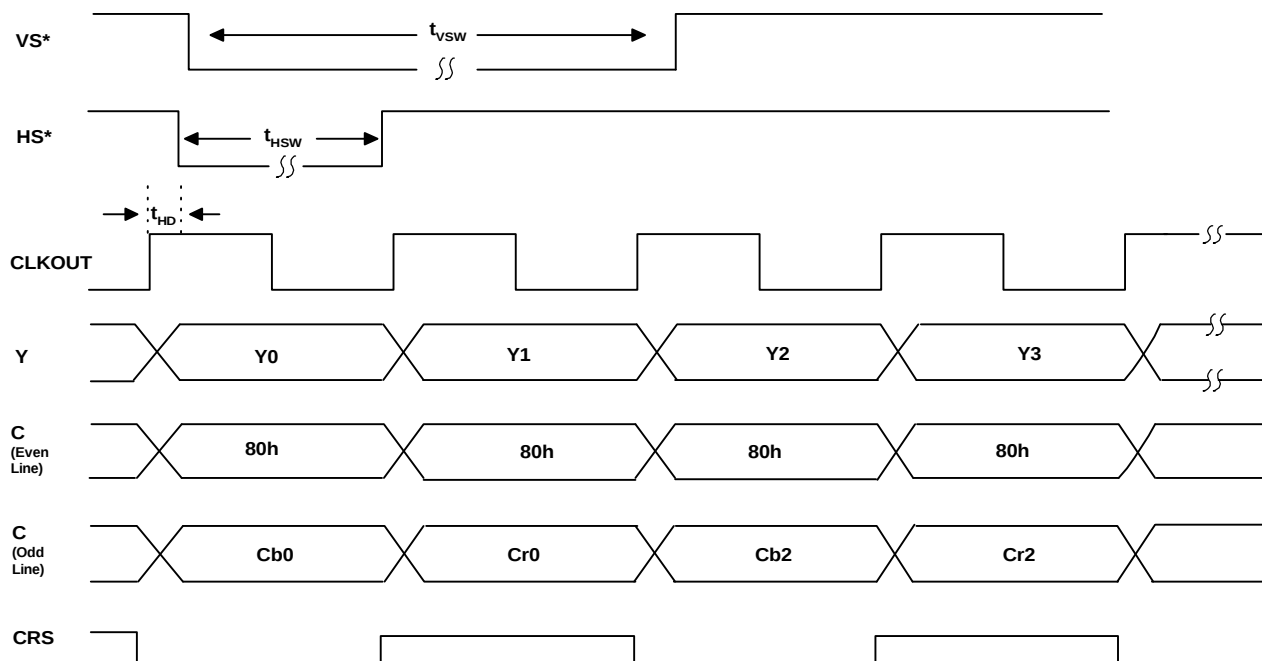


Figure 14: Timing Diagram ($M[2:0] = 4$ or 5 , $OF = 1$)

Note: See the HStart register description for the relationship between HS* and the first active data (Cb0)

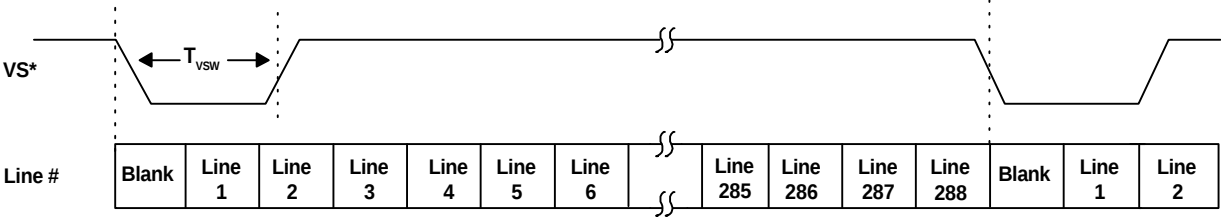


Figure 15: Vertical Sync to Video Timing - ELFA = 1

Note: when ELFA = 0, the one blank line following the falling edge of VS* is increased to the value from the Vstart register.

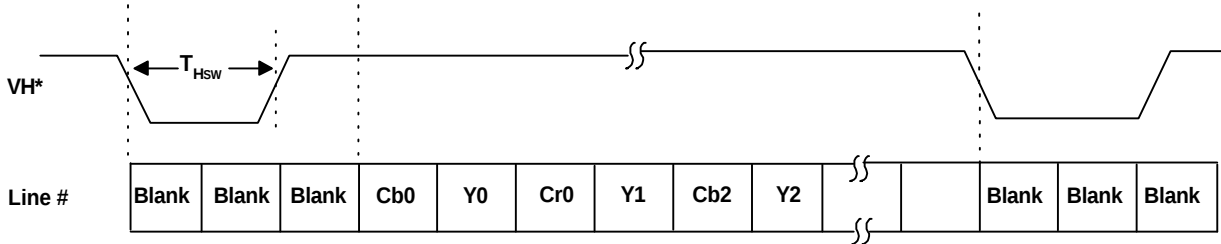


Figure 16: Horizontal Sync to Video Timing

Note: The number of blank pixels from the leading edge of HS* to the first active pixel is determined from the HSTART register.

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH5001A-L	LCC	52	5V

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