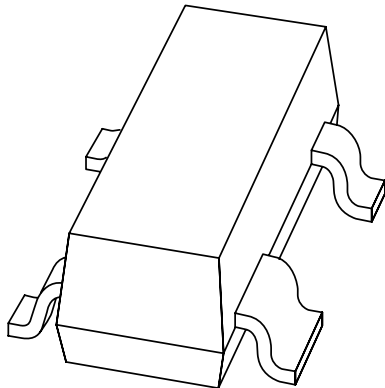


# DATA SHEET



**BF992**

Silicon N-channel dual gate  
MOS-FET

Product specification  
Supersedes data of 1996 Jul 30

1999 Aug 11

# Silicon N-channel dual gate MOS-FET

**BF992**

## APPLICATIONS

- VHF applications such as VHF television tuners and FM tuners with 12 V supply voltage. The device is also suitable for use in professional communications equipment.

## DESCRIPTION

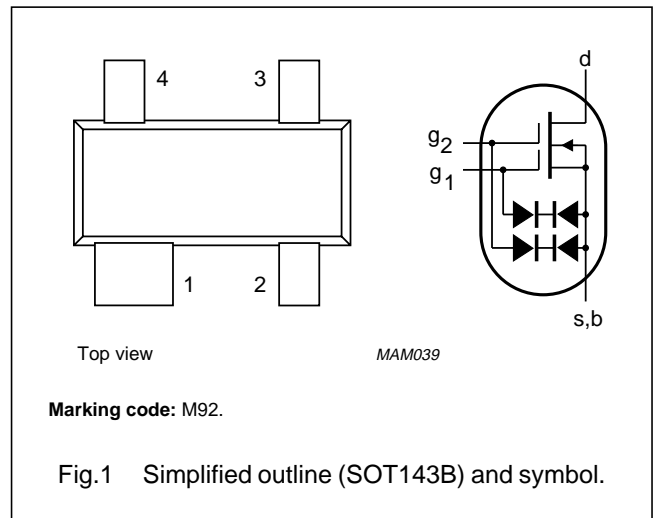
Depletion type field-effect transistor in a plastic micro-miniature SOT143B package with source and substrate interconnected.

The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

<b>CAUTION</b>
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

## PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g <sub>2</sub>	gate 2
4	g <sub>1</sub>	gate 1



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage (DC)		–	20	V
I <sub>D</sub>	drain current (DC)		–	40	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 60 °C	–	200	mW
Y <sub>fs</sub>	forward transfer admittance	f = 1 kHz; I <sub>D</sub> = 15 mA; V <sub>DS</sub> = 10 V; V <sub>G2-S</sub> = 4 V	25	–	mS
C <sub>ig1-s</sub>	input capacitance at gate 1	f = 1 MHz; I <sub>D</sub> = 15 mA; V <sub>DS</sub> = 10 V; V <sub>G2-S</sub> = 4 V	4	–	pF
C <sub>rs</sub>	reverse transfer capacitance	f = 1 MHz; I <sub>D</sub> = 15 mA; V <sub>DS</sub> = 10 V; V <sub>G2-S</sub> = 4 V	30	–	fF
F	noise figure	G <sub>S</sub> = 2 mS; I <sub>D</sub> = 15 mA; V <sub>DS</sub> = 10 V; V <sub>G2-S</sub> = 4 V; f = 200 MHz	1.2	–	dB
T <sub>j</sub>	operating junction temperature		–	150	°C

Silicon N-channel dual gate MOS-FET

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	20	V
$I_D$	drain current		–	40	mA
$I_{G1}$	gate 1 current		–	$\pm 10$	mA
$I_{G2}$	gate 2 current		–	$\pm 10$	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 60\text{ }^\circ\text{C}$ ; see Fig.2; note 1	–	200	mW
$T_{stg}$	storage temperature		–65	+150	$^\circ\text{C}$
$T_j$	operating junction temperature		–	150	$^\circ\text{C}$

**Note**

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.

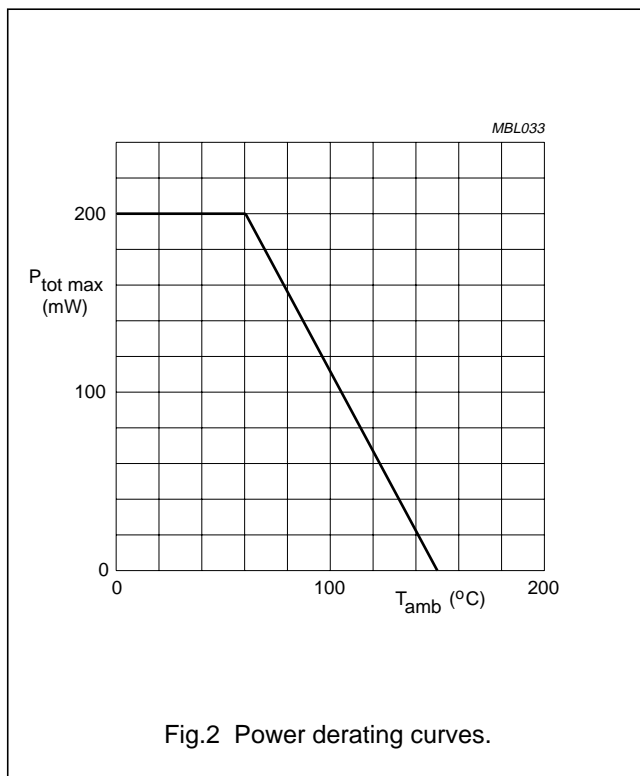


Fig.2 Power derating curves.

## Silicon N-channel dual gate MOS-FET

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	note 1	460	K/W

## Note

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.

## STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{G1-SS} = \pm 10\text{ mA}$	8	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{G2-SS} = \pm 10\text{ mA}$	8	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 10\text{ V}$ ; $I_D = 20\text{ }\mu\text{A}$	0.2	1.3	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	$V_{G1-S} = 0$ ; $V_{DS} = 10\text{ V}$ ; $I_D = 20\text{ }\mu\text{A}$	0.2	1.1	V
$\pm I_{G1-SS}$	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$ ; $V_{G1-S} = \pm 7\text{ V}$	–	25	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$ ; $V_{G2-S} = \pm 7\text{ V}$	–	25	nA

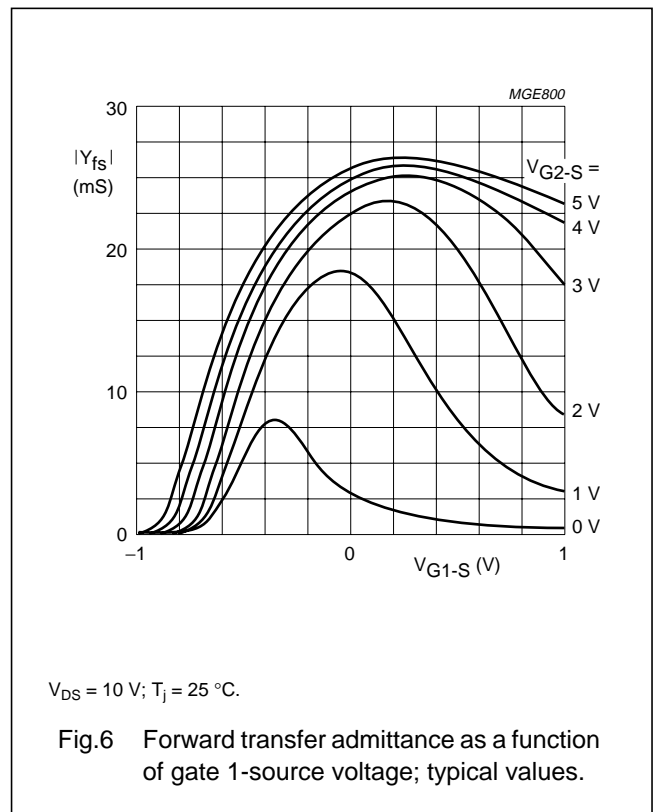
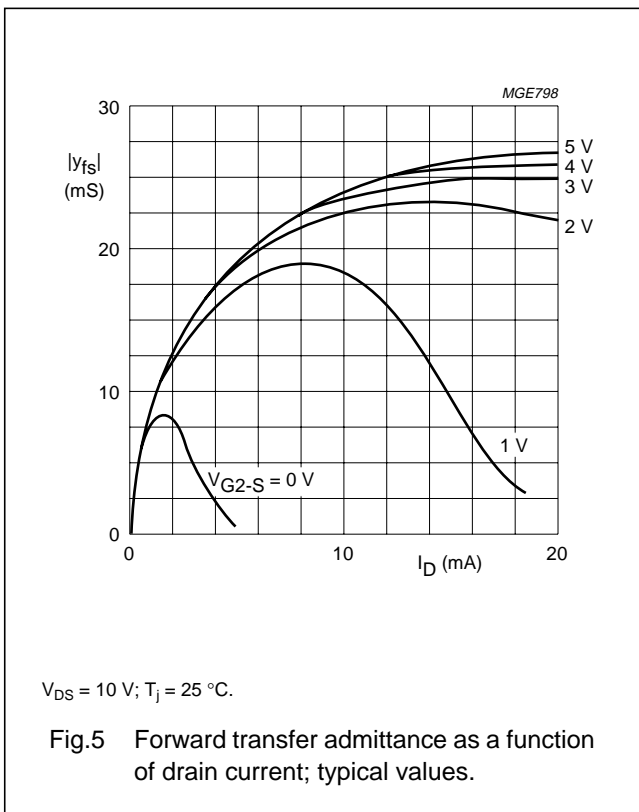
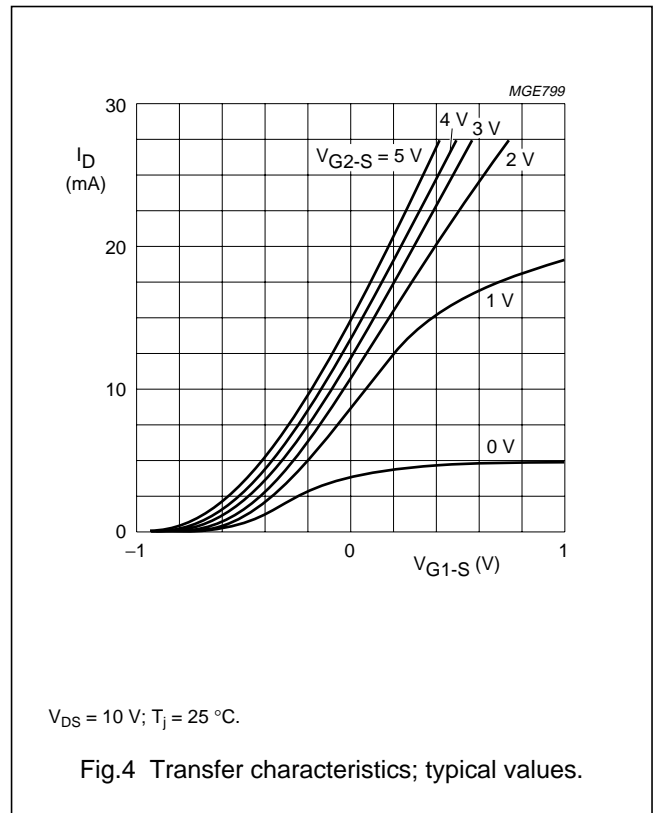
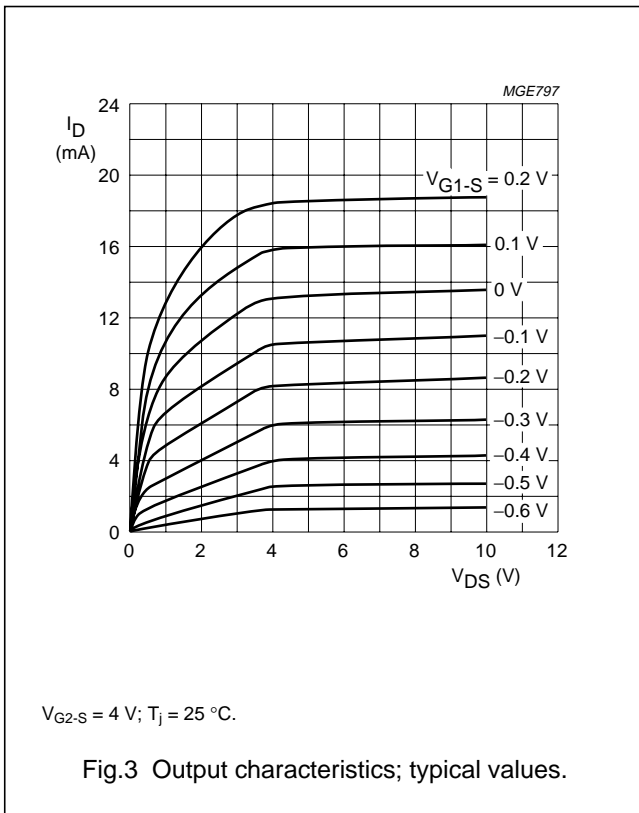
## DYNAMIC CHARACTERISTICS

Common source;  $T_{amb} = 25\text{ °C}$ ;  $V_{DS} = 10\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 15\text{ mA}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance		20	25	–	mS
$C_{ig1-s}$	input capacitance at gate 1	$f = 1\text{ MHz}$	–	4	–	pF
$C_{ig2-s}$	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1.7	–	pF
$C_{os}$	output capacitance	$f = 1\text{ MHz}$	–	2	–	pF
$C_{rs}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	30	40	fF
F	noise figure	$f = 200\text{ MHz}$ ; $G_S = 2\text{ mS}$	–	1.2	–	dB

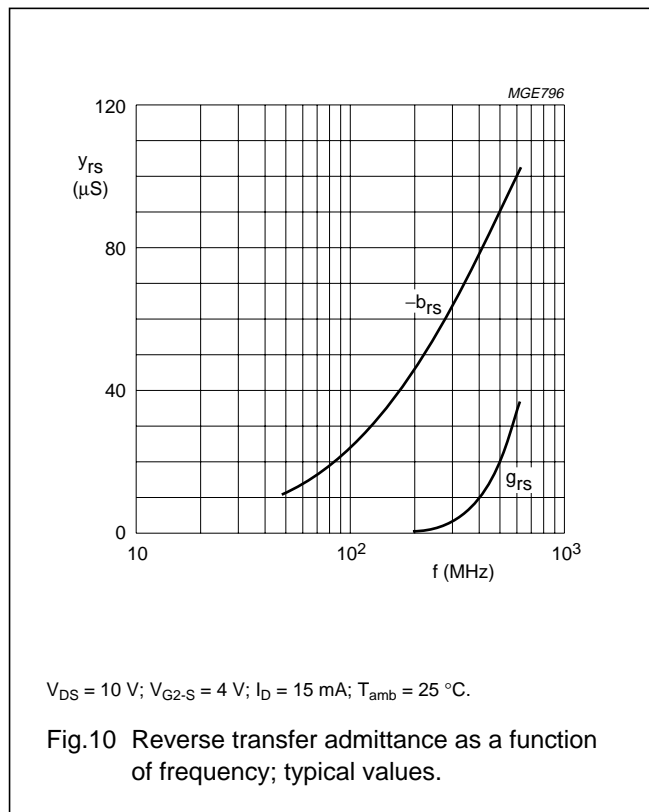
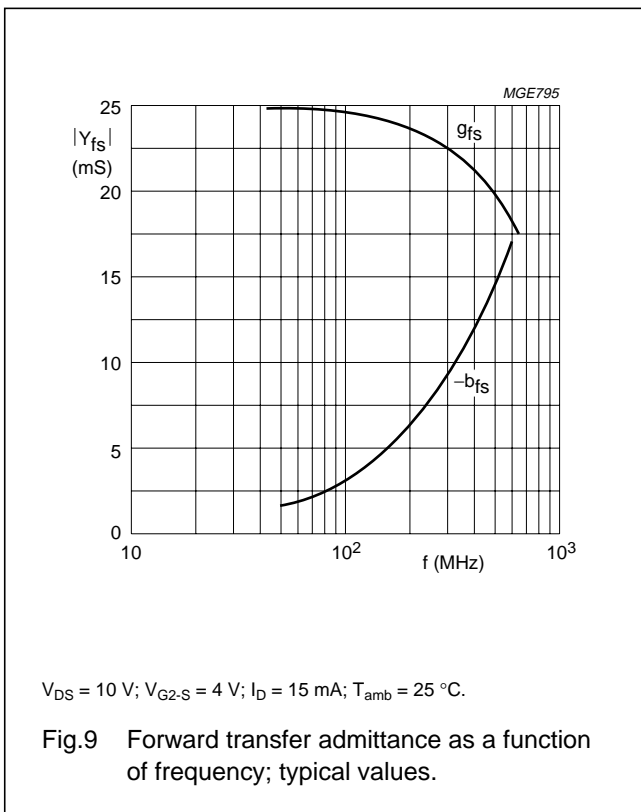
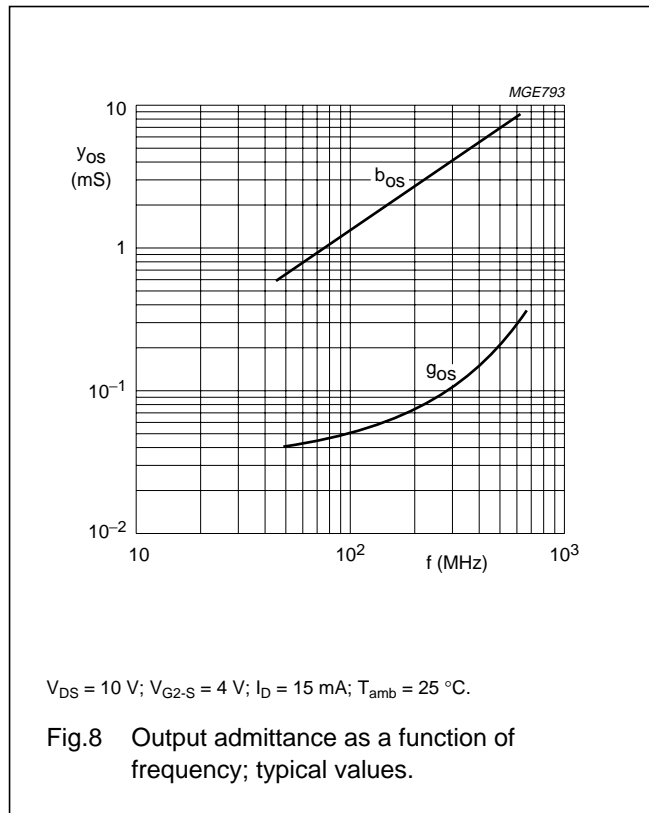
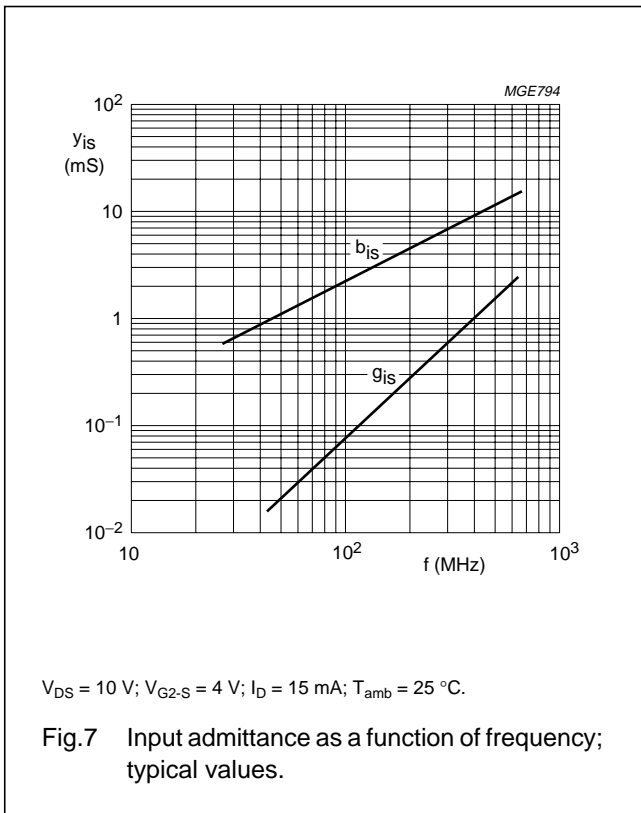
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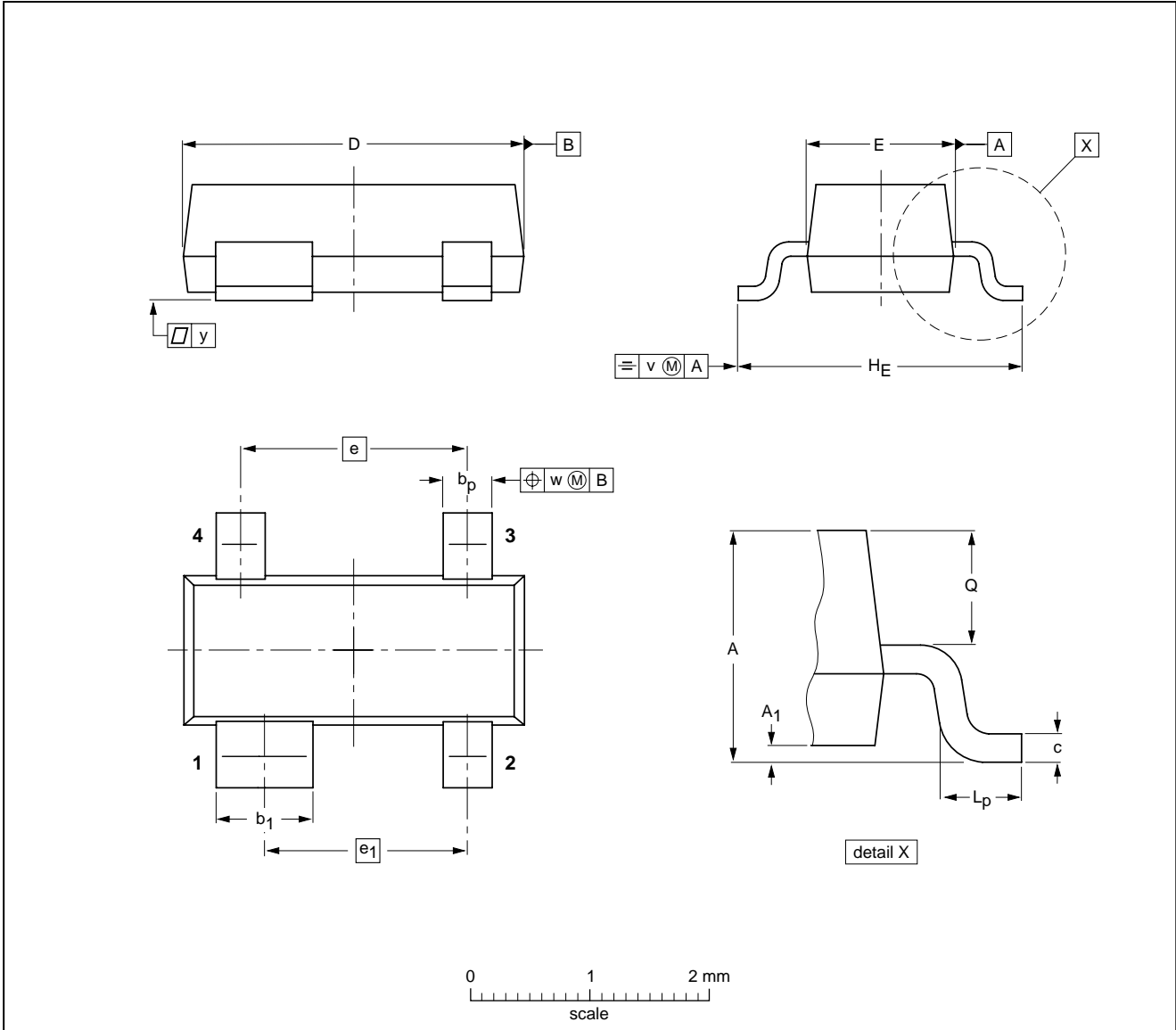
Silicon N-channel dual gate MOS-FET

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PACKAGE OUTLINE

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

## Silicon N-channel dual gate MOS-FET

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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Printed in The Netherlands

125004/03/pp12

Date of release: 1999 Aug 11

Document order number: 9397 750 06013

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