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| ACL Products | |

74AC/ACT11190

Asynchronous presettable synchronous decade up/down counter with single clock

FEATURES

- Synchronous, reversible counting
- Positive edge-triggered clock
- BCD/decade
- Asynchronous Parallel Load capability
- Output capability: $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11190 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

(continued)

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$ | TYPICAL | | UNIT |
|-------------------|---|---|---------|-----|------|
| | | | AC | ACT | |
| t_{PLH}/t_{PHL} | Propagation delay CP to Q_n ($PE = \text{High}$) | $C_L = 50\text{pF}$ | 5.2 | 7.3 | ns |
| C_{PD} | Power dissipation capacitance ¹ | $f = 1\text{MHz}; C_L = 50\text{pF}$ | 68 | 70 | pF |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or V_{CC} | 4.0 | 4.0 | pF |
| I_{LATCH} | Latch-up current | Per Jeduc JC40.2 Standard 17 | 500 | 500 | mA |
| f_{MAX} | Maximum clock frequency; $CP \rightarrow Q_n$ | $C_L = 50\text{pF}$ | 150 | 120 | MHz |

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

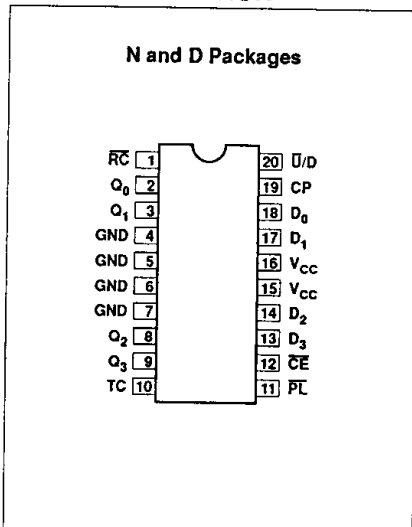
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

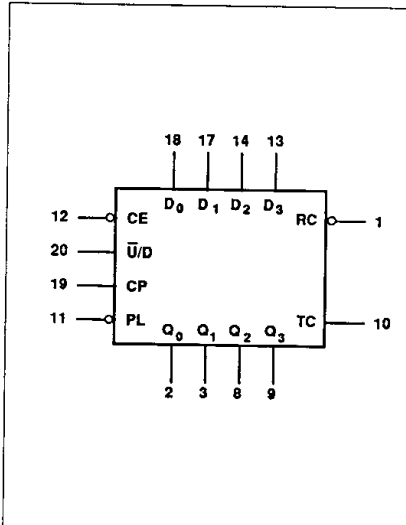
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE |
|-------------------------------------|-------------------|---------------------------|
| 20-pin plastic DIP (300mil-wide) | -40°C to +85°C | 74AC11190N 74ACT11190N |
| 20-pin plastic SOL (300mil-wide) | -40°C to +85°C | 74AC11190D 74ACT11190D |

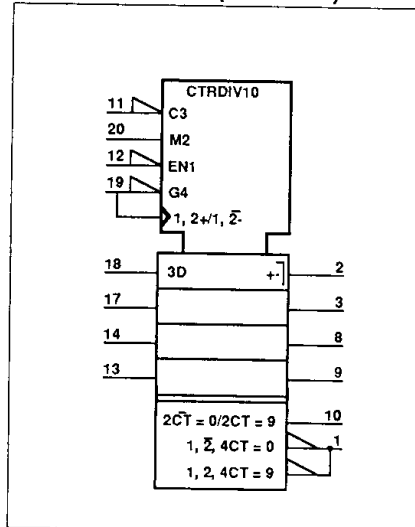
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous presetable synchronous decade up/down counter with single clock

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Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load (\overline{PL}) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a High level on the Count Enable (\overline{CE}) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock (\overline{RC}). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U/D}$ is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the RC output.

When TC is High and \overline{CE} is Low, the \overline{RC} follows the Clock Pulse. The \overline{RC} output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11190 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

In Figure 1a, each \overline{RC} output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on \overline{CE} inhibits the \overline{RC} output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the \overline{RC} output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the \overline{CE} input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own \overline{CE} , therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.

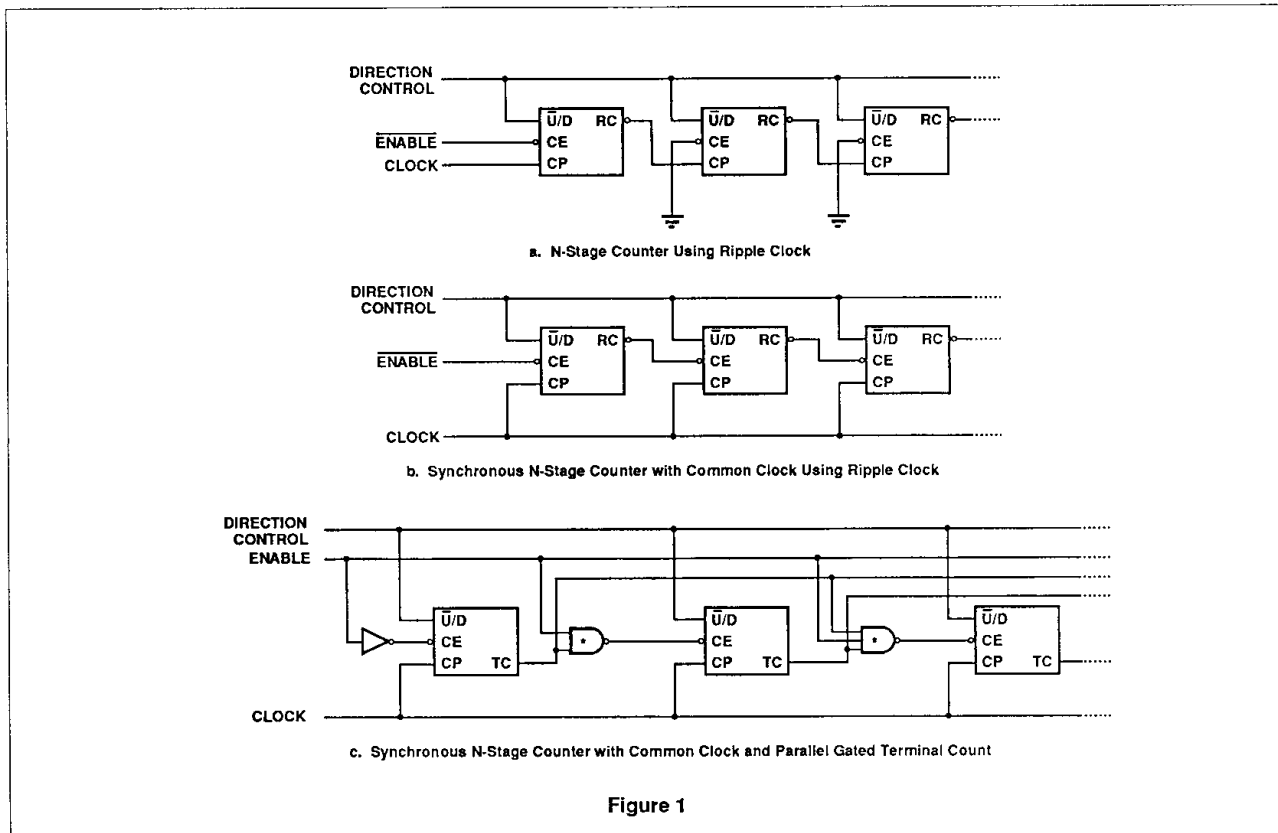


Figure 1

Asynchronous presetable synchronous decade up/down counter with single clock

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PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|----------------|-------------|--|
| 20 | \bar{U}/D | Up/down count control input |
| 12 | \bar{CE} | Count enable input (active-Low) |
| 18, 17, 14, 13 | $D_0 - D_3$ | Data inputs |
| 19 | CP | Clock pulse input (active rising edge) |
| 11 | \bar{PL} | Asynchronous load input (active-Low) |
| 2, 3, 8, 9 | $Q_0 - Q_3$ | Counter outputs |
| 1 | \bar{RC} | Ripple clock output (active-Low) |
| 10 | TC | Terminal count output |
| 4, 5, 6, 7 | GND | Ground (0V) |
| 15, 16 | V_{CC} | Positive supply voltage |

MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS |
|-------------------|------------|-------------|------------|----|-------|------------|
| | \bar{PL} | \bar{U}/D | \bar{CE} | CP | D_n | Q_n |
| Parallel load | L | X | X | X | L | L |
| | L | X | X | X | H | H |
| Count up | H | L | I | ↑ | X | count up |
| Count down | H | H | I | ↑ | X | count down |
| Hold (do nothing) | H | X | H | X | X | no change |

TC AND \bar{RC} FUNCTION TABLE

| INPUTS | | | TERMINAL COUNT STATE | | | | OUTPUTS | |
|-------------|------------|----|----------------------|-------|-------|-------|---------|------------|
| \bar{U}/D | \bar{CE} | CP | Q_0 | Q_1 | Q_2 | Q_3 | TC | \bar{RC} |
| H | H | X | H | X | X | H | L | H |
| L | H | X | H | L | L | H | H | H |
| L | L | ⌋ | H | L | L | H | H | ⌋ |
| L | H | X | L | L | L | L | L | H |
| H | H | X | L | L | L | L | H | H |
| H | L | ⌋ | L | L | L | L | H | ⌋ |

H = High voltage level

L = Low voltage level

h = High voltage level one setup time prior to the Low-to-High clock transition

l = Low voltage level one setup time prior to the Low-to-High clock transition

X = Don't care

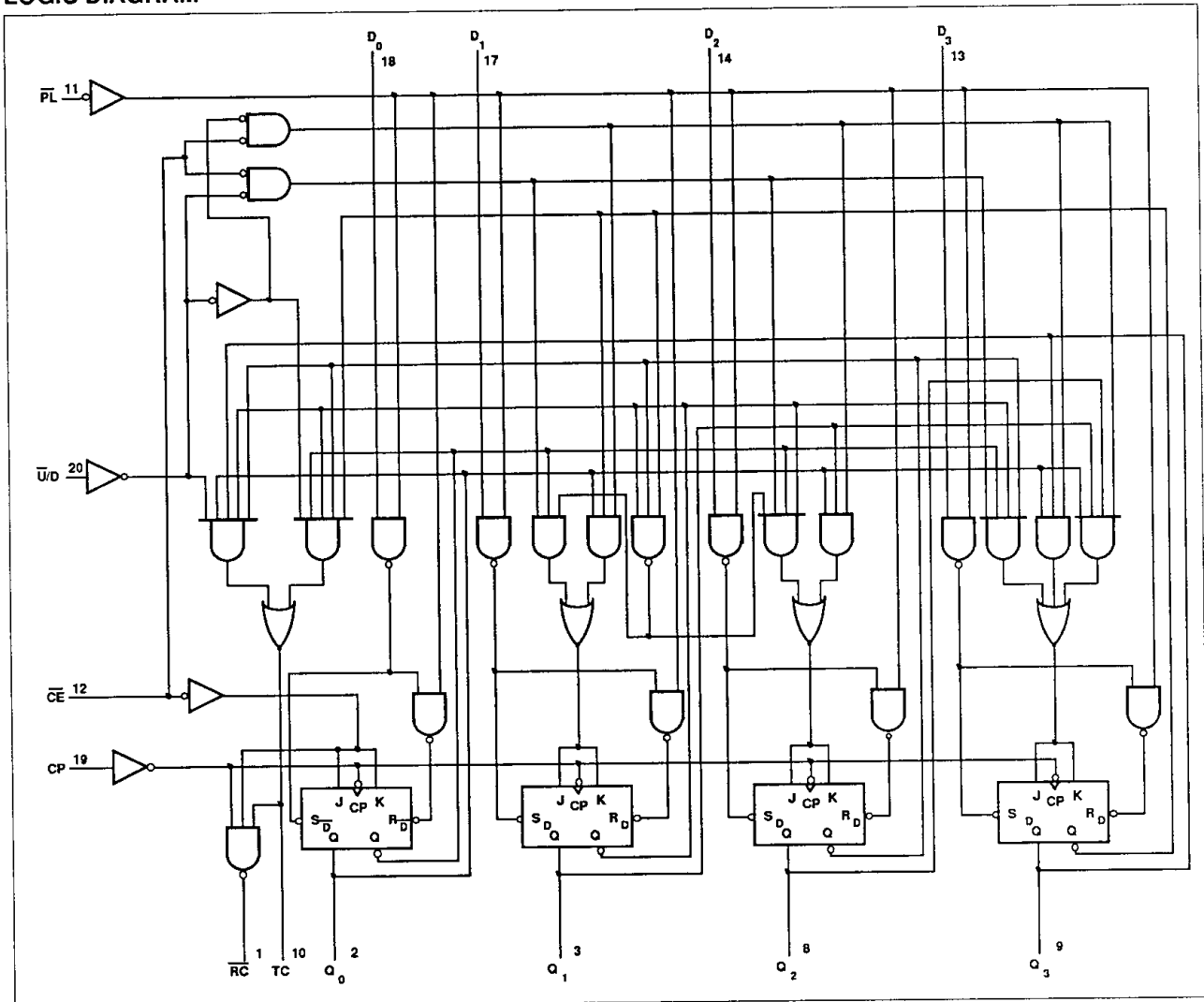
↑ = Low-to-High clock transition

⌋ = Low pulse

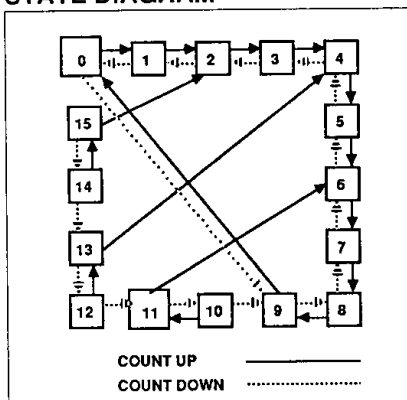
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LOGIC DIAGRAM



STATE DIAGRAM



Asynchronous presetable synchronous decade up/down counter with single clock

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | 74AC11190 | | | 74ACT11190 | | | UNIT |
|---------------------|--------------------------------------|------------------|-----|----------|------------|-----|----------|------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V_{CC} | DC supply voltage | 3.0 ¹ | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | | +85 | -40 | | +85 | °C |

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

| SYMBOL | PARAMETER | TEST CONDITIONS | RATING | UNIT |
|-----------------------------|---|--------------------------------------|------------------------|------|
| V_{CC} | DC supply voltage | | -0.5 TO +7.0 | V |
| I_{IK} or V_I | DC input diode current ² | $V_I < 0$ | -20 | mA |
| | | $V_I > V_{CC}$ | 20 | |
| | DC input voltage | | -0.5 to $V_{CC} + 0.5$ | V |
| I_{OK} or V_O | DC output diode current ² | $V_O < 0$ | -50 | mA |
| | | $V_O > V_{CC}$ | 50 | |
| | DC output voltage | | -0.5 to $V_{CC} + 0.5$ | V |
| I_O | DC output source or sink current per output pin | $V_O = 0$ to V_{CC} | ± 50 | mA |
| I_{CC} or I_{GND} | DC V_{CC} current | | ± 150 | mA |
| | DC ground current | | ± 150 | |
| T_{STG} | Storage temperature | | -65 to 150 | °C |
| P_{TOT} | Power dissipation per package | Above 70°C; derate linearly by 8mW/K | 500 | mW |
| | Power dissipation per package Plastic surface mount (SO) | Above 70°C; derate linearly by 8mW/K | 400 | mW |

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | V _{CC} | 74AC11190 | | | | 74ACT11190 | | | | UNIT | |
|-------------------------------------|--|---|-------------------------|--------------------------|------|-----------------------------------|------|--------------------------|------|-----------------------------------|------|------|------|
| | | | | T _{amb} = +25°C | | T _{amb} = -40°C to +85°C | | T _{amb} = +25°C | | T _{amb} = -40°C to +85°C | | | |
| | | | | V | Min | Max | Min | Max | Min | Max | Min | | Max |
| V _{IH} | High-level input voltage | | 3.0 | 2.10 | | 2.10 | | | | | | V | |
| | | | 4.5 | 3.15 | | 3.15 | | 2.0 | | 2.0 | | | |
| | | | 5.5 | 3.85 | | 3.85 | | 2.0 | | 2.0 | | | |
| V _{IL} | Low-level input voltage | | 3.0 | | 0.90 | | 0.90 | | | | | V | |
| | | | 4.5 | | 1.35 | | 1.35 | | 0.8 | | 0.8 | | |
| | | | 5.5 | | 1.65 | | 1.65 | | 0.8 | | 0.8 | | |
| V _{OH} | High-level output voltage | V _I = V _{IL} or V _{IH} | I _{OH} = -50μA | 3.0 | 2.9 | | 2.9 | | | | | V | |
| | | | | 4.5 | 4.4 | | 4.4 | | 4.4 | | 4.4 | | |
| | | | | 5.5 | 5.4 | | 5.4 | | 5.4 | | 5.4 | | |
| | | | I _{OH} = -4mA | 3.0 | 2.58 | | 2.48 | | | | | | |
| | | | | 4.5 | 3.94 | | 3.8 | | 3.94 | | 3.8 | | |
| | | | | 5.5 | 4.94 | | 4.8 | | 4.94 | | 4.8 | | |
| | | | | 5.5 | | | 3.85 | | | | 3.85 | | |
| V _{OL} | Low-level output voltage | V _I = V _{IL} or V _{IH} | I _{OL} = 50μA | 3.0 | | 0.1 | | 0.1 | | | | V | |
| | | | | 4.5 | | 0.1 | | 0.1 | | 0.1 | | | 0.1 |
| | | | | 5.5 | | 0.1 | | 0.1 | | 0.1 | | | 0.1 |
| | | | I _{OL} = 12mA | 3.0 | | 0.36 | | 0.44 | | | | | |
| | | | | 4.5 | | 0.36 | | 0.44 | | 0.36 | | | 0.44 |
| | | | I _{OL} = 24mA | 3.0 | | 0.36 | | 0.44 | | 0.36 | | | 0.44 |
| | | | | 5.5 | | 0.36 | | 0.44 | | 0.36 | | | 0.44 |
| I _{OL} = 75mA ¹ | 5.5 | | | | 1.65 | | | | 1.65 | | | | |
| I _I | Input leakage current | V _I = V _{CC} or GND | 5.5 | | ±0.1 | | ±1.0 | | ±0.1 | | ±1.0 | μA | |
| I _{CC} | Quiescent supply current | V _I = V _{CC} or GND, I _O = 0mA | 5.5 | | 8.0 | | 80 | | 8.0 | | 80 | μA | |
| ΔI _{CC} | Supply current, TTL inputs High ² | One input at 3.4V, other inputs at V _{CC} or GND | 5.5 | | | | | | 0.9 | | 1.0 | mA | |

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

| SYMBOL | PARAMETER | | WAVEFORM | 74AC11190 | | | | | UNIT |
|--------------------------------------|--|----------------------------|----------|--------------------------|------------|--------------|-----------------------------------|--------------|--------------|
| | | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum clock frequency | CP to Q _n | 1 | 65 | 95 | | 65 | | MHz |
| | | CP to \overline{RC} , TC | | 60 | 85 | | 60 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP to Q _n | | 1 | 2.3 2.8 | 7.6 7.2 | 10.0 9.8 | 2.3 2.8 | 11.1 11.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to TC | | | 1 | 4.3 3.5 | 9.0 9.8 | 12.0 12.3 | 4.3 3.5 | 14.2 15.1 |
| t _{PLH} t _{PHL} | Propagation delay CP to \overline{RC} | | 2 | | 3.0 3.0 | 7.6 7.4 | 10.5 9.6 | 3.0 3.0 | 12.4 11.2 |
| t _{PLH} t _{PHL} | Propagation delay \overline{CE} to \overline{RC} | | | 2 | 2.9 3.0 | 6.9 6.8 | 9.4 8.6 | 2.9 3.0 | 11.0 10.1 |
| t _{PLH} t _{PHL} | Propagation delay $\overline{U/D}$ to \overline{RC} | | 2 | | 4.8 4.5 | 11.0 10.6 | 14.3 13.6 | 4.8 4.5 | 16.8 16.2 |
| t _{PLH} t _{PHL} | Propagation delay $\overline{U/D}$ to TC | | | 4 | 3.3 3.9 | 8.4 8.7 | 11.8 11.2 | 3.3 3.9 | 14.1 13.1 |
| t _{PLH} t _{PHL} | Propagation delay D _n to Q _n | | 3 | | 3.9 4.0 | 9.6 9.0 | 12.8 11.4 | 3.9 4.0 | 15.0 13.5 |
| t _{PLH} t _{PHL} | Propagation delay D _n to TC | | | 3, 4 | 5.0 4.9 | 13.1 11.9 | 18.3 16.3 | 5.0 4.9 | 21.8 19.4 |
| t _{PLH} t _{PHL} | Propagation delay D _n to \overline{RC} | | 3, 4 | | 5.6 6.2 | 14.0 15.3 | 19.2 20.2 | 5.6 6.2 | 22.7 24.3 |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to Q _n | | | 5 | 3.4 3.5 | 10.2 9.0 | 13.6 11.6 | 3.4 3.5 | 15.8 13.7 |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to TC | | 5 | | 5.4 5.2 | 13.8 12.2 | 17.9 15.9 | 5.4 5.2 | 21.3 19.0 |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to \overline{RC} | | | 5 | 5.9 6.6 | 14.2 15.8 | 18.8 19.7 | 5.9 6.6 | 23.0 23.7 |
| t _S | Setup time, High or Low D _n to \overline{PL} | | 6 | | 3.5 | | | 3.5 | |
| t _H | Hold time, High or Low D _n to \overline{PL} | | | 6 | 0.5 | | | 0.5 | |
| t _S | Setup time, High or Low \overline{CE} to CP | | 6 | | 11.5 | | | 11.5 | |
| t _H | Hold time, High or Low \overline{CE} to CP | | | 6 | 0.0 | | | 0.0 | |
| t _S | Setup time, High or Low $\overline{U/D}$ to CP | | 6 | | 12.0 | | | 12.0 | |
| t _H | Hold time, High or Low $\overline{U/D}$ to CP | | | 6 | 0.0 | | | 0.0 | |
| t _w | \overline{PL} pulse width, Low | | 5 | | 4.5 | | | 4.5 | |
| t _w | CP pulse width, High or Low | | | 1 | 8.3 | | | 8.3 | |
| t _{REC} | Recover time, \overline{PL} to CP | | 5 | | 2.5 | | | 2.5 | |

Asynchronous presetable synchronous decade up/down counter with single clock

74AC/ACT11190

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

| SYMBOL | PARAMETER | | WAVEFORM | 74AC11190 | | | | | UNIT |
|--------------------------------------|--|----------------------------|----------|--------------------------|-------------|--------------|-----------------------------------|--------------|------|
| | | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum clock frequency | CP to Q _n | 1 | 120 | 150 | | 120 | | MHz |
| | | CP to \overline{RC} , TC | | 75 | 100 | | 75 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP to Q _n | | 1 | 1.8 2.1 | 4.9 5.4 | 7.3 7.7 | 1.8 2.1 | 8.1 8.8 | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to TC | | 1 | 3.0 3.3 | 6.0 6.7 | 8.6 9.1 | 3.0 3.3 | 9.7 10.4 | ns |
| t _{PLH} t _{PHL} | Propagation delay CP to \overline{RC} | | 2 | 2.1 2.6 | 5.1 5.2 | 7.6 7.2 | 2.1 2.6 | 8.6 8.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay \overline{CE} to \overline{RC} | | 2 | 2.5 2.8 | 4.9 5.1 | 7.0 6.9 | 2.5 2.8 | 7.8 7.7 | ns |
| t _{PLH} t _{PHL} | Propagation delay $\overline{U/D}$ to \overline{RC} | | 2 | 4.1 4.0 | 7.3 7.2 | 10.1 10.1 | 4.1 4.0 | 11.2 11.3 | ns |
| t _{PLH} t _{PHL} | Propagation delay $\overline{U/D}$ to TC | | 4 | 2.9 3.4 | 5.6 6.2 | 8.7 8.3 | 2.9 3.4 | 9.7 9.4 | ns |
| t _{PLH} t _{PHL} | Propagation delay D _n to Q _n | | 3 | 3.0 3.1 | 6.3 6.3 | 8.1 8.6 | 3.0 3.1 | 10.1 9.6 | ns |
| t _{PLH} t _{PHL} | Propagation delay D _n to TC | | 3, 4 | 4.3 4.1 | 8.3 8.0 | 12.4 11.4 | 4.3 4.1 | 14.0 13.3 | ns |
| t _{PLH} t _{PHL} | Propagation delay D _n to \overline{RC} | | 3, 4 | 4.8 5.2 | 9.0 9.8 | 13.2 13.9 | 4.0 5.2 | 14.8 15.6 | ns |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to Q _n | | 5 | 3.1 2.9 | 6.4 6.2 | 9.5 8.8 | 3.1 2.9 | 10.4 9.9 | ns |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to TC | | 5 | 4.9 4.4 | 8.8 8.2 | 12.3 11.5 | 4.9 4.4 | 13.8 12.9 | ns |
| t _{PLH} t _{PHL} | Propagation delay PL to \overline{RC} | | 5 | 5.3 5.8 | 9.1 10.1 | 12.8 13.6 | 5.3 5.8 | 14.4 15.3 | ns |
| t _S | Setup time, High or Low D _n to \overline{PL} | | 6 | 2.5 | | | 2.5 | | ns |
| t _H | Hold time, High or Low D _n to \overline{PL} | | 6 | 0.5 | | | 0.5 | | ns |
| t _S | Setup time, High or Low \overline{CE} to CP | | 6 | 7.5 | | | 7.5 | | ns |
| t _H | Hold time, High or Low \overline{CE} to CP | | 6 | 0.0 | | | 0.0 | | ns |
| t _S | Setup time, High or Low $\overline{U/D}$ to CP | | 6 | 8.0 | | | 8.0 | | ns |
| t _H | Hold time, High or Low $\overline{U/D}$ to CP | | 6 | 0.0 | | | 0.0 | | ns |
| t _w | \overline{PL} pulse width, Low | | 5 | 3.5 | | | 3.5 | | ns |
| t _w | CP pulse width, High or Low | | 1 | 5.5 | | | 5.5 | | ns |
| t _{REC} | Recover time, \overline{PL} to CP | | 5 | 2.0 | | | 2.0 | | ns |

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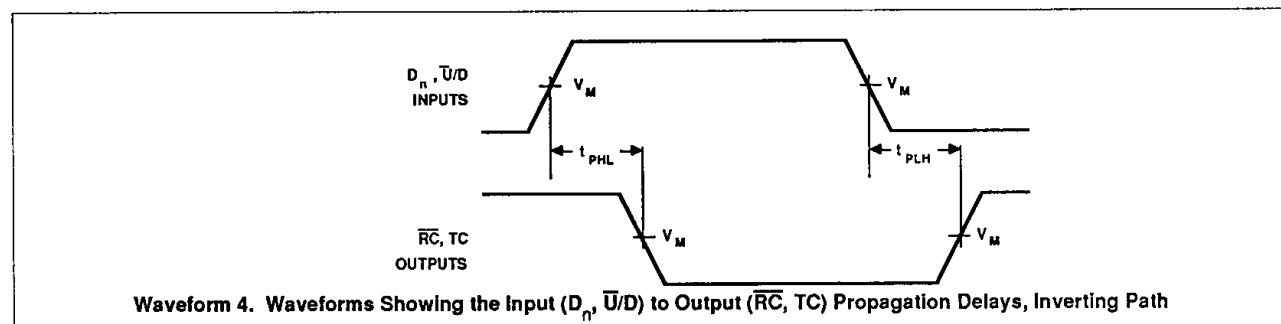
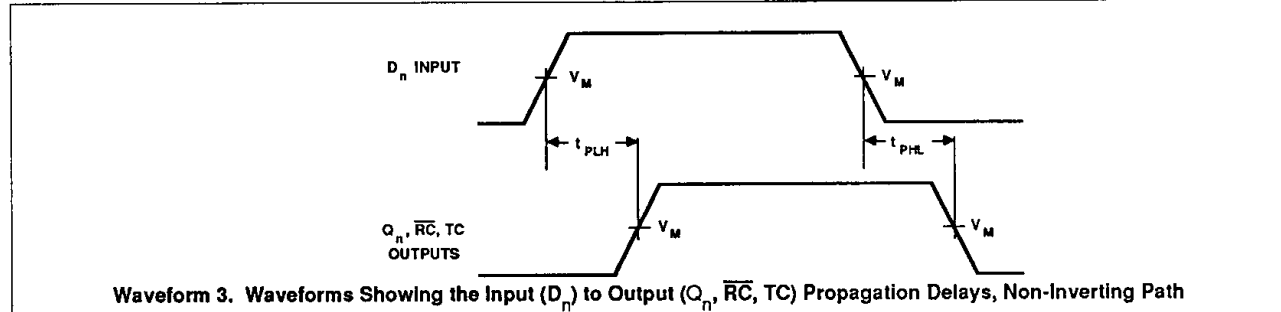
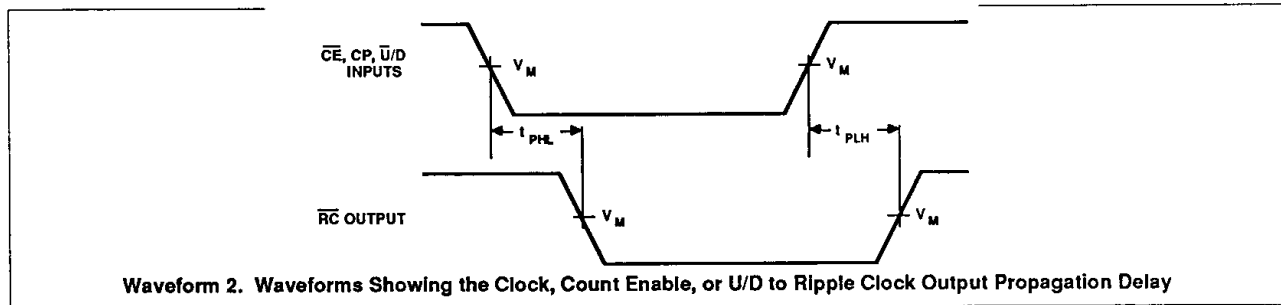
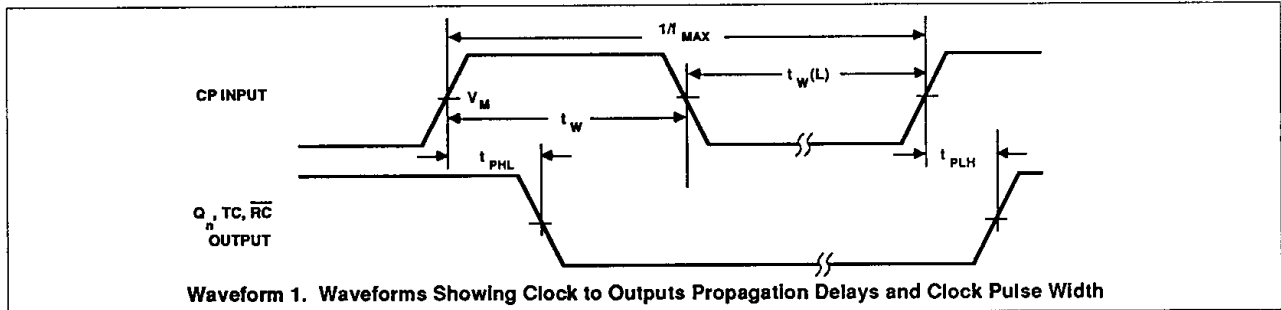
AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

| SYMBOL | PARAMETER | | WAVEFORM | 74ACT11190 | | | | | UNIT |
|------------------------|--|----------------------------|----------|--------------------------|--------------|--------------|--|--------------|--------------|
| | | | | $T_{amb} = +25^{\circ}C$ | | | $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ | | |
| | | | | Min | Typ | Max | Min | Max | |
| f_{MAX} | Maximum clock frequency | CP to Q_n | 1 | 85 | 120 | | 85 | | MHz |
| | | CP to \overline{RC} , TC | | 65 | 90 | | 65 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP to Q_n | | 1 | 3.7 4.2 | 7.0 7.6 | 9.1 9.7 | 3.7 4.2 | 10.0 11.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay CP to TC | | | 4.8 5.4 | 8.3 9.1 | 10.7 11.5 | 4.8 5.4 | 11.8 12.7 | ns |
| t_{PLH} t_{PHL} | Propagation delay CP to \overline{RC} | | 2 | 4.2 3.6 | 7.7 6.9 | 10.1 9.7 | 4.2 3.6 | 11.0 10.5 | ns |
| t_{PLH} t_{PHL} | Propagation delay \overline{CE} to \overline{RC} | | | 3.9 3.0 | 6.6 6.1 | 8.9 8.4 | 3.9 3.0 | 9.7 9.2 | ns |
| t_{PLH} t_{PHL} | Propagation delay $\overline{U/D}$ to \overline{RC} | | 2 | 4.9 4.5 | 8.7 8.6 | 11.8 11.6 | 4.9 4.5 | 12.9 13.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay $\overline{U/D}$ to TC | | | 4 4 | 3.5 4.1 | 7.0 7.5 | 10.2 10.0 | 3.5 4.1 | 11.5 11.3 |
| t_{PLH} t_{PHL} | Propagation delay D_n to Q_n | | 3 | 4.6 4.0 | 7.9 7.3 | 10.2 10.3 | 4.6 4.0 | 11.4 11.6 | ns |
| t_{PLH} t_{PHL} | Propagation delay D_n to TC | | | 3, 4 3, 4 | 5.1 4.9 | 9.7 9.6 | 13.7 13.2 | 5.1 4.9 | 15.2 14.6 |
| t_{PLH} t_{PHL} | Propagation delay D_n to \overline{RC} | | 3, 4 | 5.7 6.4 | 10.6 11.3 | 14.7 15.0 | 5.7 6.4 | 16.2 16.7 | ns |
| t_{PLH} t_{PHL} | Propagation delay \overline{PL} to Q_n | | | 5 5 | 4.1 4.1 | 7.6 7.6 | 10.7 10.5 | 4.1 4.1 | 11.8 11.8 |
| t_{PLH} t_{PHL} | Propagation delay \overline{PL} to TC | | 5 | 5.4 5.0 | 9.9 9.5 | 13.7 13.0 | 5.4 5.0 | 15.2 14.6 | ns |
| t_{PLH} t_{PHL} | Propagation delay \overline{PL} to \overline{RC} | | | 5 5 | 5.9 6.6 | 10.4 11.5 | 14.6 15.1 | 5.9 6.6 | 16.4 16.8 |
| t_s | Setup time, High or Low D_n to \overline{PL} | | 6 | 2.5 | | | 2.5 | | ns |
| t_h | Hold time, High or Low D_n to \overline{PL} | | | 6 | 1.5 | | | 1.5 | |
| t_s | Setup time, High or Low \overline{CE} to CP | | 6 | 7.0 | | | 7.0 | | ns |
| t_h | Hold time, High or Low \overline{CE} to CP | | | 6 | 1.5 | | | 1.5 | |
| t_s | Setup time, High or Low $\overline{U/D}$ to CP | | 6 | 7.5 | | | 7.5 | | ns |
| t_h | Hold time, High or Low $\overline{U/D}$ to CP | | | 6 | 0.0 | | | 0.0 | |
| t_w | \overline{PL} pulse width, Low | | 5 | 4.0 | | | 4.0 | | ns |
| t_w | CP pulse width, High or Low | | | 1 | 7.7 | | | 7.7 | |
| t_{REC} | Recover time, \overline{PL} to CP | | 5 | 2.0 | | | 2.0 | | ns |

Asynchronous presetable synchronous decade up/down counter with single clock

74AC/ACT11190

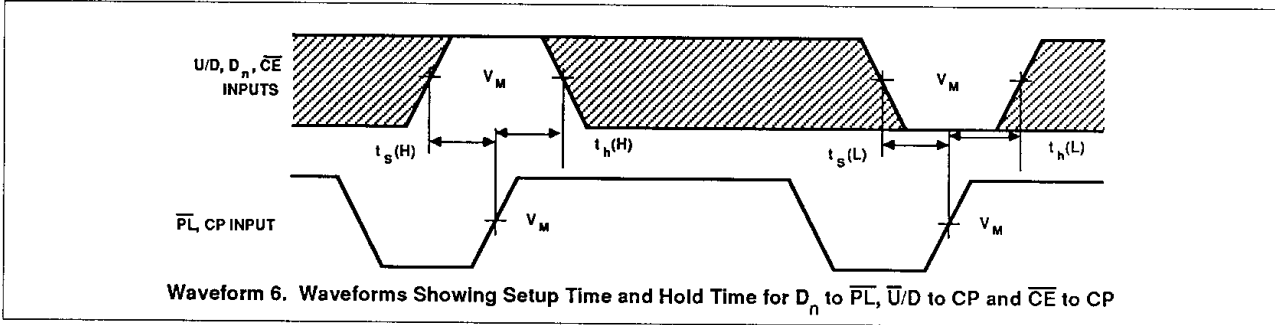
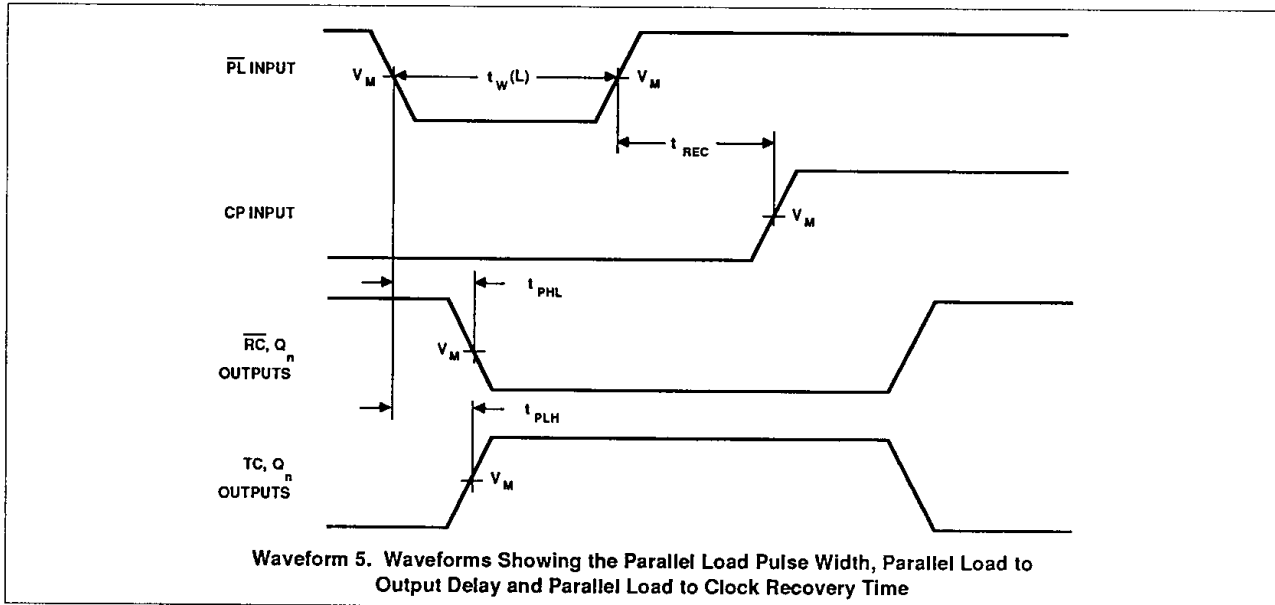
AC WAVEFORMS



Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

AC WAVEFORMS (Continued)



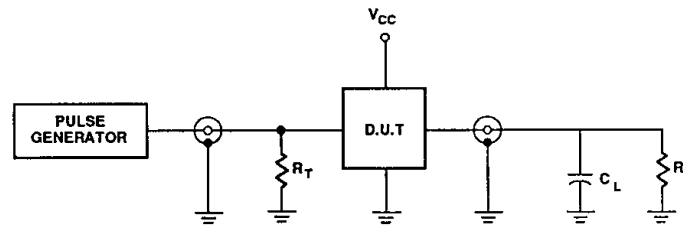
WAVEFORM CONDITIONS

| | INPUTS | OUTPUTS |
|-----|---|---------------------------------------|
| AC | $V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$ | $V_{OUT} = V_{OL} \text{ to } V_{OH}$ |
| ACT | $V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$ | $V_M = 50\% V_{CC}$ |

Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500 Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR \leq 10MHz

$t_r = t_f = 3ns$