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## S1D13806 Embedded Memory Display Controller

# Hardware Functional Specification

**Document Number: X28B-A-001-12**

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# 1 Introduction

## 1.1 Scope

This User Guide provides technical information for the S1D13806 Embedded Memory Display Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This guide is updated as appropriate. Please check the Epson Electronics America Website at www.eea.epson.com or the Epson Research and Development Website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

## 1.2 Overview Description

The S1D13806 is a highly integrated color LCD/CRT/TV graphics controller with embedded memory supporting a wide range of CPUs and display devices. The S1D13806 architecture is designed to meet the low cost, low power requirements of the embedded markets, such as Mobile Communications, Hand-Held PC's, and Office Automation.

The S1D13806 supports multiple CPUs, all LCD panel types, CRT, TV, and additionally provides a number of differentiating features. EPSON Independent Simultaneous Display technology allows the user to configure two different images on two different displays, while the SwivelView™, Hardware Cursor, Ink Layer, and BitBLT features offer substantial performance benefits. Products requiring digital camera input can take advantage of the directly supported WINNOV Videum® Cam digital interface. While focusing on devices targeted by the Microsoft Windows CE Operating System, the S1D13806's impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

# 2 Features

*Table 2-1 : S1D13806 Features*

| S1D13806 Features | |
|---|---|
| **Embedded Memory**<br>1280K byte embedded synchronous DRAM.<br>Up to 50MHz data rate (100M Bytes/second).<br>Display buffer address space is directly and contiguously available through the 21-bit address bus. | **Display Modes**<br>4/8/16 bit-per-pixel (bpp) color depths.<br>Up to 64K colors on TFT,CRT and TV.<br>Up to 64K colors in 16 bpp mode on color passive LCD panels using dithering (4096 colors in 4/8 bpp).<br>Up to 64 shades of gray on monochrome passive panels using Frame Rate Modulation (FRM) and Dithering.<br>4/8 bit-per-pixel color depths are mapped using three 256x4 Look-Up Tables (LUT).<br>Separate LUTs for LCD and CRT/TV.<br>16 bit-per-pixel modes are mapped directly bypassing the LUT. |
| **CPU Interfaces**<br>Epson E0C33.<br>Hitachi SH-4.<br>Hitachi SH-3.<br>MIPS/ISA.<br>Motorola MC68000.<br>Motorola MC68030.<br>Motorola PowerPC MPC82x.<br>MPU bus interface with programmable READY.<br>NEC MIPS VR41xx.<br>PC Card (PCMCIA).<br>Philips MIPS PR31500/PR31700.<br>StrongARM (PC Card).<br>Toshiba MIPS TX39xx.<br>One-stage write buffer for minimum wait-state CPU writes.<br>Registers are memory-mapped – M/R# pin selects between display buffer and register address space. | **Display Features**<br>SwivelView™: 90°, 180°, 270° hardware rotation of display image.<br>EPSON Independent Simultaneous Display (EISD): displays independent images on different displays (CRT or TV and passive or TFT panel).<br>Virtual Display Support: displays images larger than the physical display size through the use of panning and scrolling.<br>2D BitBLT Engine.<br>Hardware Cursor/Ink Layer: separate 64x64x2 hardware cursor or 2-bit ink layer for both LCD and CRT/TV.<br>Double Buffering/Multi-pages: for smooth animation and instantaneous screen update. |
| **Display Support**<br>4/8-bit monochrome or 4/8/16-bit color LCD interface for single-panel, single-drive displays.<br>8-bit monochrome or 8/16-bit color LCD interface for dual-panel, dual-drive displays.<br>Direct support for 9-bit, 12-bit, 18-bit, 2x9-bit, 2x12-bit TFT/D-TFD.<br>Direct support for CRT.<br>Direct support for S-Video/Composite TV output (NTSC or PAL format). | **Miscellaneous**<br>Power save mode is initiated by software.<br>Built-in MediaPlug Interface for Winnov Camera.<br>Highly Flexible Clocking.<br>Eight configuration pins (CONF[7:0]) are used to configure the chip at power-on.<br>13 General Purpose Input/Output pins.<br>Operating voltage from 3.0 volts to 3.6 volts.<br>144-pin QFP20 package.<br>220-pin PFBGA package |

# 3 Typical System Implementation Diagrams

For pin mapping of each system implementation, see Table 4-10, “CPU Interface Pin Mapping,” on pag e34.

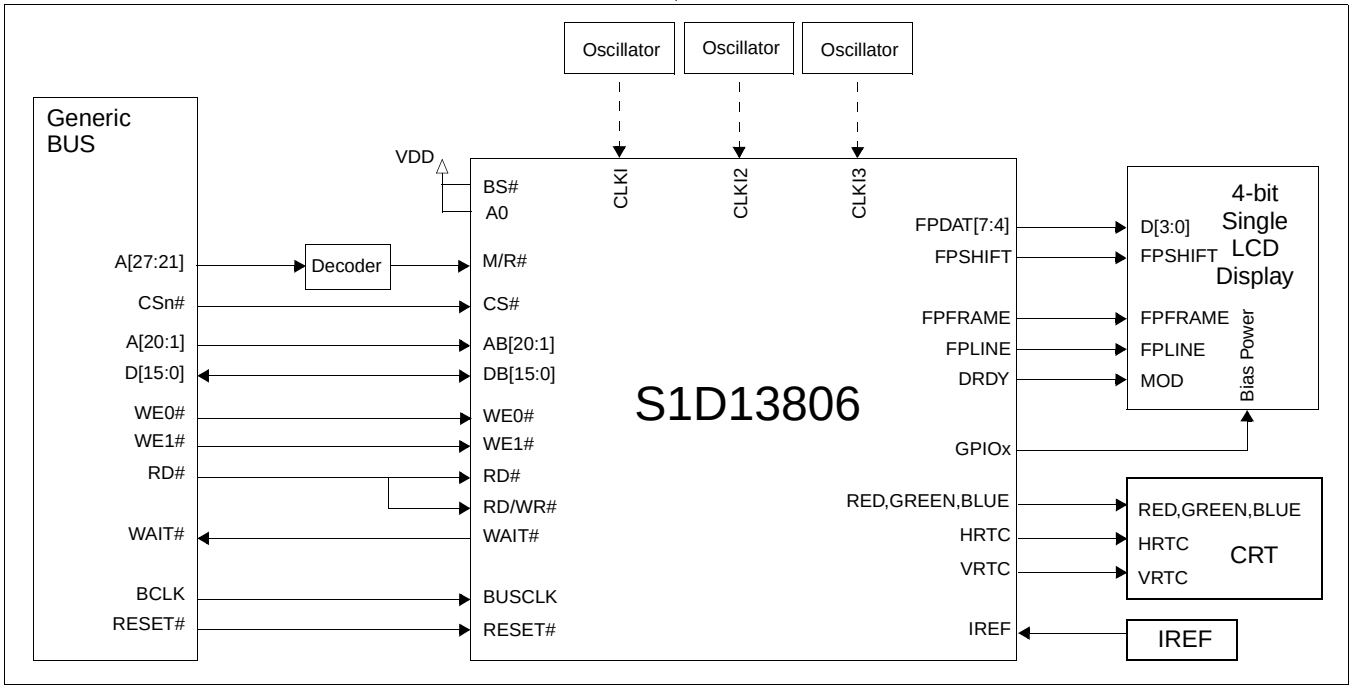



*Figure 3-1: Typical System Diagram (Generic Bus)*

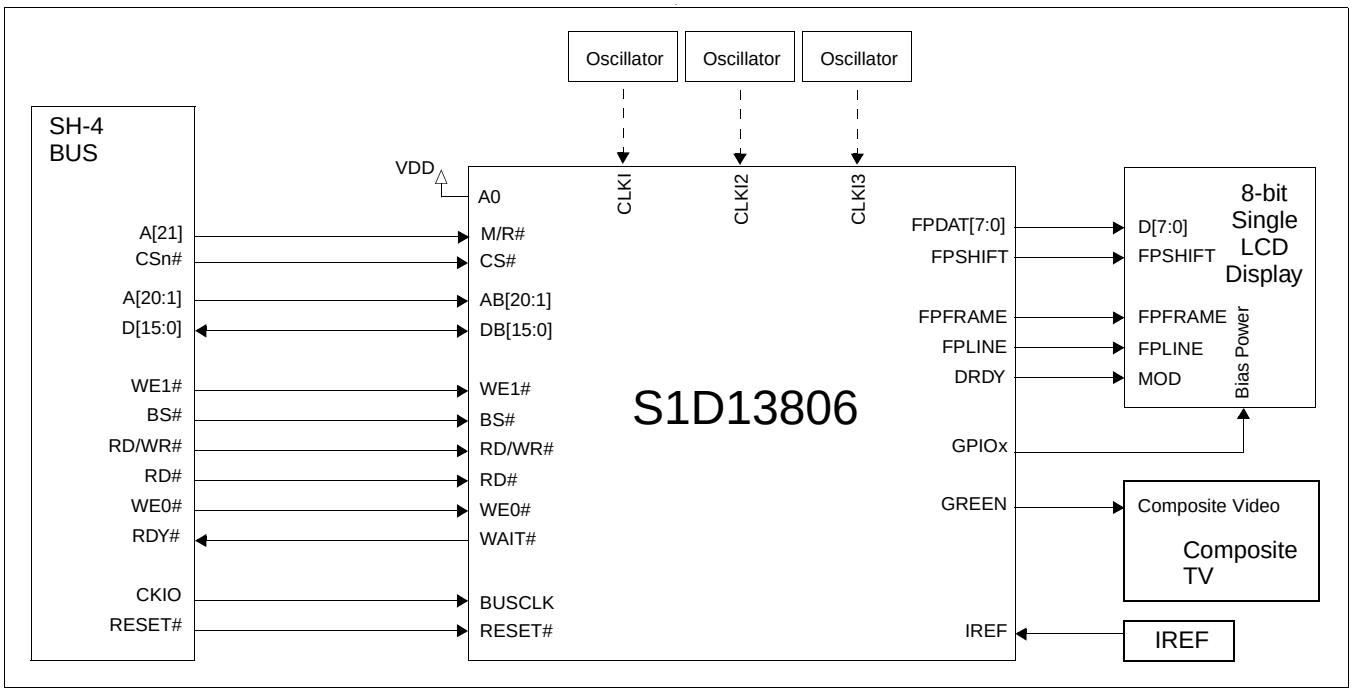



*Figure 3-2: Typical System Diagram (Hitachi SH-4 Bus)*

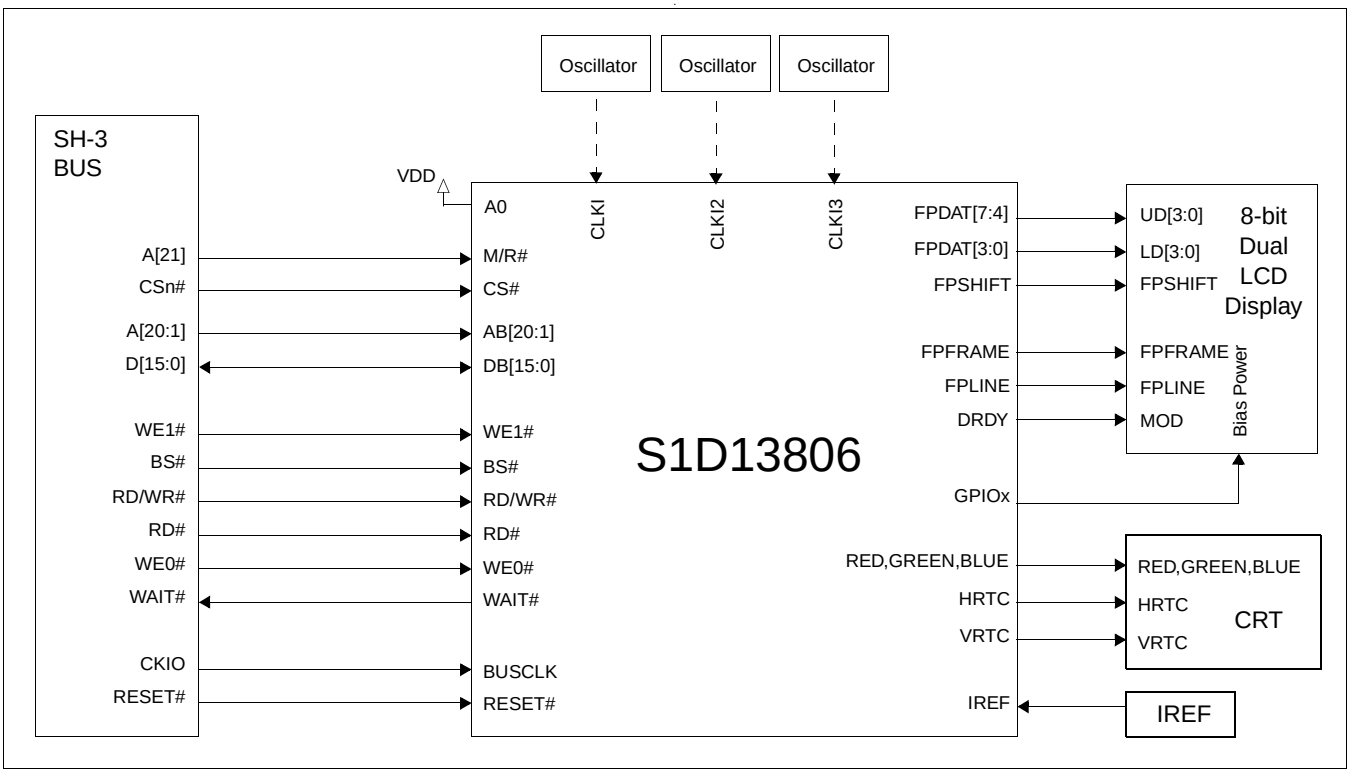



*Figure 3-3: Typical System Diagram (Hitachi SH-3 Bus)*

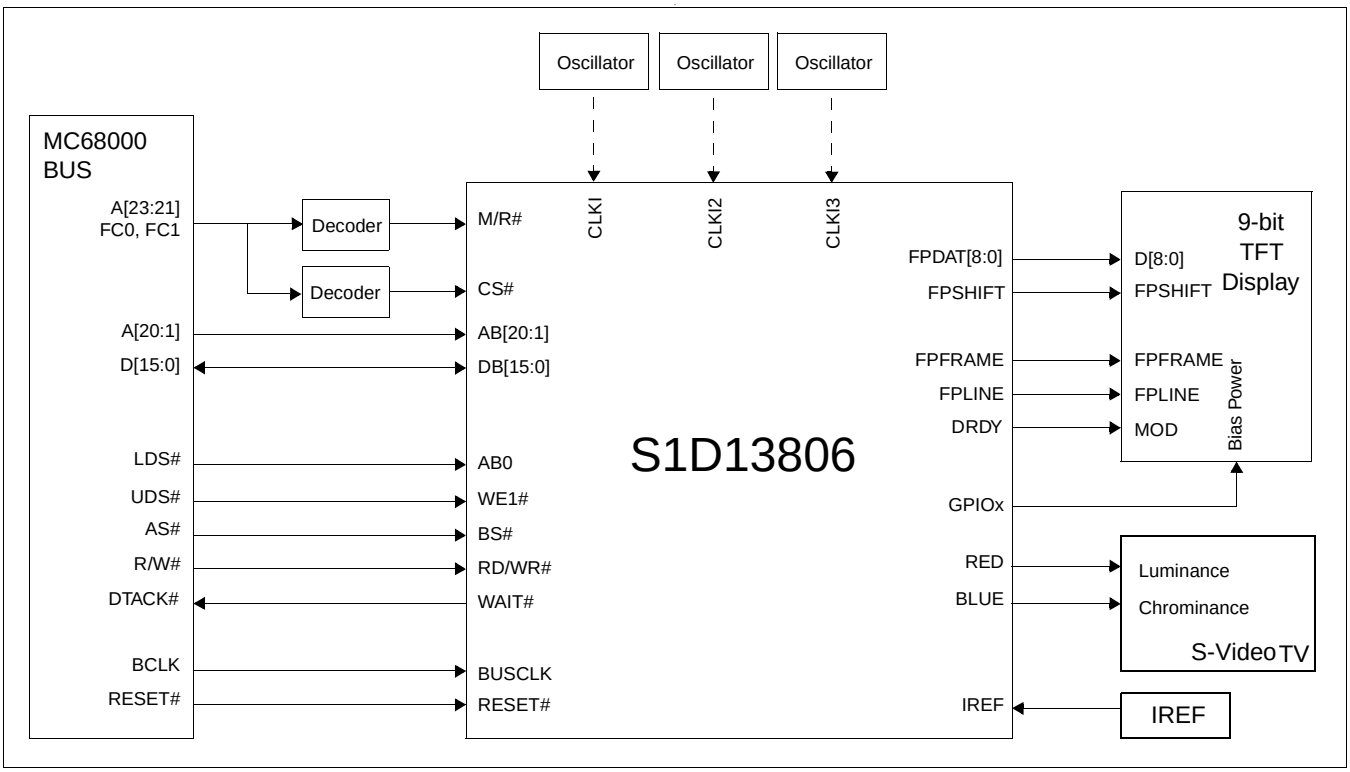



*Figure 3-4: Typical System Diagram (MC68K Bus 1, Motorola 16-Bit 68000)*

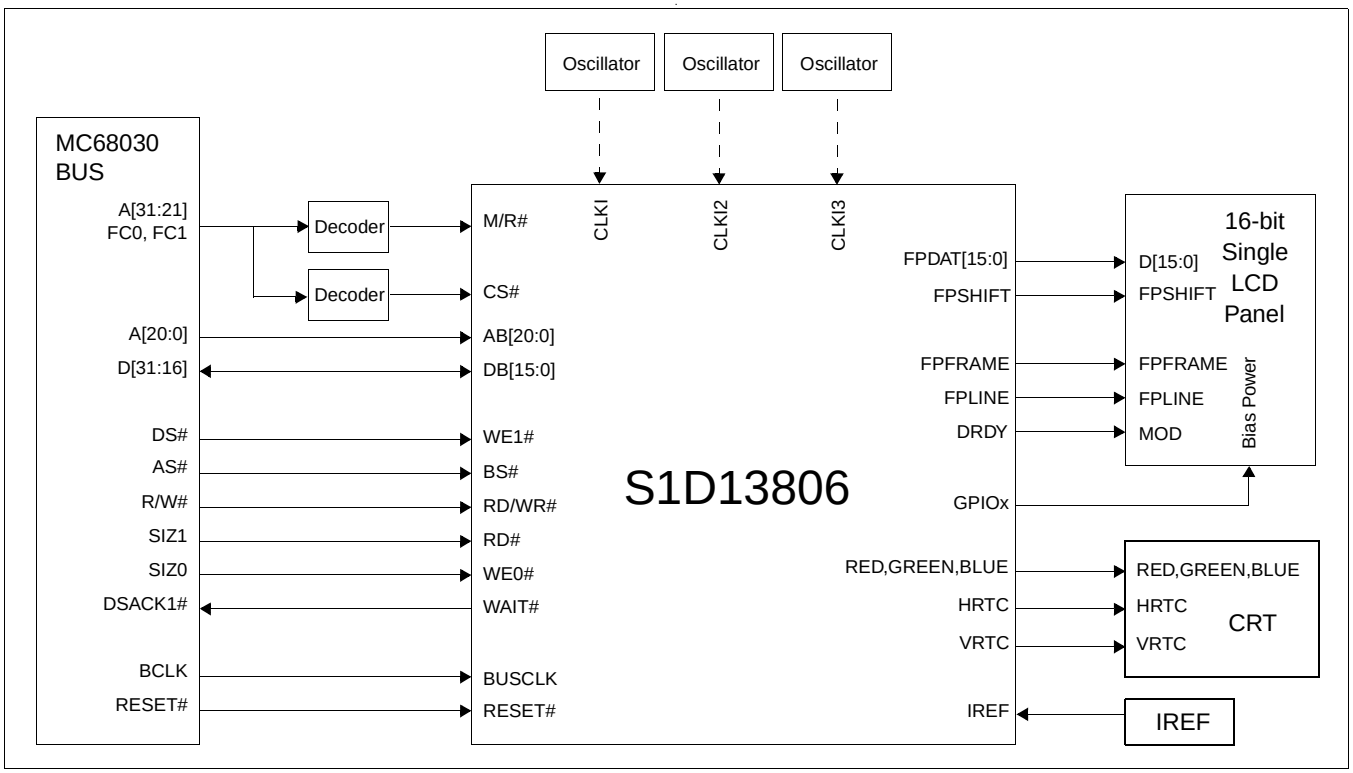



*Figure 3-5: Typical System Diagram (MC68K Bus 2, Motorola 32-Bit 68030)*

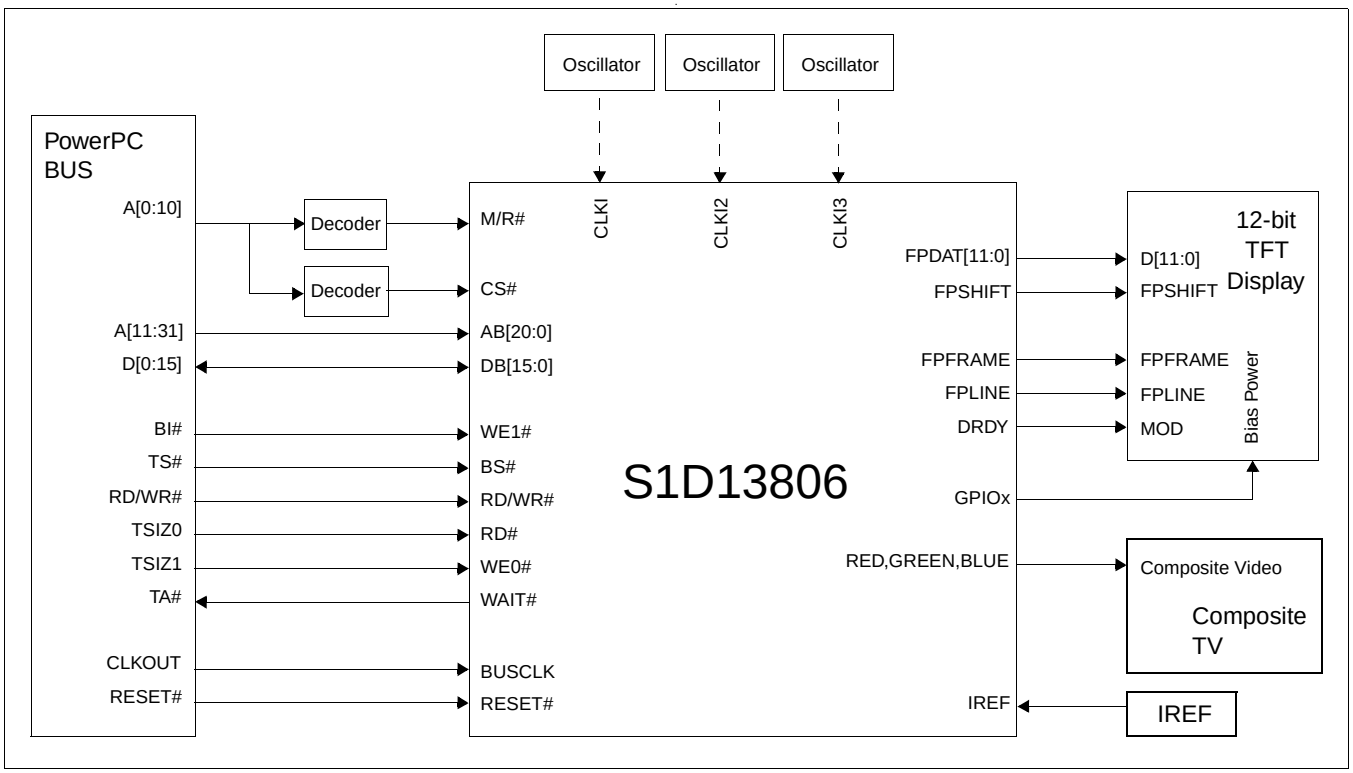



*Figure 3-6: Typical System Diagram (Motorola Power PC Bus)*

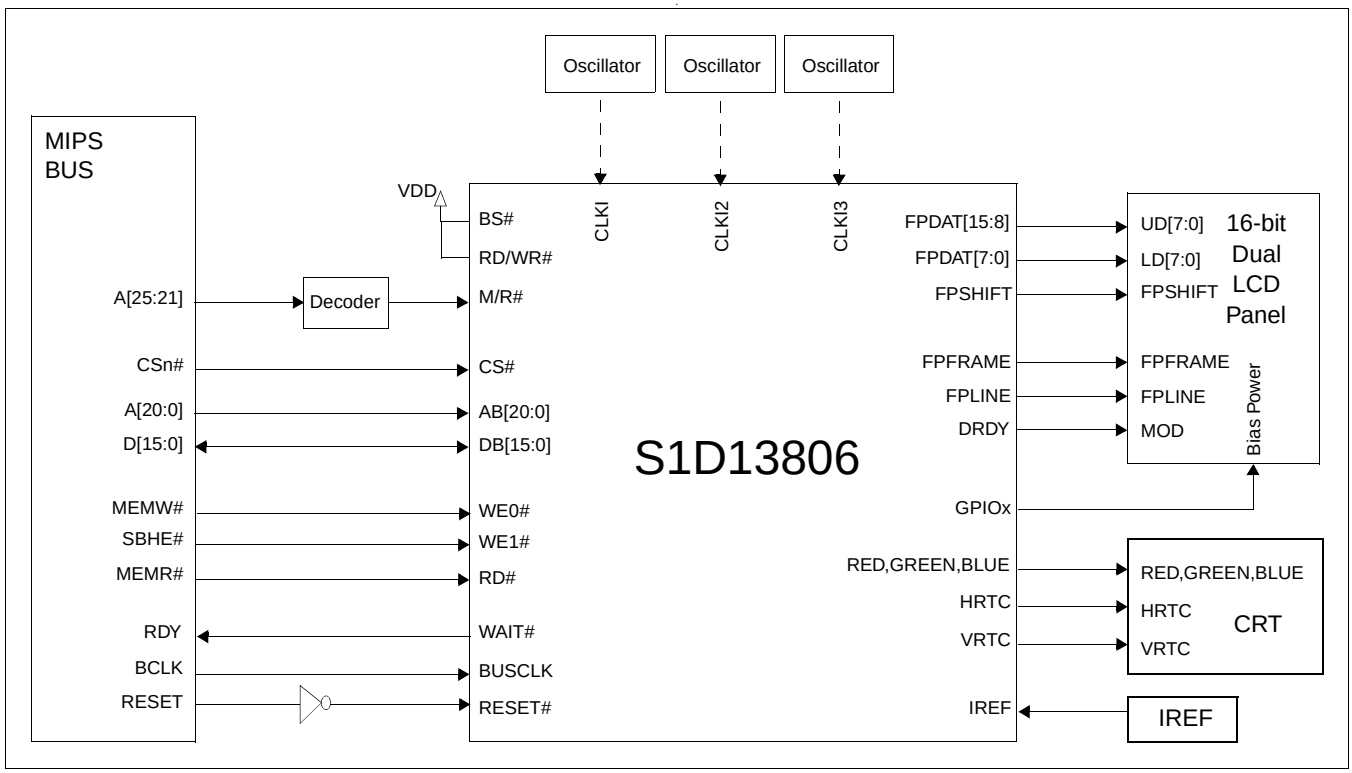



*Figure 3-7: Typical System Diagram (NEC MIPS VR41xx Bus)*

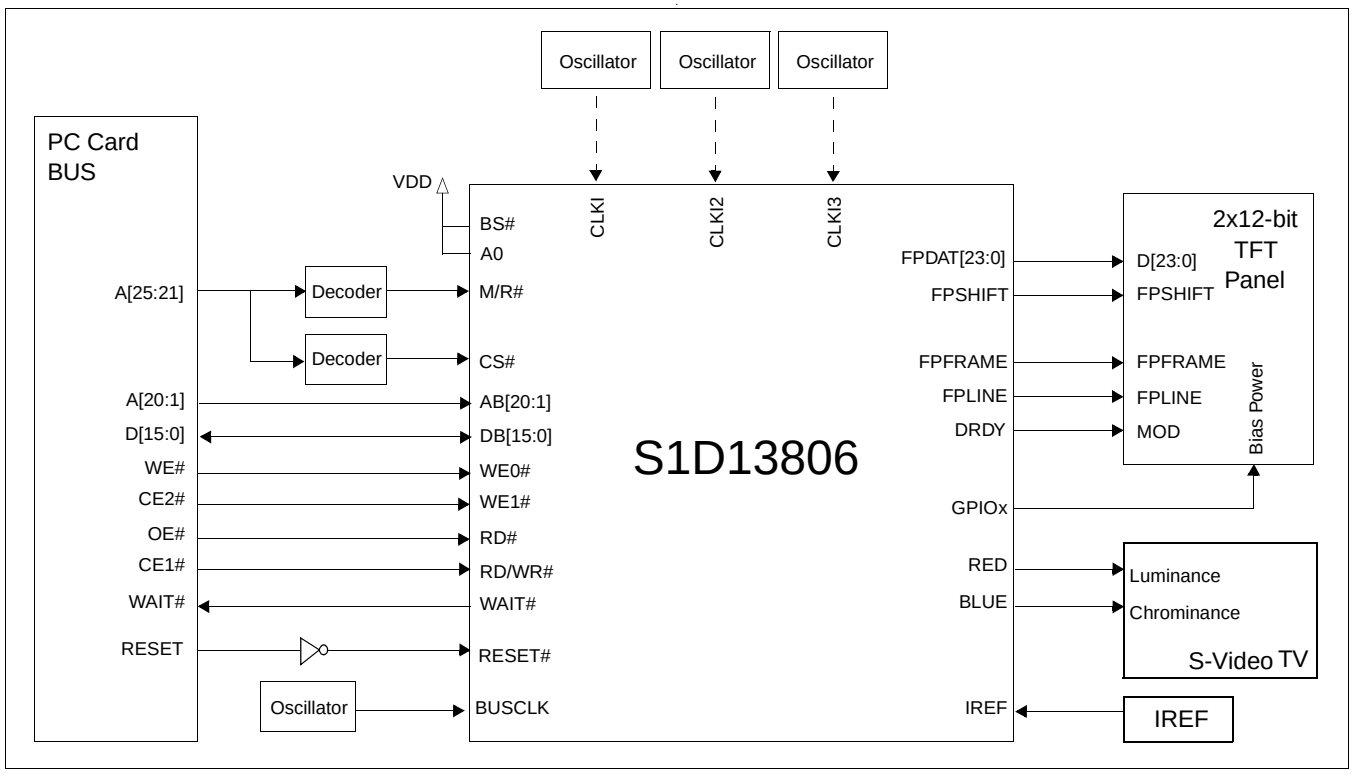



*Figure 3-8: Typical System Diagram (PC Card Bus)*

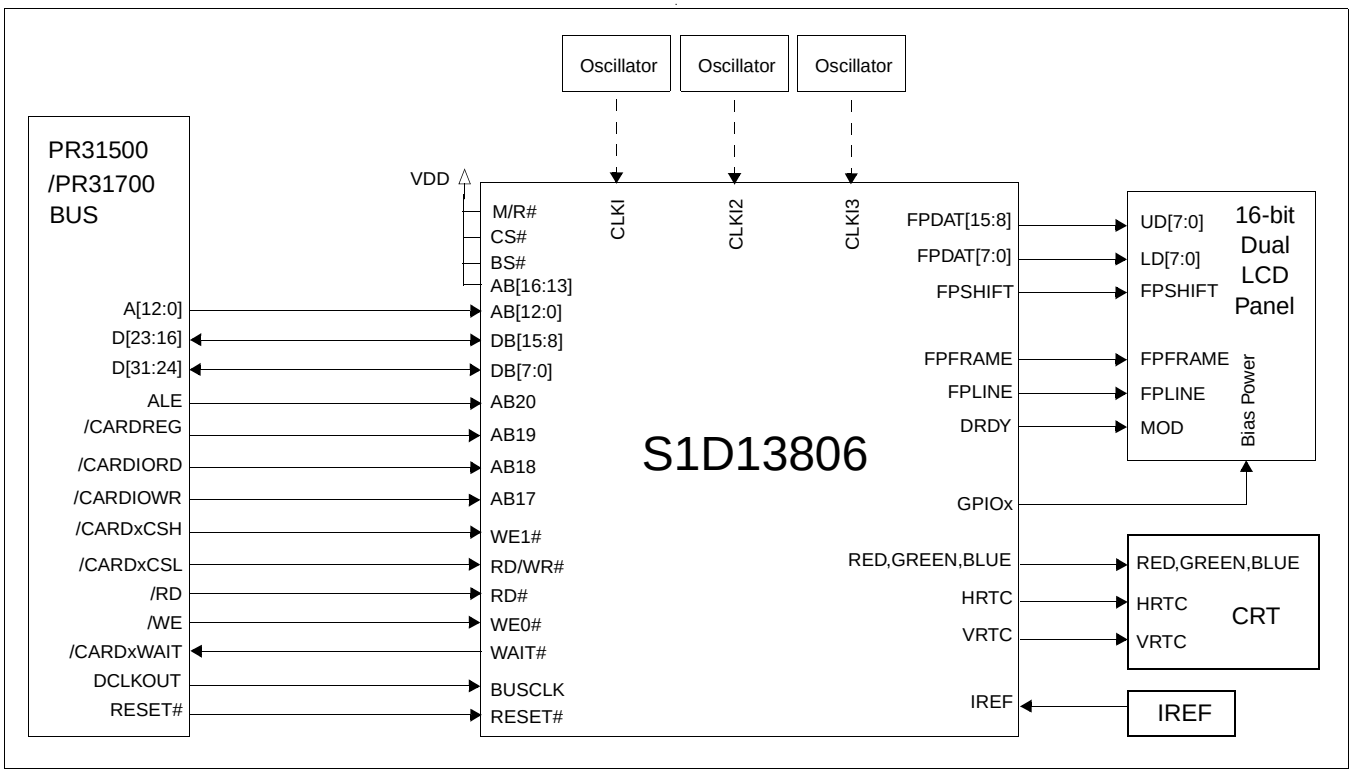



*Figure 3-9: Typical System Diagram (Philips MIPS PR31500/PR31700 Bus)*

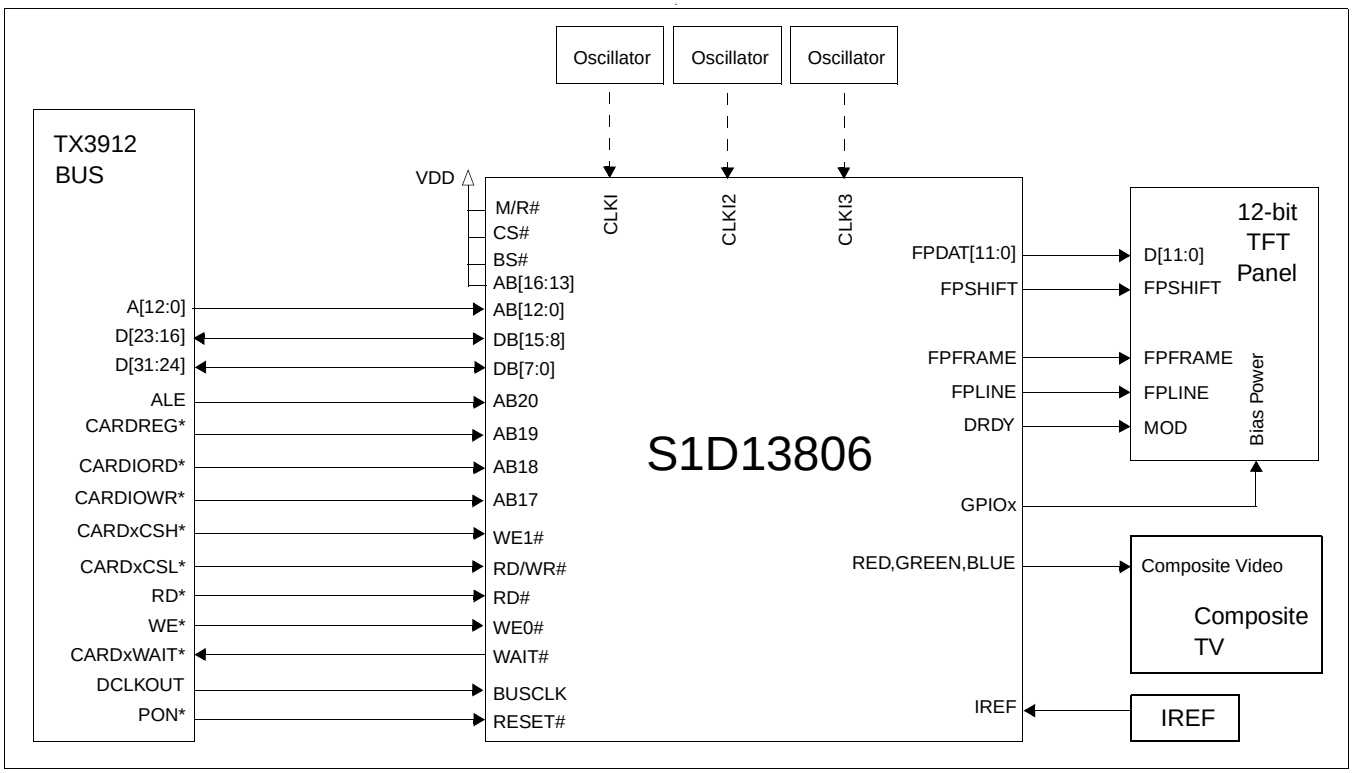



*Figure 3-10: Typical System Diagram (Toshiba MIPS TX39xx Bus)*

# 4 Pins

## 4.1 Pinout Diagram

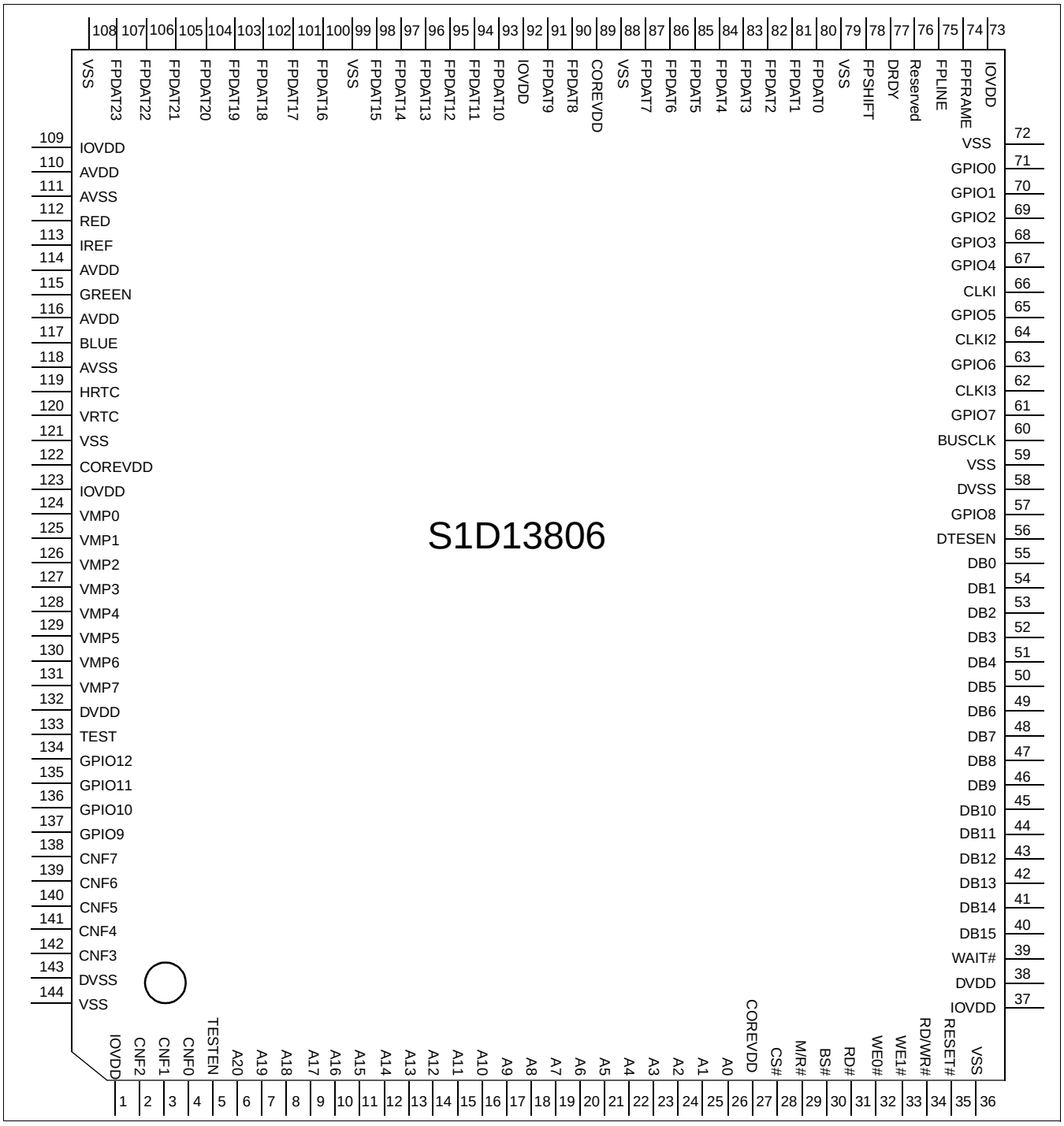



*Figure 4-1: Pinout Diagram* 144-Pin QFP20 Surface Mount Packages

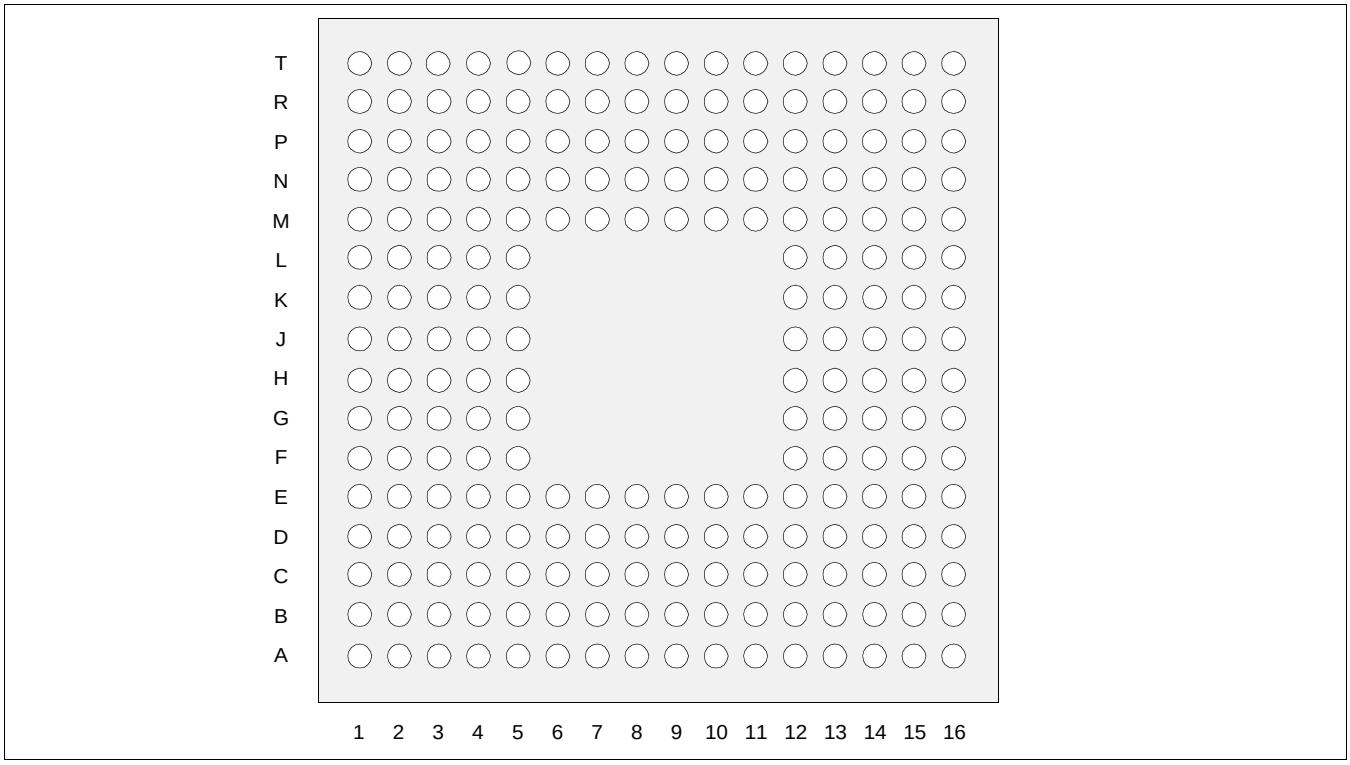



*Figure 4-2: Pinout Diagram 220-Pin PFBGA Surface Mount Package*

*Table 4-1: PFBGA 220-pin Mapping*

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **T** | AB | NC | DVDD | NC | DB12 | NC | DB6 | DB2 | DTESTEN | BUSCLK | GPIO6 | CLKI | NC | GPIO0 | NC | NC |
| **R** | NC | NC | NC | NC | DB13 | DB10 | DB7 | DB4 | NC | DVSS | GPIO7 | GPIO5 | GPIO4 | NC | NC | NC |
| **P** | RESET# | RD/WR# | NC | WAIT# | DB14 | DB11 | DB8 | DB5 | DB0 | NC | NC | GPIO3 | GPIO1 | NC | NC | FPFRAME |
| **N** | WE1# | NC | NC | NC | IOVDD | NC | NC | DB3 | GPIO8 | CLKI3 | NC | VSS | NC | FPLINE | NC | NC |
| **M** | BS# | M/R# | WE0# | VSS | NC | DB15 | DB9 | DB1 | VSS | CLKI2 | GPIO2 | NC | IOVDD | DRDY | FPSHIFT | VSS |
| **L** | COREVDD | AB1 | NC | RD# | NC | | | | | | | Reserved | NC | FPDAT0 | FPDAT1 | NC |
| **K** | AB2 | AB4 | NC | AB0 | CS# | | | | | | | FPDAT2 | FPDAT5 | FPDAT3 | FPDAT4 | NC |
| **J** | AB6 | NC | AB7 | AB5 | AB3 | | | | | | | FPDAT8 | VSS | FPDAT6 | PFDAT7 | COREVDD |
| **H** | AB9 | AB11 | AB12 | AB10 | AB8 | | | | | | | FPDAT12 | FPDAT10 | FPDAT9 | NC | IOVDD |
| **G** | NC | AB14 | AB15 | AB13 | AB17 | | | | | | | FPDAT16 | FPDAT15 | NC | FPDAT11 | FPDAT13 |
| **F** | AB16 | NC | AB18 | NC | CNF0 | | | | | | | FPDAT21 | NC | NC | FPDAT14 | VSS |
| **E** | AB19 | AB20 | TESTEN | IOVDD | NC | CNF4 | GPIO10 | VMP7 | VMP2 | NC | RED | NC | VSS | FPDAT20 | FPDAT17 | FPDAT18 |
| **D** | NC | NC | CNF1 | NC | VSS | NC | GPIO12 | VMP5 | VMP0 | NC | AVDD | IOVDD | NC | FPDAT22 | FPDAT19 | NC |
| **C** | CNF2 | NC | NC | CNF3 | CNF5 | NC | NC | VMP3 | COREVDD | HRTC | BLUE | AVDD | NC | NC | NC | FPDAT23 |
| **B** | NC | NC | NC | CNF6 | GPIO9 | TEST | VMP6 | NC | IOVDD | VRTC | AVSS | GREEN | AVSS | NC | NC | NC |
| **A** | NC | NC | DVSS | NC | CNF7 | GPIO11 | DVDD | VMP4 | VMP1 | VSS | NC | NC | IREF | AVDD | NC | NC |
| | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** |

**Note**

NC is no connection.

Reserved must be left unconnected and floating.

## 4.2 Pin Description

**Key:**

| | | |
|---|---|---|
| Hi-Z | = | High impedance |
| I | = | Input |
| O | = | Output |
| IO | = | Bi-Directional (Input/Output) |
| A | = | Analog |
| P | = | Power pin |
| C | = | CMOS level input |
| CD | = | CMOS level input with pull down resistor (typical value of 50KΩ at 3.3V) |
| CS | = | CMOS level Schmitt input |
| COx | = | CMOS output driver, x denotes driver type (1=2/-2mA, 2=6/-6mA @ 3.3V) |
| TSx | = | Tri-state CMOS output driver, x denotes driver type (1=2/-2mA, 2=6/-6mA @ 3.3V) |
| TSxU | = | Tri-state CMOS output driver with pull up resistor (typical value of 100KΩ at 3.3V), x denotes driver type (1=2/-2mA, 2=6/-6mA @ 3.3V) |
| TSxD | = | Tri-state CMOS output driver with pull down resistor (typical value of 100KΩ at 3.3V), x denotes driver type (1=2/-2mA, 2=6/-6mA @ 3.3V) |

### 4.2.1 Host Interface

*Table 4-2 : Host Interface Pin Descriptions*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| AB0 | I | 26 | K4 | CS | Hi-Z | • For Generic Bus, this pin must be connected to $V_{SS}$ or IO $V_{DD}$.<br>• For SH-4/SH-3 Bus, this pin must be connected to $V_{SS}$ or IO $V_{DD}$.<br>• For MC68K Bus 1, this pin inputs the lower data strobe (LDS#).<br>• For MC68K Bus 2, this pin inputs system address bit 0 (A0).<br>• For MIPS/ISA Bus, this pin inputs system address bit 0 (SA0).<br>• For PC Card (PCMCIA) Bus, this pin must be connected to $V_{SS}$ or IO $V_{DD}$.<br>• For Philips PR31500/31700 Bus, this pin inputs system address bit 0 (A0).<br>• For Toshiba TX3912 Bus, this pin inputs system address bit 0 (A0).<br>• For PowerPC Bus, this pin inputs system address bit 31 (A31).<br>SeeTable 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| AB[12:1] | I | 14-25 | H3, H2, H4, H1, H5, J3, J1, J4, K2, J5, K1, L2 | C | Hi-Z | • For PowerPC Bus, these pins input the system address bits 19 through 30 (A[19:30]).<br>• For all other busses, these pins input the system address bits 12 through 1 (A[12:1]).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |

*Table 4-2 : Host Interface Pin Descriptions (Continued)*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| AB[16:13] | I | 10-13 | F1, G3, G2, G4 | C | Hi-Z | • For Philips PR31500/31700 Bus, these pins are connected to $V_{DD}$.<br>• For Toshiba TX3912 Bus, these pins are connected to $V_{DD}$.<br>• For PowerPC Bus, these pins input the system address bits 15 through 18 (A[15:18]).<br>• For all other busses, these pins input the system address bits 16 through 13 (A[16:13]).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| AB17 | I | 9 | G5 | C | Hi-Z | • For Philips PR31500/31700 Bus, this pin inputs the IO write command (/CARDIOWR).<br>• For Toshiba TX3912 Bus, this pin inputs the IO write command (CARDIOWR*).<br>• For PowerPC Bus, this pin inputs the system address bit 14 (A14).<br>• For all other busses, this pin inputs the system address bit 17 (A17).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| AB18 | I | 8 | F3 | C | Hi-Z | • For Philips PR31500/31700 Bus, this pin inputs the IO read command (/CARDIORD).<br>• For Toshiba TX3912 Bus, this pin inputs the IO read command (CARDIORD*).<br>• For PowerPC Bus, this pin inputs the system address bit 13 (A13).<br>• For all other busses, this pin inputs the system address bit 18 (A18).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| AB19 | I | 7 | E1 | C | Hi-Z | • For Philips PR31500/31700 Bus, this pin inputs the card control register access (/CARDREG).<br>• For Toshiba TX3912 Bus, this pin inputs the card control register access (CARDREG*).<br>• For PowerPC Bus, this pin inputs the system address bit 12 (A12).<br>• For all other busses, this pin inputs the system address bit 19 (A19).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| AB20 | I | 6 | E2 | C | Hi-Z | • For the MIPS/ISA Bus, this pin inputs system address bit 20. Note that for the ISA Bus, the unlatched LA20 must first be latched before input to AB20.<br>• For Philips PR31500/31700 Bus, this pin inputs the address latch enable (ALE).<br>• For Toshiba TX3912 Bus, this pin inputs the address latch enable (ALE).<br>• For PowerPC Bus, this pin inputs the system address bit 11 (A11).<br>• For all other busses, this pin inputs the system address bit 20 (A20).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |

*Table 4-2 : Host Interface Pin Descriptions (Continued)*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| DB[15:0] | IO | 40-55 | M6, P5, R5, T5, P6, R6, M7, P7, R7, T7, P8, R8, N8, T8, M8, P9 | C/TS2 | Hi-Z | These pins are the system data bus.<br>• For SH-3/SH-4 Bus, these pins are connected to D[15:0].<br>• For MC68K Bus 1, these pins are connected to D[15:0].<br>• For MC68K Bus 2, these pins are connected to D[31:16] for 32-bit devices (e.g. MC68030) or D[15:0] for 16-bit devices (e.g. MC68340).<br>• For Generic Bus, these pins are connected to D[15:0].<br>• For MIPS/ISA Bus, these pins are connected to SD[15:0].<br>• For Philips PR31500/31700 Bus, pins DB[15:8] are connected to D[23:16] and pins DB[7:0] are connected to D[31:24].<br>• For Toshiba TX3912 Bus, pins DB[15:8] are connected to D[23:16] and pins DB[7:0] are connected to D[31:24].<br>• For PowerPC Bus, these pins are connected to D[0:15].<br>• For PC Card (PCMCIA) Bus, these pins are connected to D[15:0].<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| WE1# | IO | 33 | N1 | CS/TS2 | Hi-Z | This is a multi-purpose pin:<br>• For SH-3/SH-4 Bus, this pin inputs the write enable signal for the upper data byte (WE1#).<br>• For MC68K Bus 1, this pin inputs the upper data strobe (UDS#).<br>• For MC68K Bus 2, this pin inputs the data strobe (DS#).<br>• For Generic Bus, this pin inputs the write enable signal for the upper data byte (WE1#).<br>• For MIPS/ISA Bus, this pin inputs the system byte high enable signal (SBHE#).<br>• For Philips PR31500/31700 Bus, this pin inputs the odd byte access enable signal (/CARDxCSH).<br>• For Toshiba TX3912 Bus, this pin inputs the odd byte access enable signal (CARDxCSH*).<br>• For PowerPC Bus, this pin outputs the burst inhibit signal (BI#).<br>• For PC Card (PCMCIA) Bus, this pin inputs the card enable 2 signal (CE2#).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| M/R# | I | 29 | M2 | C | Hi-Z | • For Philips PR31500/31700 Bus, this pin is connected to $V_{DD}$.<br>• For Toshiba TX3912 Bus, this pin is connected to $V_{DD}$.<br>• For all other busses, this input pin is used to select between the display buffer and register address spaces of the S1D13806. M/R# is set high to access the display buffer and low to access the registers. See *Register Mapping*.<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34. |
| CS# | I | 28 | K5 | C | Hi-Z | • For Philips PR31500/31700 Bus, this pin is connected to $V_{DD}$.<br>• For Toshiba TX3912 Bus, this pin is connected to $V_{DD}$.<br>• For all other busses, this is the Chip Select input.<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34. See the respective AC Timing diagram for detailed functionality. |

*Table 4-2 : Host Interface Pin Descriptions (Continued)*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| BUSCLK | I | 60 | T10 | C | Hi-Z | This pin inputs the system bus clock. It is possible to apply a 2x clock and divide it by 2 internally - see CONF5 in *Summary of Configuration Options*.<br>• For SH-3/SH-4 Bus, this pin is connected to CKIO.<br>• For MC68K Bus 1, this pin is connected to CLK.<br>• For MC68K Bus 2, this pin is connected to CLK.<br>• For Generic Bus, this pin is connected to BCLK.<br>• For MIPS/ISA Bus, this pin is connected to CLK.<br>• For Philips PR31500/31700 Bus, this pin is connected to DCLKOUT.<br>• For Toshiba TX3912 Bus, this pin is connected to DCLKOUT.<br>• For PowerPC Bus, this pin is connected to CLKOUT.<br>• For PC Card (PCMCIA) Bus, this pin is connected to an external input clock source.<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| BS# | I | 30 | M1 | CS | Hi-Z | This is a multi-purpose pin:<br>• For SH-3/SH-4 Bus, this pin inputs the bus start signal (BS#).<br>• For MC68K Bus 1, this pin inputs the address strobe (AS#).<br>• For MC68K Bus 2, this pin inputs the address strobe (AS#).<br>• For Generic Bus, this pin is connected to $V_{DD}$.<br>• For MIPS/ISA Bus, this pin is connected to $V_{DD}$.<br>• For Philips PR31500/31700 Bus, this pin is connected to $V_{DD}$.<br>• For Toshiba TX3912 Bus, this pin is connected to $V_{DD}$.<br>• For PowerPC Bus, this pin inputs the Transfer Start signal (TS#).<br>• For PC Card (PCMCIA) Bus, this pin is connected to $V_{DD}$.<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| RD/WR# | I | 34 | P2 | CS | Hi-Z | This is a multi-purpose pin:<br>• For SH-3/SH-4 Bus, this pin inputs the read write signal (RD/WR#). The S1D13806 needs this signal for early decode of the bus cycle.<br>• For MC68K Bus 1, this pin inputs the read write signal (R/W#).<br>• For MC68K Bus 2, this pin inputs the read write signal (R/W#).<br>• For Generic Bus, this pin inputs the read command for the upper data byte (RD1#).<br>• For MIPS/ISA Bus, this pin is connected to $V_{DD}$.<br>• For Philips PR31500/31700 Bus, this pin inputs the even byte access enable signal (/CARDxCSL).<br>• For Toshiba TX3912 Bus, this pin inputs the even byte access enable signal (CARDxCSL*).<br>• For PowerPC Bus, this pin inputs the read write signal (RD/WR#).<br>• For PC Card (PCMCIA) Bus, this pin inputs the card enable 1 signal (CE1#).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |

*Table 4-2 : Host Interface Pin Descriptions (Continued)*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| RD# | I | 31 | L4 | CS | Hi-Z | This is a multi-purpose pin:<br>• For SH-3/SH-4 Bus, this pin inputs the read signal (RD#).<br>• For MC68K Bus 1, this pin is connected to $V_{DD}$.<br>• For MC68K Bus 2, this pin inputs the bus size bit 1 (SIZ1).<br>• For Generic Bus, this pin inputs the read command for the lower data byte (RD0#).<br>• For MIPS/ISA Bus, this pin inputs the memory read signal (MEMR#).<br>• For Philips PR31500/31700 Bus, this pin inputs the memory read command (/RD).<br>• For Toshiba TX3912 Bus, this pin inputs the memory read command (RD*).<br>• For PowerPC Bus, this pin inputs the transfer size 0 signal (TSIZ0).<br>• For PC Card (PCMCIA) Bus, this pin inputs the output enable signal (OE#).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| WE0# | I | 32 | M3 | CS | Hi-Z | This is a multi-purpose pin:<br>• For SH-3/SH-4 Bus, this pin inputs the write enable signal for the lower data byte (WE0#).<br>• For MC68K Bus 1, this pin must be connected to $V_{DD}$<br>• For MC68K Bus 2, this pin inputs the bus size bit 0 (SIZ0).<br>• For Generic Bus, this pin inputs the write enable signal for the lower data byte (WE0#).<br>• For MIPS/ISA Bus, this pin inputs the memory write signal (MEMW#).<br>• For Philips PR31500/31700 Bus, this pin inputs the memory write command (/WE).<br>• For Toshiba TX391 Bus, this pin inputs the memory write command (WE*).<br>• For PowerPC Bus, this pin inputs the Transfer Size 1 signal (TSIZ1).<br>• For PC Card (PCMCIA) Bus, this pin inputs the write enable signal (WE#).<br>See Table 4-10, “CPU Interface Pin Mapping,” on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |
| RESET# | I | 35 | P1 | CS | 0 | Active low input that clears all internal registers and forces all outputs to their inactive states. Note that active high RESET signals must be inverted before input to this pin.<br>• For Toshiba TX3912 Bus, this pin is called NOP*. |

*Table 4-2 : Host Interface Pin Descriptions (Continued)*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| WAIT# | IO | 39 | P4 | C/TS2 | Hi-Z | The active polarity of the WAIT# output is configurable; the state of CONF[3:0] on the rising edge of RESET# defines the active polarity of WAIT# for some busses - see *"Summary of Configuration Options"*.<br>• For SH-3 Bus, this pin outputs the wait request signal (WAIT#).<br>• For SH-4 Bus, this pin outputs the ready signal (RDY#).<br>• For MC68K Bus 1, this pin outputs the data transfer acknowledge signal (DTACK#).<br>• For MC68K Bus 2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#).<br>• For Generic Bus, this pin outputs the wait signal (WAIT#).<br>• For MIPS/ISA Bus, this pin outputs the IO channel ready signal (IOCHRDY).<br>• For Philips PR31500/31700 Bus, this pin outputs the wait state signal (/CARDxWAIT).<br>• For Toshiba TX3912 Bus, this pin outputs the wait state signal (CARDxWAIT*).<br>• For PowerPC Bus, this pin outputs the transfer acknowledge signal (TA#).<br>• For PC Card (PCMCIA) Bus, this pin outputs the wait signal (WAIT#).<br>See Table 4-10, "CPU Interface Pin Mapping," on page 34 for summary. See the respective AC Timing diagram for detailed functionality. |

**Note**

When WAIT# is always driven, WAIT# is in its inactive state at RESET#. CONF[3:0] determines whether WAIT# is active high or low.

### 4.2.2 LCD Interface

*Table 4-3 : LCD Interface Pin Descriptions*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| FPDAT[23:0] | O | 107-100, 91-90, 98-93, 87-80 | C16, D14, F12, E14, D15, E16, E15, G12, G13, F15, G16, H12, G15, H13, H14, J12, J15, J14, K13, K15, K14, K12, L15, L14 | CO2 | 0 | Panel data bus. Not all pins are used for some panels - see Table 4-10, “CPU Interface Pin Mapping,” on page 34 for details. Unused pins are driven low. |
| FPFRAME | O | 74 | P16 | CO2 | 0 | Frame pulse |
| FPLINE | O | 75 | N14 | CO2 | 0 | Line pulse |
| FPSHIFT | O | 78 | M15 | CO2 | 0 | Shift clock |
| DRDY | O | 77 | M14 | CO2 | 0 | This is a multi-purpose pin:<br>• For TFT/D-TFD panels this is the display enable output (DRDY).<br>• For passive LCD with Format 1 interface this is the 2nd Shift Clock (FPSHIFT2).<br>• For all other LCD panels this is the LCD backplane bias signal (MOD).<br>See Table 4-11, “LCD Interface Pin Mapping,” on page 35 and REG[030h] for details. |

### 4.2.3 MediaPlug Interface

*Table 4-4 : MediaPlug Pin Description*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| VMP[7] | O | 131 | E8 | CO2 | 0 | MediaPlug VMPLCTL pin. |
| VMP[6] | I | 130 | B7 | CD | Hi-Z | MediaPlug VMPRCTL pin.<br>Internal pull-down resistors (typical value of 50KΩ at 3.3V respectively) pull the reset states to 0. External pull-up resistors can be used to pull the reset states to 1. |
| VMP[5:2] | IO | 129-126 | D8, A8, C8, E9 | C/TS2U | 0 or Hi-Z | MediaPlug VMPD[0:3] pins. See Section 17.3, “MediaPlug Interface Pin Mapping” on page 188.<br>Internal pull-up resistors (typical value of 100KΩ at 3.3V respectively) pull the reset states to 1. External pull-down resistors can be used to pull the reset states to 0. |
| VMP[1] | O | 125 | A9 | CO2 | 0 | MediaPlug VMPCLK pin. |
| VMP[0] | O | 124 | D9 | CO2 | 0 | MediaPlug VMPCLKN pin. |

**Note**
The RESET# states of VMP[5:2] are 0 if VMP is enabled, otherwise Hi-Z.

**Note**
When the MediaPlug interface is enabled, GPIO12 is configured as the MediaPlug output pin VMPEPWR.

### 4.2.4 CRT Interface

*Table 4-5 : CRT Interface Pin Descriptions*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| HRTC | O | 119 | C10 | CO2 | 0 | Horizontal retrace signal for CRT |
| VRTC | O | 120 | B10 | CO2 | 0 | Vertical retrace signal for CRT |
| RED | O | 112 | E11 | A | — | Analog output for CRT color Red / S-Video Luminance |
| GREEN | O | 115 | B12 | A | — | Analog output for CRT color Green / Composite Video Out |
| BLUE | O | 117 | C11 | A | — | Analog output for CRT color Blue / S-Video Chrominance |
| IREF | I | 113 | A13 | A | — | Current reference for DAC. If the DAC is not needed, this pin must be left unconnected and floating. |

### 4.2.5 General Purpose IO

*Table 4-6 : General Purpose IO Pin Descriptions*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| GPIO12 | IO | 134 | D7 | C/TS2 | 1 or Hi-Z | Bi-directional GPIO pin.<br>When the MediaPlug interface is enabled, GPIO12 is configured as the MediaPlug output pin VMPEPWR. |
| GPIO[11:0] | IO | 135-137, 57, 61, 63, 65, 67-71 | A6, E7, B5, N9, R11, T11, R12, R13, P12, M11, P13, T14 | C/TS2 | Hi-Z | Bi-directional GPIO pin. |

**Note**
The RESET# state of GPIO12 is 1 if MediaPlug is enabled, otherwise Hi-Z.

### 4.2.6 Configuration

*Table 4-7 : Configuration Pin Descriptions*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| CONF[7:0] | I | 138-142, 2-4 | A5, B4, C5, E6, C4, C1, D3, F5 | C | Hi-Z | Input Configuration pin.<br>State of pins are latched at RESET# to configure S1D13806 -- Table 4.3, “Summary of Configuration Options,” on page 33 for details. |

### 4.2.7 Miscellaneous

*Table 4-8 : Miscellaneous Interface Pin Descriptions*

| Pin Name | Type | QFP Pin # | PFBGA Pin # | Cell | RESET# State | Description |
|---|---|---|---|---|---|---|
| CLKI | I | 66 | T12 | C | Hi-Z | Input clock for the internal pixel clock (PCLK), memory clock (MCLK), and MediaPlug clock. |
| CLKI2 | I | 64 | M10 | C | Hi-Z | Input clock for the internal pixel clock (PCLK) and MediaPlug clock. |
| CLKI3 | I | 62 | N10 | C | Hi-Z | Input clock for memory clock (MCLK) (Possible to use for PCLK and MediaPlug clock.) |
| TESTEN | I | 5 | E3 | CD | Hi-Z | Test Enable. This pin should be connected to $V_{SS}$ for normal operation. |
| DTESEN | I | 56 | T9 | C | Hi-Z | Test Enable for embedded SDRAM. This pin should be connected to $V_{SS}$ for normal operation. |
| TEST | — | 133 | B6 | — | — | Test Pin. **This pin must be left unconnected and floating.** |
| IOVDD | P | 1, 37, 73, 92, 109, 123 | E4, N5, M13, H16, D12, B9 | P | — | $V_{DD}$ for IO (IO $V_{DD}$) |
| COREVDD | P | 27, 89, 122 | L1, J16, C9 | P | — | $V_{DD}$ for core (Core $V_{DD}$) |
| AVDD | P | 110, 114, 116 | A14, C12, D11 | P | — | $V_{DD}$ for DAC (DAC $V_{DD}$). When the DAC is not used this pin must be connected to DVDD. |
| DVDD | P | 38, 132 | A7, T3 | P | — | $V_{DD}$ for embedded SDRAM (SDRAM $V_{DD}$) |
| VSS | P | 36, 59, 72, 79, 88, 99, 108, 121, 144 | M4, M9, N12, M16, J13, F16, E13, A10, D5 | P | — | $V_{SS}$ |
| AVSS | P | 111, 118 | B13, B11 | P | — | $V_{SS}$ for DAC (DAC $V_{SS}$) |
| DVSS | P | 58, 143 | A3, R10 | P | — | $V_{SS}$ for embedded SDRAM (SDRAM $V_{SS}$) |
| Reserved | — | 76 | L12 | -- | — | **This pin must be left unconnected and floating.** |

## 4.3 Summary of Configuration Options

*Table 4-9 : Summary of Power-On/Reset Options*

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="6">state of this pin at rising edge of RESET# is used to configure: (1/0)</th></tr>
<tr><th colspan="5">1</th><th>0</th></tr>
<tr><td>CONF6, CONF[3:0]</td><td colspan="6">Select host bus interface as follows:<br>
<table>
<tr><th>CONF6</th><th>CONF3</th><th>CONF2</th><th>CONF1</th><th>CONF0</th><th>Host Bus</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Generic; Little Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Generic; Little Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Generic; Little Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Generic; Big Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Generic; Big Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Generic; Big Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>MIPS/ISA; Little Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>MIPS/ISA; Little Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>MIPS/ISA; Little Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>MC68000; Big Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>MC68030; Big Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>PR31500/31700/TX3912; Little Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>PR31500/31700/TX3912; Little Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>PC Card; Little Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>PC Card; Little Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>MPC821; Big Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>SH3; Little Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>SH3; Little Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>SH4; Little Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>SH3; Big Endian; Active Low WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>SH3; Big Endian; Active Low WAIT# always driven</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>SH4; Big Endian; Active High WAIT# with tristate note</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>CONF4</td><td colspan="6">Reserved. Must be tied to ground.</td></tr>
<tr><td>CONF5</td><td colspan="5">BUSCLK input divided by 2</td><td>BUSCLK input not divided</td></tr>
<tr><td>CONF7</td><td colspan="5">Configures GPIO12 as MediaPlug output pin VMPEPWR and enables MediaPlug functionality.</td><td>Configure GPIO12 for normal use and disables MediaPlug functionality.</td></tr>
</table>

**Note**

WAIT# is tristated (high impedance) when the chip is not accessed by the host

## 4.4 Multiple Function Pin Mapping

*Table 4-10 : CPU Interface Pin Mapping*

| S1D13806 Pin Names | Generic | Hitachi SH-4/ SH-3 | MIPS/ISA | Motorola MC68K Bus 1 | Motorola MC68K Bus 2 | Motorola PowerPC | PC Card | Philips PR31500 /PR31700 | Toshiba TX3912 |
|---|---|---|---|---|---|---|---|---|---|
| AB20 | A20 | A20 | LatchA20 | A20 | A20 | A11 | A20 | ALE | ALE |
| AB19 | A19 | A19 | SA19 | A19 | A19 | A12 | A19 | /CARDREG | CARDREG* |
| AB18 | A18 | A18 | SA18 | A18 | A18 | A13 | A18 | /CARDIORD | CARDIORD* |
| AB17 | A17 | A17 | SA17 | A17 | A17 | A14 | A17 | /CARDIOWR | CARDIOWR* |
| AB[16:13] | A[16:13] | A[16:13] | SA[16:13] | A[16:13] | A[16:13] | A[15:18] | A[16:13] | Connected to $V_{DD}$ | |
| AB[12:1] | A[12:1] | A[12:1] | SA[12:1] | A[12:1] | A[12:1] | A[19:30] | A[12:1] | A[12:1] | A[12:1] |
| AB0 | Connected to $V_{DD}$[1] | Connected to $V_{DD}$[1] | SA0 | LDS# | A0 | A31 | Connected to $V_{DD}$[1] | A0 | A0 |
| DB[15:8] | D[15:0] | D[15:8] | SD[15:0] | D[15:8] | D[31:24] | D[0:7] | D[15:0] | D[23:16] | D[23:16] |
| DB[7:0] | D[7:0] | D[7:0] | SD[7:0] | D[7:0] | D[23:16] | D[8:15] | D[7:0] | D[31:24] | D[31:24] |
| WE1# | WE1# | WE1# | SBHE# | UDS# | DS# | BI# | CE2# | /CARDxCSH | CARDxCSH* |
| M/R# | External Decode | | | | | | | Connected to $V_{DD}$ | |
| CS# | External Decode | | | | | | | Connected to $V_{DD}$ | |
| BUSCLK | BCLK | CKIO | CLK | CLK | CLK | CLKOUT | External Oscillator[2] | DCLKOUT | DCLKOUT |
| BS# | Connected to $V_{DD}$ | BS# | Connected to $V_{DD}$ | AS# | AS# | TS# | Connected to $V_{DD}$ | Connected to $V_{DD}$ | |
| RD/WR# | RD1# | RD/WR# | Connected to $V_{DD}$ | R/W# | R/W# | RD/WR# | CE1# | /CARDxCSL | CARDxCSL* |
| RD# | RD0# | RD# | MEMR# | Connected to $V_{DD}$ | SIZ1 | TSIZ0 | OE# | /RD | RD* |
| WE0# | WE0# | WE0# | MEMW# | Connected to $V_{DD}$ | SIZ0 | TSIZ1 | WE# | /WE | WE* |
| WAIT# | WAIT# | WAIT# | IOCHRDY | DTACK# | DSACK1# | TA# | WAIT# | /CARDxWAIT | CARDxWAIT* |
| RESET# | RESET# | RESET# | inverted RESET | RESET# | RESET# | RESET# | inverted RESET | RESET# | PON* |

**Note**

All GPIO pins default to input on reset and unless programmed otherwise, must be connected to either $V_{SS}$ or IO $V_{DD}$ if not used.

**Note**

[1] AB0 is not used internally for these busses and must be connected to either $V_{SS}$ or IO $V_{DD}$.

[2] For further information on interfacing the S1D13806 to the PC Card bus, see *Interfacing to the PC Card Bus*, document number X28B-G-005-xx.

## 4.5 LCD Interface Pin Mapping

*Table 4-11 : LCD Interface Pin Mapping*

| S1D13806 Pin Names | Monochrome Passive Panel | | | Color Passive Panel | | | | | | Color Active (TFT) Panel | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Single | | Dual | Single | Single Format 1 | Single Format 2 | Single | Dual | | | | | | |
| | 4-bit | 8-bit | 8-bit | 4-bit | 8-bit | 8-bit | 16-Bit | 8-bit | 16-bit | 9-bit | 12-bit | 18-bit | 2x9-bit | 2x12-bit |
| FPFRAME | FPFRAME | | | | | | | | | | | | | |
| FPLINE | FPLINE | | | | | | | | | | | | | |
| FPSHIFT | FPSHIFT | | | | | | | | | | | | | |
| DRDY | MOD | | | | FPSHIFT2 | MOD | | | | DRDY | | | | |
| FPDAT0 | driven 0 | D0 | LD0 | driven 0 | D0 (B5)[1] | D0 (G3)[1] | D0 (R6)[1] | LD0 (241-R2)[1] | LD0 (241-G3)[1] | R2 | R3 | R5 | R02 | R03 |
| FPDAT1 | driven 0 | D1 | LD1 | driven 0 | D1 (R5)[1] | D1 (R3)[1] | D1 (G5)[1] | LD1 (241-B1)[1] | LD1 (241-R3)[1] | R1 | R2 | R4 | R01 | R02 |
| FPDAT2 | driven 0 | D2 | LD2 | driven 0 | D2 (G4)[1] | D2 (B2)[1] | D2 (B4)[1] | LD2 (241-G1)[1] | LD2 (241-B2)[1] | R0 | R1 | R3 | R00 | R01 |
| FPDAT3 | driven 0 | D3 | LD3 | driven 0 | D3 (B3)[1] | D3 (G2)[1] | D3 (R4)[1] | LD3 (241-R1)[1] | LD3 (241-G2)[1] | G2 | G3 | G5 | G02 | G03 |
| FPDAT4 | D0 | D4 | UD0 | D0 (R2)[1] | D4 (R3)[1] | D4 (R2)[1] | D8 (B5)[1] | UD0 (1-R2)[1] | UD0 (1-G3)[1] | G1 | G2 | G4 | G01 | G02 |
| FPDAT5 | D1 | D5 | UD1 | D1 (B1)[1] | D5 (G2)[1] | D5 (B1)[1] | D9 (R5)[1] | UD1 (1-B1)[1] | UD1 (1-R3)[1] | G0 | G1 | G3 | G00 | G01 |
| FPDAT6 | D2 | D6 | UD2 | D2 (G1)[1] | D6 (B1)[1] | D6 (G1)[1] | D10 (G4)[1] | UD2 (1-G1)[1] | UD2 (1-B2)[1] | B2 | B3 | B5 | B02 | B03 |
| FPDAT7 | D3 | D7 | UD3 | D3 (R1)[1] | D7 (R1)[1] | D7 (R1)[1] | D11 (B3)[1] | UD3 (1-R1)[1] | UD3 (1-G2)[1] | B1 | B2 | B4 | B01 | B02 |
| FPDAT8 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D4 (G3)[1] | driven 0 | LD4 (241-R2)[1] | B0 | B1 | B3 | B00 | B01 |
| FPDAT9 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D5 (B2)[1] | driven 0 | LD5 (241-B1)[1] | driven 0 | R0 | R2 | driven 0 | R00 |
| FPDAT10 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D6 (R2)[1] | driven 0 | LD6 (241-G1)[1] | driven 0 | driven 0 | R1 | R12 | R13 |
| FPDAT11 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D7 (G1)[1] | driven 0 | LD7 (241-R1)[1] | driven 0 | G0 | G2 | driven 0 | G00 |
| FPDAT12 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D12 (R3)[1] | driven 0 | UD4 (1-R2)[1] | driven 0 | driven 0 | G1 | G12 | G13 |
| FPDAT13 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D13 (G2)[1] | driven 0 | UD5 (1-B1)[1] | driven 0 | driven 0 | G0 | G11 | G12 |
| FPDAT14 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D14 (B1)[1] | driven 0 | UD6 (1-G1)[1] | driven 0 | B0 | B2 | driven 0 | B00 |
| FPDAT15 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | D15 (R1)[1] | driven 0 | UD7 (1-R1)[1] | driven 0 | driven 0 | B1 | B12 | B13 |
| FPDAT16 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | B0 | B11 | B12 |
| FPDAT17 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | R0 | R11 | R12 |
| FPDAT18 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | R10 | R11 |
| FPDAT19 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | R10 |
| FPDAT20 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | G10 | G11 |
| FPDAT21 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | G10 |
| FPDAT22 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | B10 | B11 |
| FPDAT23 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | driven 0 | B10 |

**Note**

[1]These pin mappings use signal names commonly used for each panel type, however signal names may differ between panel manufacturers. The values shown in brackets represent the color components as mapped to the corresponding FPDATxx signals at the first valid edge of FPSHIFT. For further FPDATxx to LCD interface mapping, see Section 6.5, “Display Interface” on page 64.

## 4.6 CRT/TV Interface

The following figure shows external circuitry for the CRT/TV interface.

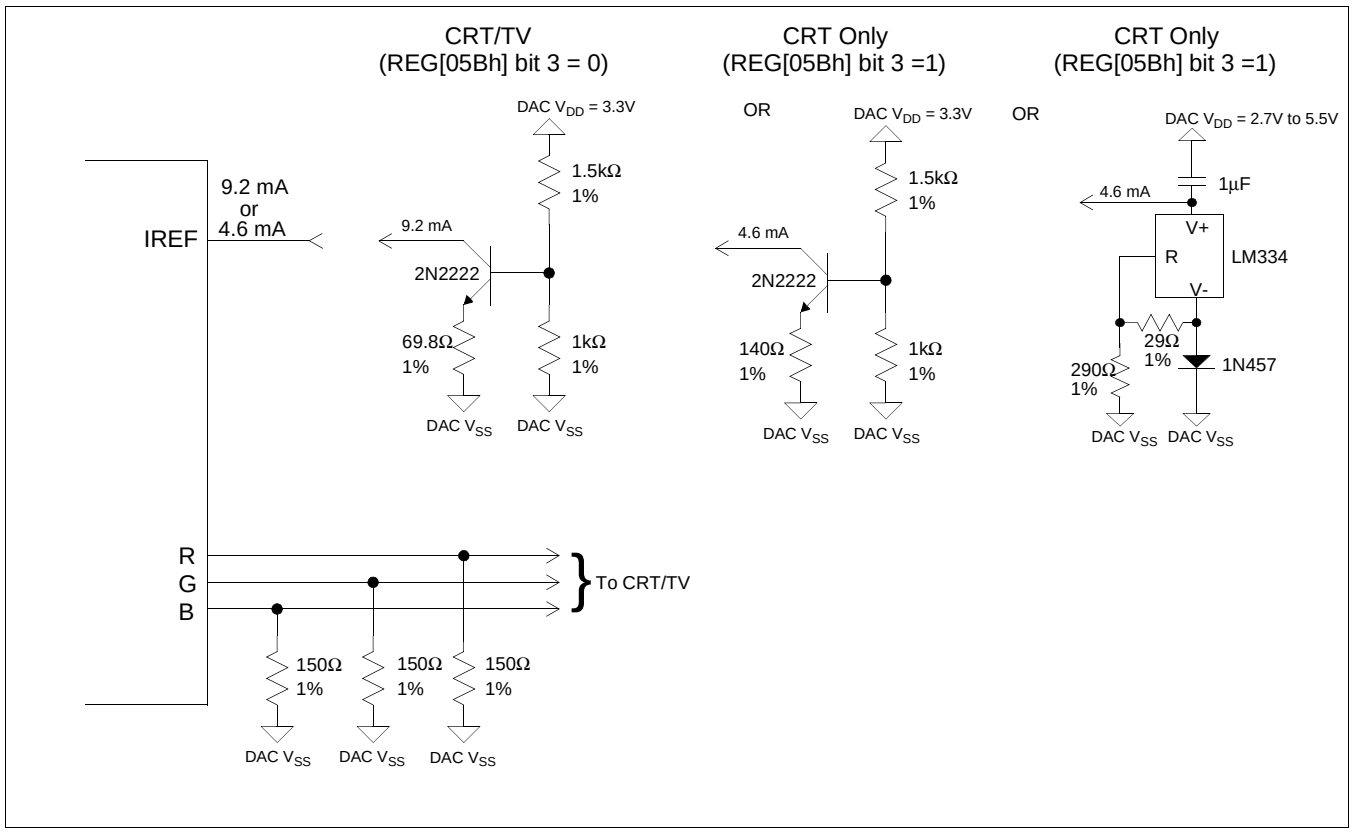



*Figure 4-3: External Circuitry for CRT Interface*

**Note**

Example implementation only, individual characteristics of components may affect actual IREF current.

# 5 D.C. Characteristics

*Table 5-1 : Absolute Maximum Ratings*

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| IO $V_{DD}$ | Supply Voltage | $V_{SS}$ - 0.3 to 4.0 | V |
| Core $V_{DD}$ | Supply Voltage | $V_{SS}$ - 0.3 to 4.0 | V |
| DAC $V_{DD}$ | Supply Voltage | $V_{SS}$ - 0.3 to 4.0 | V |
| SDRAM $V_{DD}$ | Supply Voltage | $V_{SS}$ - 0.3 to 4.0 | V |
| $V_{IN}$ | Input Voltage | $V_{SS}$ - 0.3 to $V_{DD}$ + 0.5 | V |
| $V_{OUT}$ | Output Voltage | $V_{SS}$ - 0.3 to $V_{DD}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | -65 to 150 | ° C |
| $T_{SOL}$ | Solder Temperature/Time | 260 for 10 sec. max at lead | ° C |

*Table 5-2 : Recommended Operating Conditions*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| IO $V_{DD}$ | Supply Voltage | $V_{SS}$ = 0 V | 3.0 | 3.3 | 3.6 | V |
| Core $V_{DD}$ | Supply Voltage | $V_{SS}$ = 0 V | 3.0 | 3.3 | 3.6 | V |
| DAC $V_{DD}$ | Supply Voltage | $V_{SS}$ = 0 V | 3.0 | 3.3 | 3.6 | V |
| SDRAM $V_{DD}$ | Supply Voltage | $V_{SS}$ = 0 V | 3.0 | 3.3 | 3.6 | V |
| $V_{IN}$ | Input Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $T_{OPR}$ | Operating Temperature | | -40 | 25 | 85 | ° C |

*Table 5-3 : Electrical Characteristics for VDD = 3.3V typical*

| Symbol | Parameter | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{DDS}$ | Quiescent Current | Quiescent Conditions | | | | 170 | uA |
| $I_{IZ}$ | Input Leakage Current | — | | -1 | | 1 | µA |
| $I_{OZ}$ | Output Leakage Current | — | | -1 | | 1 | µA |
| $V_{OH}$ | High Level Output Voltage | VDD = min<br>$I_{OH}$ = -2mA (Type1),<br>-6mA (Type2) | | $V_{DD}$ - 0.3 | | | V |
| $V_{OL}$ | Low Level Output Voltage | VDD = min<br>$I_{OL}$ = 2mA (Type1),<br>6mA (Type2) | | | | 0.3 | V |
| $V_{IH}$ | High Level Input Voltage | LVTTL level, $V_{DD}$ = max | | 2.0 | | | V |
| $V_{IL}$ | Low Level Input Voltage | LVTTL level, $V_{DD}$ = min | | | | 0.8 | V |
| $V_{T+}$ | High Level Input Voltage | LVTTL Schmitt | | 1.1 | | 2.4 | V |
| $V_{T-}$ | Low Level Input Voltage | LVTTL Schmitt | | 0.6 | | 1.8 | V |
| $V_{H1}$ | Hysteresis Voltage | LVTTL Schmitt | | 0.1 | | | V |
| $R_{PD}$ | Pull-Down Resistance | $V_I = V_{DD}$ | Type 1 | 20 | 50 | 120 | kΩ |
| | | | Type 2 | 40 | 100 | 240 | kΩ |
| $R_{PU}$ | Pull-Up Resistance | $V_I$ = 0V | Type 1 | 20 | 50 | 120 | kΩ |
| | | | Type 2 | 40 | 100 | 240 | kΩ |
| $C_I$ | Input Pin Capacitance | | | | | 10 | pF |
| $C_O$ | Output Pin Capacitance | | | | | 10 | pF |
| $C_{IO}$ | Bi-Directional Pin Capacitance | | | | | 10 | pF |

# 6 A.C. Characteristics

Conditions: $V_{DD}$ = 3.3V ± 10% (IO and Core)
$T_A$ = -40° C to 85° C
$T_{rise}$ and $T_{fall}$ for all inputs must be ≤ 5 ns (10% ~ 90%)
$C_L$ = 50pF (CPU Interface), unless noted
$C_L$ = 100pF (LCD Panel Interface)
$C_L$ = 10pF (Display Memory Interface)
$C_L$ = 10pF (CRT Interface)

## 6.1 Clock Timing

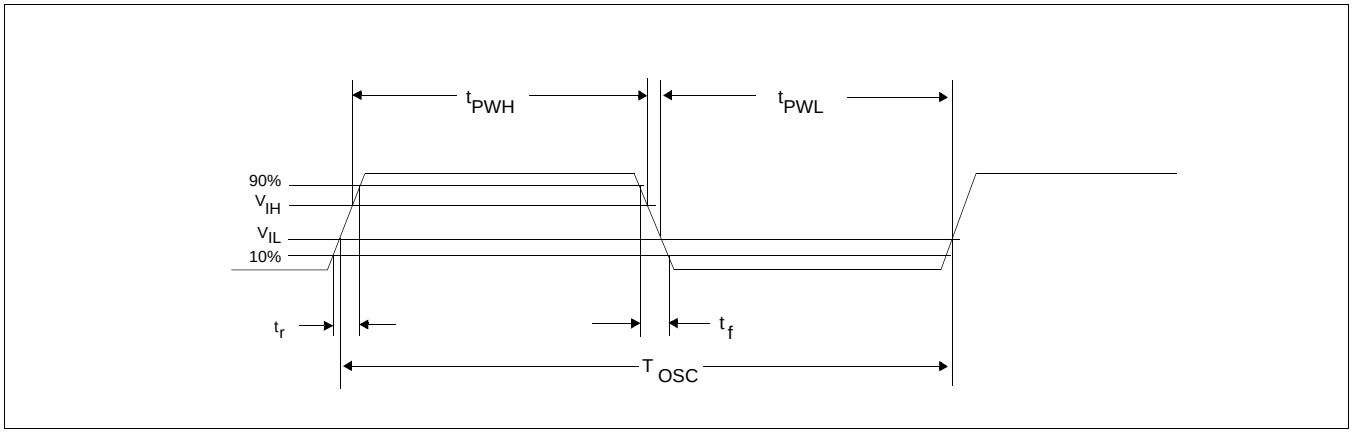



*Figure 6-1: Clock Input Requirement*

*Table 6-1 : Clock Input Requirements for BUSCLK, CLKI, CLKI2, and CLKI3 When Not Divided*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{OSC}$ | Input Clock Frequency | | Note | MHz |
| $T_{OSC}$ | Input Clock Period | $1/f_{OSC}$ | | ns |
| $t_{PWH}$ | Input Clock Pulse Width High | 6 | | ns |
| $t_{PWL}$ | Input Clock Pulse Width Low | 6 | | ns |
| $t_f$ | Input Clock Fall Time (10% - 90%) | | 5 | ns |
| $t_r$ | Input Clock Rise Time (10% - 90%) | | 5 | ns |

**Note**
For maximum internal clock frequency values see Table 6-4:, “Internal Clock Requirements,” on page 41.

*Table 6-2 : Clock Input Requirements for MCLK Source when Source Divided*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{OSC}$ | Input Clock Frequency | | 80 | MHz |
| $T_{OSC}$ | Input Clock Period | $1/f_{OSC}$ | | ns |
| $t_{PWH}$ | Input Clock Pulse Width High | 5.6 | | ns |
| $t_{PWL}$ | Input Clock Pulse Width Low | 5.6 | | ns |
| $t_f$ | Input Clock Fall Time (10% - 90%) | | 5 | ns |
| $t_r$ | Input Clock Rise Time (10% - 90%) | | 5 | ns |

**Note**
For MCLK source selection see Section 7.3, “Clock Selection” on page 94.

**Note**
For maximum internal clock frequency values see Table 6-4:, “Internal Clock Requirements,” on page 41.

*Table 6-3 : Clock Input Requirements for LCD PCLK, CRT/TV PCLK, or MediaPlug Source when Source Divided*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{OSC}$ | Input Clock Frequency | | 100 | MHz |
| $T_{OSC}$ | Input Clock Period | $1/f_{OSC}$ | | ns |
| $t_{PWH}$ | Input Clock Pulse Width High | 4.5 | | ns |
| $t_{PWL}$ | Input Clock Pulse Width Low | 4.5 | | ns |
| $t_f$ | Input Clock Fall Time (10% - 90%) | | 5 | ns |
| $t_r$ | Input Clock Rise Time (10% - 90%) | | 5 | ns |

**Note**
For PCLK source selection see Section 7.3, “Clock Selection” on page 94.

**Note**
For maximum internal clock frequency values see Table 6-4:, “Internal Clock Requirements,” on page 41.

## 6.2 Internal Clocks

This section provides the minimum and maximum required frequencies of the internal clocks used by the S1D13806. For detailed information on the internal clocks, refer to Section 7, “Clocks” on page 92.

*Table 6-4: Internal Clock Requirements*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{MCLK}$ | Memory Clock Frequency | 5 | 50 | MHz |
| $f_{LCD\ PCLK}$ | LCD Pixel Clock Frequency | | Note 1 | MHz |
| $f_{CRT/TV\ PCLK}$ | CRT/TV Pixel Clock Frequency | | Note 2 | MHz |
| $f_{MediaPlug\ Clock}$ | MediaPlug Clock Frequency | | 20 | MHz |
| $f_{BCLK}$ | Internal Bus Clock Frequency | | Note 3 | MHz |

**Note**

1. The maximum LCD pixel clock for TFT panels is 65MHz.
   The maximum LCD pixel clock for passive panels is 40MHz.
2. The maximum CRT pixel clock is 65MHz.
   The TV pixel clock for NTSC output is fixed at 14.318MHz.
   The TV pixel clock for PAL output is fixed at 17.734MHz.
3. For maximum BCLK frequencies refer to the specific CPU Interface Timing in Section 6.3, “CPU Interface Timing” on page 42.

# 6.3 CPU Interface Timing

## 6.3.1 Generic Interface Timing

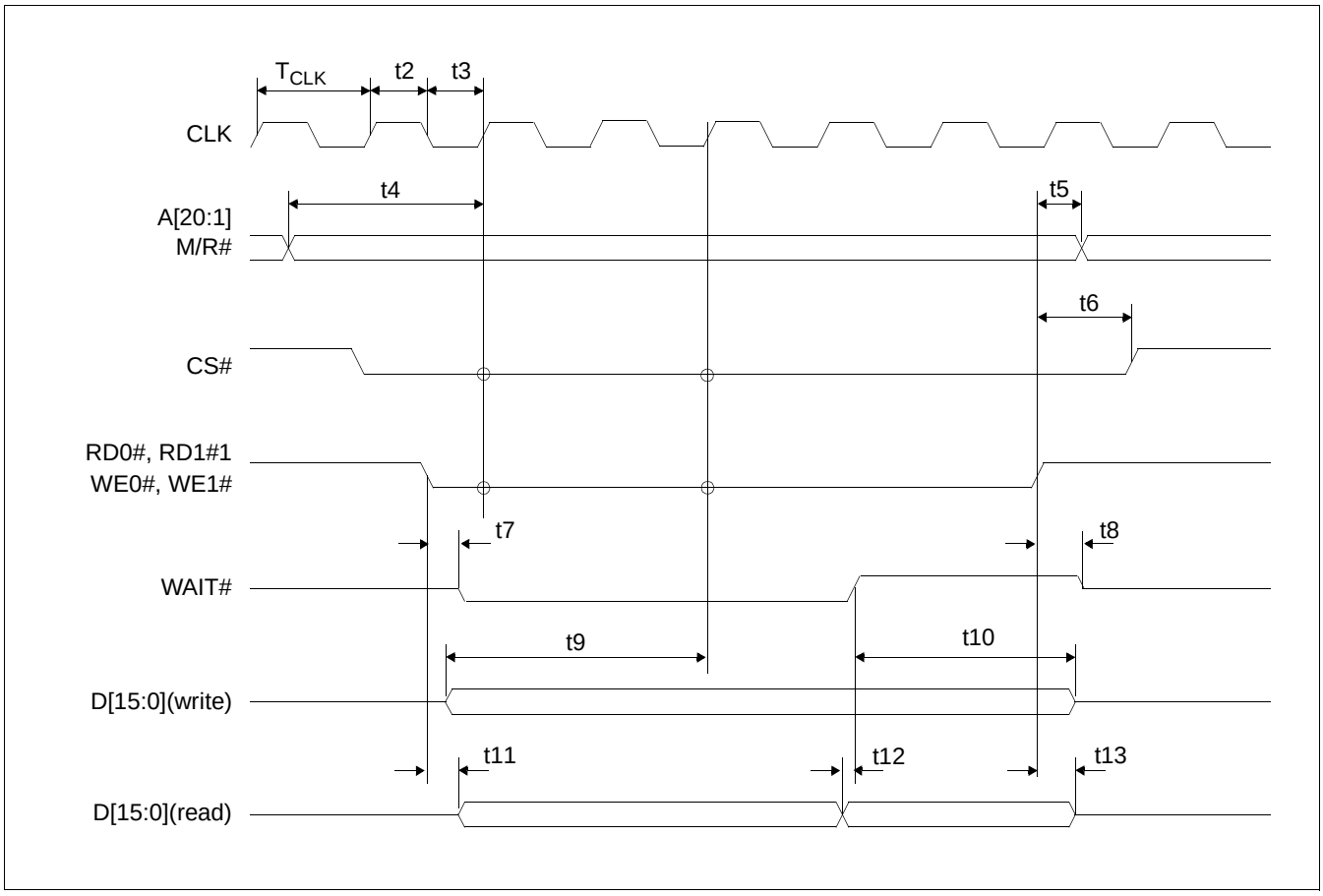



*Figure 6-2: Generic Interface Timing*

**Note**
BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**
WAIT# is always driven when CONF6 =1.

*Table 6-5 : Generic Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{CLK}$ | Clock Frequency | | 50 | MHz |
| $T_{CLK}$ | Clock period | $1/f_{CLK}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | A[20:1], M/R# setup to first CLK where CS# = 0 and either RD0#, RD1# = 0 or WE0#, WE1# = 0 | 4 | | ns |
| t5 | A[20:1], M/R# hold from rising edge of either RD0#, RD1# or WE0#, WE1# | 0 | | ns |
| t6 | CS# hold from rising edge of either RD0#, RD1# or WE0#, WE1# | 0 | | ns |
| t7 | Falling edge of either RD0#, RD1# or WE0#, WE1# to WAIT# driven low | 5 | 15 | ns |
| t8 | Rising edge of either RD0#, RD1# or WE0#, WE1# to WAIT# tri-state | 4 | 13 | ns |
| t9 | D[15:0] setup to third CLK where CS# = 0 and WE0#, WE1# = 0 (write cycle) | 0 | | ns |
| t10 | D[15:0] hold (write cycle) | 0 | | ns |
| t11 | Falling edge RD0#, RD1# to D[15:0] driven (read cycle) | 3 | | ns |
| t12 | D[15:0] setup to rising edge WAIT# (read cycle) | 0 | | ns |
| t13 | Rising edge of RD0#, RD1# to D[15:0] tri-state (read cycle) | 3 | 10 | ns |

### 6.3.2 Hitachi SH-4 Interface Timing

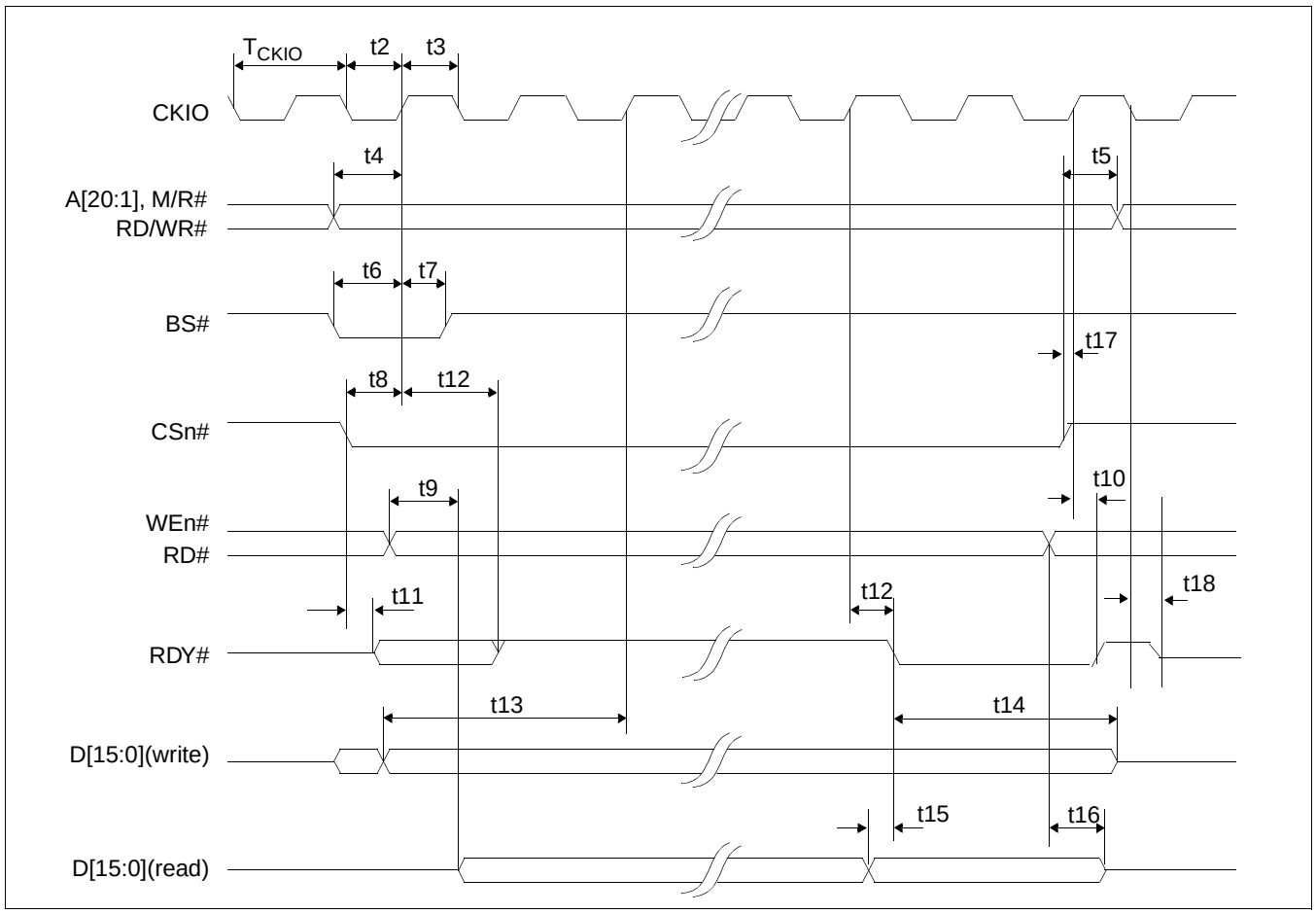



*Figure 6-3: Hitachi SH-4 Interface Timing*

**Note**
BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**
The SH-4 Wait State Control Register for the area in which the S1D13806 resides must be set to a non-zero value. The SH-4 read-to-write cycle transition must be set to a non-zero value (with reference to BUSCLK).

**Note**
RDY# is always driven when CONF6 =1.

*Table 6-6 : Hitachi SH-4 Interface Timing*

| Symbol | Parameter | Min[1] | Max[1] | Units |
|---|---|---|---|---|
| $f_{CKIO}$ | Clock Frequency | | 66 | MHz |
| $T_{CKIO}$ | Clock period | $1/f_{CKIO}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | A[20:1], M/R#, RD/WR# setup to CKIO | 4 | | ns |
| t5 | A[20:1], M/R#, RD/WR# hold from CS# | 0 | | ns |
| t6 | BS# setup | 4 | | ns |
| t7 | BS# hold | 3 | | ns |
| t8 | CSn# setup | 3 | | ns |
| t9 | Falling edge RD# to DB[15:0] driven | 3 | | ns |
| t10 | CKIO to RDY# high | 4 | 22 | ns |
| t11 | Falling edge CSn# to RDY# driven | 3 | 12 | ns |
| t12 | CKIO to RDY# delay | 4 | 13 | ns |
| t13 | DB[15:0] setup to 2nd CKIO after BS# (write cycle) | 0 | | ns |
| t14 | DB[15:0] hold (write cycle) | 0 | | ns |
| t15 | DB[15:0] valid to RDY# falling edge (read cycle) | 0 | | ns |
| t16 | Rising edge RD# to DB[15:0] tri-state (read cycle) | 6 | 29 | ns |
| t17 | CSn# high setup to CKIO | 3 | | ns |
| t18 | Falling edge CKIO to RDY# tri-state | 3 | 15 | ns |

**Note**

1. Two software WAIT states are required.

### 6.3.3 Hitachi SH-3 Interface Timing

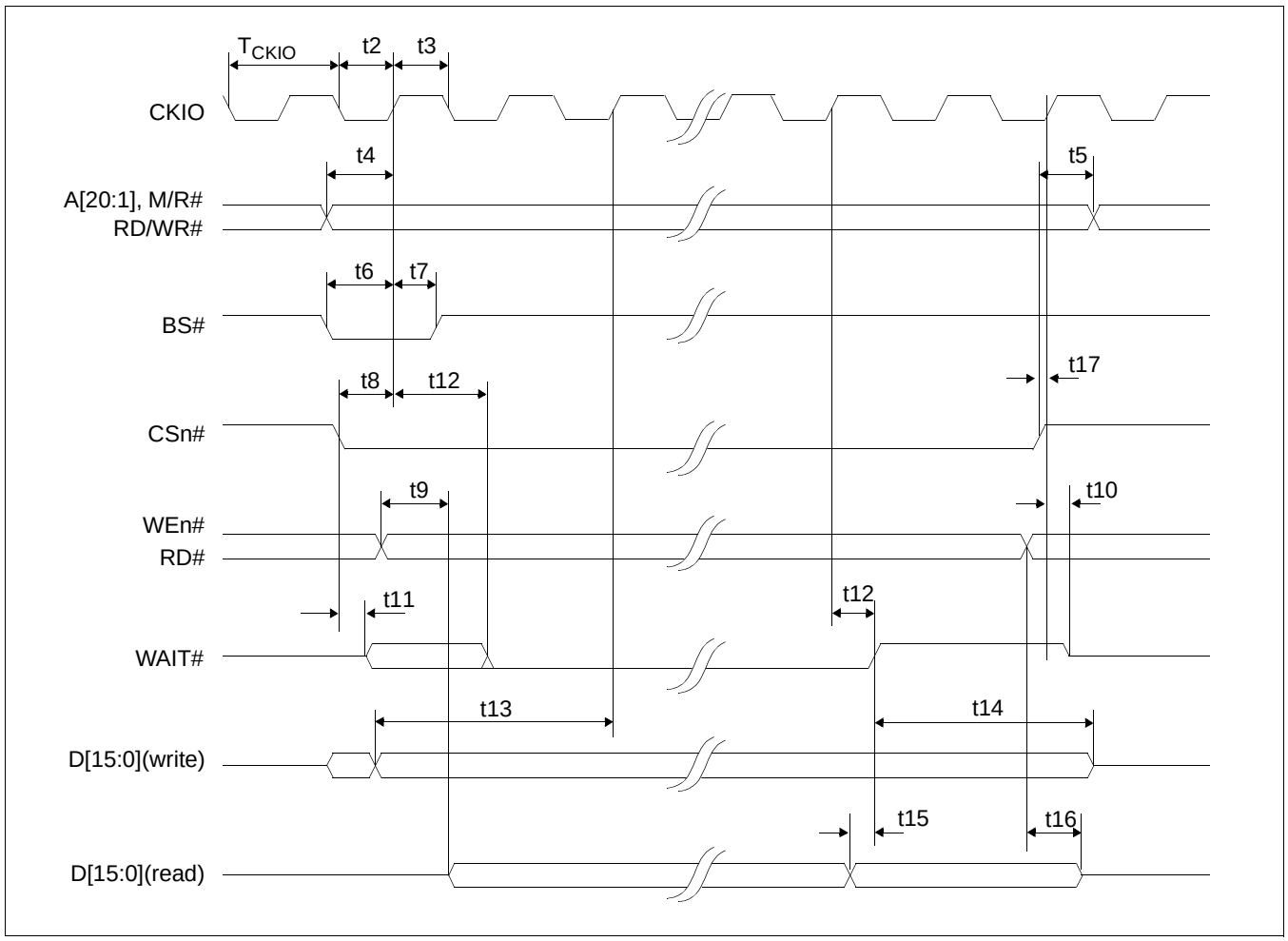



*Figure 6-4: Hitachi SH-3 Interface Timing*

**Note**
BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**
The SH-3 Wait State Control Register for the area in which the S1D13806 resides must be set to a non-zero value.

**Note**
WAIT# is always driven when CONF6 =1.

*Table 6-7 : Hitachi SH-3 Interface Timing*

| Symbol | Parameter | Min[1] | Max[1] | Units |
|---|---|---|---|---|
| $f_{CKIO}$ | Clock Frequency | | 66 | MHz |
| $T_{CKIO}$ | Clock period | $1/f_{CKIO}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | A[20:1], M/R#, RD/WR# setup to CKIO | 4 | | ns |
| t5 | A[20:1], M/R#, RD/WR# hold from CS# | 0 | | ns |
| t6 | BS# setup | 4 | | ns |
| t7 | BS# hold | 3 | | ns |
| t8 | CSn# setup | 3 | | ns |
| t9 | Falling edge RD# to DB[15:0] driven | 3 | | ns |
| t10 | Rising edge CSn# to WAIT# tri-state | 4 | 17 | ns |
| t11 | Falling edge CSn# to WAIT# driven | 3 | 16 | ns |
| t12 | CKIO to WAIT# delay | 4 | 21 | ns |
| t13 | DB[15:0] setup to 2nd CKIO after BS# (write cycle) | 0 | | ns |
| t14 | DB[15:0] hold (write cycle) | 0 | | ns |
| t15 | DB[15:0] valid to WAIT# rising edge (read cycle) | 0 | | ns |
| t16 | Rising edge RD# to DB[15:0] tri-state (read cycle) | 6 | 29 | ns |
| t17 | CSn# high setup to CKIO | 3 | | ns |

**Note**

1. Two software WAIT states are required when $f_{CKIO}$ is greater than 33MHz.

### 6.3.4 MIPS/ISA Interface Timing (e.g. NEC VR41xx)

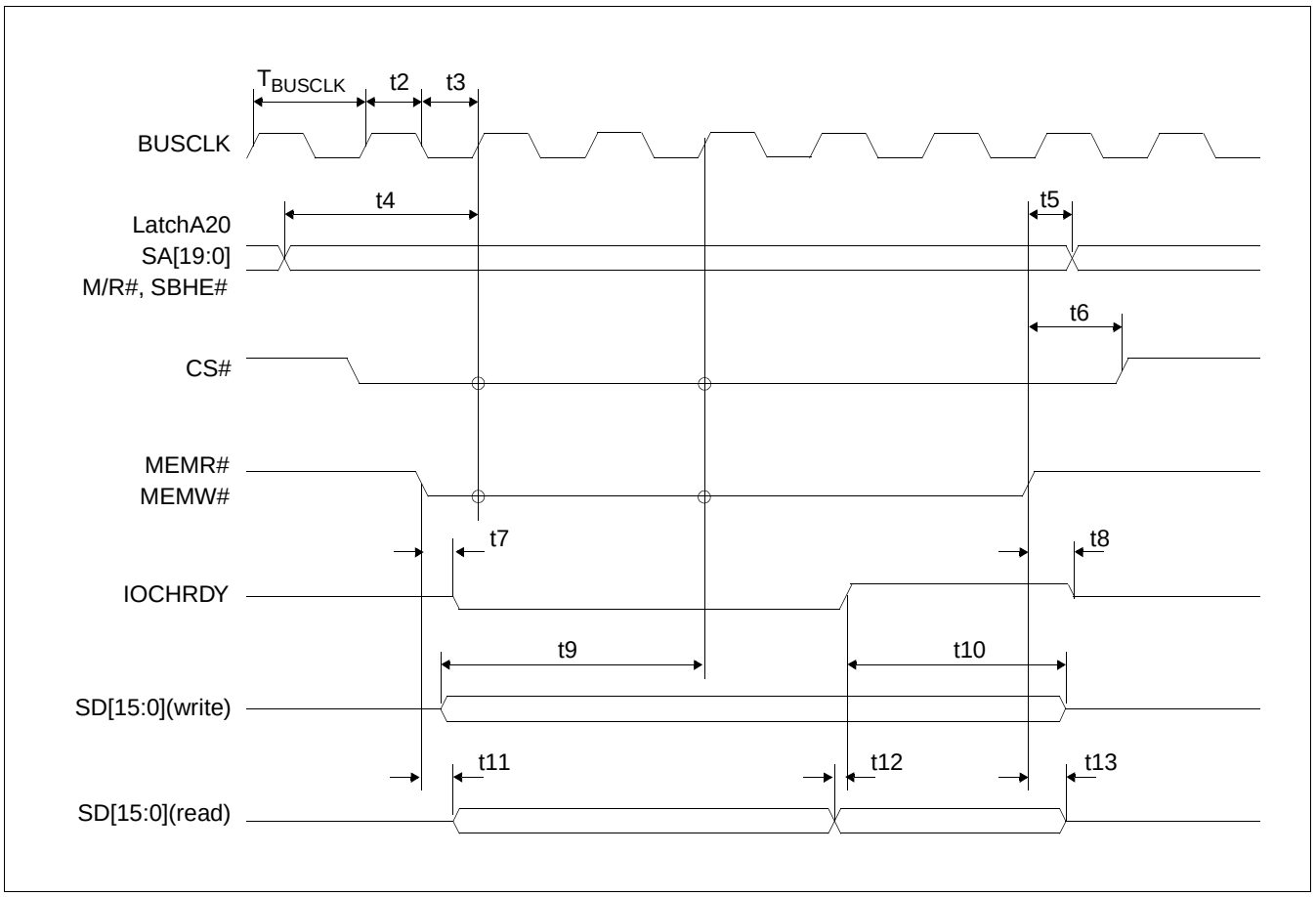



*Figure 6-5: MIPS/ISA Interface Timing*

**Note**

BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**

IOCHRDY is always driven when CONF6 =1.

*Table 6-8 : MIPS/ISA Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{BUSCLK}$ | Clock Frequency | | 50 | MHz |
| $T_{BUSCLK}$ | Clock period | $1/f_{BUSCLK}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | LatchA20, SA[19:0], M/R#, SBHE# setup to first BUSCLK where CS# = 0 and either MEMR# = 0 or MEMW# = 0 | 4 | | ns |
| t5 | LatchA20, SA[19:0], M/R#, SBHE# hold from rising edge of either MEMR# or MEMW# | 0 | | ns |
| t6 | CS# hold from rising edge of either MEMR# or MEMW# | 0 | | ns |
| t7 | Falling edge of either MEMR# or MEMW# to IOCHRDY# driven low | 3 | 15 | ns |
| t8 | Rising edge of either MEMR# or MEMW# to IOCHRDY# tri-state | 2 | 11 | ns |
| t9 | SD[15:0] setup to third BUSCLK where CS# = 0 MEMW# = 0 (write cycle) | 0 | | ns |
| t10 | SD[15:0] hold (write cycle) | 0 | | ns |
| t11 | Falling edge MEMR# toSD[15:0] driven (read cycle) | 4 | | ns |
| t12 | SD[15:0] setup to rising edge IOCHRDY# (read cycle) | 0 | | ns |
| t13 | Rising edge of MEMR# toSD[15:0] tri-state (read cycle) | 6 | 29 | ns |

### 6.3.5 Motorola MC68K Bus 1 Interface Timing (e.g. MC68000)

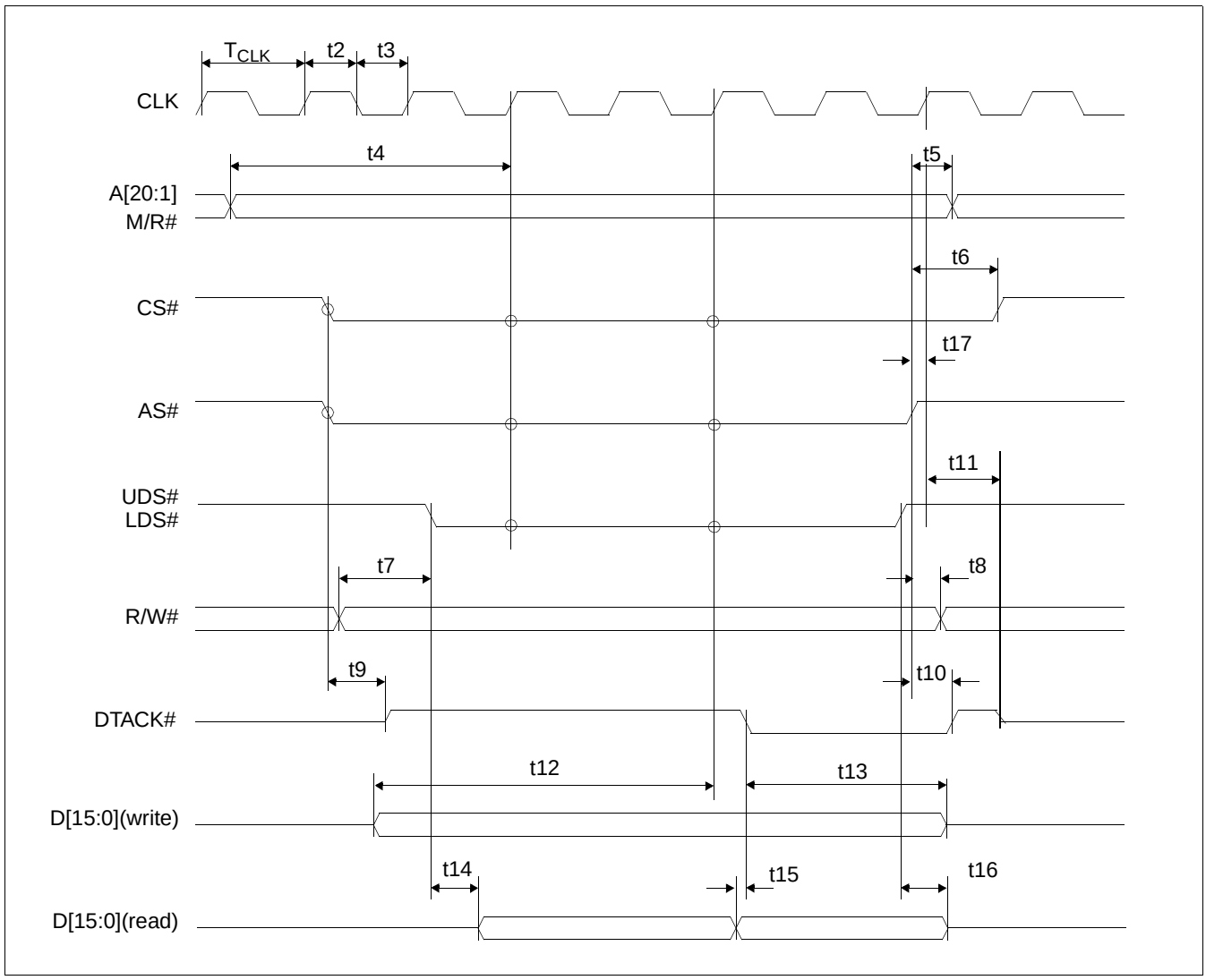



*Figure 6-6: Motorola MC68K Bus 1 Interface Timing*

**Note**

BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**

DTACK# is always driven when CONF6 =1.

*Table 6-9 : Motorola MC68K Bus 1 Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{CLK}$ | Clock Frequency | | 50 | MHz |
| $T_{CLK}$ | Clock period | $1/f_{CLK}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | A[20:1], M/R# setup to first CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 | 5 | | ns |
| t5 | A[20:1], M/R# hold from AS# | 0 | | ns |
| t6 | CS# hold from AS# | 0 | | ns |
| t7 | R/W# setup to before to either UDS#=0 or LDS# = 0 | 10 | | ns |
| t8 | R/W# hold from AS# | 0 | | ns |
| t9 | AS# = 0 and CS# = 0 to DTACK# driven high | 1 | | ns |
| t10 | AS# high to DTACK# high | 4 | 19 | ns |
| t11 | First BCLK where AS# = 1 to DTACK# high impedance | | 16 | ns |
| t12 | D[15:0] valid to third CLK where CS# = 0 AS# = 0, and either UDS#=0 or LDS# = 0 (write cycle) | 0 | | ns |
| t13 | D[15:0] hold from falling edge of DTACK# (write cycle) | 0 | | ns |
| t14 | Falling edge of UDS#=0 or LDS# = 0 to DB driven (read cycle) | 3 | | ns |
| t15 | D[15:0] valid to DTACK# falling edge (read cycle) | 0 | | ns |
| t16 | UDS# and LDS# high to D[15:0] invalid/high impedance (read cycle) | 6 | 30 | ns |
| t17 | AS# high setup to CLK | 4 | | ns |

### 6.3.6 Motorola MC68K Bus 2 Interface Timing (e.g. MC68030)

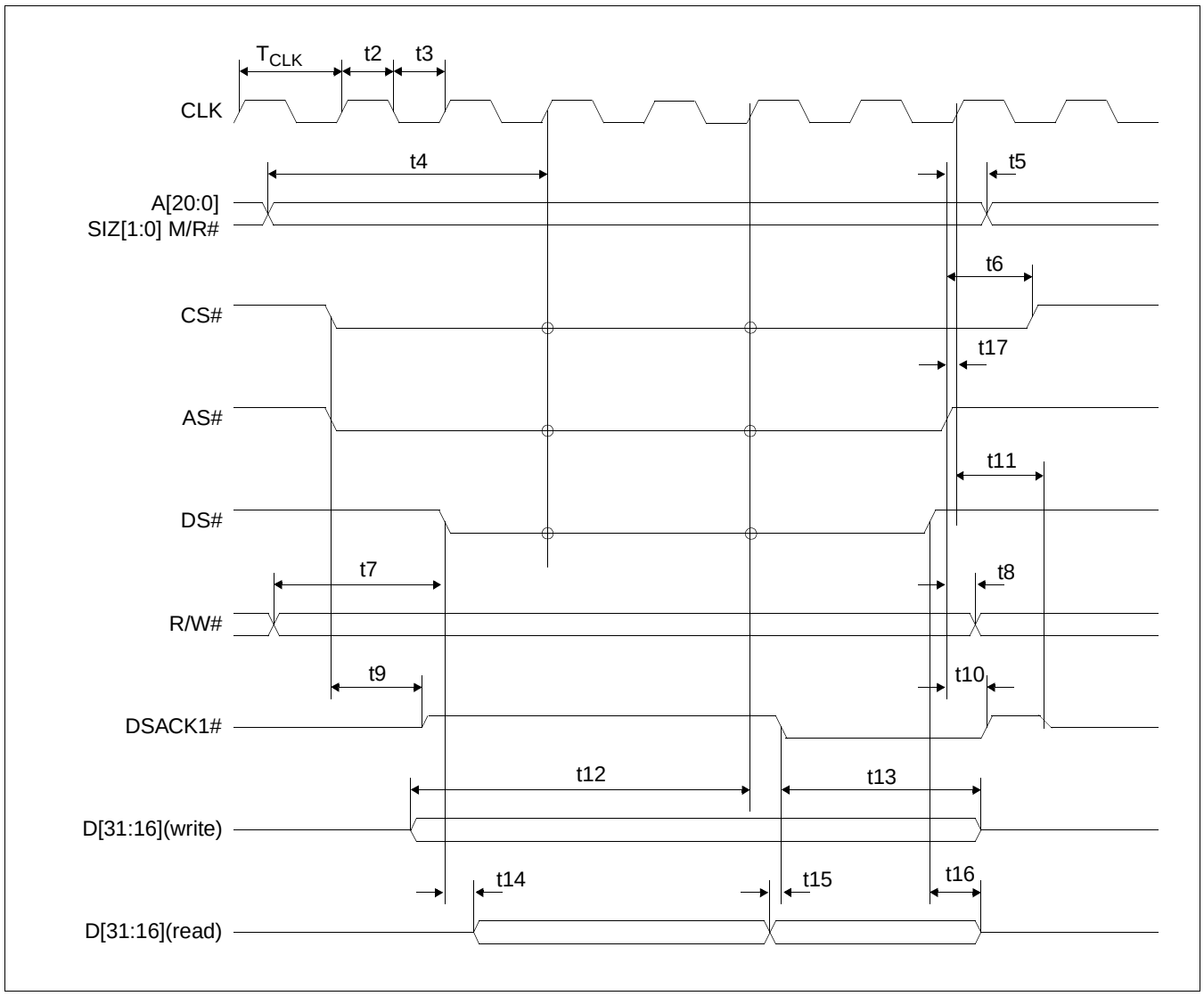



*Figure 6-7: Motorola MC68K Bus 2 Interface Timing*

**Note**
BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**
DSACK1# is always driven when CONF6 =1.

*Table 6-10 : Motorola MC68K Bus 2 Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{CLK}$ | Clock Frequency | | 50 | MHz |
| $T_{CLK}$ | Clock period | $1/f_{CLK}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | A[20:0], SIZ[1:0], M/R# setup to first CLK where CS# = 0 AS# = 0, and DS#= 0 | 5 | | ns |
| t5 | A[20:0], SIZ[1:0], M/R# hold from AS# | 0 | | ns |
| t6 | CS# hold from AS# | 0 | | ns |
| t7 | R/W# setup to DS# | 10 | | ns |
| t8 | R/W# hold from AS# | 0 | | ns |
| t9 | AS# = 0 and CS# = 0 to DSACK1# driven high | 1 | | ns |
| t10 | AS# high to DSACK1# high | 4 | 19 | ns |
| t11 | First BCLK where AS# = 1 to DSACK1# high impedance | 3 | 16 | ns |
| t12 | D[31:16] valid to third CLK where CS# = 0 AS# = 0, and DS#= 0 (write cycle) | 0 | | ns |
| t13 | D[31:16] hold from falling edge of DSACK1# (write cycle) | 0 | | ns |
| t14 | Falling edge of DS#= 0 to DB driven (read cycle) | 3 | | ns |
| t15 | D[31:16] valid to DSACK1# falling edge (read cycle) | 0 | | ns |
| t16 | DS# high to D[31:16] invalid/high impedance (read cycle) | 6 | 30 | ns |
| t17 | AS# high setup to CLK | 4 | | ns |

### 6.3.7 Motorola PowerPC Interface Timing (e.g. MPC8xx, MC68040, Coldfire)

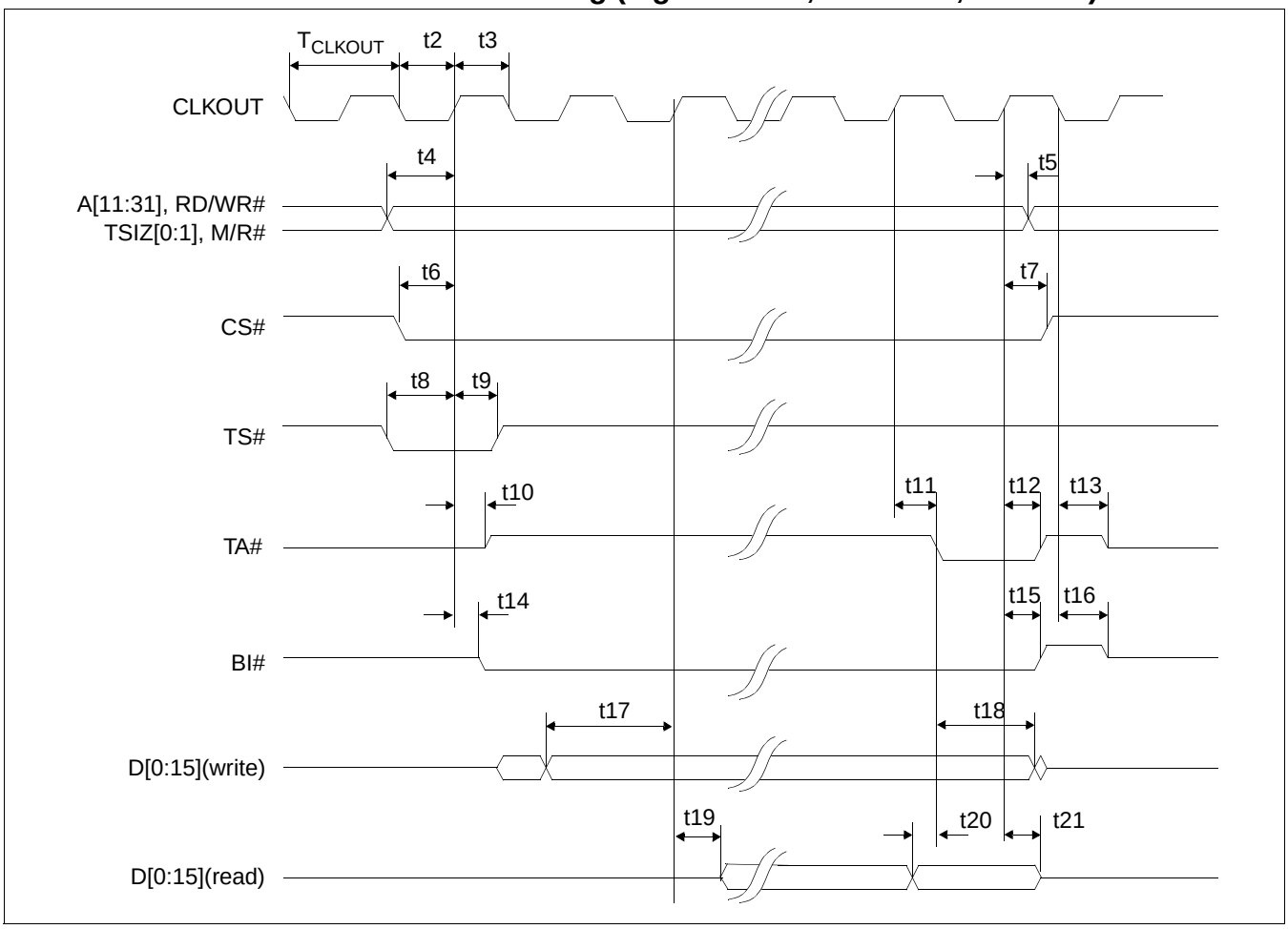



*Figure 6-8: Motorola PowerPC Interface Timing*

**Note**

BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

**Note**

TA# is always driven when CONF6 =1.

*Table 6-11 : Motorola PowerPC Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{CLKOUT}$ | Clock Frequency | | 45 | MHz |
| $T_{CLKOUT}$ | Clock period | $1/f_{CLKOUT}$ | | ns |
| t2 | Clock pulse width low | 6 | | ns |
| t3 | Clock pulse width high | 6 | | ns |
| t4 | AB[11:31], RD/WR#, TSIZ[0:1], M/R# setup | 0 | | ns |
| t5 | AB[11:31], RD/WR#, TSIZ[0:1], M/R# hold | 0 | | ns |
| t6 | CS# setup | 1 | | ns |
| t7 | CS# hold | 1 | | ns |
| t8 | TS# setup | 1 | | ns |
| t9 | TS# hold | 1 | | ns |
| t10 | CLKOUT to TA# driven | 5 | | ns |
| t11 | CLKOUT to TA# low | 4 | 14 | ns |
| t12 | CLKOUT to TA# high | 5 | 15 | ns |
| t13 | negative edge CLKOUT to TA# tri-state | 3 | 12 | ns |
| t14 | CLKOUT to BI# driven | 5 | 15 | ns |
| t15 | CLKOUT to BI# high | 4 | 14 | ns |
| t16 | negative edge CLKOUT to BI# tri-state | 3 | 9 | ns |
| t17 | DB[15:0] setup to 2nd CLKOUT after TS# = 0 (write cycle) | 0 | | ns |
| t18 | DB[15:0] hold (write cycle) | 0 | | ns |
| t19 | CLKOUT to DB driven (read cycle) | 0 | | ns |
| t20 | DB[15:0] valid to TA# falling edge (read cycle) | 0 | | ns |
| t21 | CLKOUT to DB[15:0] tri-state (read cycle) | 3 | 11 | ns |

**Note**

Output pin loading on DB[15:0], TA#, BI# is 10pF.

### 6.3.8 PC Card Timing (e.g. StrongARM)

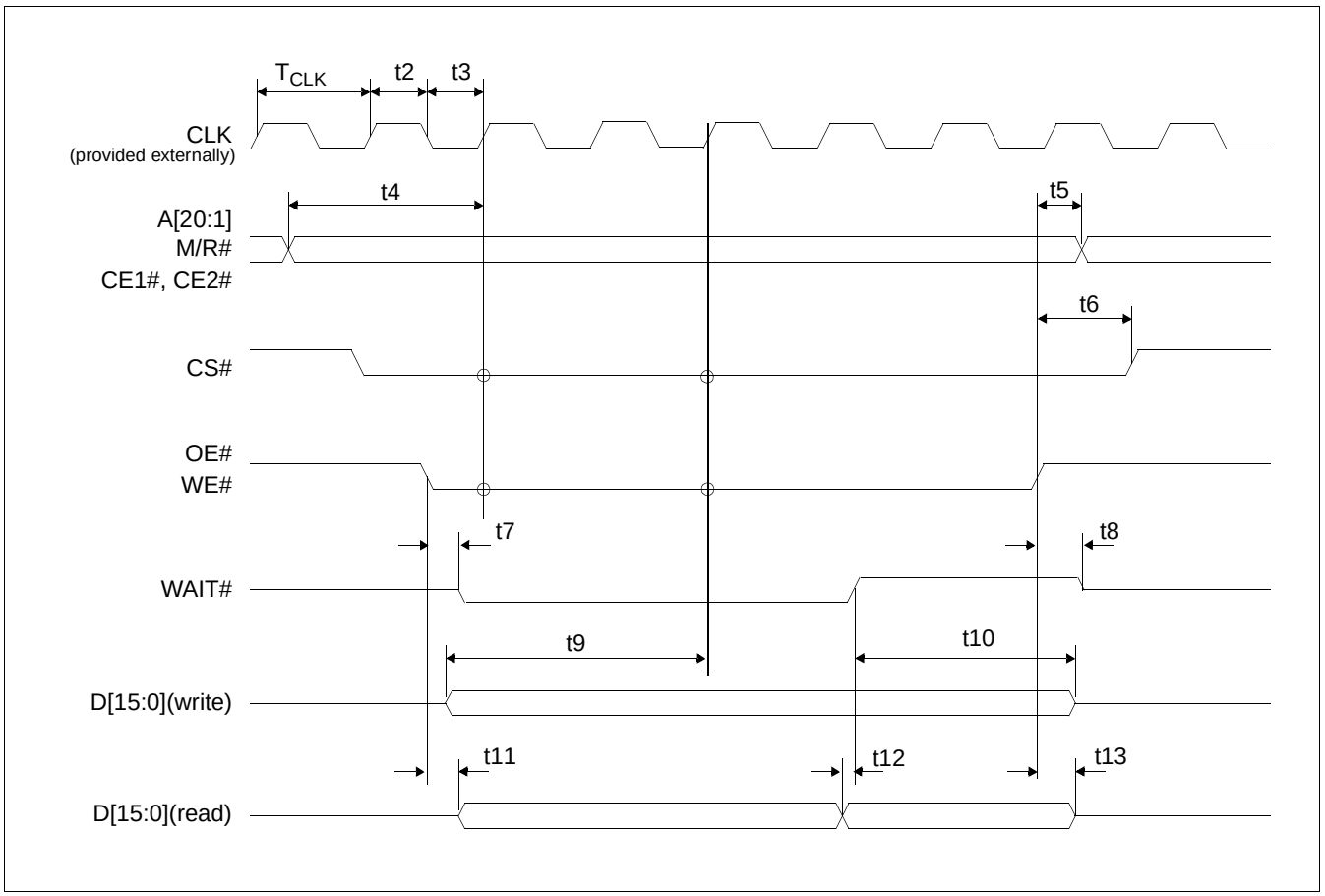



*Figure 6-9: PC Card Timing*

**Note**

BUSCLK cannot be divided by 2 for this interface. CONF5 must be set to 0 (BUSCLK not divided).

*Table 6-12: PC Card Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{CLK}$ | Clock frequency | | 50 | MHz |
| $T_{CLK}$ | Clock period | $1/f_{CLK}$ | | ns |
| t2 | Clock pulse width high | 6 | | ns |
| t3 | Clock pulse width low | 6 | | ns |
| t4 | A[20:1], M/R# setup to first CLK where CE1# = 0 or CE2# = 0 **and** either OE# = 0 or WE# = 0 | 4 | | ns |
| t5 | A[20:1], M/R# hold from rising edge of either OE# or WE# | 0 | | ns |
| t6 | CS# hold from rising edge of either OE# or WE# | 0 | | ns |
| t7 | Falling edge of either OE# or WE# to WAIT# driven low | 5 | 15 | ns |
| t8 | Rising edge of either OE# or WE# to WAIT# tri-state | 3 | 13 | ns |
| t9 | D[15:0] setup to third CLK where CE1# = 0, CE2# = 0 and WE# = 0 (write cycle) | 0 | | ns |
| t10 | D[15:0] hold (write cycle) | 0 | | ns |
| t11 | Falling edge OE# to D[15:0] driven (read cycle) | 9 | | ns |
| t12 | D[15:0] setup to rising edge WAIT# (read cycle) | 0 | | ns |
| t13 | Rising edge of OE# to D[15:0] tri-state (read cycle) | 3 | 10 | ns |

### 6.3.9 Philips Interface Timing (e.g. PR31500/PR31700)

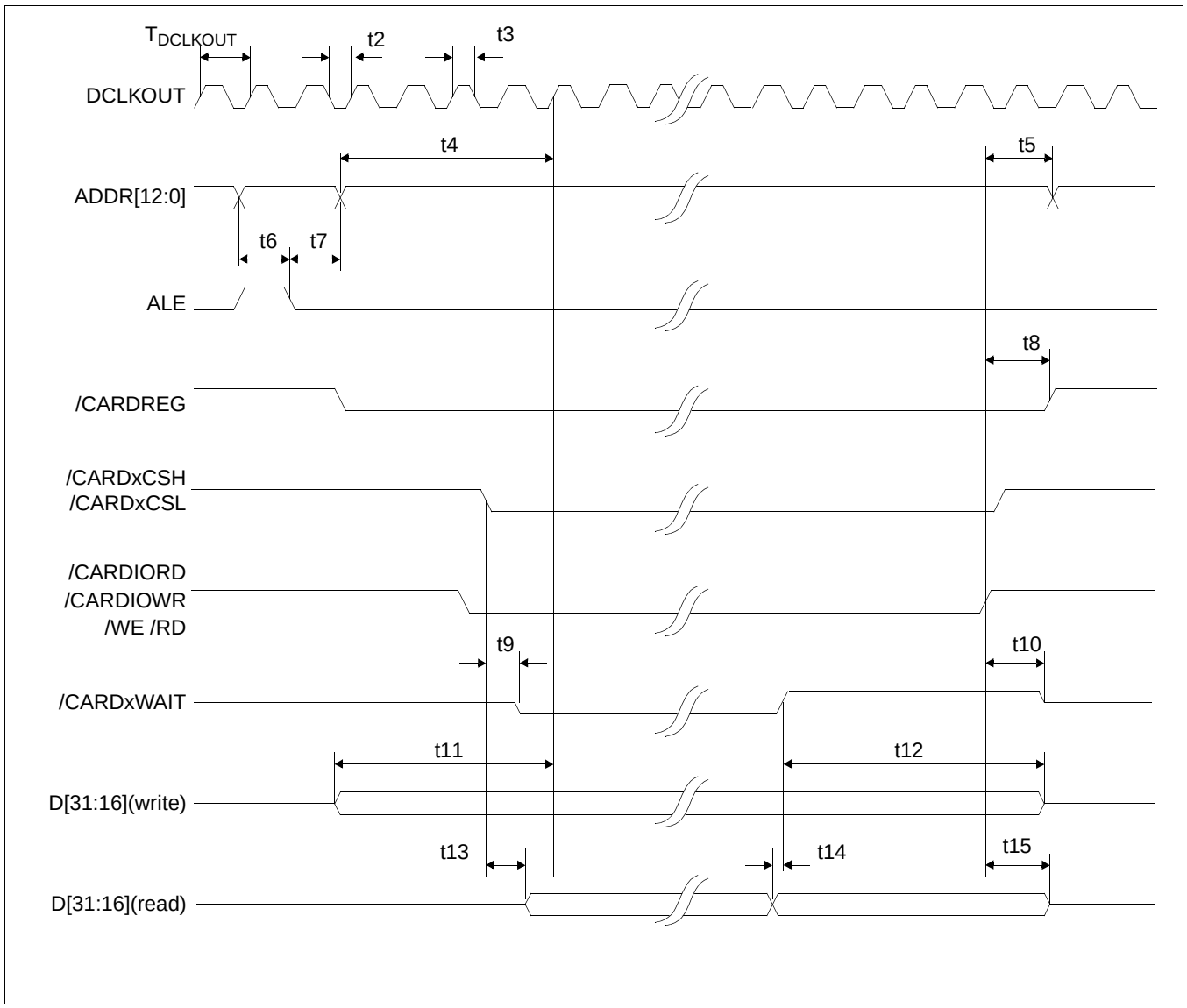



*Figure 6-10: Philips Interface Timing*

**Note**

/CARDxWAIT is always driven when CONF6 =1.

*Table 6-13 : Philips Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{DCLKOUT}$ | Clock frequency | | 75 | MHz |
| $T_{DCLKOUT}$ | Clock period | $1/f_{DCLKOUT}$ | | ns |
| t2 | Clock pulse width low | 6 | | ns |
| t3 | Clock pulse width high | 6 | | ns |
| t4 | ADDR[12:0] setup to first CLK of cycle | 10 | | ns |
| t5 | ADDR[12:0] hold from command invalid | 0 | | ns |
| t6 | ADDR[12:0] setup to falling edge ALE | 10 | | ns |
| t7 | ADDR[12:0] hold from falling edge ALE | 5 | | ns |
| t8 | /CARDREG hold from command invalid | 0 | | ns |
| t9 | Falling edge of chip select to /CARDxWAIT driven | 0 | 15 | ns |
| t10 | Command invalid to /CARDxWAIT tri-state | 5 | 25 | ns |
| t11 | D[31:16] valid to first CLK of cycle (write cycle) | 10 | | ns |
| t12 | D[31:16] hold from rising edge of /CARDxWAIT | 0 | | |
| t13 | Chip select to D[31:16] driven (read cycle) | 1 | | ns |
| t14 | D[31:16] setup to rising edge /CARDxWAIT (read cycle) | 0 | | ns |
| t15 | Command invalid to D[31:16] tri-state (read cycle) | 5 | 25 | ns |

**Note**

If BUSCLK exceeds 37.5MHz, it must be divided by 2 using CONF5 (see Table 4-9, “Summary of Power-On/Reset Options,” on page 33).

### 6.3.10 Toshiba Interface Timing (e.g. TX39xx)

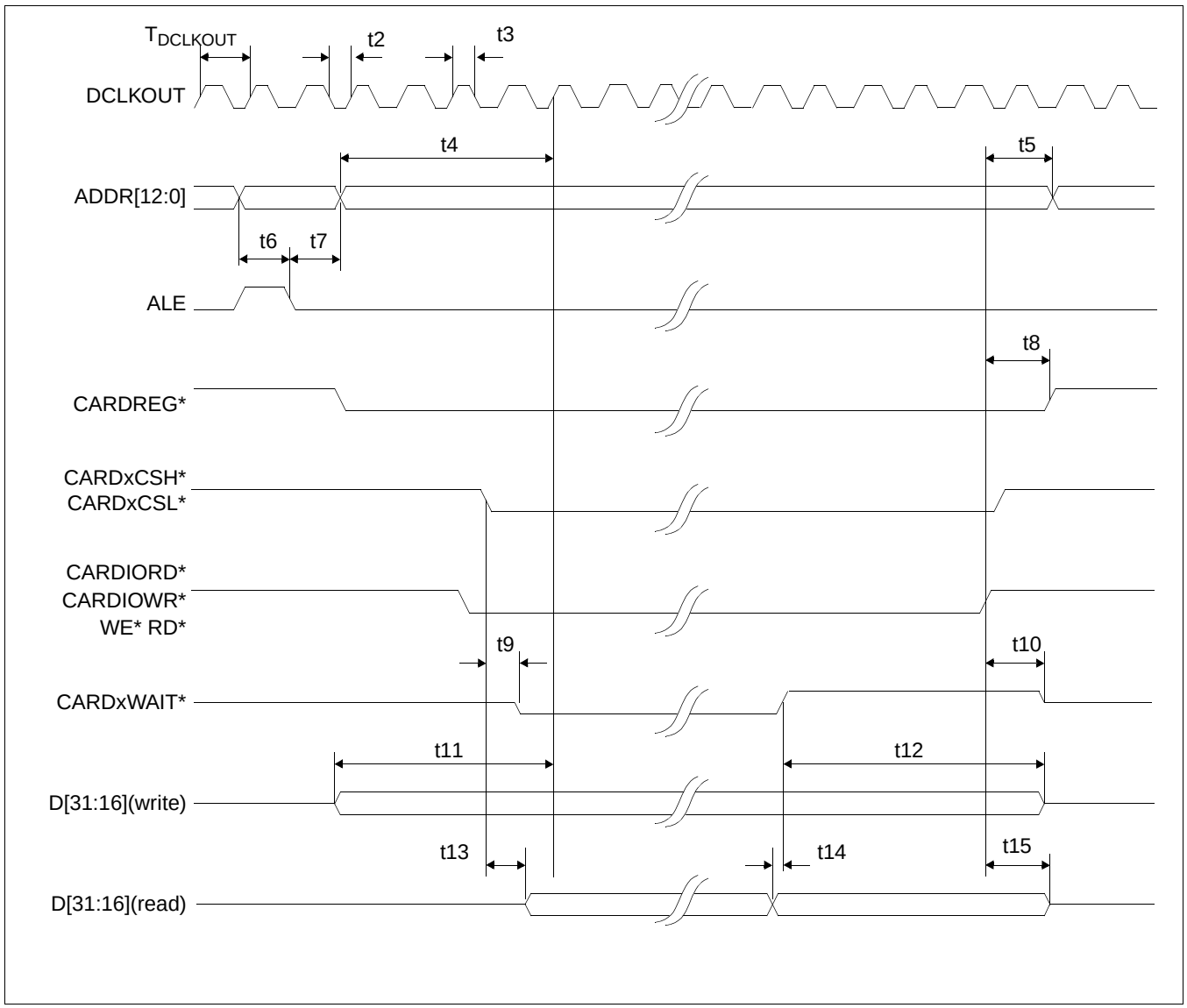



*Figure 6-11: Toshiba Interface Timing*

**Note**

CARDxWAIT* is always driven when CONF6 =1.

*Table 6-14 : Toshiba Interface Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{DCLKOUT}$ | Clock frequency | | 75 | MHz |
| $T_{DCLKOUT}$ | Clock period | $1/f_{DCLKOUT}$ | | ns |
| t2 | Clock pulse width low | 6 | | ns |
| t3 | Clock pulse width high | 6 | | ns |
| t4 | ADDR[12:0] setup to first CLK of cycle | 10 | | ns |
| t5 | ADDR[12:0] hold from command invalid | 0 | | ns |
| t6 | ADDR[12:0] setup to falling edge ALE | 10 | | ns |
| t7 | ADDR[12:0] hold from falling edge ALE | 5 | | ns |
| t8 | CARDREG* hold from command invalid | 0 | | ns |
| t9 | Falling edge of chip select to CARDxWAIT* driven | 0 | 15 | ns |
| t10 | Command invalid to CARDxWAIT* tri-state | 5 | 25 | ns |
| t11 | D[31:16] valid to first CLK of cycle (write cycle) | 10 | | ns |
| t12 | D[31:16] hold from rising edge of CARDxWAIT* | 0 | | |
| t13 | Chip select to D[31:16] driven (read cycle) | 1 | | ns |
| t14 | D[31:16] setup to rising edge CARDxWAIT* (read cycle) | 0 | | ns |
| t15 | Command invalid to D[31:16] tri-state (read cycle) | 5 | 25 | ns |

**Note**

If BUSCLK exceeds 37.5MHz, it must be divided by 2 using CONF5 (see Table 4-9, “Summary of Power-On/Reset Options,” on page 33).

# 6.4 Power Sequencing

## 6.4.1 LCD Power Sequencing

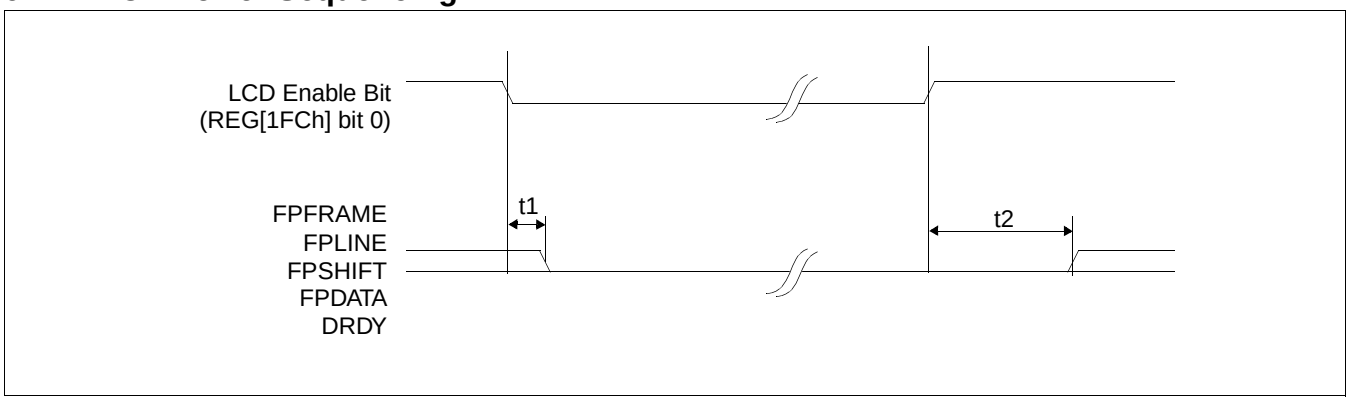



*Figure 6-12: LCD Panel Power-off/Power-on Timing*

*Table 6-15 : LCD Panel Power-off/Power-on*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| t1 | LCD Enable Bit low to FPFRAME, FPLINE, FPSHIFT, FPDATA, DRDY inactive | | 1 | $T_{FPLINE}$ |
| t2 | LCD Enable Bit high to FPFRAME, FPLINE, FPSHIFT, FPDATA, DRDY active | 1 | 2 | $T_{FPLINE}$ |

**Note**
Where $T_{FPLINE}$ is the period of FPLINE.

**Note**
The above timing assumes REG[1F0h] bit 4 is set to 1.

### 6.4.2 Power Save Status

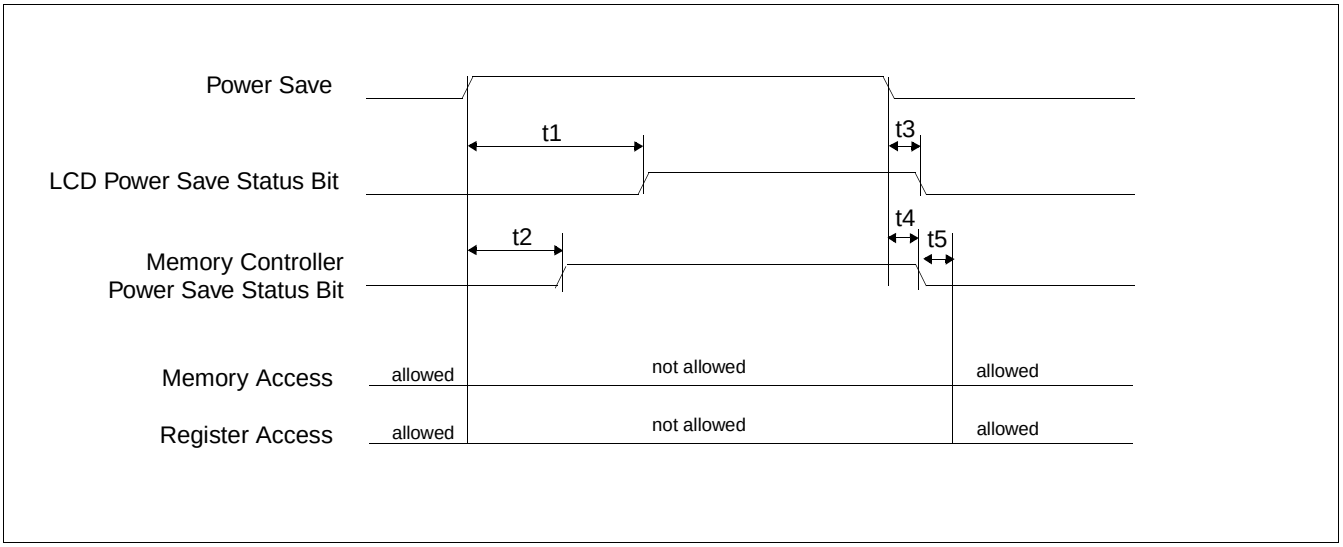



*Figure 6-13: Power Save Status Bits and Local Bus Memory Access Relative to Power Save Mode*

**Note**
Memory access should not be performed after Power Save Mode has been initiated.

**Note**
Power Save is initiated through the Power Save Mode Enable bit (REG[1F0h] bit 0).

*Table 6-16 : Power Save Status and Local Bus Memory Access Relative to Power Save Mode*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| t1 | Power Save initiated to rising edge of LCD Power Save Status | 1 | 2 | $T_{FPLINE}$ |
| t2 | Power Save initiated to rising edge of Memory Controller Power Save Status | | note 1 | MCLK |
| t3 | Power Save deactivated to falling edge of LCD Power Save Status | | 1 | $T_{FPFRAME}$ |
| t4 | Power Save deactivated to falling edge of Memory Controller Power Save Status | | 12 | MCLK |
| t5 | Falling edge of Memory Controller Power Save Status to the earliest time where memory access is allowed | | 8 | MCLK |

1. $t2_{max}$ = The maximum value for t2 is based on the SDRAM Refresh Rate (REG[021h] bits 2:0) as follows.

*Table 6-17 : SDRAM Refresh Period Selection*

| REG[021h] bits 2:0 | SDRAM Refresh Period (MCLKs) |
|---|---|
| 000 | 76 |
| 001 | 140 |
| 010 | 268 |
| 011 | 524 |

# 6.5 Display Interface

## 6.5.1 Single Monochrome 4-Bit Panel Timing

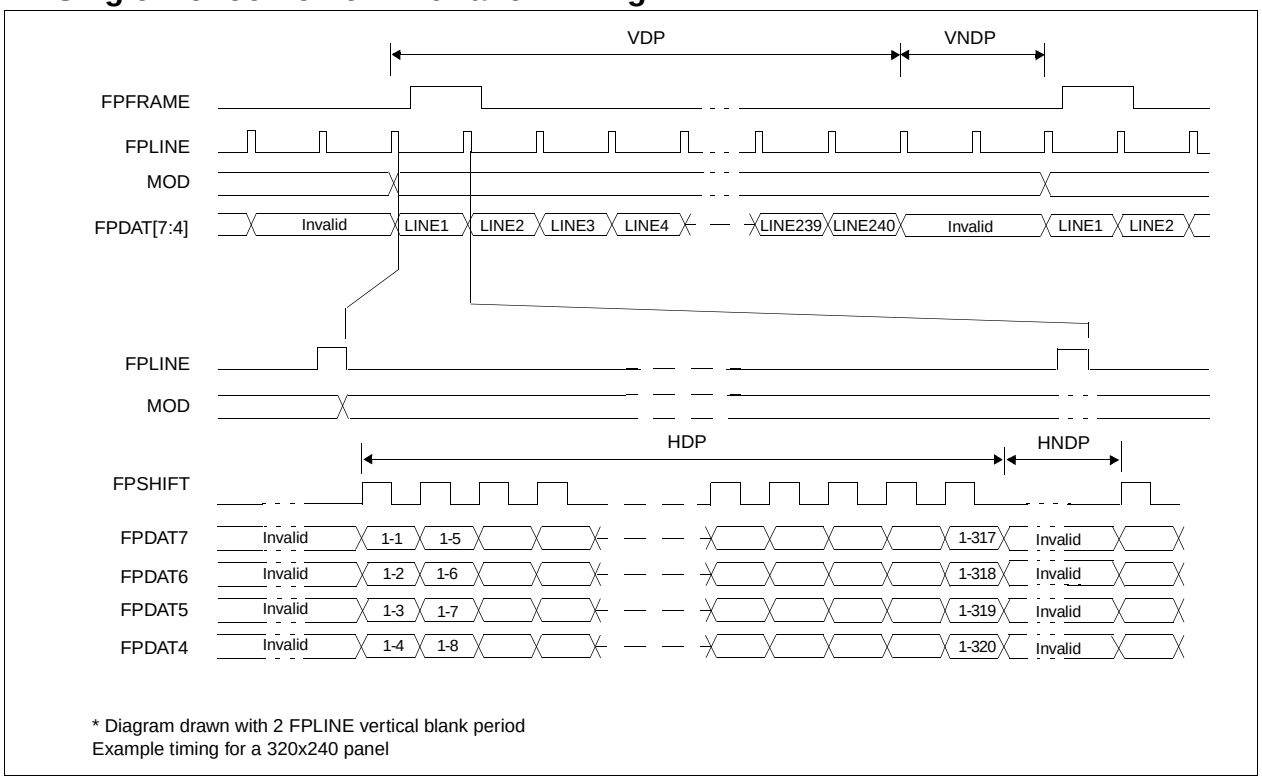



*Figure 6-14: Single Monochrome 4-Bit Panel Timing*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

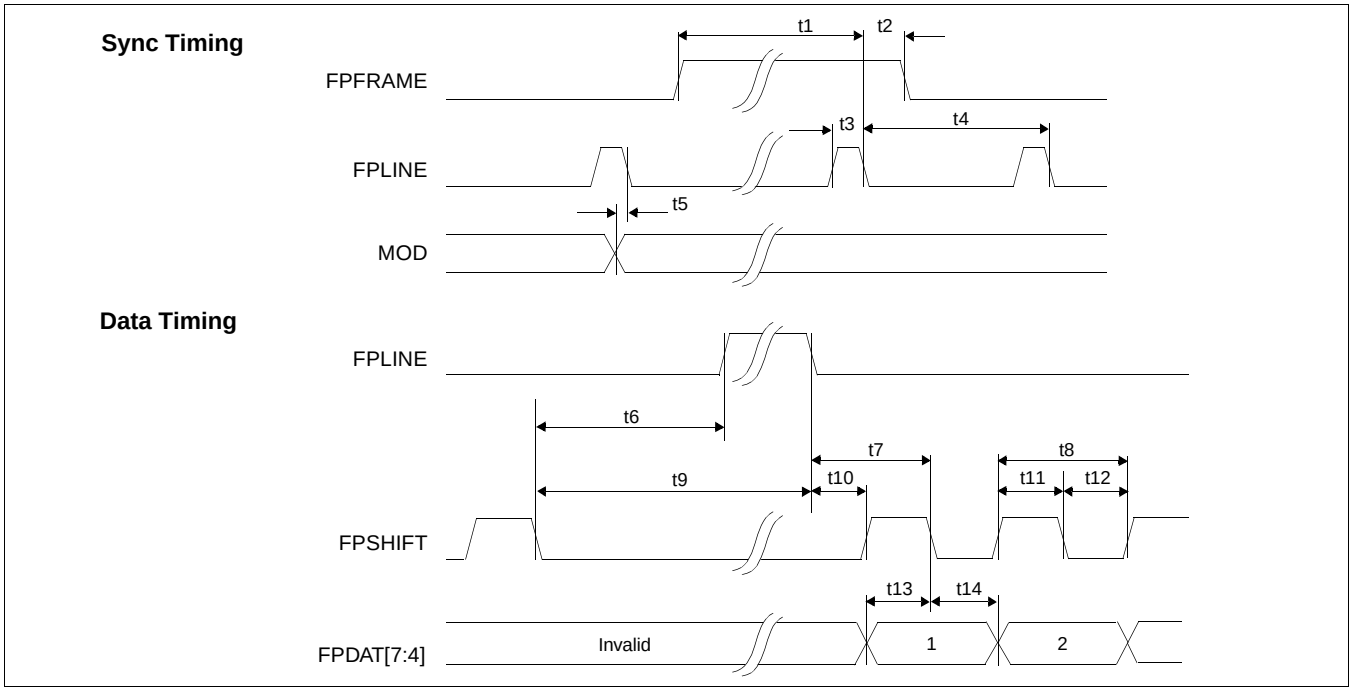



*Figure 6-15: Single Monochrome 4-Bit Panel A.C. Timing*

*Table 6-18 : Single Monochrome 4-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 2 | | | Ts |
| t8 | FPSHIFT period | 4 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 2 | | | Ts |
| t12 | FPSHIFT pulse width low | 2 | | | Ts |
| t13 | FPDAT[7:4] setup to FPSHIFT falling edge | 2 | | | Ts |
| t14 | FPDAT[7:4] hold to FPSHIFT falling edge | 2 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. $t1_{min}$ = $t4_{min}$ - 12
3. $t4_{min}$ = [((REG[032h] bits [6:0]) + 1) $\times$ 8 + ((REG[034h] bits [4:0]) + 1) $\times$ 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) $\times$ 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 26] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 25] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 15] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 14] for 16 bpp color depth
7. $t10_{min}$= 17 for 4 bpp or 8 bpp color depth
   = 16 for 16 bpp color depth

## 6.5.2 Single Monochrome 8-Bit Panel Timing

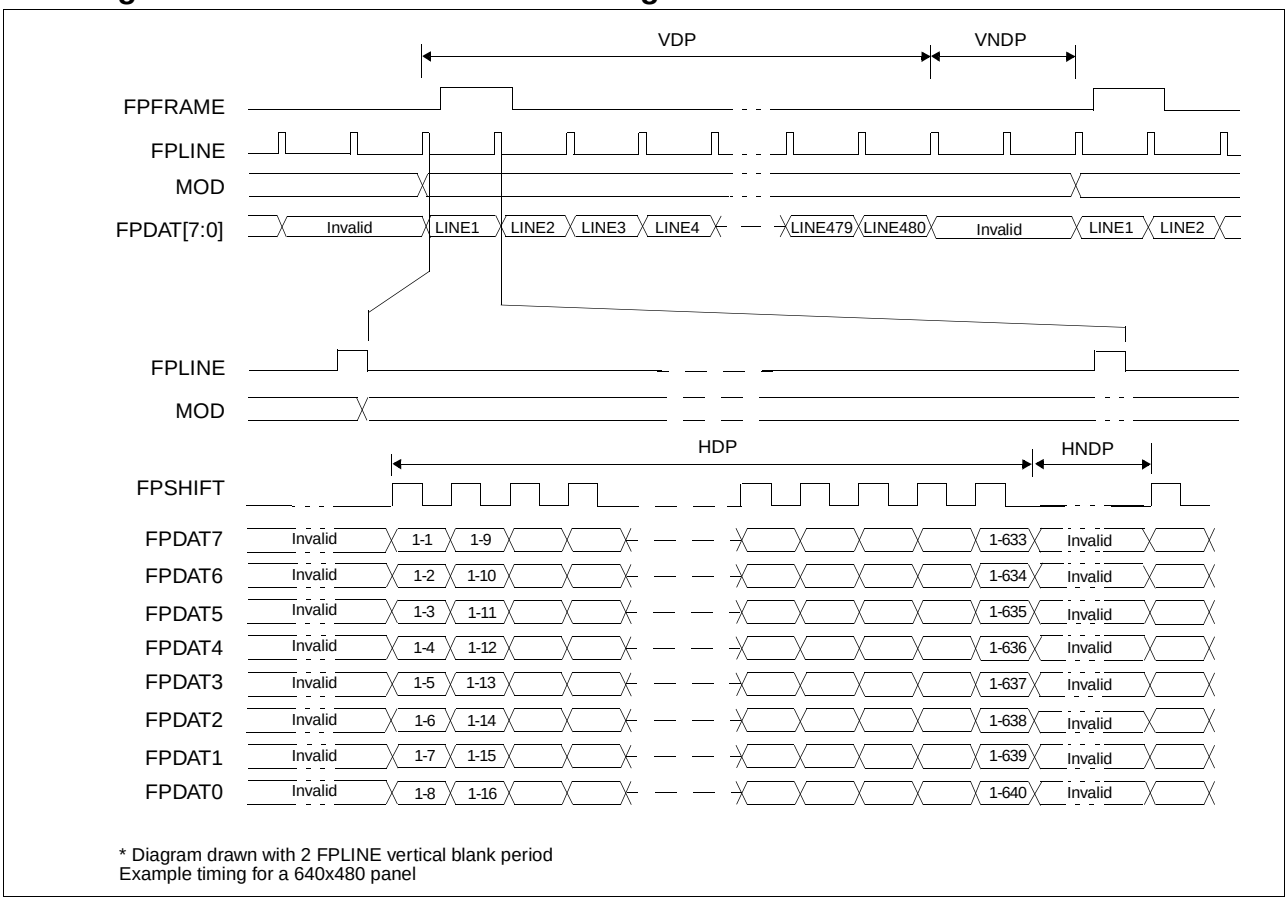



*Figure 6-16: Single Monochrome 8-Bit Panel Timing*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

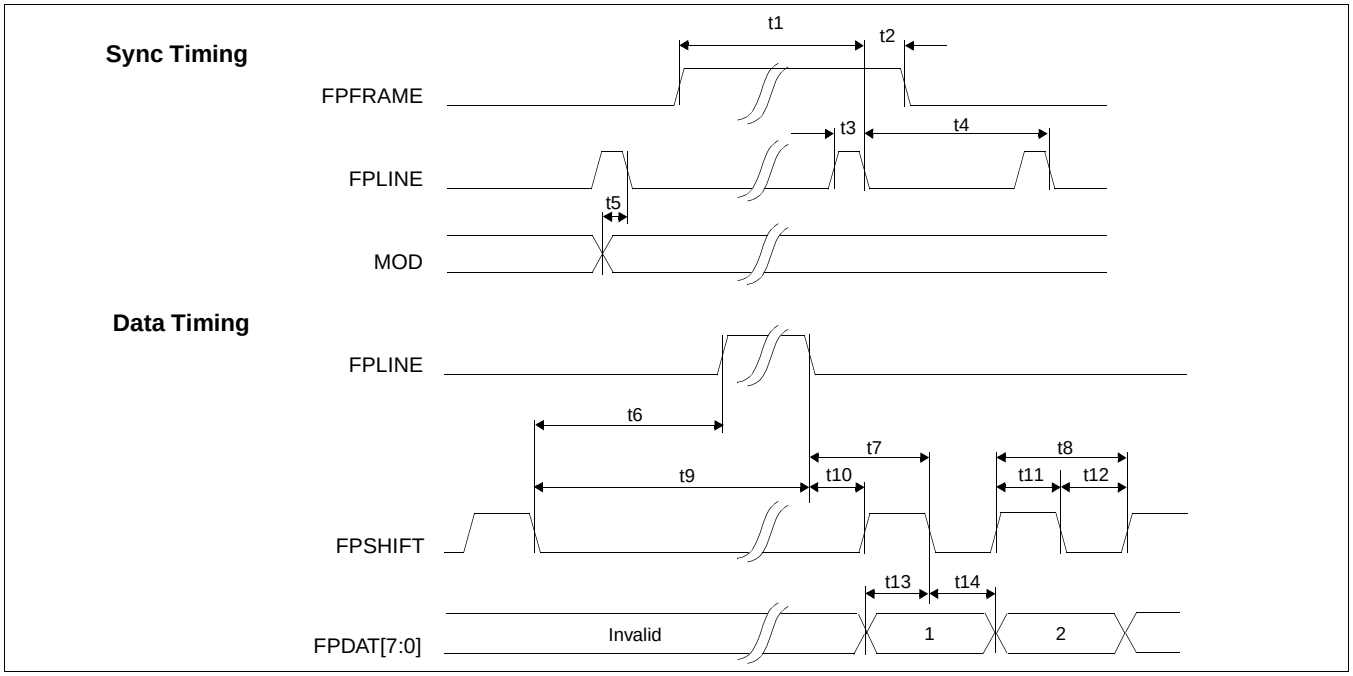



*Figure 6-17: Single Monochrome 8-Bit Panel A.C. Timing*

*Table 6-19 : Single Monochrome 8-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 4 | | | Ts |
| t8 | FPSHIFT period | 8 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 4 | | | Ts |
| t12 | FPSHIFT pulse width low | 4 | | | Ts |
| t13 | FPDAT[7:0] setup to FPSHIFT falling edge | 4 | | | Ts |
| t14 | FPDAT[7:0] hold to FPSHIFT falling edge | 4 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. $t1_{min}$ = $t4_{min}$ - 12
3. $t4_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 24] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 23] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 13] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 12] for 16 bpp color depth
7. $t10_{min}$ = 17 for 4 bpp or 8 bpp color depth
   = 16 for 16 bpp color depth

### 6.5.3 Single Color 4-Bit Panel Timing

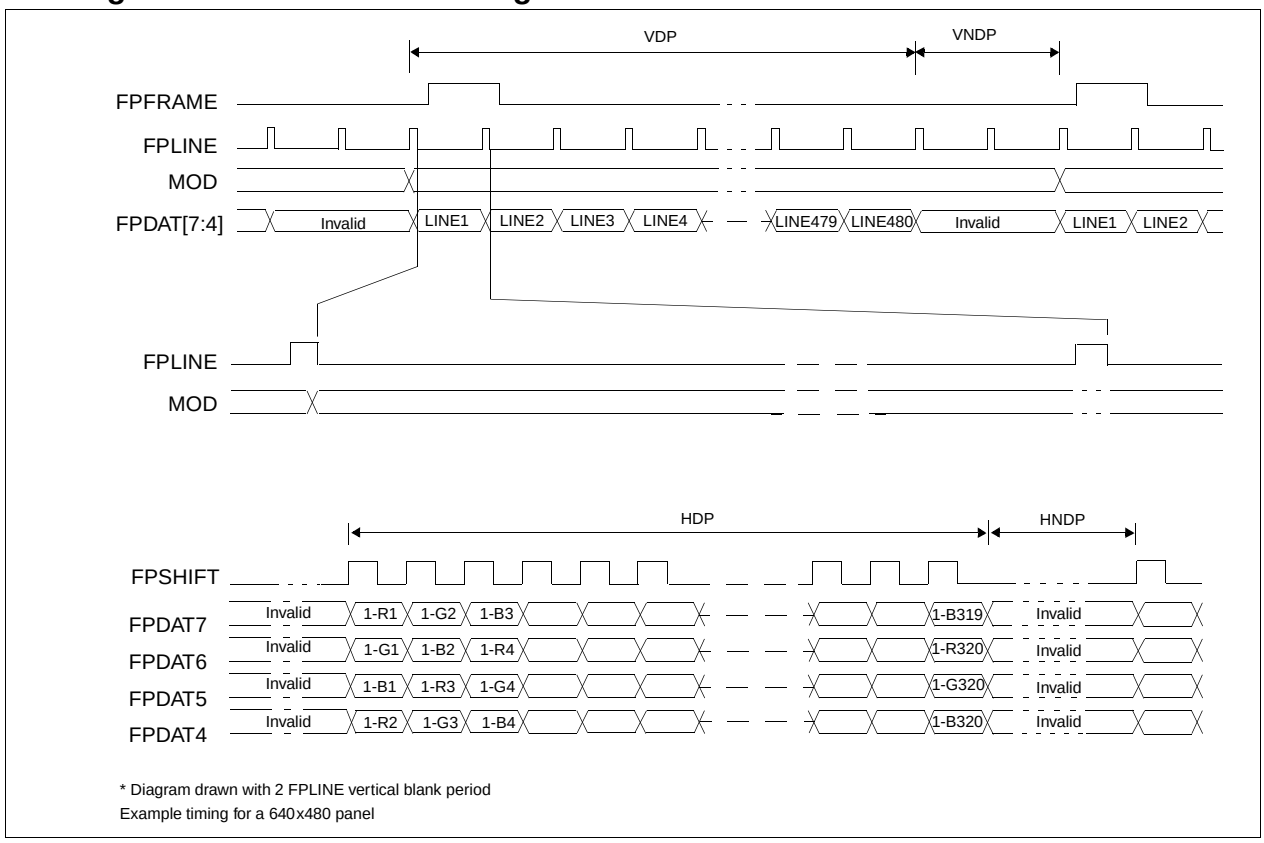



*Figure 6-18: Single Color 4-Bit Panel Timing*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

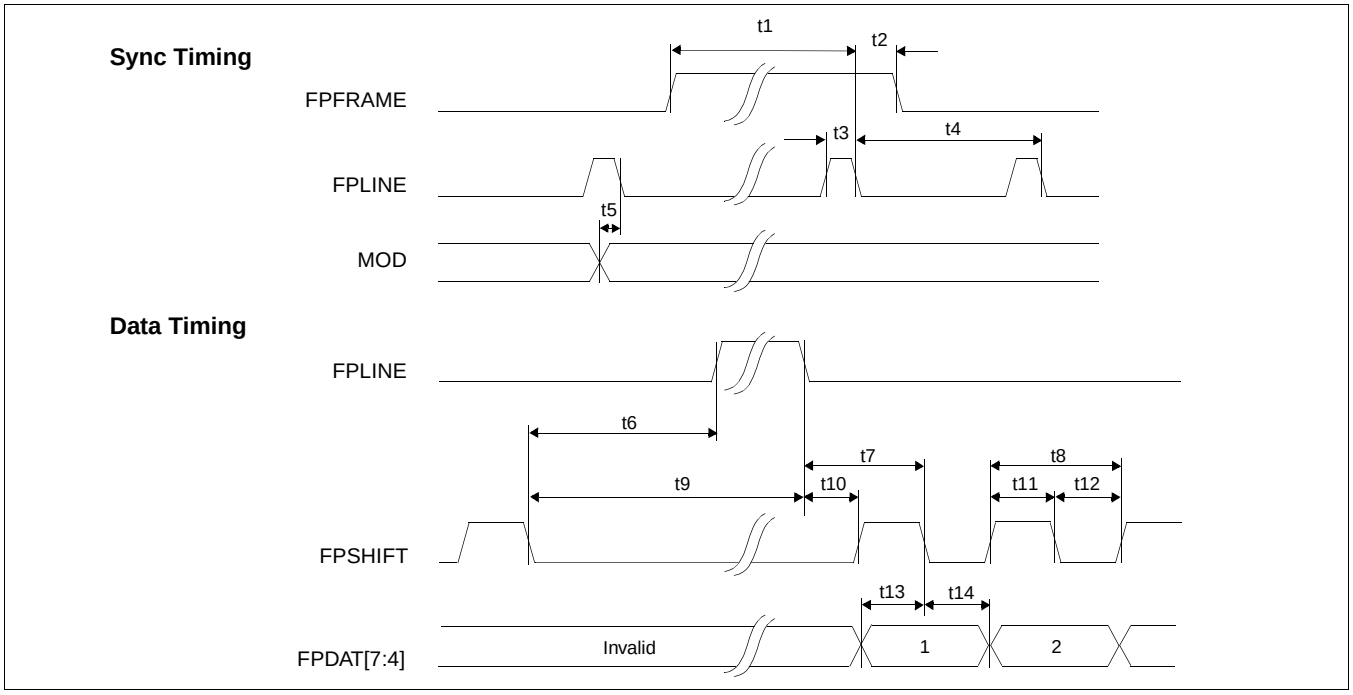


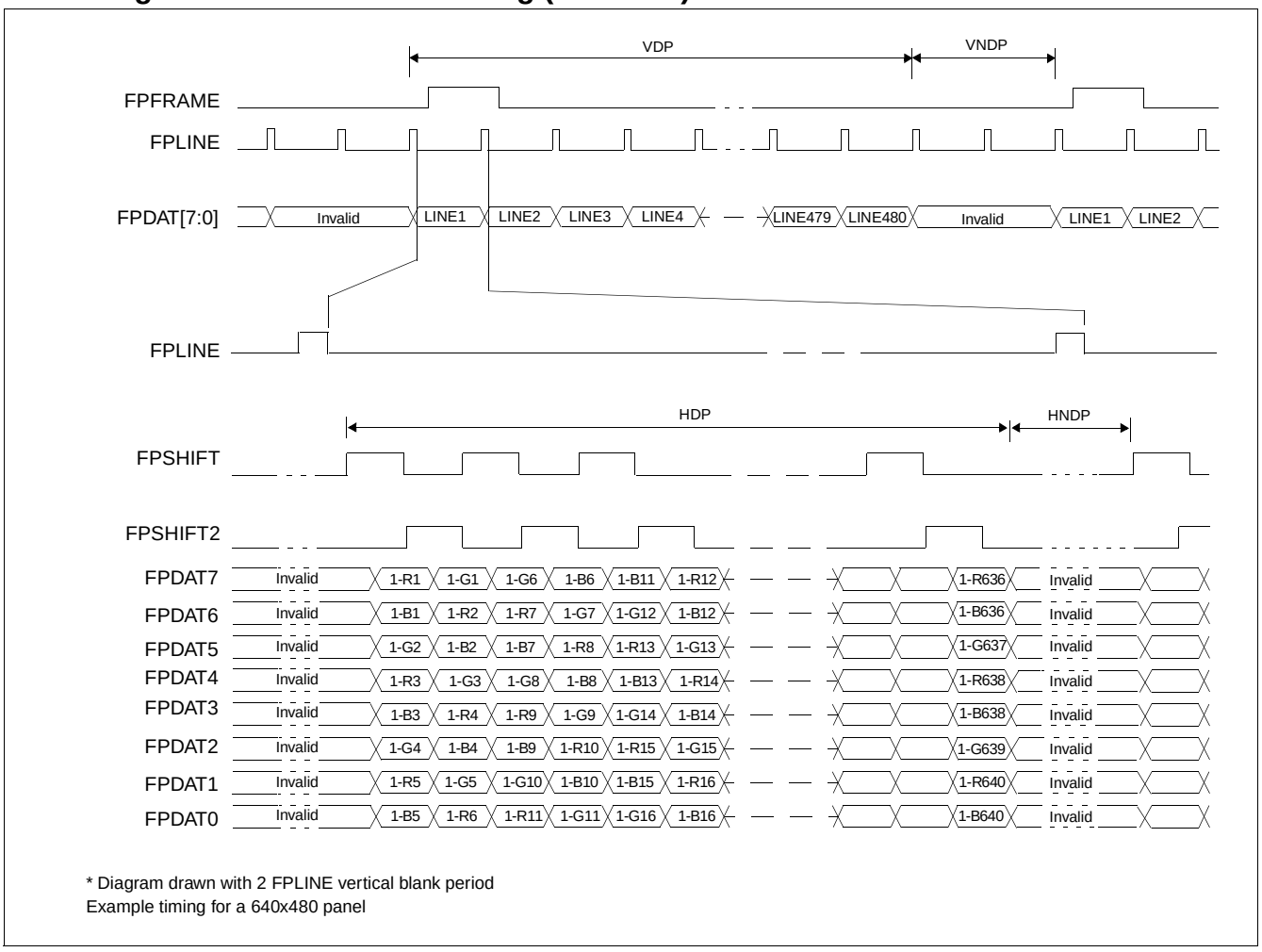

*Figure 6-19: Single Color 4-Bit Panel A.C. Timing*

*Table 6-20 : Single Color 4-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 0.5 | | | Ts |
| t8 | FPSHIFT period | 1 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 0.5 | | | Ts |
| t12 | FPSHIFT pulse width low | 0.5 | | | Ts |
| t13 | FPDAT[7:4] setup to FPSHIFT falling edge | 0.5 | | | Ts |
| t14 | FPDAT[7:4] hold from FPSHIFT falling edge | 0.5 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is LCD pixel clock source divided by 1, 2, 3 or 4 (see REG[014h]).
2. $t1_{min}$ = $t4_{min}$ - 12
3. $t4_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 28.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 27.5] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 17.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 16.5] for 16 bpp color depth
7. $t10_{min}$ = 18 for 4 bpp or 8 bpp color depth
   = 17 for 16 bpp color depth

### 6.5.4 Single Color 8-Bit Panel Timing (Format 1)




* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

*Figure 6-20: Single Color 8-Bit Panel Timing (Format 1)*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

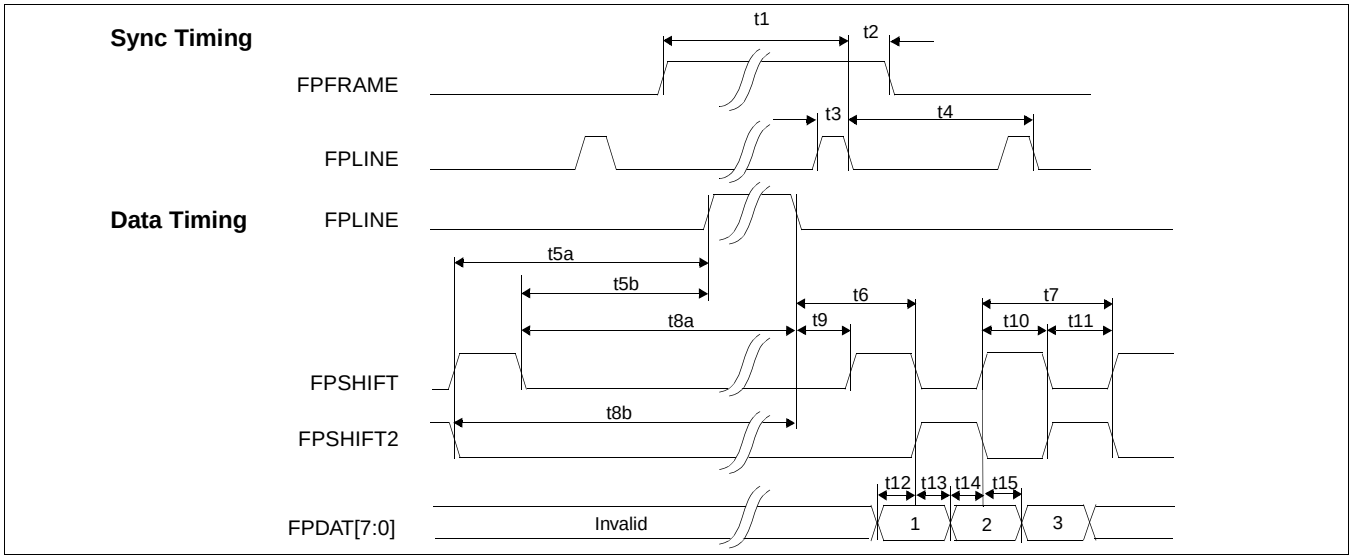



*Figure 6-21: Single Color 8-Bit Panel A.C. Timing (Format 1)*

*Table 6-21 : Single Color 8-Bit Panel A.C. Timing (Format 1)*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5a | FPSHIFT2 falling edge to FPLINE rising edge | note 4 | | | Ts |
| t5b | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t6 | FPLINE falling edge to FPSHIFT falling, FPSHIFT2 rising edge | t9 + 2 | | | Ts |
| t7 | FPSHIFT, FPSHIFT2 period | 4 | | | Ts |
| t8a | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t8b | FPSHIFT2 falling edge to FPLINE falling edge | note 7 | | | Ts |
| t9 | FPLINE falling edge to FPSHIFT rising edge | note 8 | | | Ts |
| t10 | FPSHIFT pulse width high, FPSHIFT2 pulse width low | 2 | | | Ts |
| t11 | FPSHIFT pulse width low, FPSHIFT2 pulse width high | 2 | | | Ts |
| t12 | FPDAT[7:0] setup to FPSHIFT falling edge | 1 | | | Ts |
| t13 | FPDAT[7:0] hold from FPSHIFT falling edge | 1 | | | Ts |
| t14 | FPDAT[7:0] setup to FPSHIFT2 falling edge | 1 | | | Ts |
| t15 | FPDAT[7:0] hold from FPSHIFT2 falling edge | 1 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t1_{min}$ = $t4_{min}$ - 12Ts
3. $t4_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5a_{min}$= [((REG[034h] bits [4:0]) + 1) × 8 - 26] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 16 bpp color depth
5. $t5b_{min}$= [((REG[034h] bits [4:0]) + 1) × 8 - 28] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 27] for 16 bpp color depth
6. $t8a_{min}$= [((REG[034h] bits [4:0]) + 1) × 8 - 17] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 16] for 16 bpp color depth
7. $t8b_{min}$= [((REG[034h] bits [4:0]) + 1) × 8 - 15] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 16 bpp color depth
8. $t9_{min}$ = 17 for 4 bpp or 8 bpp color depth
   = 16 for 16 bpp color depth

### 6.5.5 Single Color 8-Bit Panel Timing (Format 2)

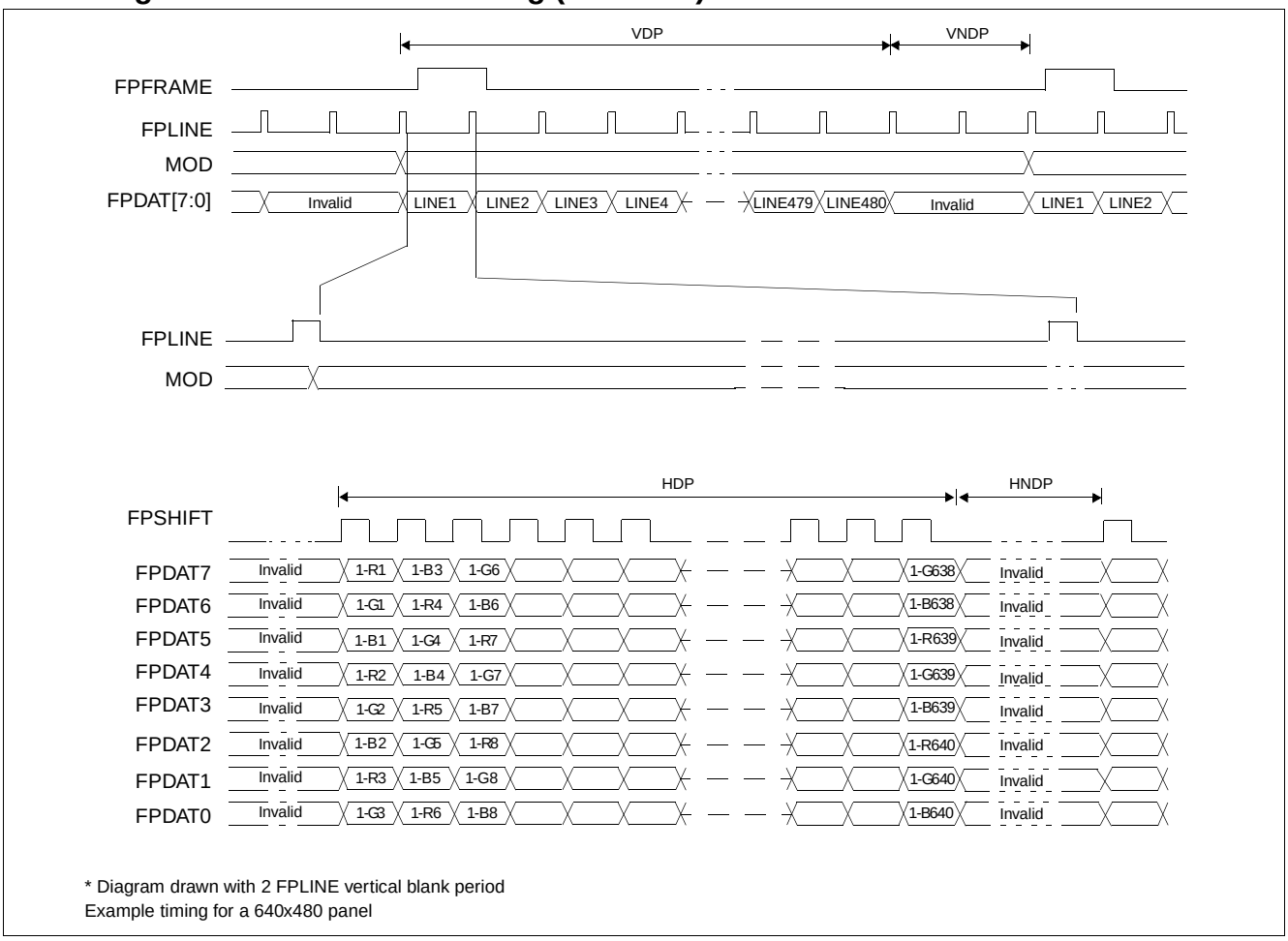



*Figure 6-22: Single Color 8-Bit Panel Timing (Format 2)*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

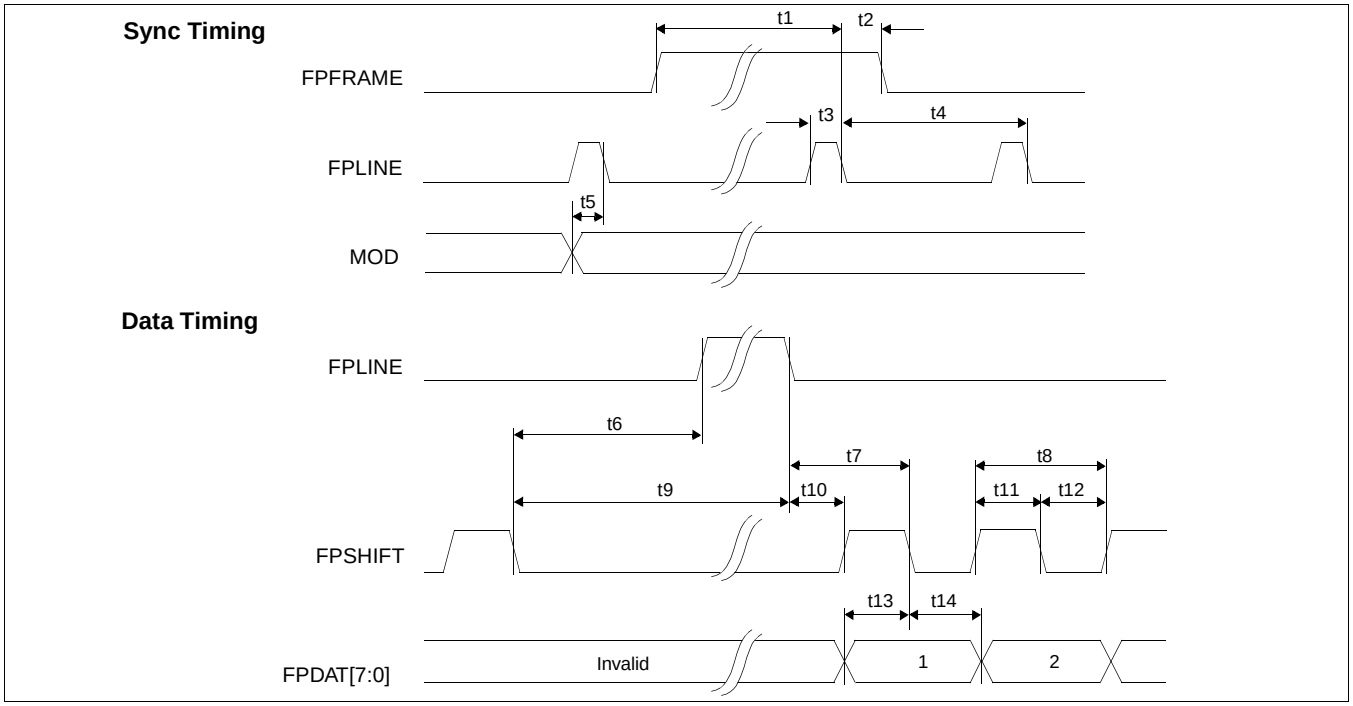



*Figure 6-23: Single Color 8-Bit Panel A.C. Timing (Format 2)*

*Table 6-22 : Single Color 8-Bit Panel A.C. Timing (Format 2)*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 2 | | | Ts |
| t8 | FPSHIFT period | 2 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 1 | | | Ts |
| t12 | FPSHIFT pulse width low | 1 | | | Ts |
| t13 | FPDAT[7:0] setup to FPSHIFT falling edge | 1 | | | Ts |
| t14 | FPDAT[7:0] hold to FPSHIFT falling edge | 1 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t1_{min}$ = $t3_{min}$ - 12
3. $t3_{min}$ = [((REG[032h] bits [6:0]) + 1) $\times$ 8 + ((REG[034h] bits [4:0]) + 1) $\times$ 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) $\times$ 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 27] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 26] for or 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 16] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) $\times$ 8 - 15] for 16 bpp color depth
7. $t10_{min}$= 17 for 4 bpp or 8 bpp color depth
   = 16 for 16 bpp color depth

## 6.5.6 Single Color 16-Bit Panel Timing

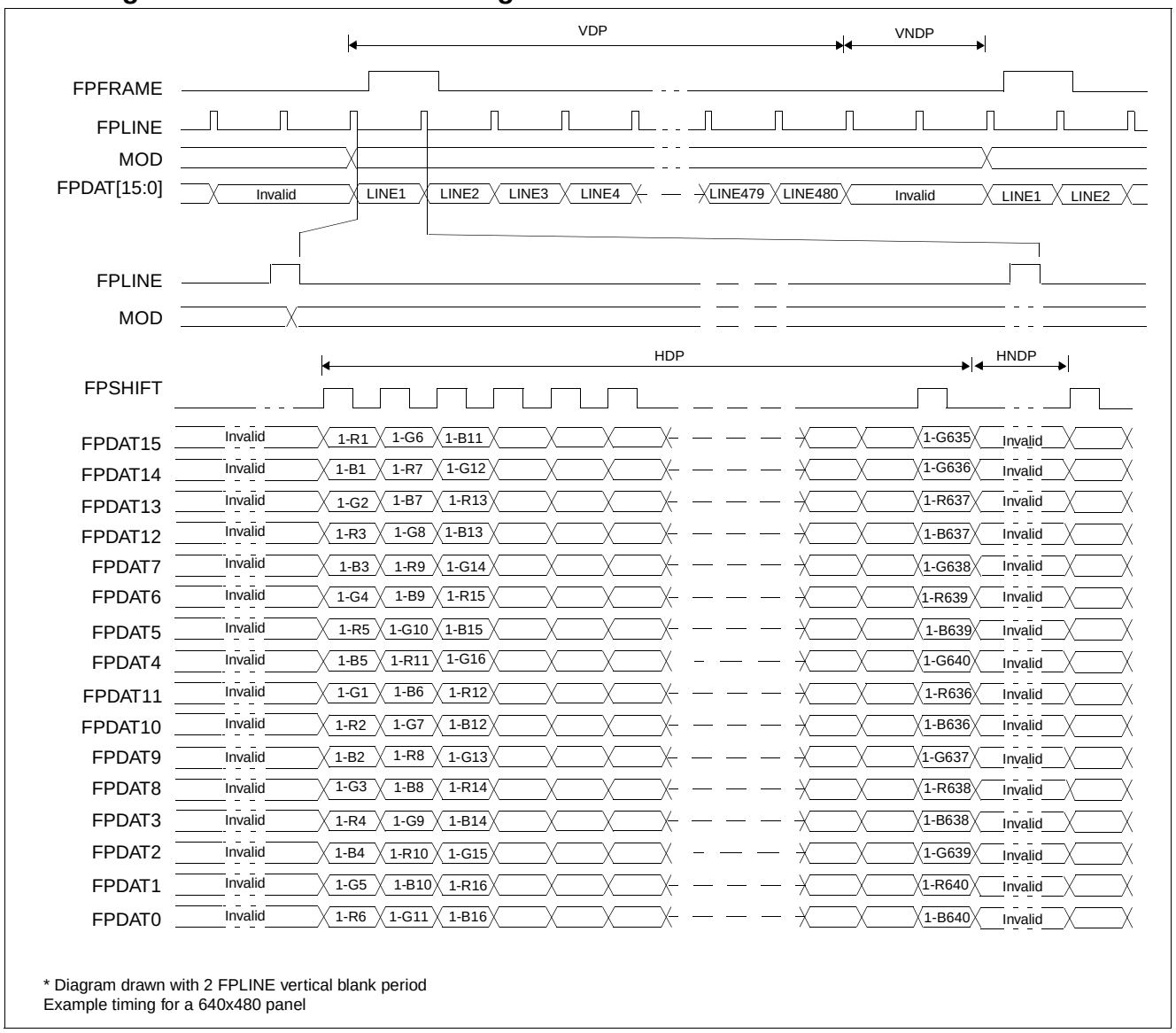



*Figure 6-24: Single Color 16-Bit Panel Timing*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

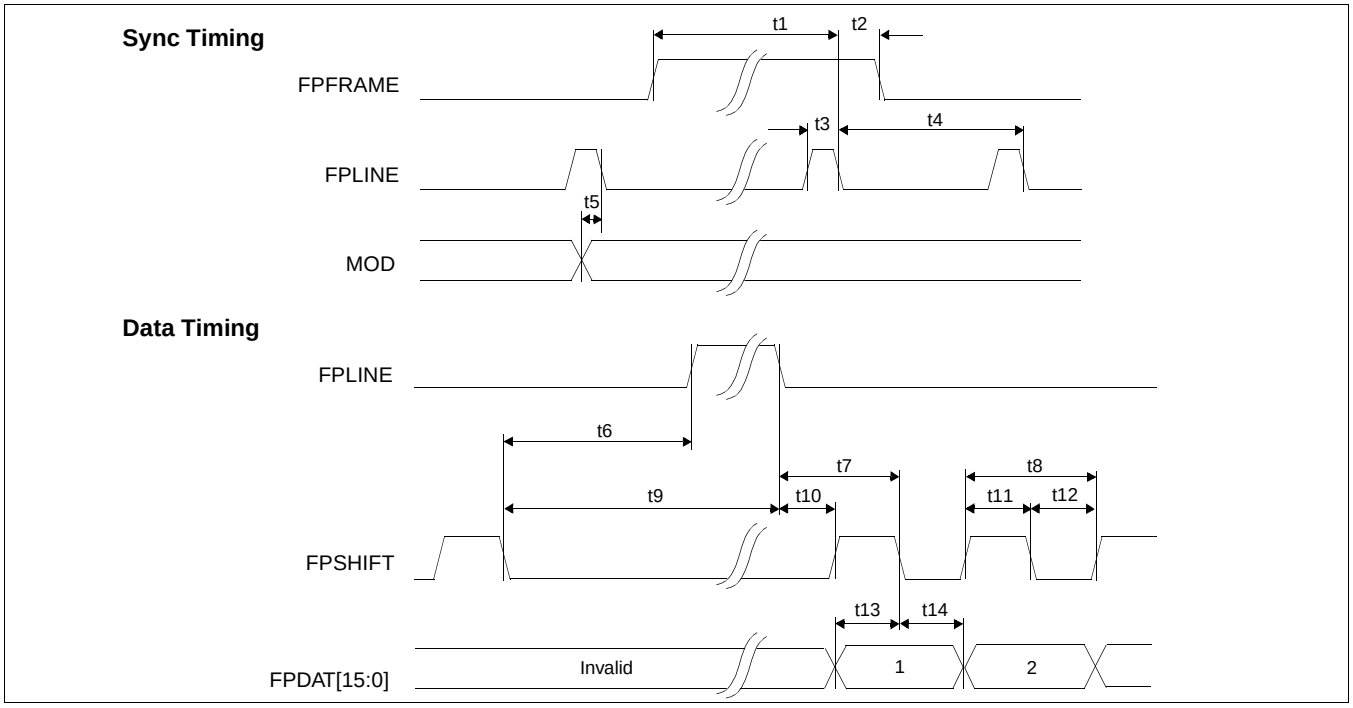



*Figure 6-25: Single Color 16-Bit Panel A.C. Timing*

*Table 6-23 : Single Color 16-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 3 | | | Ts |
| t8 | FPSHIFT period | 5 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 2 | | | Ts |
| t12 | FPSHIFT pulse width low | 2 | | | Ts |
| t13 | FPDAT[15:0] setup to FPSHIFT falling edge | 2 | | | Ts |
| t14 | FPDAT[15:0] hold to FPSHIFT falling edge | 2 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t1_{min}$ = $t3_{min}$ - 12
3. $t3_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 26] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 25] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 15] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 14] for 16 bpp color depth
7. $t10_{min}$ = 17 for 4 bpp or 8 bpp color depth
   = 16 for 16 bpp color depth

### 6.5.7 Dual Monochrome 8-Bit Panel Timing

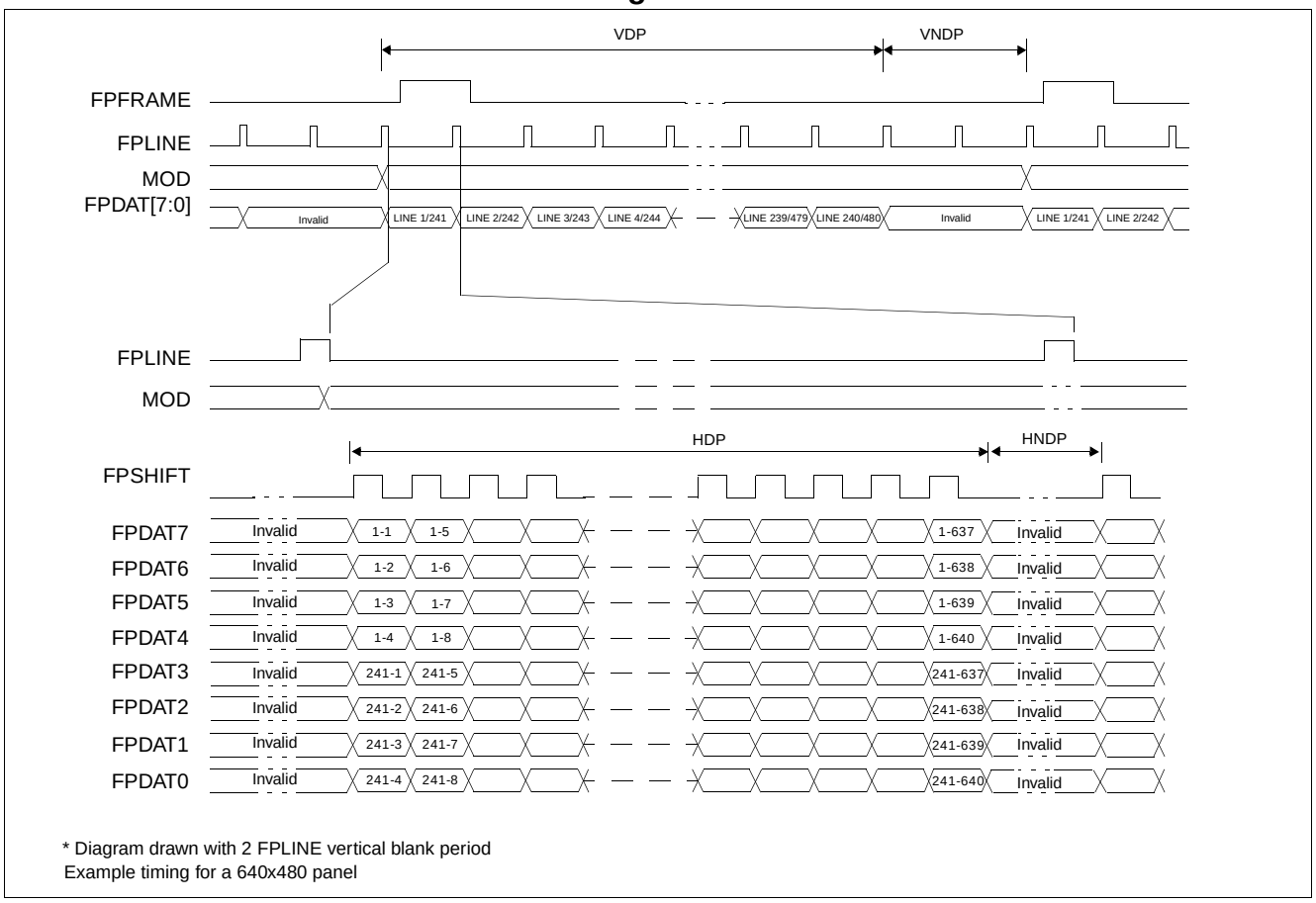



*Figure 6-26: Dual Monochrome 8-Bit Panel Timing*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:1])
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

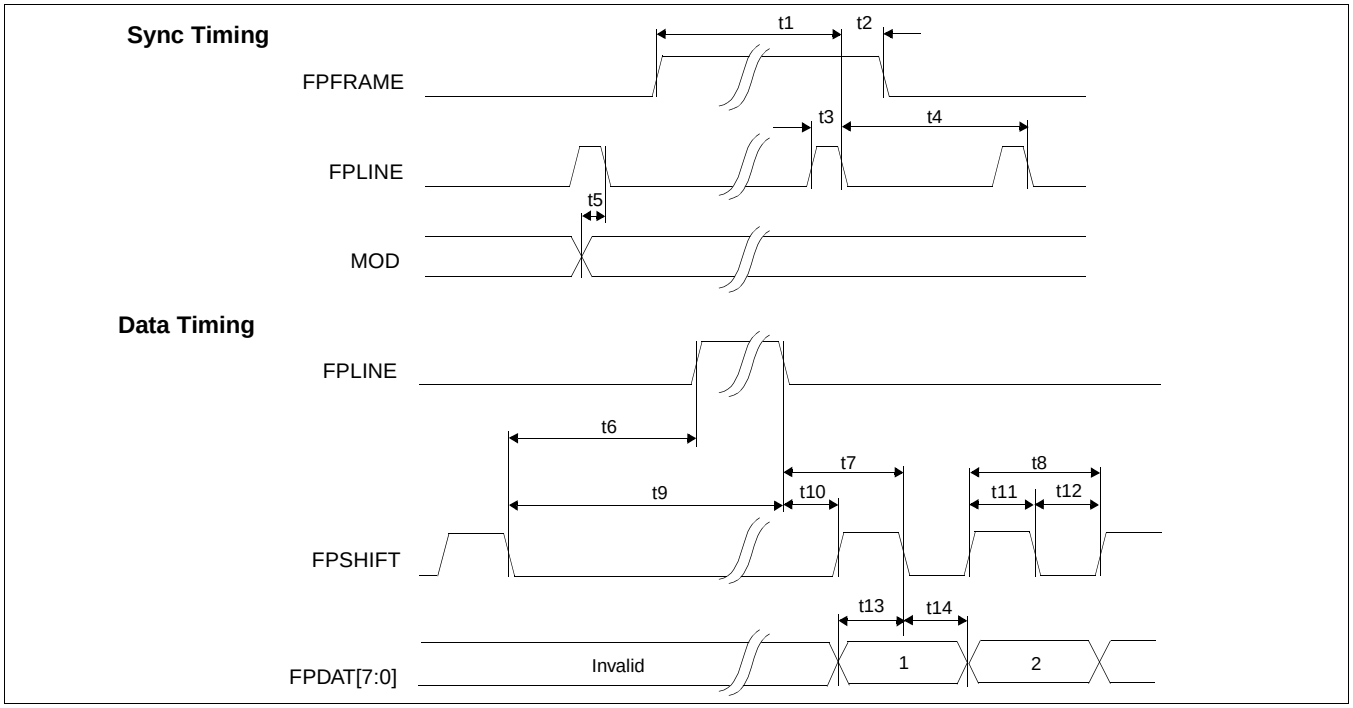



*Figure 6-27: Dual Monochrome 8-Bit Panel A.C. Timing*

*Table 6-24 : Dual Monochrome 8-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 2 | | | Ts |
| t8 | FPSHIFT period | 4 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t12 | FPSHIFT pulse width low | 2 | | | Ts |
| t11 | FPSHIFT pulse width high | 2 | | | Ts |
| t13 | FPDAT[7:0] setup to FPSHIFT falling edge | 2 | | | Ts |
| t14 | FPDAT[7:0] hold to FPSHIFT falling edge | 2 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t1_{min}$ = $t3_{min}$ - 12
3. $t3_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 18] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 17] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 7] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 6] for 16 bpp color depth
7. $t10_{min}$ = 9 for 4 bpp or 8 bpp color depth
   = 8 for 16 bpp color depth

## 6.5.8 Dual Color 8-Bit Panel Timing

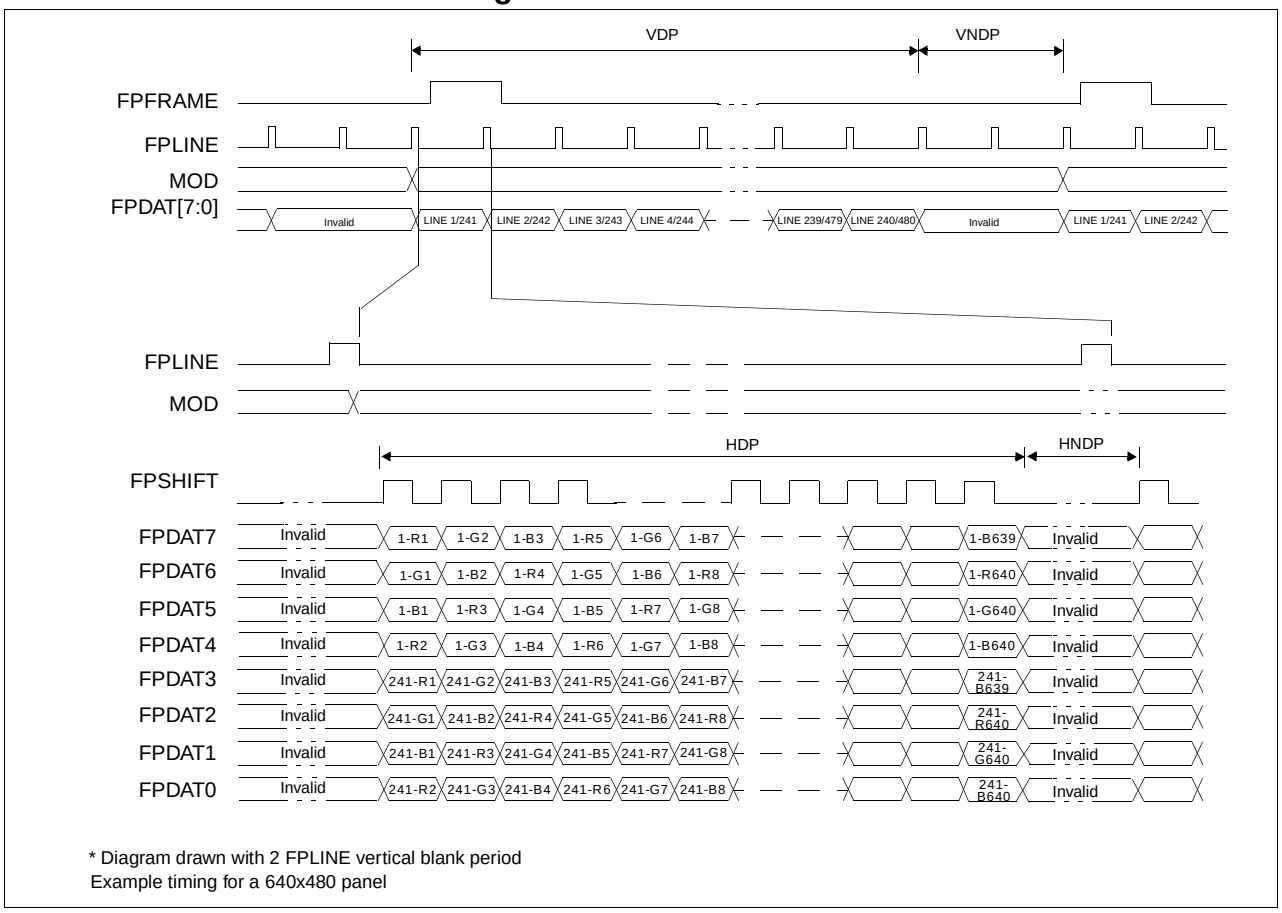



*Figure 6-28: Dual Color 8-Bit Panel Timing*

VDP = Vertical Display Period = ((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) ÷ 2
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

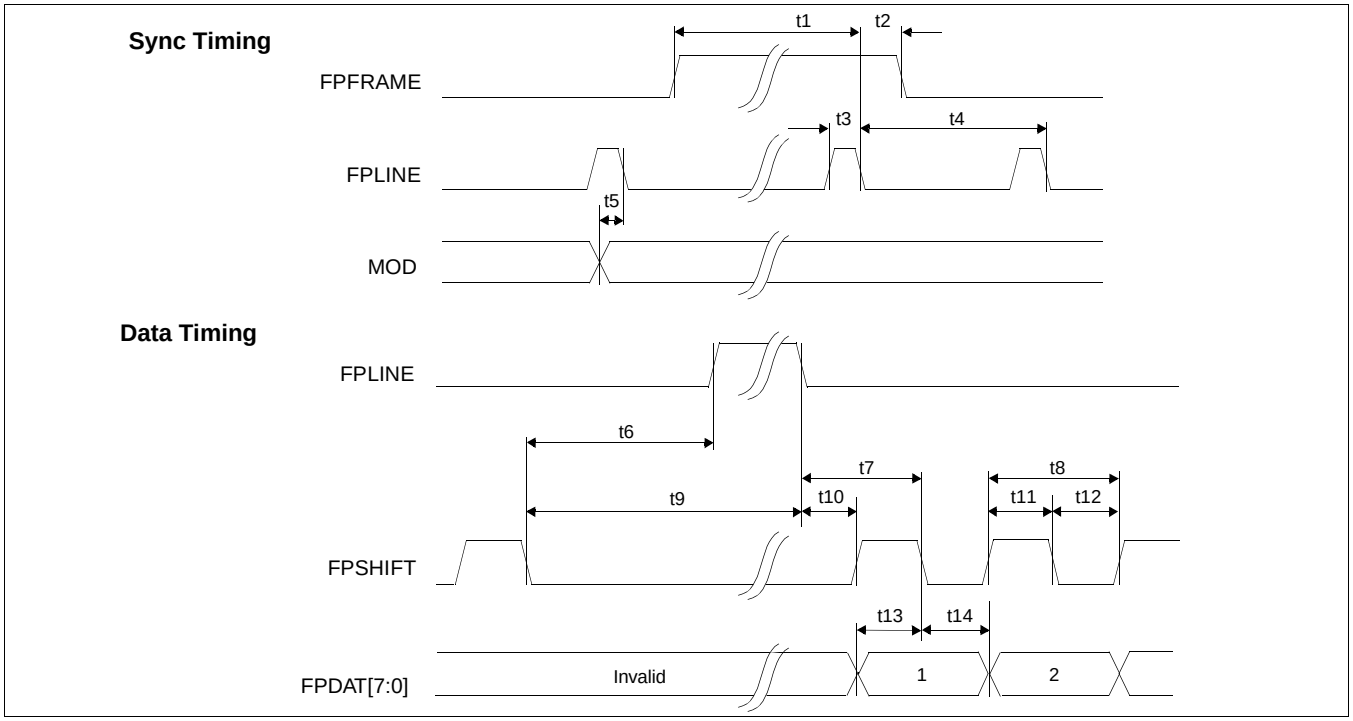


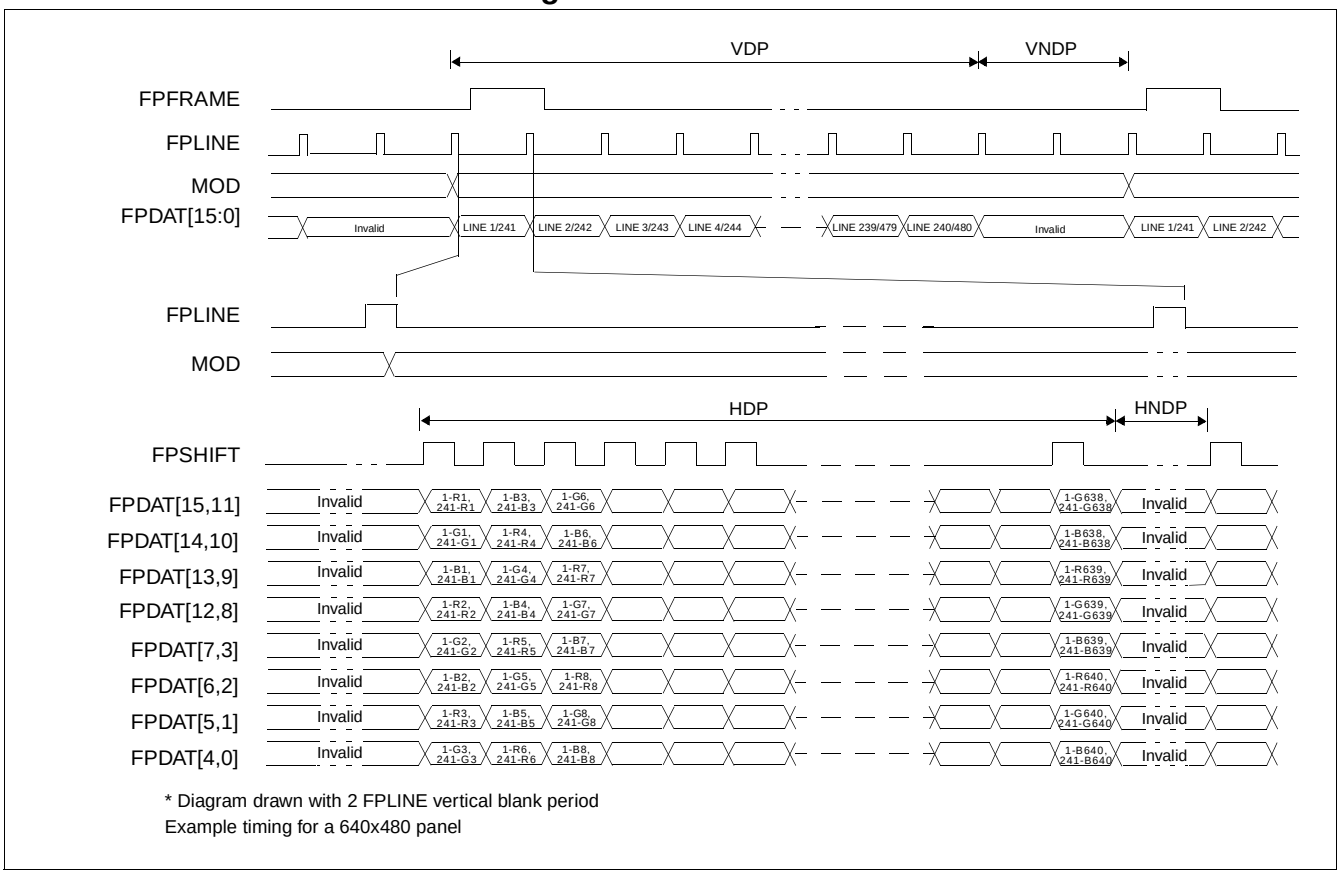

*Figure 6-29: Dual Color 8-Bit Panel A.C. Timing*

*Table 6-25 : Dual Color 8-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 0.5 | | | Ts |
| t8 | FPSHIFT period | 1 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 0.5 | | | Ts |
| t12 | FPSHIFT pulse width low | 0.5 | | | Ts |
| t13 | FPDAT[7:0] setup to FPSHIFT falling edge | 0.5 | | | Ts |
| t14 | FPDAT[7:0] hold to FPSHIFT falling edge | 0.5 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t1_{min}$ = $t3_{min}$ - 12
3. $t3_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 18.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 17.5] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 8.5] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 6.5] for 16 bpp color depth
7. $t10_{min}$= 10 for 4 bpp or 8 bpp color depth
   = 9 for 16 bpp color depth

## 6.5.9 Dual Color 16-Bit Panel Timing




* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

*Figure 6-30: Dual Color 16-Bit Panel Timing*

VDP = Vertical Display Period = ((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) ÷ 2
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = ((REG[034h] bits [4:0]) + 1) × 8Ts

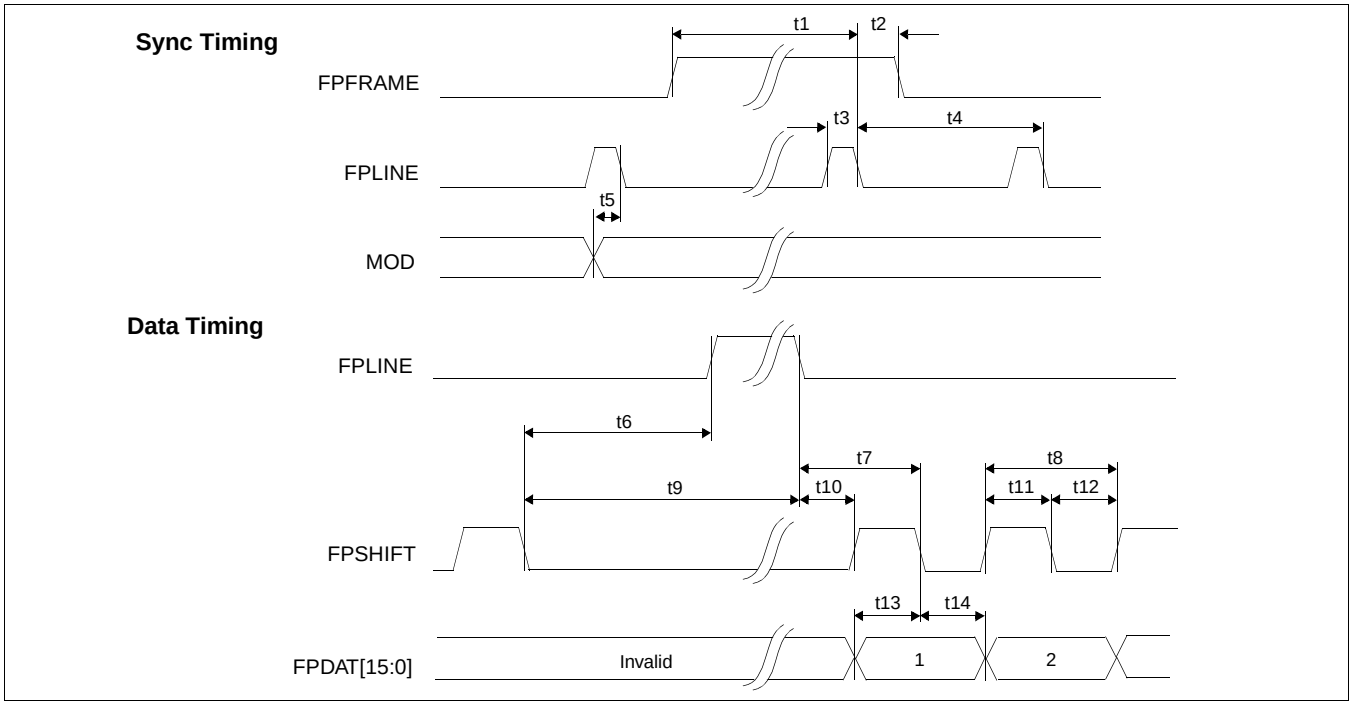



*Figure 6-31: Dual Color 16-Bit Panel A.C. Timing*

*Table 6-26 : Dual Color 16-Bit Panel A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPFRAME setup to FPLINE falling edge | note 2 | | | Ts (note 1) |
| t2 | FPFRAME hold from FPLINE falling edge | 12 | | | Ts |
| t3 | FPLINE pulse width | 11 | | | Ts |
| t4 | FPLINE period | note 3 | | | Ts |
| t5 | MOD transition to FPLINE falling edge | 3 | | note 4 | Ts |
| t6 | FPSHIFT falling edge to FPLINE rising edge | note 5 | | | Ts |
| t7 | FPLINE falling edge to FPSHIFT falling edge | t10 + 2 | | | Ts |
| t8 | FPSHIFT period | 2 | | | Ts |
| t9 | FPSHIFT falling edge to FPLINE falling edge | note 6 | | | Ts |
| t10 | FPLINE falling edge to FPSHIFT rising edge | note 7 | | | Ts |
| t11 | FPSHIFT pulse width high | 1 | | | Ts |
| t12 | FPSHIFT pulse width low | 1 | | | Ts |
| t13 | FPDAT[15:0] setup to FPSHIFT falling edge | 1 | | | Ts |
| t14 | FPDAT[15:0] hold to FPSHIFT falling edge | 1 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t1_{min}$ = $t3_{min}$ - 12
3. $t3_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
4. $t5_{max}$ = [((REG[034h] bits [4:0]) + 1) × 8 + 3]
5. $t6_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 19] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 18] for 16 bpp color depth
6. $t9_{min}$ = [((REG[034h] bits [4:0]) + 1) × 8 - 8] for 4 bpp or 8 bpp color depth
   = [((REG[034h] bits [4:0]) + 1) × 8 - 7] for 16 bpp color depth
7. $t10_{min}$ = 9 for 4 bpp or 8 bpp color depth
   = 8 for 16 bpp color depth

## 6.5.10 TFT/D-TFD Panel Timing

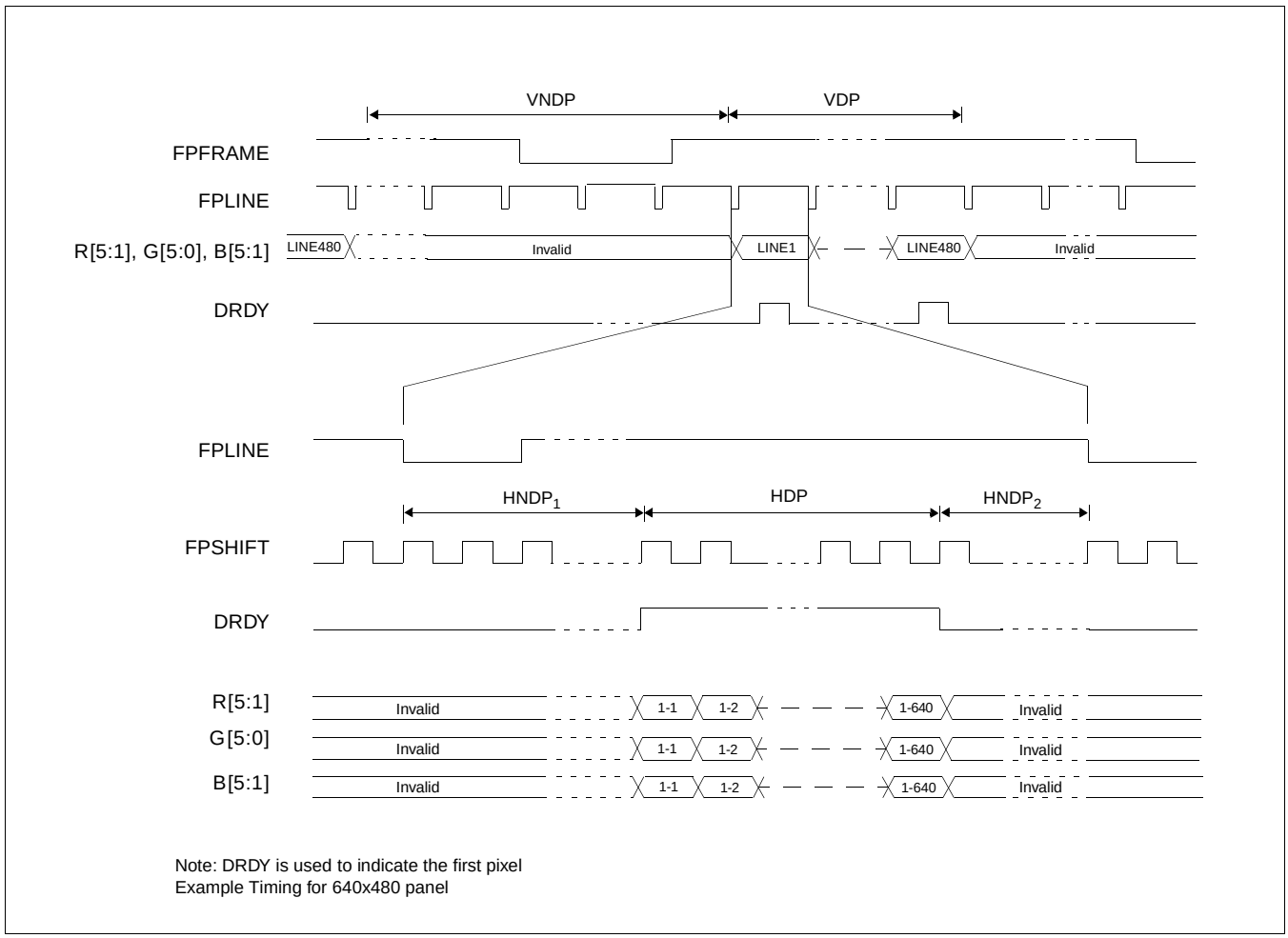



*Figure 6-32: TFT/D-TFD Panel Timing*

VDP = Vertical Display Period = (REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1
VNDP = Vertical Non-Display Period = (REG[03Ah] bits [5:0]) + 1
HDP = Horizontal Display Period = ((REG[032h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = $HNDP_1 + HNDP_2$ = ((REG[034h] bits [4:0]) + 1) × 8Ts

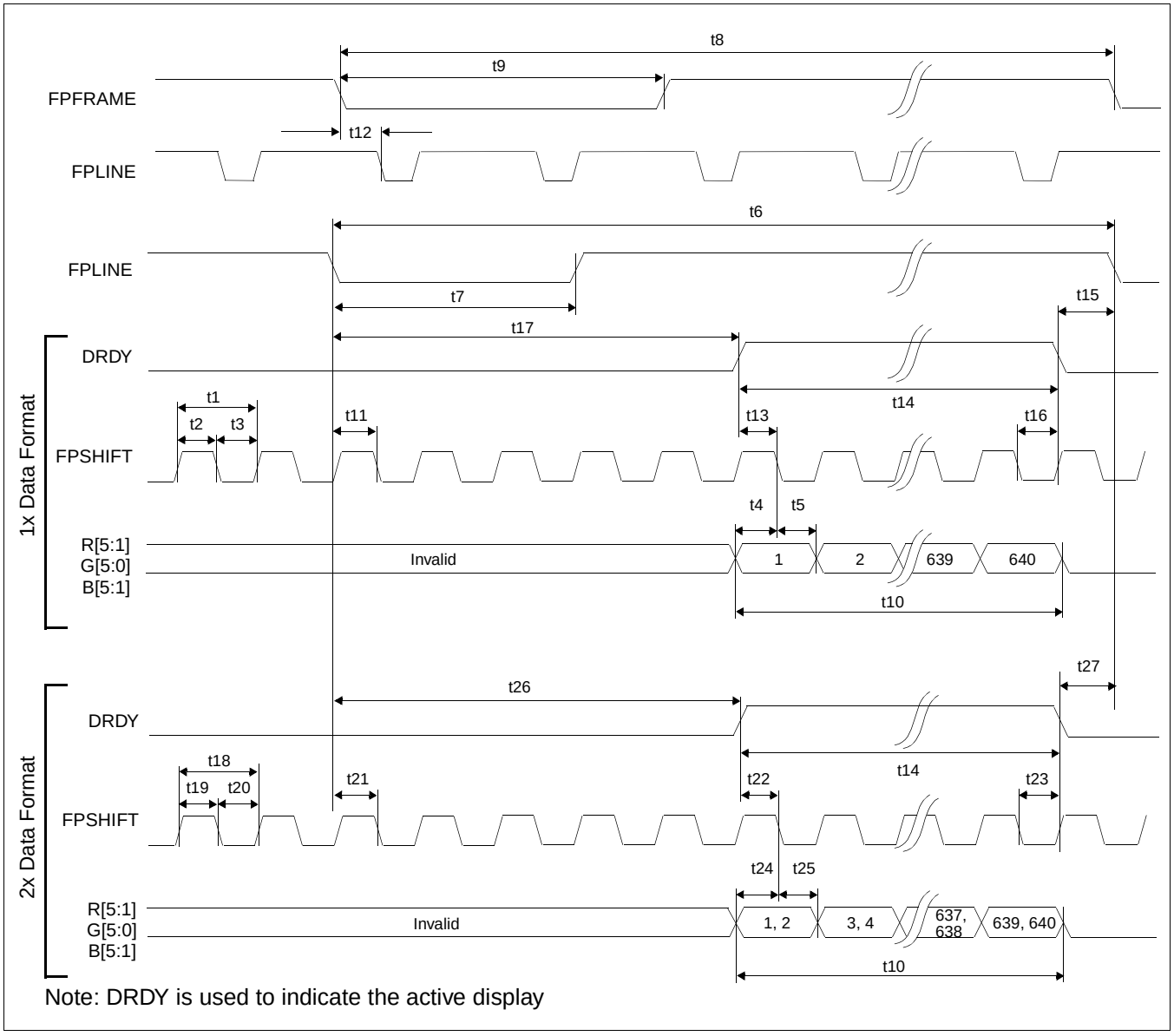



*Figure 6-33: TFT/D-TFD A.C. Timing*

*Table 6-27 : TFT/D-TFD A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | FPSHIFT period | 1 | | | Ts (note 1) |
| t2 | FPSHIFT pulse width high | 0.45 | | | Ts |
| t3 | FPSHIFT pulse width low | 0.45 | | | Ts |
| t4 | data setup to FPSHIFT falling edge | 0.45 | | | Ts |
| t5 | data hold from FPSHIFT falling edge | 0.45 | | | Ts |
| t6 | FPLINE cycle time | note 2 | | | Ts |
| t7 | FPLINE pulse width low | note 3 | | | Ts |
| t8 | FPFRAME cycle time | note 4 | | | lines |
| t9 | FPFRAME pulse width low | note 5 | | | lines |
| t10 | horizontal display period | note 6 | | | Ts |
| t11 | FPLINE setup to FPSHIFT falling edge | 0.45 | | | Ts |
| t12 | FPFRAME falling edge to FPLINE falling edge phase difference | note 7 | | | Ts |
| t13 | DRDY to FPSHIFT falling edge setup time | 0.45 | | | Ts |
| t14 | DRDY pulse width | note 8 | | | Ts |
| t15 | DRDY falling edge to FPLINE falling edge (1x) | note 9 | | | Ts |
| t16 | DRDY hold from FPSHIFT falling edge | 0.45 | | | Ts |
| t17 | FPLINE Falling edge to DRDY active (1x) | note 10 | | | Ts |
| t18 | FPSHIFT period | 2 | | | Ts |
| t19 | FPSHIFT pulse width high | 1 | | | Ts |
| t20 | FPSHIFT pulse width low | 1 | | | Ts |
| t21 | FPLINE setup to FPSHIFT falling edge | note 11 | | | Ts |
| t22 | DRDY to FPSHIFT falling edge setup time | 1 | | | Ts |
| t23 | DRDY hold from FPSHIFT falling edge | 1 | | | Ts |
| t24 | data setup to FPSHIFT falling edge | 1 | | | Ts |
| t25 | data hold from FPSHIFT falling edge | 1 | | | Ts |
| t26 | FPLINE Falling edge to DRDY active (2x) | note 12 | | | Ts |
| t27 | DRDY falling edge to FPLINE falling edge (2x) | note 13 | | | Ts |

1. Ts = LCD pixel clock period. LCD pixel clock frequency is source divided by 1, 2, 3 or 4(see REG[014h]).
2. $t6_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8 + ((REG[034h] bits [4:0]) + 1) × 8]
3. $t7_{min}$ = [((REG[036h] bits [3:0]) + 1) × 8]
4. $t8_{min}$ = [((REG[039h] bits [1:0], REG[038h] bits [7:0]) + 1) + ((REG[03Ah] bits [5:0]) + 1)]
5. $t9_{min}$ = [((REG[03Ch] bits [2:0]) + 1)]
6. $t10_{min}$ = [((REG[032h] bits [6:0]) + 1) × 8]
7. $t12_{min}$= [(REG[035h] bits [4:0]) × 8 + 1]
8. $t14_{min}$= [((REG[032h] bits [6:0]) + 1) × 8]
9. $t15_{min}$= [(REG[035h] bits [4:0]) × 8 + 5] for 4 bpp or 8 bpp color depth
   = [(REG[035h] bits [4:0]) × 8 + 6] for 16 bpp color depth
10. $t17_{min}$= [((REG[034h] bits [4:0]) + 1) × 8 - (REG[035h] bits [4:0]) × 8 - 5] for 4 bpp or 8 bpp color depth
    = [((REG[034h] bits [4:0]) + 1) × 8 - (REG[035h] bits [4:0]) × 8 - 6] for 16 bpp color depth
11. $t21_{min}$= 1 for 4 bpp or 8 bpp color depth
    = 0 for 16 bpp color depth
12. $t26_{min}$= [((REG[034h] bits [4:0]) + 1) × 8 - (REG[035h] bits [4:0]) × 8 - 4] for 4 bpp or 8 bpp color depth
    = [((REG[034h] bits [4:0]) + 1) × 8 - (REG[035h] bits [4:0]) × 8 - 5] for 16 bpp color depth
13. $t27_{min}$= [(REG[035h] bits [4:0]) × 8 + 4] for 4 bpp or 8 bpp color depth
    = [(REG[035h] bits [4:0]) × 8 + 5] for 16 bpp color depth

## 6.5.11 CRT Timing

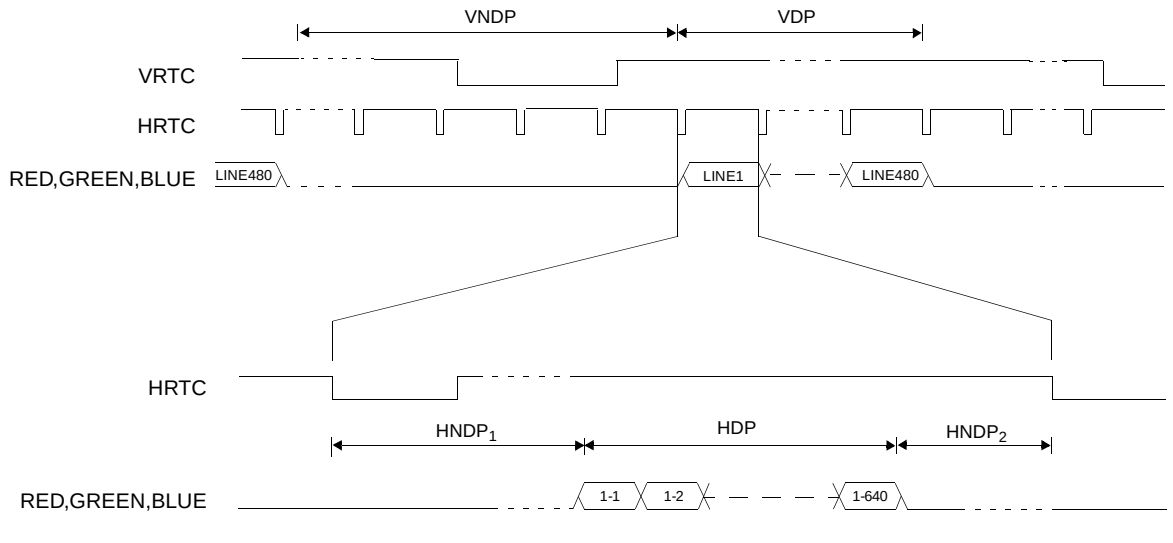



*Figure 6-34: CRT Timing*

| | | |
|---|---|---|
| VDP | = Vertical Display Period | = (REG[057h] bits [1:0], REG[056h] bits [7:0]) + 1 |
| VNDP | = Vertical Non-Display Period | = (REG[058h] bits [6:0]) + 1 |
| HDP | = Horizontal Display Period | = ((REG[050h] bits [6:0]) + 1) × 8Ts |
| HNDP | = Horizontal Non-Display Period | = $HNDP_1$ + $HNDP_2$<br>= ((REG[052h] bits [5:0]) + 1) × 8Ts |
| $HNDP_2$ | = HRTC Start Position | = (REG[053h] bits [5:0]) × 8 + 4Ts for 4/8 bpp<br>= (REG[053h] bits [5:0]) × 8 + 5Ts for 16 bpp |

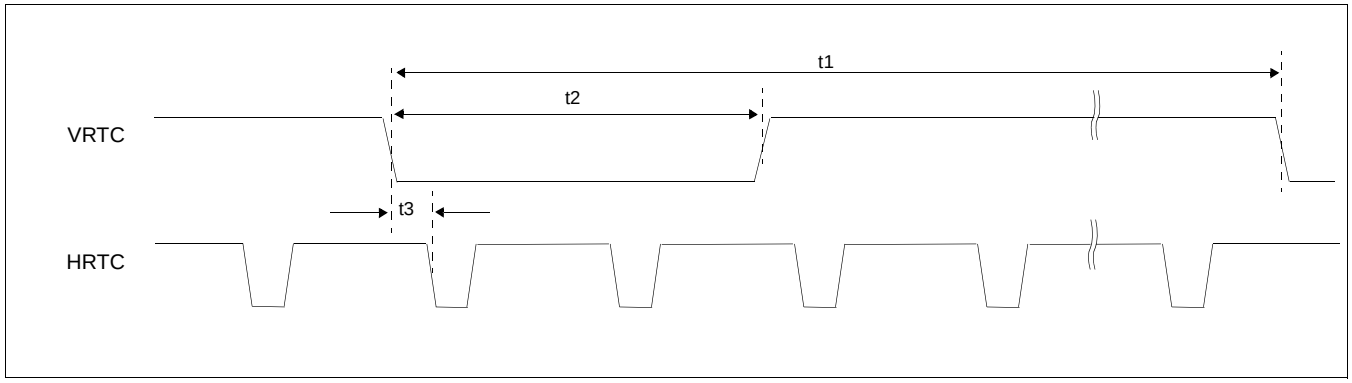



*Figure 6-35: CRT A.C. Timing*

*Table 6-28 : CRT A.C. Timing*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| t1 | VRTC cycle time | | note 1 | | lines |
| t2 | VRTC pulse width low | | note 2 | | lines |
| t3 | VRTC falling edge to FPLINE falling edge phase difference | | note 3 | | Ts |

1. t1 = [((REG[057h] bits 1:0, REG[056h] bits 7:0) + 1) + ((REG[058h] bits 6:0) + 1)]
2. t2 = [((REG[05Ah] bits 2:0) + 1)]
3. t3 = [((REG[053h] bits 4:0) + 1) × 8]

# 6.6 TV Timing

## 6.6.1 TV Output Timing

The overall NTSC and PAL video timing is shown in Figure 6-36: and Figure 6-37: respectively.

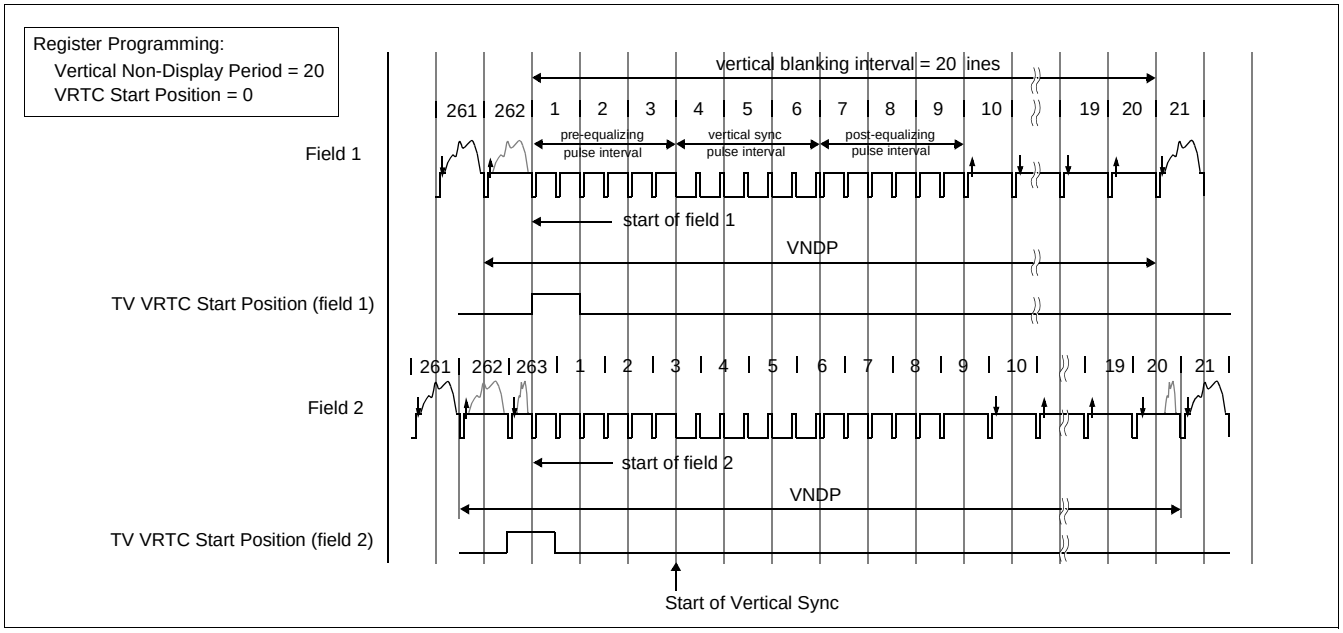



*Figure 6-36: NTSC Video Timing*

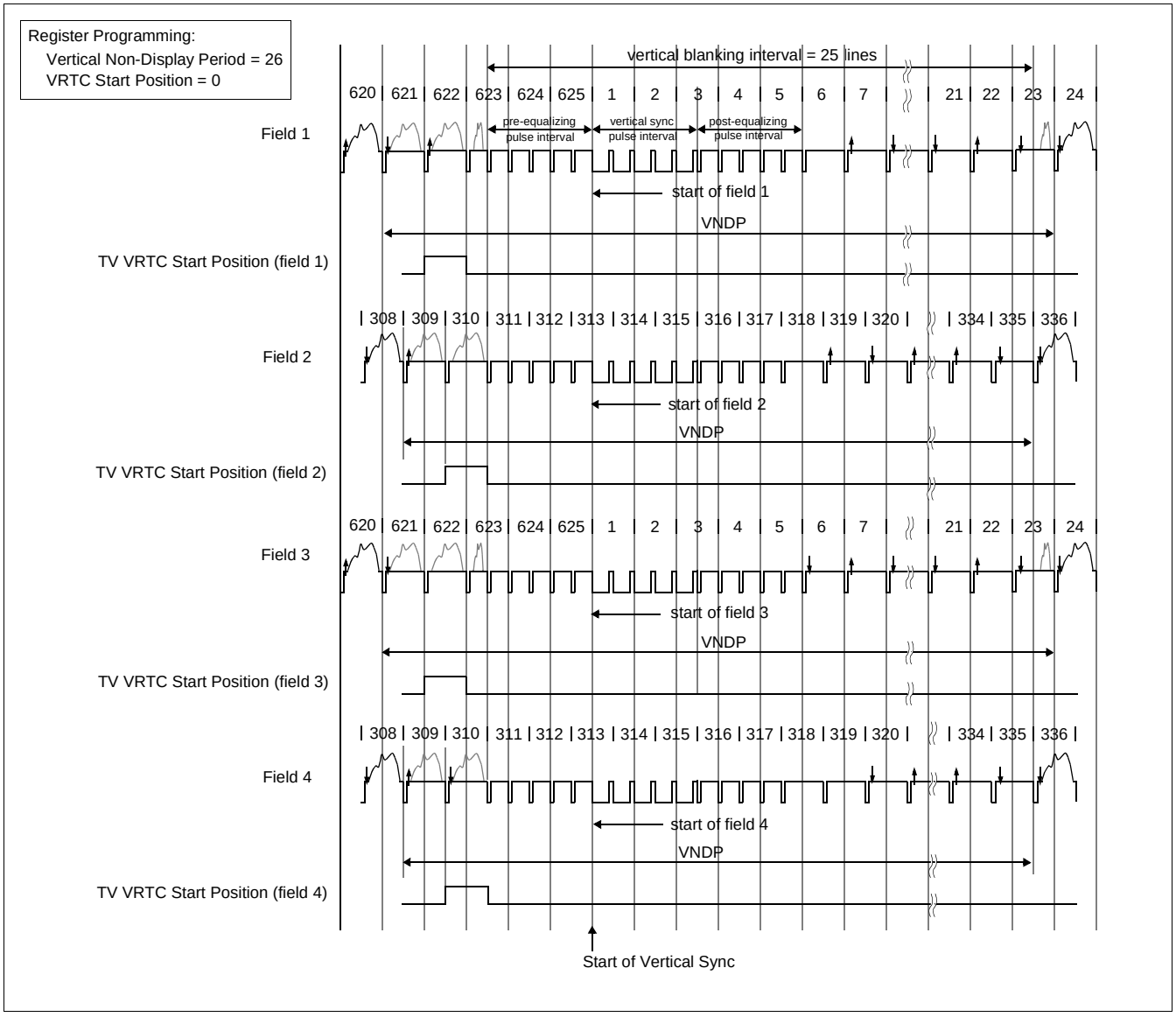



*Figure 6-37: PAL Video Timing*

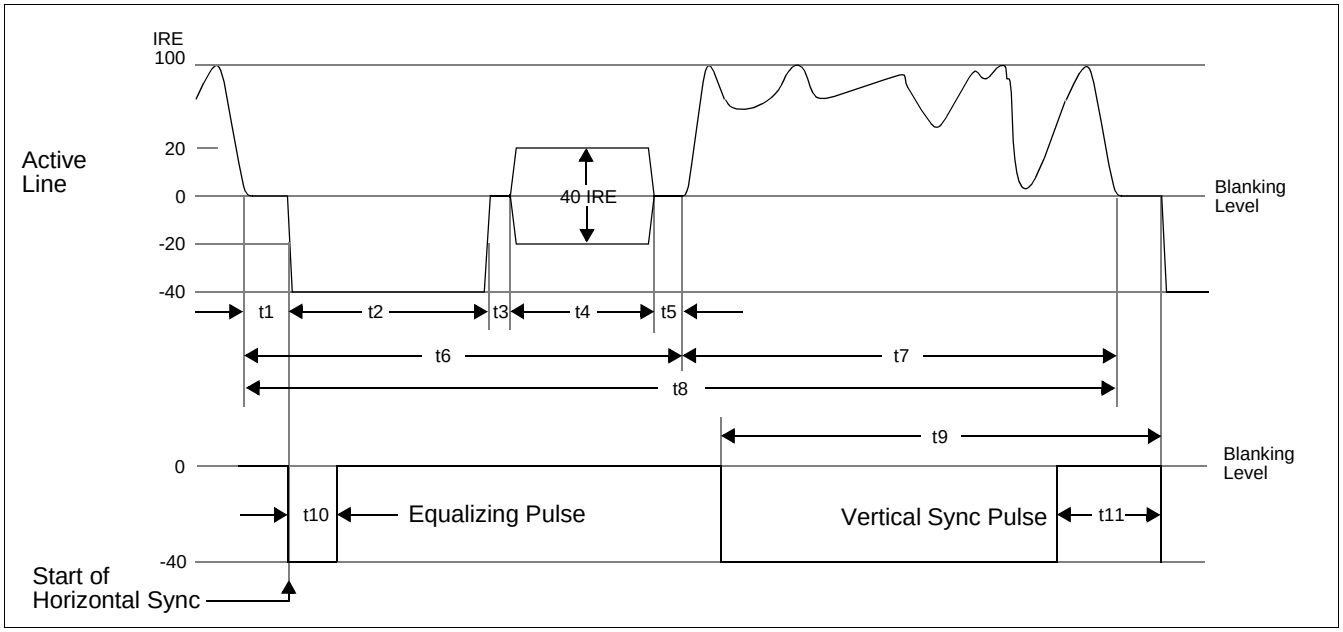



*Figure 6-38: Horizontal Timing for NTSC/PAL*

*Table 6-29 : Horizontal Timing for NTSC/PAL*

| Symbol | Parameter | NTSC | PAL | Units |
|---|---|---|---|---|
| $T_{4SC}$ | (4x Subcarrier clock) period | 69.841 | 56.387 | ns |
| t1 | Front Porch | note 1 | note 1 | $T_{4SC}$ |
| t2 | Horizontal Sync | 67 | 83 | $T_{4SC}$ |
| t3 | Breezeway | 9 | 16 | $T_{4SC}$ |
| t4 | Color Burst | 39 | 44 | $T_{4SC}$ |
| t5 | Color Back Porch | note 2 | note 3 | $T_{4SC}$ |
| t6 | Horizontal Blanking | note 4 | note 5 | $T_{4SC}$ |
| t7 | Active Video | note 6 | note 6 | $T_{4SC}$ |
| t8 | Line Period | 910 | 1135 | $T_{4SC}$ |
| t9 | Half Line Period | 455 | 568 / 567 | $T_{4SC}$ |
| t10 | Equalizing Pulse | 33 | 41 | $T_{4SC}$ |
| t11 | Vertical Serration | 67 | 83 | $T_{4SC}$ |

1. t1 = ((REG[053] bits[5:0]) + 1) × 8 - 6 (4bpp, 8bpp modes)
   = ((REG[053] bits[5:0]) + 1) × 8 - 5 (16bpp mode)
2. $t5_{NTSC}$ = (((REG[052] bits[5:0]) × 8) + 6) - (((REG[053] bits[5:0]) + 1) × 8) - 109 (4bpp, 8bpp modes)
   = (((REG[052] bits[5:0]) × 8) + 6) - (((REG[053] bits[5:0]) + 1) × 8) - 110 (16bpp mode)
3. $t5_{PAL}$ = (((REG[052] bits[5:0]) × 8) + 7) - (((REG[053] bits[5:0]) + 1) × 8) - 137 (4bpp, 8bpp modes)
   = (((REG[052] bits[5:0]) × 8) + 7) - (((REG[053] bits[5:0]) + 1) × 8) - 138 (16bpp mode)
4. $t6_{NTSC}$ = ((REG[052] bits[5:0]) × 8) + 6
5. $t6_{PAL}$ = ((REG[052] bits[5:0]) × 8) + 7
6. t7 = ((REG[050] bits[6:0]) + 1) × 8

**Important:**
REG[050] and REG[052] must be programmed to satisfy the Line Period (t8).
For NTSC, (((REG[050] bits[6:0]) + 1) × 8) + (((REG[052] bits[5:0]) × 8) + 6) = 910.
For PAL, (((REG[050] bits[6:0]) + 1) × 8) + (((REG[052] bits[5:0]) × 8) + 7) = 1135.

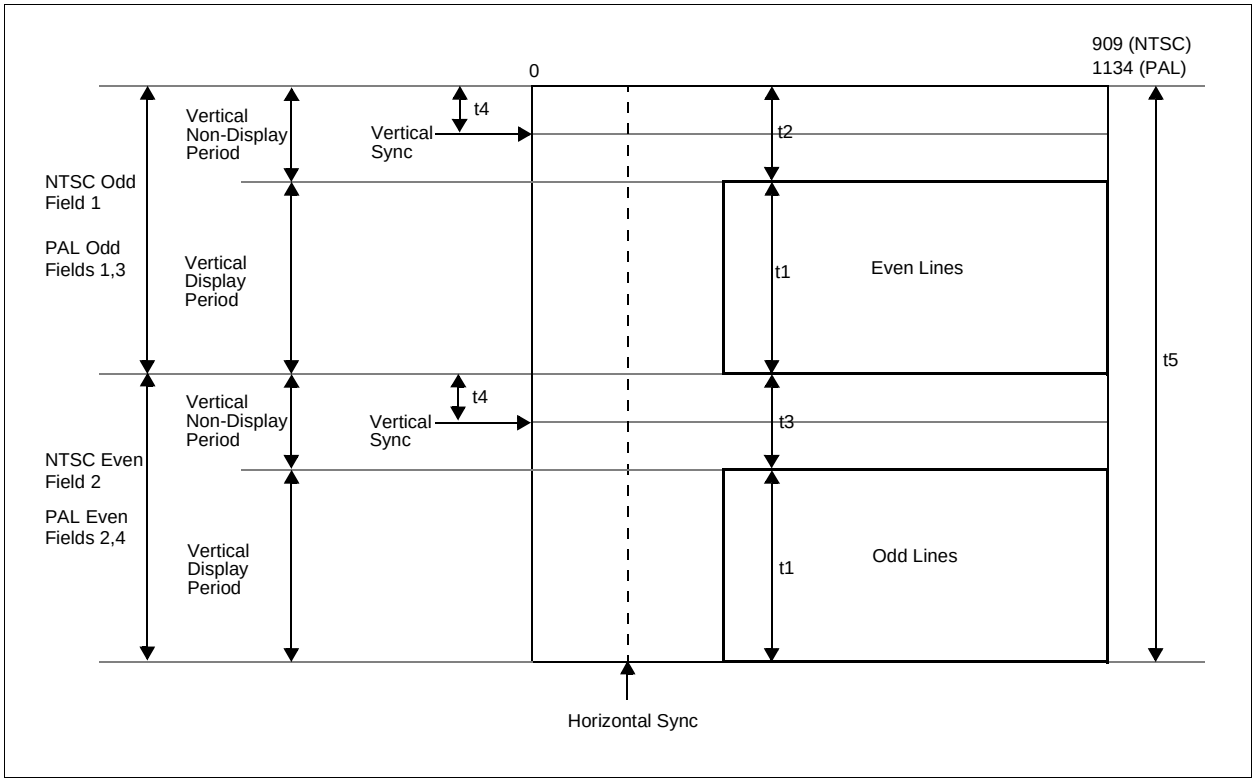



*Figure 6-39: Vertical Timing for NTSC/PAL*

*Table 6-30 : Vertical Timing for NTSC/PAL*

| Symbol | Parameter | NTSC | PAL | Units |
|---|---|---|---|---|
| $T_{LINE}$ | Line Period | 63.55556 | 63.99964 | us |
| t1 | Vertical Field Period | note 1 | note 1 | $T_{LINE}$ |
| t2 | Vertical Even Blanking | note 2 | note 2 | $T_{LINE}$ |
| t3 | Vertical Odd Blanking | note 3 | note 3 | $T_{LINE}$ |
| t4 | Vertical Sync Position | note 4 | note 5 | $T_{LINE}$ |
| t5 | Frame Period | 525 | 625 | $T_{LINE}$ |

1. t1 = ({(REG[057h] bits[1:0]), (REG[056] bits[7:0])} + 1) ÷ 2 (rounded up)
2. t2 = ((REG[058h] bits[6:0]) + 1) for NTSC field 1
   = ((REG[058h] bits [6:0]) + 2) for PAL fields 1 and 3
3. t3 = ((REG[058h] bits[6:0]) + 2) for NTSC field 2
   = ((REG[058h] bits [6:0]) + 1) for PAL fields 2 and 4
4. $t4_{NTSC}$ = ((REG[059h] bits[6:0]) + 4) for field 1
   = ((REG[059h] bits[6:0]) + 4.5) for field 2
5. $t4_{PAL}$ = ((REG[059h] bits[6:0]) + 5) for field 1 and field 3
   = ((REG[059h] bits[6:0]) + 4.5) for field 2 and field 4

**Important**

REG[056], REG[057], and REG[058] must be programmed to satisfy the Frame Period (t5).
For NTSC, ({(REG[057] bits[1:0]), (REG[056] bits[7:0])} + 1) + ((REG[058] bits[6:0]) + 1) × 2 + 1) = 525
For PAL, ({(REG[057] bits[1:0]), (REG[056] bits[7:0])} + 1) + ((REG[058] bits[6:0]) + 1) × 2 + 1) = 625.

## 6.7 MediaPlug Interface Timing

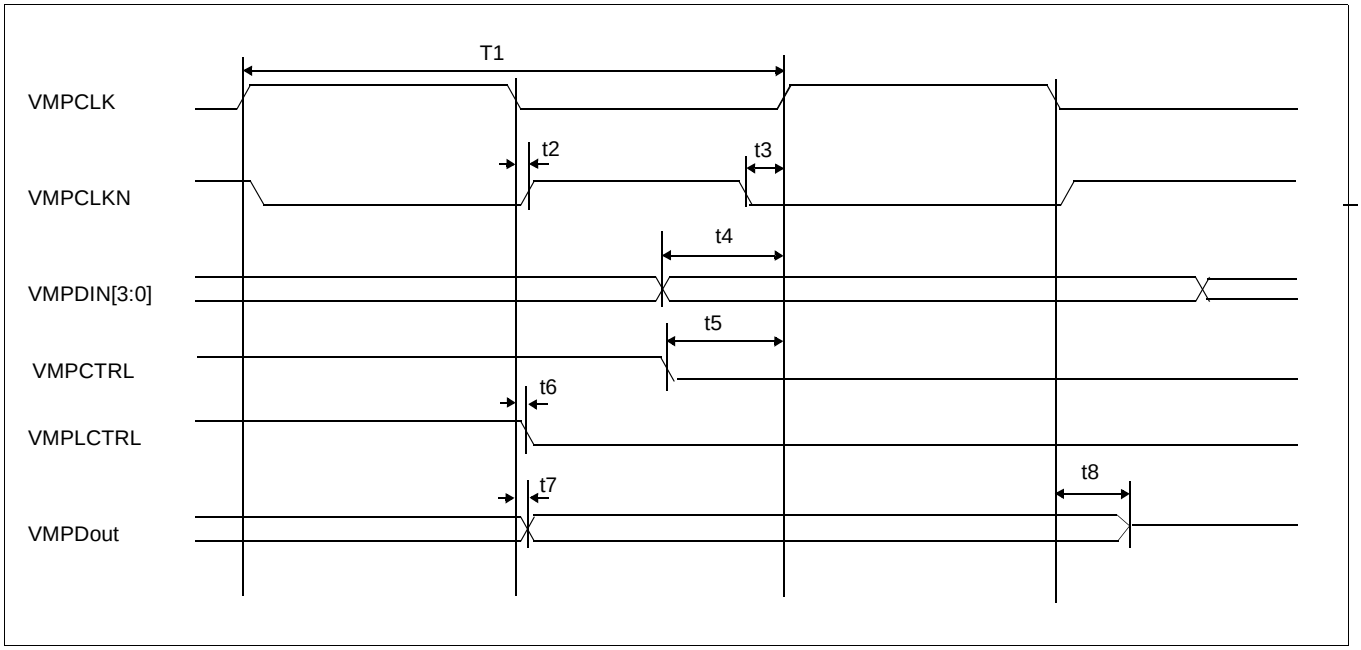



*Figure 6-40: MediaPlug A.C. Timing*

**Note**
The above timing diagram assumes no load.

*Table 6-31: MediaPlug A.C. Timing*

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| T1 | VMPCLK clock period | 50 | | ns |
| t2 | VMPCLK falling edge to VMPCLKN rising edge skew | 0.1 | 0.6 | ns |
| t3 | VMPCLKN falling edge to VMPCLK rising edge skew | .3 | 1.1 | ns |
| t4 | Input data setup | 17 | | ns |
| t5 | VMPCTRL setup | 16 | | ns |
| t6 | Local control signal delay from VMPCLK falling edge | 0 | 1.1 | ns |
| t7 | Output data delay from VMPCLK falling edge | 0 | 1.1 | ns |
| t8 | Output data tristate delay from VMPCLK falling edge | 0.4 | 1.4 | ns |

**Note**
VMPCLK, VMPCLKN are twice the period of the MediaPlug Clock. See Section 7, “Clocks” on page 92.

# 7 Clocks

## 7.1 Clock Overview

The following diagram provides a logical representation of the S1D13806 internal clocks.

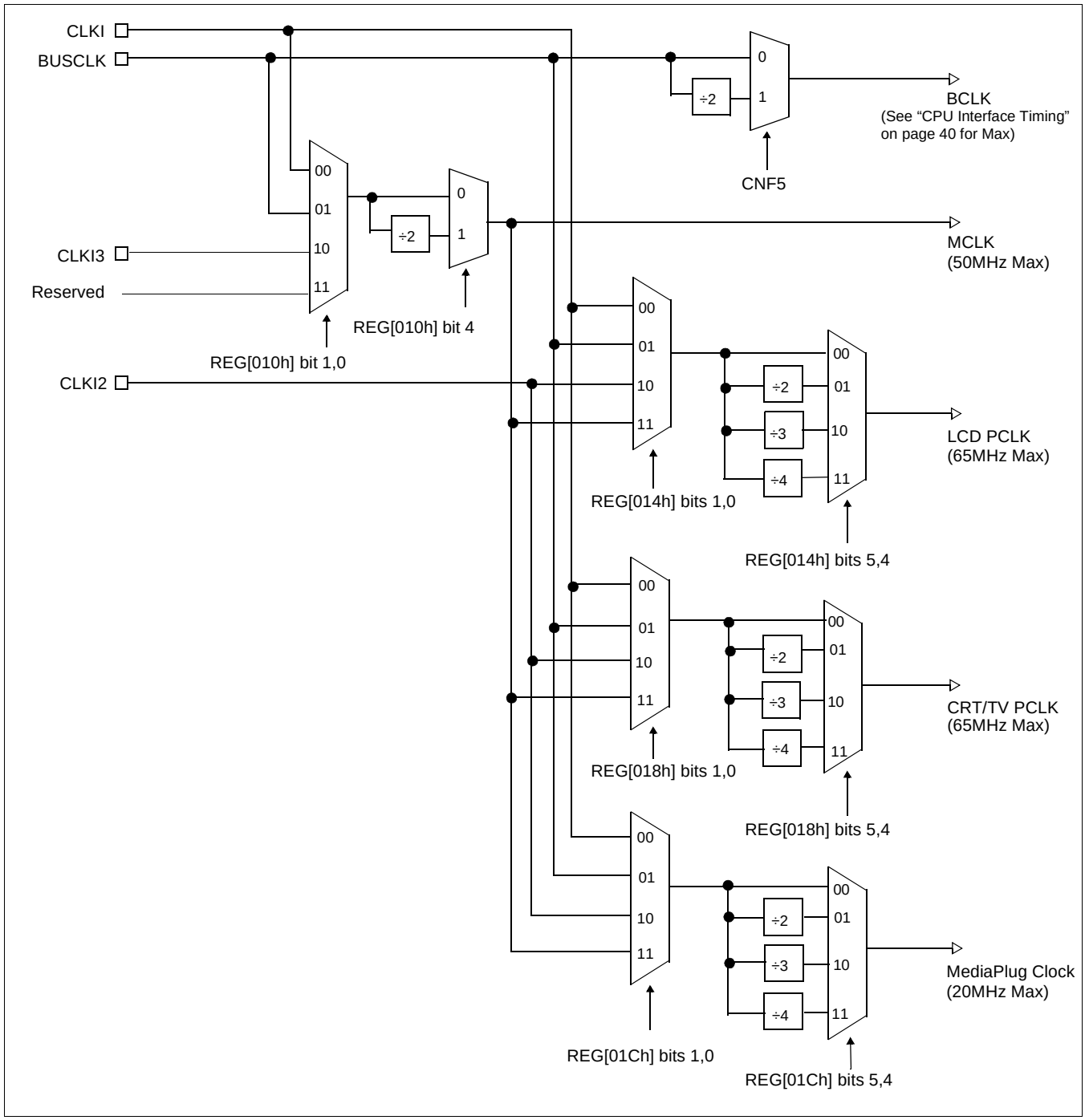



*Figure 7-1: Clock Overview Diagram*

## 7.2 Clock Descriptions

### 7.2.1 MCLK

MCLK should be configured as close to its maximum (50MHz) as possible. The S1D13806 contains sophisticated clock management, therefore, very little power is saved by reducing the MCLK frequency.

The frequency of MCLK is directly proportional to the bandwidth of the video memory. The bandwidth available to the CPU (for screen updates) is that left over after screen refresh takes its share. CPU bandwidth can be seriously reduced when the MCLK frequency is reduced, especially for high-resolution, high-color modes where screen refresh has high bandwidth requirements.

### 7.2.2 LCD PCLK

LCD PCLK should be chosen to match the optimum frame rate of the panel. See Section 18, “Clocking” on page 189 for details on the relationship between PCLK and frame rate, and for the maximum supportable PCLK frequencies for any given video mode.

Some flexibility is possible in the selection of PCLK. Firstly, panels typically have a range of permissible frame rates. Secondly, it may be possible to choose a higher PCLK frequency and tailor the horizontal non-display period (see REG[052h]) to bring down the frame-rate to its optimal value.

### 7.2.3 CRT/TV PCLK

TVs and older CRTs usually have very precise frequency requirements, so it may be necessary to dedicate one of the clock inputs to this function. More recent CRTs work within a range of frequencies, so it may be possible to support them with the BUSCLK or MCLK.

### 7.2.4 MediaPlug Clock

The MediaPlug Clock frequency is internally divided by 2 to provide the output signals VMPCLK and VMPCLKN for the MediaPlug interface. VMPCLK requires a clock in the range of 6-8MHz, therefore the MediaPlug Clock must be in the range of 12-16MHz. For AC timing see Section 6.7, “MediaPlug Interface Timing” on page 91.

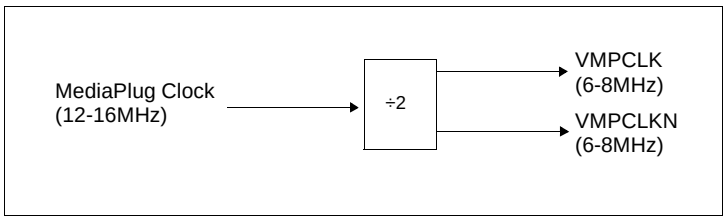



*Figure 7-2: MediaPlug Clock Output Signals*

## 7.3 Clock Selection

*Table 7-1 : Clock Selection*

| | Clock Source Options | Internal Clocks | | | |
|---|---|---|---|---|---|
| | | **MCLK** | **LCD PCLK** | **CRT/TV PCLK[1]** | **MediaPlug Clock** |
| **External Clocks** | **CLKI** | REG[010h] = 00h | REG[014h] = 00h | REG[018h] = 00h | REG[01Ch] = 00h |
| | **CLKI ÷ 2** | REG[010h] = 10h | REG[014h] = 10h | REG[018h] = 10h | REG[01Ch] = 10h |
| | **CLKI ÷ 3** | — | REG[014h] = 20h | REG[018h] = 20h | REG[01Ch] = 20h |
| | **CLKI ÷ 4** | — | REG[014h] = 30h | REG[018h] = 30h | REG[01Ch] = 30h |
| | **CLKI2** | — | REG[014h] = 02h | REG[018h] = 02h | REG[01Ch] = 02h |
| | **CLKI2 ÷ 2** | — | REG[014h] = 12h | REG[018h] = 12h | REG[01Ch] = 12h |
| | **CLKI2 ÷ 3** | — | REG[014h] = 22h | REG[018h] = 22h | REG[01Ch] = 22h |
| | **CLKI2 ÷ 4** | — | REG[014h] = 32h | REG[018h] = 32h | REG[01Ch] = 32h |
| | **CLKI3** | REG[010h] = 02h | — | — | — |
| | **CLKI3 ÷ 2** | REG[010h] = 12h | — | — | — |
| | **BUSCLK** | REG[010h] = 01h | REG[014h] = 01h | REG[018h] = 01h | REG[01Ch] = 01h |
| | **BUSCLK ÷ 2** | REG[010h] = 11h | REG[014h] = 11h | REG[018h] = 11h | REG[01Ch] = 11h |
| | **BUSCLK ÷ 3** | — | REG[014h] = 21h | REG[018h] = 21h | REG[01Ch] = 21h |
| | **BUSCLK ÷ 4** | — | REG[014h] = 31h | REG[018h] = 31h | REG[01Ch] = 31h |
| | **MCLK[2]** | — | REG[014h] = 03h | REG[018h] = 03h | REG[01Ch] = 03h |
| | **MCLK ÷ 2[2]** | — | REG[014h] = 13h | REG[018h] = 13h | REG[01Ch] = 13h |
| | **MCLK ÷ 3[2]** | — | REG[014h] = 23h | REG[018h] = 23h | REG[01Ch] = 23h |
| | **MCLK ÷ 4[2]** | — | REG[014h] = 33h | REG[018h] = 33h | REG[01Ch] = 33h |

**Note**

1. The CRT/TV pixel clock may be further multiplied by 2 when TV with Flicker Filter is enabled using REG[018h] bit 7.
2. MCLK may be a previously divided down version of CLKI, CLKI3, or BUSCLK.

## 7.4 Clocks vs. Functions

The S1D13806 has five clock signals. Not all clock signals must be active for certain functions to be carried out. The following table shows which clocks are required for each function.

*Table 7-2: Clocks vs. Functions*

| Function | Required Clocks[1] | | | | |
|---|---|---|---|---|---|
| | **BUSCLK** | **LCD PCLK** | **CRT/TV PCLK** | **MCLK** | **MediaPlug Clock** |
| Register read/write | Yes[2] | No | No | No | No |
| LCD LUT read/write | Yes | Yes | -- | -- | -- |
| CRT/TV LUT read/write | Yes | -- | Yes | -- | -- |
| Memory read/write | Yes | -- | -- | Yes[3] | -- |
| 2D Operation | Yes | -- | -- | Yes | -- |
| MediaPlug Registers read/write | Yes | -- | -- | -- | Yes |
| Power Save Mode | see Section 19, “Power Save Mode” on page 202 | | | | |

**Note**

[1] The S1D13806 contains sophisticated power management that dynamically shuts down clocks when not required.

[2] Before turning off the BUSCLK source externally, wait a minimum of 3 BUSCLK after a register read and a minimum of 4 BUSCLK after a register write.

[3] Before turning off the MCLK source externally, wait a minimum of 6 MCLK after a memory read and a minimum of 16 MCLK after a memory write.

# 8 Registers

This section discusses how and where to access the S1D13806 registers. It also provides detailed information about the layout and usage of each register.

## 8.1 Initializing the S1D13806

Before programming the S1D13806 registers, the following bits must be set.

- Register/Memory Select bit (REG[001h] bit 7)
- SDRAM Initialization bit (REG[020h] bit 7)

### 8.1.1 Register Memory Select Bit

At reset, the Register/Memory Select bit is set to 1. This means that only REG[000h] (read-only) and REG[001h] are accessible **until a write to REG[001h] sets bit 7 to 0 making all registers and memory accessible**. When debugging a new hardware design, this can sometimes give the appearance that the interface is not working, so it is important to remember to clear this bit before proceeding with debugging.

### 8.1.2 SDRAM Initialization Bit

To initialize the embedded SDRAM in the S1D13806, this bit must be set to 1 a minimum of 200µs after reset. **This bit must be set to 1 before memory access is performed.**

## 8.2 Register Mapping

The S1D13806 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0, the registers may be accessed. The register space is decoded by A[20:0].

When A20 = 1 the BitBLT data register ports are decoded allowing the system to access the display buffer through the 2D BitBLT engine using address lines A[19:0]. When A20 = 0 and A12 = 0 the registers are decoded using A[8:0] as an index. When A20 = 0 and A12 = 1 the MediaPlug register ports are decoded using A[11:0].

The MediaPlug register ports are defined only when the configuration input CONF7 = 1 on reset. When CONF7 = 0 on reset, A12 is always treated as 0 and the MediaPlug register space is not available - see Table 4-9, “Summary of Power-On/Reset Options,” on page 33.

Table 8-1, “Register Mapping with CS# = 0 and M/R# = 0” shows the decoding for each register type.

*Table 8-1 : Register Mapping with CS# = 0 and M/R# = 0*

| Register Types (Range) | Address A20-A0 Decoding |
|---|---|
| BitBLT data registers (1M byte) | 10 0000 to 1F FFFFh |
| MediaPlug registers (4K bytes) | 1000h to 1FFFh |
| On-chip registers (512 bytes) | 0 to 1FFh |

**Note**

The registers may be aliased within the allocated register space. If aliasing is undesirable, the register space must be fully decoded.

## 8.3 Register Set

The S1D13806 register set is as follows.

*Table 8-2 : S1D13806 Register Set*

| Register | Pg | Register | Pg |
|---|---|---|---|
| **Basic Registers** | | | |
| REG[000h] Revision Code Register | 101 | REG[001h] Miscellaneous Register | 101 |
| **General IO Pins Registers** | | | |
| REG[004h] General IO Pins Configuration Register 0 | 102 | REG[005h] General IO Pins Configuration Register 1 | 102 |
| REG[008h] General IO Pins Control Register 0 | 102 | REG[009h] General IO Pins Control Register 1 | 103 |
| **Configuration Readback Register** | | | |
| REG[00Ch] Configuration Status Register | 103 | | |
| **Clock Configuration Registers** | | | |
| REG[010h] Memory Clock Configuration Register | 103 | REG[014h] LCD Pixel Clock Configuration Register | 104 |
| REG[018h] CRT/TV Pixel Clock Configuration Register | 105 | REG[01Ch] MediaPlug Clock Configuration Register | 106 |
| REG[01Eh] CPU To memory Wait State Select Register | 107 | | |
| **Memory Configuration Registers** | | | |
| REG[020h] Memory Configuration Register | 108 | REG[021h] SDRAM Refresh Rate Register | 109 |
| REG[02Ah] SDRAM Timing Control Register 0 | 109 | REG[02Bh] SDRAM Timing Control Register 1 | 109 |
| **Panel Configuration Registers** | | | |
| REG[030h] Panel Type Register | 110 | REG[031h] MOD Rate Register | 111 |
| REG[032h] LCD Horizontal Display Width Register | 111 | REG[034h] LCD Horizontal Non-Display Period Register | 112 |
| REG[036h] TFT FPLINE Pulse Width Register | 113 | REG[038h] LCD Vertical Display Height Register 0 | 113 |
| REG[039h] LCD Vertical Display Height Register 1 | 113 | REG[03Ah] LCD Vertical Non-Display Period Register | 114 |
| REG[03Bh] TFT FPFRAME Start Position Register | 114 | REG[03Ch] TFT FPFRAME Pulse Width Register | 115 |
| **LCD Display Mode Registers** | | | |
| REG[040h] LCD Display Mode Register | 115 | REG[041h] LCD Miscellaneous Register | 117 |
| REG[042h] LCD Display Start Address Register 0 | 118 | REG[043h] LCD Display Start Address Register 1 | 118 |
| REG[044h] LCD Display Start Address Register 2 | 118 | REG[046h] LCD Memory Address Offset Register 0 | 118 |
| REG[047h] LCD Memory Address Offset Register 1 | 118 | REG[048h] LCD Pixel Panning Register | 119 |
| REG[04Ah] LCD Display FIFO High Threshold Control Register | 119 | REG[04Bh] LCD Display FIFO Low Threshold Control Register | 120 |
| **CRT/TV Configuration Registers** | | | |
| REG[050h] CRT/TV Horizontal Display Width Register | 120 | REG[052h] CRT/TV Horizontal Non-Display Period Register | 120 |
| REG[053h] CRT/TV HRTC Start Position Register | 121 | REG[054h] CRT/TV HRTC Pulse Width Register | 121 |
| REG[056h] CRT/TV Vertical Display Height Register 0 | 122 | REG[057h] CRT/TV Vertical Display Height Register 1 | 122 |
| REG[058h] CRT/TV Vertical Non-Display Period Register | 122 | REG[059h] CRT/TV VRTC Start Position Register | 123 |
| REG[05Ah] CRT VRTC Pulse Width Register | 123 | REG[05Bh] TV Output Control Register | 124 |
| **CRT/TV Display Mode Registers** | | | |
| REG[060h] CRT/TV Display Mode Register | 125 | REG[062h] CRT/TV Display Start Address Register 0 | 126 |
| REG[063h] CRT/TV Display Start Address Register 1 | 126 | REG[064h] CRT/TV Display Start Address Register 2 | 126 |
| REG[066h] CRT/TV Memory Address Offset Register 0 | 126 | REG[067h] CRT/TV Memory Address Offset Register 1 | 126 |
| REG[068h] CRT/TV Pixel Panning Register | 127 | REG[06Ah] CRT/TV FIFO High Threshold Control Register | 127 |
| REG[06Bh] CRT/TV FIFO Low Threshold Control Register | 128 | | |
| | | | |

*Table 8-2 : S1D13806 Register Set*

*Table 8-2 : S1D13806 Register Set*

| Register | Pg | Register | Pg |
|---|---|---|---|
| **MediaPlug Data Registers** | | | |
| REG[1008h] to REG[1FFEh] MediaPlug Data Registers | 155 | | |
| **BitBLT Data Registers** | | | |
| REG[100000h] to REG[1FFFFEh] BitBLT Data Registers | 155 | | |

# 8.4 Register Descriptions

## 8.4.1 Basic Registers

| **Revision Code Register** REG[000h] | | | | | | | RO |
|---|---|---|---|---|---|---|---|
| Product Code Bit 5 | Product Code Bit 4 | Product Code Bit 3 | Product Code Bit 2 | Product Code Bit 1 | Product Code Bit 0 | Revision Code Bit 1 | Revision Code Bit 0 |

bits 7-2 Product Code Bits [5:0]
This read-only register indicates the product code of the controller. The product code for S1D13806 is 000111b.

bits 1-0 Revision Code Bits [1:0]
This read-only register indicates the revision code of the controller. The revision code is 00b.

| **Miscellaneous Register** REG[001h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| Register/ Memory Select | n/a | n/a | n/a | n/a | Reserved | Reserved | Reserved |

bit 7 Register/Memory Select Bit
At reset, the Register/Memory Select bit is set to 1. This means that only REG[000h] (read-only) and REG[001h] are accessible **until a write to REG[001h] sets bit 7 to 0 making all registers and memory accessible**. When debugging a new hardware design, this can sometimes give the appearance that the interface is not working, so it is important to remember to clear this bit before proceeding with debugging.

bit 2 Reserved.
This bit must be set to 0.

bit 1 Reserved.
This bit must be set to 0.

bit 0 Reserved.
This bit must be set to 0.

### 8.4.2 General IO Pins Registers

| **General IO Pins Configuration Register 0**<br>REG[004h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| GPIO7 Pin IO Config. | GPIO6 Pin IO Config. | GPIO5 Pin IO Config. | GPIO4 Pin IO Config. | GPIO3 Pin IO Config. | GPIO2 Pin IO Config. | GPIO1 Pin IO Config. | GPIO0 Pin IO Config. |

bit 7-0 GPIO[7:0] Pin IO Configuration Bits
When bit *n* = 1, GPIO[*n*] is configured as an output pin. (where *n* ranges from 0 to 7)
When bit *n* = 0 (default), GPIO[*n*] is configured as an input pin. (where *n* ranges from 0 to 7).

| **General IO Pins Configuration Register 1**<br>REG[005h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | GPIO12 Pin IO Config. | GPIO11 Pin IO Config. | GPIO10 Pin IO Config. | GPIO9 Pin IO Config. | GPIO8 Pin IO Config. |

bit 4-0 GPIO[12:8] Pin IO Configuration Bits
When bit *n* = 1, GPIO[*n+8*] is configured as an output pin. (where *n* ranges from 0 to 4)
When bit *n* = 0 (default), GPIO[*n+8*] is configured as an input pin. (where *n* ranges from 0 to 4)

**Note**
Note that CONF7 must be properly configured at the rising edge of RESET# to enable GPIO12 as an IO pin, otherwise GPIO12 is used for the Media Plug interface and this register has no effect. The following table shows GPIO12 usage.

*Table 8-3 : Media Plug/GPIO12 Pin Functionality*

| **Pin** | **CONF7 on Reset** | |
|---|---|---|
| | **0** | **1** |
| GPIO12 | GPIO12 | VMPEPWR |

| **General IO Pins Control Register 0**<br>REG[008h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| GPIO7 Pin IO Status | GPIO6 Pin IO Status | GPIO5 Pin IO Status | GPIO4Pin IO Status | GPIO3 Pin IO Status | GPIO2 Pin IO Status | GPIO1 Pin IO Status | GPIO0 Pin IO Status |

bit 7-0 GPIO[7:0] Pin IO Status Bits
When GPIO[*n*] is configured as an output, writing a 1 to bit *n* drives GPIO[*n*] high and writing a 0 to this bit drives GPIO[*n*] low. (*n* ranges from 0 to 7)
When GPIO[*n*] is configured as an input, a read from bit *n* returns the status of GPIO[*n*]. (*n* ranges from 0 to 7)

| **General IO Pins Control Register 1**<br>REG[009h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | GPIO12 Pin IO Status | GPIO11 Pin IO Status | GPIO10 Pin IO Status | GPIO9 Pin IO Status | GPIO8 Pin IO Status |

bit 4-0 GPIO[12:8] Pin IO Status Bits
When GPIO[*n+8*] is configured as an output, writing a 1 to bit *n* drives GPIO[*n+8*] high and writing a 0 to this bit drives GPIO[*n+8*] low. (*n* ranges from 0 to 4)
When GPIO[*n+8*] is configured as an input, a read from bit *n+8* returns the status of GPIO[*n+8*]. (*n* ranges from 0 to 4)

**Note**
CONF7 must be properly configured at the rising edge of RESET# to enable GPIO12 as an IO pin, otherwise GPIO12 is used for the Media Plug interface and this register has no effect on GPIO12. See Table 8-3, “Media Plug/GPIO12 Pin Functionality” for GPIO12 usage.

### 8.4.3 Configuration Readback Register

| **Configuration Status Register**<br>REG[00Ch] | | | | | | | RO |
|---|---|---|---|---|---|---|---|
| CONF[7] Config. Status | CONF[6] Config. Status | CONF[5] Config. Status | CONF[4] Config. Status | CONF[3] Config. Status | CONF[2] Config. Status | CONF[1] Config. Status | CONF[0] Config. Status |

bits 7-0 CONF[7:0] Configuration Status Bits
These read-only bits return the status of CONF[7:0] at the rising edge of RESET#.

### 8.4.4 Clock Configuration Registers

| **Memory Clock Configuration Register**<br>REG[010h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | MCLK Divide Select | n/a | n/a | MCLK Source Select Bit 1 | MCLK Source Select Bit 0 |

**Note**
For further information on MCLK, see Section 7.2, “Clock Descriptions” on page 93.

bit 4 MCLK Divide Select
When this bit = 1, the internal memory clock (MCLK) frequency is half of the MCLK source frequency.
When this bit = 0, the memory clock frequency is equal to the MCLK source frequency.

**Note**
The MCLK frequency should always be set to the maximum frequency allowed by the SDRAM. This provides maximum performance and minimizes overall system power consumption.

bit 1-0 MCLK Source Select Bits [1:0]
These bits determine the source of the internal memory clock (MCLK).

*Table 8-4 : MCLK Source Select*

| MCLK Source Select Bits | MCLK Source |
|---|---|
| 00 | CLKI |
| 01 | BUSCLK |
| 10 | CLKI3 |
| 11 | Reserved |

**Note**
The MCLK Divide Select bit must be set to 1 before changing the MCLK Source Select bits.

**LCD Pixel Clock Configuration Register**
REG[014h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | LCD PCLK Divide Select Bit 1 | LCD PCLK Divide Select Bit 0 | n/a | n/a | LCD PCLK Source Select Bit 1 | LCD PCLK Source Select Bit 0 |

**Note**
For further information on the LCD PCLK, refer to Section 7.2, “Clock Descriptions” on page 93.

bits 5-4 LCD PCLK Divide Select Bits [1:0]
These bits determine the divide used to generate the LCD pixel clock from the LCD pixel clock source.

*Table 8-5 : LCD PCLK Divide Selection*

| LCD PCLK Divide Select Bits | LCD PCLK Source to LPCLK Frequency Ratio |
|---|---|
| 00 | 1:1 |
| 01 | 2:1 |
| 10 | 3:1 |
| 11 | 4:1 |

bits 1-0 LCD PCLK Source Select Bits [1:0]
These bits determine the source of the pixel clock for the LCD display.

*Table 8-6 : LCD PCLK Source Selection*

| LCD PCLK Source Select Bits | LCD PCLK Source |
|---|---|
| 00 | CLKI |
| 01 | BUSCLK |
| 10 | CLKI2 |
| 11 | MCLK |

**Note**
MCLK may be a previously divided down version of CLKI, CLKI3, or BUSCLK.

**CRT/TV Pixel Clock Configuration Register**
REG[018h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Flicker Filter Clock Enable | n/a | CRT/TV PCLK Divide Select Bit 1 | CRT/TV PCLK Divide Select Bit 0 | n/a | n/a | CRT/TV PCLK Source Select Bit 1 | CRT/TV PCLK Source Select Bit 0 |

**Note**
For further information on the CRT/TV PCLK, refer to Section 7.2, “Clock Descriptions” on page 93.

bit 7 Flicker Filter Clock Enable
This bit must be set to 1 when TV with flicker filter is enabled. For details on TV with flicker filter, see REG[1FCh] bits 2-0.

bits 5-4 CRT/TV PCLK Divide Select Bits[1:0]
These bits determine the divide used to generate the CRT/TV pixel clock from the CRT/TV pixel clock source.

*Table 8-7 : CRT/TV PCLK Divide Selection*

| CRT/TV PCLK Divide Select Bits | CRT/TV PCLK Source to DPCLK Frequency Ratio |
|---|---|
| 00 | 1:1 |
| 01 | 2:1 |
| 10 | 3:1 |
| 11 | 4:1 |

bits 1-0 CRT/TV PCLK Source Select Bits [1:0]
These bits determine the source of the pixel clock for the CRT/TV display.

*Table 8-8 : CRT/TV PCLK Source Selection*

| CRT/TV PCLK Source Select Bits | CRT/TV PCLK Source |
|---|---|
| 00 | CLKI |
| 01 | BUSCLK |
| 10 | CLKI2 |
| 11 | MCLK |

**Note**
MCLK may be a previously divided down version of CLKI, CLKI3, or BUSCLK.

**MediaPlug Clock Configuration Register**
REG[01Ch] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | MediaPlug Clock Divide Select Bit 1 | MediaPlug Clock Divide Select Bit 0 | n/a | n/a | MediaPlug Clock Source Select Bit 1 | MediaPlug Clock Source Select Bit 0 |

**Note**
For further information on the MediaPlug Clock, refer to Section 7.2, “Clock Descriptions” on page 93.

bits 5-4 MediaPlug Clock Divide Select Bits [1:0]
These bits determine the divide used to generate the MediaPlug Clock from the MediaPlug Clock source.

*Table 8-9 : MediaPlug Clock Divide Selection*

| MediaPlug Clock Divide Select Bits | MediaPlug Clock Source to MediaPlug Clock Frequency Ratio |
|---|---|
| 00 | 1:1 |
| 01 | 2:1 |
| 10 | 3:1 |
| 11 | 4:1 |

bits 1-0 MediaPlug Clock Source Select Bits [1:0]
These bits determine the source of the MediaPlug Clock for the MediaPlug Interface. See Section 6.7, “MediaPlug Interface Timing” on page 91 for AC Timing.

*Table 8-10 : MediaPlug Clock Source Selection*

| MediaPlug Clock Source Select Bits | MediaPlug Clock Source |
|---|---|
| 00 | CLKI |
| 01 | BUSCLK |
| 10 | CLKI2 |
| 11 | MCLK |

**Note**
MCLK may be a previously divided down version of CLKI, CLKI3, or BUSCLK.

**CPU To Memory Wait State Select Register**
REG[01Eh] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | CPU to Memory Wait State Select Bit 1 | CPU to Memory Wait State Select Bit 0 |

bits 1-0 CPU to Memory Wait State Select Bits [1:0]
These bits are used to optimize the handshaking between the host interface and the memory controller. The bits should be set according to the relationship between BCLK and MCLK (memory clock)

**Note**
BCLK can be either BUSCLK or BUSCLK ÷ 2 depending on the setting of CONF5 (see Table 4-9, “Summary of Power-On/Reset Options,” on page 33).

Failure to meet the following conditions may lead to system crash which is recoverable only by RESET.

*Table 8-11 : Minimum Memory Timing Selection*

| Wait State Bits [1:0] | Condition |
|---|---|
| 00 | no restrictions |
| 01 | 2 × period (MCLK) - 4ns > period(BCLK) |
| 10 | period(MCLK) - 4ns > period(BCLK) |
| 11 | Reserved |

### 8.4.5 Memory Configuration Registers

| **Memory Configuration Register**<br>REG[020h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| SDRAM Init | n/a | n/a | n/a | n/a | n/a | n/a | n/a |

bit 7 SDRAM Initialization

**This bit must be set to 1 before memory accesses are performed.** Setting this bit to 1 after reset initializes the embedded SDRAM. Subsequent toggling of this bit after the first initialization has no effect.

When the SDRAM Initialization bit is set, the actual initialization sequence occurs at the first SDRAM refresh cycle. The initialization sequence requires approximately 16 MCLKs to complete and memory accesses cannot be made while the initialization is in progress. Any concurrently issued memory access will occur after the completion of the initialization sequence. At least one SDRAM refresh period must happen before issuing any memory accesses.

**Note**

The default SDRAM refresh rate is based on the MCLK source frequency and is set using REG[21h] bits 2-0. If the refresh rate or MCLK rate is changed, the wait time will be different.

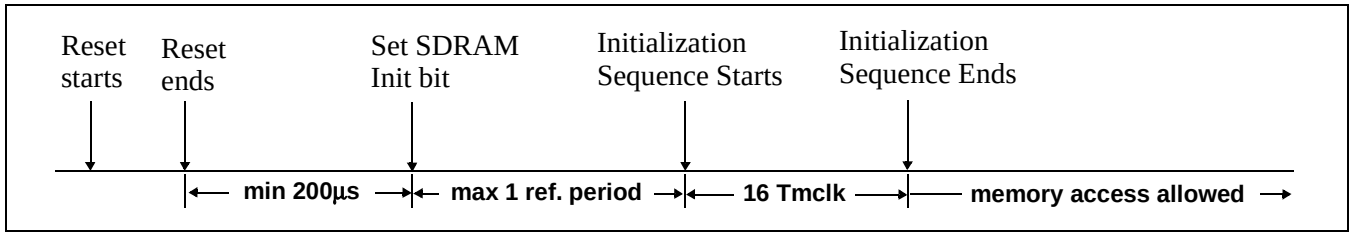



*Figure 8-1: SDRAM Initialization Sequence*

| **SDRAM Refresh Rate Register** REG[021h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | Reserved | n/a | n/a | n/a | Reserved | SDRAM Refresh Rate Bit 1 | SDRAM Refresh Rate Bit 0 |

bit 6 Reserved.
This bit must be set to 0.

bit 2 Reserved.
This bit must be set to 0.

bits 1-0 SDRAM Refresh Rate Select Bits [2:0]
These bits are set according to the MCLK source frequency (i.e., BUSCLK, CLKI, or CLKI3 as determined by REG[010h] bits 1-0).

*Table 8-12 : SDRAM Refresh Rate Selection*

| SDRAM Refresh Rate Bits [1:0] | MCLK Source Frequency (MHz) |
|---|---|
| 00 | 4.096 <= MClk < 8.192 |
| 01 | 8.192 <= MClk < 16.384 |
| 10 | 16.384 <= MClk < 32.768 |
| 11 | 32.768 <= MClk <= 50.000 |

| **SDRAM Timing Control Register 0** REG[02Ah] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| SDRAM Timing Control Bit 7 | SDRAM Timing Control Bit 6 | SDRAM Timing Control Bit 5 | SDRAM Timing Control Bit 4 | SDRAM Timing Control Bit 3 | SDRAM Timing Control Bit 2 | SDRAM Timing Control Bit 1 | SDRAM Timing Control Bit 0 |

| **SDRAM Timing Control Register 1** REG[02Bh] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | SDRAM Timing Control Bit 12 | SDRAM Timing Control Bit 11 | SDRAM Timing Control Bit 10 | SDRAM Timing Control Bit 9 | SDRAM Timing Control Bit 8 |

REG[02Ah] bits 7-0 SDRAM Timing Control Bits [12:0]
REG[02Bh] bits 4-0 The SDRAM Timing Control registers must be set according to the frequency of MCLK as follows.

*Table 8-13 : SDRAM Timings Control Register Settings*

| MCLK Source Frequency (MHz) | REG[02Ah] | REG[02Bh] |
|---|---|---|
| 42 ≤ MCLK ≤ 50 | 00h | 01h |
| 33 ≤ MCLK < 42 | 00h | 12h |
| MCLK < 33 | 11h | 13h |

### 8.4.6 Panel Configuration Registers

| **Panel Type Register** REG[030h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| EL Panel Mode Enable | TFT 2x Data Format Select | Panel Data Width Bit 1 | Panel Data Width Bit 0 | Panel Data Format Select | Color/Mono. Panel Select | Dual/Single Panel Select | TFT/ Passive LCD Panel Select |

bit 7 EL Panel Mode Enable
When this bit = 1, EL Panel support circuit is enabled.
When this bit = 0, there is no hardware effect.
This bit enables the S1D13806 built-in circuit for EL panels which require the Frame Rate Modulation (FRM) to remain static for one frame every 262143 frames (approximately 1 hour at 60Hz refresh). When this bit is enabled, the need for external circuitry to perform the above function is eliminated.

bit 6 TFT 2x Data Format Select
**For TFT/D-TFD only.**
When this bit = 1, the TFT 2x Data format is selected.
When this bit = 0, the standard TFT Data format is selected.

For details on the TFT 2x Data format, see Section 6.5.10, “TFT/D-TFD Panel Timing” on page 82.

bits 5-4 Panel Data Width Bits [1:0]
These bits select passive LCD/TFT/D-TFD panel data width size.

*Table 8-14 : Panel Data Width Selection*

| **Panel Data Width Bits [1:0]** | **Passive LCD Panel Data Width** | **TFT/D-TFD Panel Data Width** | |
|---|---|---|---|
| | | **1x Data Format** | **2x Data Format** |
| 00 | 4-bit | 9-bit | 2 x 9-bit |
| 01 | 8-bit | 12-bit | 2 x 12-bit |
| 10 | 16-bit | 18-bit | Reserved |
| 11 | Reserved | Reserved | Reserved |

bit 3 Panel Data Format Select
When this bit = 1, 8-bit single color passive LCD panel data format 2 is selected. For AC timing see Section 6.5.5, “Single Color 8-Bit Panel Timing (Format 2)” on page 72.
When this bit = 0, 8-bit single color passive LCD panel data format 1 is selected. For AC timing see Section 6.5.4, “Single Color 8-Bit Panel Timing (Format 1)” on page 70.

bit 2 Color/Mono Panel Select
When this bit = 1, color passive LCD panel is selected.
When this bit = 0, monochrome passive LCD panel is selected.

bit 1 Dual/Single Panel Select
When this bit = 1, dual passive LCD panel is selected.
When this bit = 0, single passive LCD panel is selected.

bit 0 TFT/Passive LCD Panel Select
When this bit = 1, TFT/D-TFD panel is selected.
When this bit = 0, passive LCD panel is selected.

**MOD Rate Register**
REG[031h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | MOD Rate Bit 5 | MOD Rate Bit 4 | MOD Rate Bit 3 | MOD Rate Bit 2 | MOD Rate Bit 1 | MOD Rate Bit 0 |

bits 5-0 MOD Rate Bits [5:0]
For a non-zero value these bits specify the number of FPLINE between toggles of the MOD output signal (DRDY).
When these bits are all 0's the MOD output signal toggles every FPFRAME. These bits are for passive LCD panels only.

**LCD Horizontal Display Width Register**
REG[032h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | LCD Horizontal Display Width Bit 6 | LCD Horizontal Display Width Bit 5 | LCD Horizontal Display Width Bit 4 | LCD Horizontal Display Width Bit 3 | LCD Horizontal Display Width Bit 2 | LCD Horizontal Display Width Bit 1 | LCD Horizontal Display Width Bit 0 |

bits 6-0 LCD Horizontal Display Width Bits [6:0]
These bits specify the LCD panel horizontal display width, in 8 pixel resolution.

Horizontal display width in number of pixels = ((ContentsOfThisRegister)+ 1) × 8

The Horizontal Display Width has certain limitations on the values that may be used for each type of LCD panel. Use of values that do not meet the limitations listed in the following table result in undefined behavior.

*Table 8-15: Horizontal Display Width (Pixels)*

| Panel Type | Horizontal Display Width (Pixels) |
|---|---|
| Passive Single | must be divisible by 16 |
| Passive Dual | must be divisible by 32 |
| TFT | must be divisible by 8 |

**Note**
This register must be programmed such that REG[032h] ≥ 3 (32 pixels).

**LCD Horizontal Non-Display Period Register**
REG[034h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | LCD Horizontal Non-Display Period Bit 4 | LCD Horizontal Non-Display Period Bit 3 | LCD Horizontal Non-Display Period Bit 2 | LCD Horizontal Non-Display Period Bit 1 | LCD Horizontal Non-Display Period Bit 0 |

bits 4-0 LCD Horizontal Non-Display Period Bits [4:0]
These bits specify the LCD panel HNDP width in 8 pixel resolution.

HNDP width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

**Note**
This register must be programmed such that REG[034h] ≥ 3 (32 pixels).

**Note**
For TFT/D-TFD only:
REG[034h] + 1 ≥ (REG[035h] + 1) + (REG[036h] bits 3-0 + 1)

**TFT FPLINE Start Position Register**
REG[035h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | TFT FPLINE Start Position Bit 4 | TFT FPLINE Start Position Bit 3 | TFT FPLINE Start Position Bit 2 | TFT FPLINE Start Position Bit 1 | TFT FPLINE Start Position Bit 0 |

bits 4-0 TFT FPLINE Start Position Bits [4:0]
**For TFT/D-TFD panels only**, these bits specify the delay, in 8 pixel resolution, from the start of the horizontal non-display period to the leading edge of the FPLINE pulse.

For TFT 1x Data Format at 4/8 bpp color depth:
FPLINE start position in number of pixels = [(ContentsOfThisRegister) x 8 + 5]

For TFT 1x Data Format at 16 bpp color depth:
FPLINE start position in number of pixels = [(ContentsOfThisRegister) x 8 + 6]

For TFT 2x Data Format at 4/8 bpp color depth:
FPLINE start position in number of pixels = [(ContentsOfThisRegister) x 8 + 4]

For TFT 2x Data Format at 16 bpp color depth:
FPLINE start position in number of pixels = [(ContentsOfThisRegister) x 8 + 5]

**Note**
REG[034h] + 1 ≥ (REG[035h] + 1) + (REG[036h] bits 3-0 + 1)

| **TFT FPLINE Pulse Width Register** REG[036h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD FPLINE Polarity Select | n/a | n/a | n/a | TFT FPLINE Pulse Width Bit 3 | TFT FPLINE Pulse Width Bit 2 | TFT FPLINE Pulse Width Bit 1 | TFT FPLINE Pulse Width Bit 0 |

bit 7 LCD FPLINE Polarity Select

This bit selects the polarity of FPLINE for all LCD panels.

When this bit = 1, the FPLINE pulse is active high for TFT/D-TFD and active low for passive LCD.

When this bit = 0, the FPLINE pulse is active low for TFT/D-TFD and active high for passive LCD.

*Table 8-16 : LCD FPLINE Polarity Selection*

| LCD FPLINE Polarity Select | Passive LCD FPLINE Polarity | TFT FPLINE Polarity |
|---|---|---|
| 0 | active high | active low |
| 1 | active low | active high |

bits 3-0 TFT FPLINE Pulse Width Bits [3:0]

**For TFT/D-TFD panels only**, these bits specify the pulse width of the FPLINE output signal in 8 pixel resolution.

FPLINE pulse width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

The maximum FPLINE pulse width is 128 pixels.

**Note**

REG[034h] + 1 ≥ (REG[035h] + 1) + (REG[036h] bits 3-0 + 1)

| **LCD Vertical Display Height Register 0** REG[038h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD Vertical Display Height Bit 7 | LCD Vertical Display Height Bit 6 | LCD Vertical Display Height Bit 5 | LCD Vertical Display Height Bit 4 | LCD Vertical Display Height Bit 3 | LCD Vertical Display Height Bit 2 | LCD Vertical Display Height Bit 1 | LCD Vertical Display Height Bit 0 |

| **LCD Vertical Display Height Register 1** REG[039h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | LCD Vertical Display Height Bit 9 | LCD Vertical Display Height Bit 8 |

REG[038h] bits 7-0 LCD Vertical Display Height Bits [9:0]
REG[039h] bits 1-0 These bits specify the LCD panel vertical display height, in 1 line resolution.

Vertical display height in number of lines = (ContentsOfThisRegister) + 1

**LCD Vertical Non-Display Period Register**
REG[03Ah] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LCD Vertical Non-Display Period Status (RO) | n/a | LCD Vertical Non-Display Period Bit 5 | LCD Vertical Non-Display Period Bit 4 | LCD Vertical Non-Display Period Bit 3 | LCD Vertical Non-Display Period Bit 2 | LCD Vertical Non-Display Period Bit 1 | LCD Vertical Non-Display Period Bit 0 |

bit 7 LCD Vertical Non-Display Period Status
This is a read-only status bit.
When a read from this bit = 1, a LCD panel vertical non-display period is occurring.
When a read from this bit = 0, the LCD panel output is in a vertical display period.

bits 5-0 LCD Vertical Non-Display Period Bits [5:0]
These bits specify the LCD panel vertical non-display period height in 1 line resolution.

Vertical non-display period height in number of lines = (ContentsOfThisRegister) + 1

**Note**
For TFT/D-TFD only:
(REG[03Ah] bits 5-0 + 1) ≥ (REG[03Bh] + 1) + (REG[03Ch] bits 2-0 + 1)

**TFT FPFRAME Start Position Register**
REG[03Bh] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | TFT FPFRAME Start Position Bit 5 | TFT FPFRAME Start Position Bit 4 | TFT FPFRAME Start Position Bit 3 | TFT FPFRAME Start Position Bit 2 | TFT FPFRAME Start Position Bit 1 | TFT FPFRAME Start Position Bit 0 |

bits 5-0 TFT FPFRAME Start Position Bits [5:0]
**For TFT/D-TFD panels only**, these bits specify the delay in lines from the start of the vertical non-display period to the leading edge of the FPFRAME pulse.

FPFRAME start position in number of lines = (ContentsOfThisRegister) + 1

**Note**
(REG[03Ah] bits 5-0 + 1) ≥ (REG[03Bh] + 1) + (REG[03Ch] bits 2-0 + 1)

| **TFT FPFRAME Pulse Width Register** REG[03Ch] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD FPFRAME Polarity Select | n/a | n/a | n/a | n/a | TFT FPFRAME Pulse Width Bit 2 | TFT FPFRAME Pulse Width Bit 1 | TFT FPFRAME Pulse Width Bit 0 |

bit 7 LCD FPFRAME Polarity Select
This bit selects the polarity of FPFRAME for all LCD panels.
When this bit = 1, the FPFRAME pulse is active high for TFT/D-TFD and active low for passive LCD.
When this bit = 0, the FPFRAME pulse is active low for TFT/D-TFD and active high for passive LCD.

*Table 8-17 : LCD FPFRAME Polarity Selection*

| LCD FPFRAME Polarity Select | Passive LCD FPFRAME Polarity | TFT FPFRAME Polarity |
|---|---|---|
| 0 | active high | active low |
| 1 | active low | active high |

bits 2-0 TFT FPFRAME Pulse Width Bits [2:0]
**For TFT/D-TFD panels only**, these bits specify the pulse width of the FPFRAME output signal in number of lines.

FPFRAME pulse width in number of lines = (ContentsOfThisRegister) + 1

**Note**
(REG[03Ah] bits 5-0 + 1) ≥ (REG[03Bh] + 1) + (REG[03Ch] bits 2-0 + 1)

## 8.4.7 LCD Display Mode Registers

| **LCD Display Mode Register** REG[040h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD Display Blank | n/a | n/a | SwivelView Enable Bit 1 | n/a | LCD Bit-per-pixel Select Bit 2 | LCD Bit-per-pixel Select Bit 1 | LCD Bit-per-pixel Select Bit 0 |

bit 7 LCD Display Blank
When this bit = 1, the LCD display pipeline is disabled and all LCD data outputs are forced to zero (i.e. the screen is blanked).
When this bit = 0, the LCD display pipeline is enabled.

**Note**
If a dual panel is used, the Dual Panel Buffer (REG[041h] bit 0) must be disabled (set to 1) before blanking the LCD display.

bit 4 SwivelView Enable Bit 1

When this bit = 1, the LCD display image is rotated 180° clockwise. Please refer to Section 15, “SwivelView™” on page 177 for application and limitations.

When this bit = 0, there is no hardware effect.

This bit in conjunction with SwivelView™ Enable Bit 0 achieves the following hardware rotations.

*Table 8-18: Setting SwivelView Modes*

| SwivelView Enable Bits | SwivelView™ Modes | | | |
|---|---|---|---|---|
| | Normal | SwivelView 90° | SwivelView 180° | SwivelView 270° |
| SwivelView Enable Bit 0 (REG[1FCh] bit 6) | 0 | 1 | 0 | 1 |
| SwivelView Enable Bit 1 (REG[040h] bit 4) | 0 | 0 | 1 | 1 |

bits 2-0 LCD Bit-per-pixel Select Bits [2:0]

These bits select the color depth (bit-per-pixel) for the displayed data.

**Note**

16 bpp color depth bypasses the LUT and supports up to 64K colors (4096 colors if dithering disabled, see REG[041h] bit 1). TFT/D-TFD panels support up to 64K colors.

*Table 8-19 : LCD Bit-per-pixel Selection*

| Bit-per-pixel Select Bits [1:0] | Color Depth (bpp) |
|---|---|
| 000-001 | Reserved |
| 010 | 4 bpp |
| 011 | 8 bpp |
| 100 | Reserved |
| 101 | 16 bpp |
| 110-111 | Reserved |

**LCD Miscellaneous Register**
REG[041h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | Dithering Disable | Dual Panel Buffer Disable |

bit 1 Dithering Disable

When this bit = 0, dithering on the passive LCD panel for 16 bpp mode is enabled allowing a maximum of 64K colors ($2^{16}$) or 64 gray shades.
When this bit = 1, dithering on the passive LCD panel for 16 bpp mode is disabled, allowing a maximum of 4096 colors ($2^{12}$) or 16 gray shades.
The dithering algorithm provides more shades of each primary color when in 16 bpp mode. This bit has no effect in 4/8 bpp modes where dithering is not supported.

All passive STN color panels are controlled using 3 bits for each pixel (RGB) for a total of 8 possible colors. LCD controllers use a combination of Frame Rate Modulation (FRM) and dithering to achieve more than 8 colors per pixel. FRM can achieve 16 shades of color for each RGB component resulting in a total of 4096 possible colors (16x16x16). Dithering uses a 4 pixel square formation and applies a set of 4 hard-coded patterns for each of the 16 shades of color. This expands the original 16 shades of color from the FRM logic to 64 shades per RGB component which results in 256K colors per pixel (64x64x64).

For the S1D13806, 16 bpp is arranged as 5-6-5 RGB. In this mode, when dithering is enabled, the LUT is bypassed and the original 16-bit data is used as a pointer into the 64 shades per color in the following manner.

(5-6-5 RGB) 32 possible Red, 64 possible Green, 32 possible Blue

This combination of FRM and dithering results in 256K colors/pixel, however, the 16 bpp limitation of the S1D13806 limits this to 64K colors/pixel.

bit 0 Dual Panel Buffer Disable

This bit is used to disable the dual panel buffer.
When this bit = 1, the dual panel buffer is disabled.
When this bit = 0, the dual panel buffer is enabled.
When a single panel is selected, the dual panel buffer is automatically disabled and this bit has no effect.

**Note**

The dual panel buffer is needed to fully support dual panels. Disabling the dual panel buffer may allow higher resolution/color display modes than would otherwise be possible. However, disabling the dual panel buffer reduces image contrast and overall display quality. For details on Frame Rate Calculation, see Section 18, “Clocking” on page 189.

| **LCD Display Start Address Register 0** REG[042h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD Display Start Address Bit 7 | LCD Display Start Address Bit 6 | LCD Display Start Address Bit 5 | LCD Display Start Address Bit 4 | LCD Display Start Address Bit 3 | LCD Display Start Address Bit 2 | LCD Display Start Address Bit 1 | LCD Display Start Address Bit 0 |

| **LCD Display Start Address Register 1** REG[043h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD Display Start Address Bit 15 | LCD Display Start Address Bit 14 | LCD Display Start Address Bit 13 | LCD Display Start Address Bit 12 | LCD Display Start Address Bit 11 | LCD Display Start Address Bit 10 | LCD Display Start Address Bit 9 | LCD Display Start Address Bit 8 |

| **LCD Display Start Address Register 2** REG[044h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | LCD Display Start Address Bit 19 | LCD Display Start Address Bit 18 | LCD Display Start Address Bit 17 | LCD Display Start Address Bit 16 |

REG[042h] bits 7-0 LCD Display Start Address Bits [19:0]
REG[043h] bits 7-0 This register forms the 20-bit address of the starting word of the LCD image in the
REG[044h] bits 3-0 display buffer.

**This is a word address.** An entry of 0 0000h into these registers represents the first word of the display buffer, an entry of 0 0001h represents the second word of the display buffer, and so on.

| **LCD Memory Address Offset Register 0** REG[046h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCD Memory Address Offset Bit 7 | LCD Memory Address Offset Bit 6 | LCD Memory Address Offset Bit 5 | LCD Memory Address Offset Bit 4 | LCD Memory Address Offset Bit 3 | LCD Memory Address Offset Bit 2 | LCD Memory Address Offset Bit 1 | LCD Memory Address Offset Bit 0 |

| **LCD Memory Address Offset Register 1** REG[047h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | LCD Memory Address Offset Bit 10 | LCD Memory Address Offset Bit 9 | LCD Memory Address Offset Bit 8 |

REG[046h] bits 7-0 LCD Memory Address Offset Bits [10:0]
REG[047h] bits 2-0 These bits are the LCD display's 11-bit address offset from the starting word of line "n" to the starting word of line "n + 1".

A virtual image can be formed by setting this register to a value greater than the width of the display. The displayed image is a window into the larger virtual image.

| **LCD Pixel Panning Register** REG[048h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | LCD Pixel Panning Bit 1 | LCD Pixel Panning Bit 0 |

bits 1-0 LCD Pixel Panning Bits [1:0]

This register is used to control the horizontal pixel panning of the LCD display. The display can be panned to the left by programming its respective Pixel Panning Bits to a non-zero value. This value represents the number of pixels panned. The maximum pan value is dependent on the display mode as shown in the table below.

*Table 8-20 : LCD Pixel Panning Selection*

| Color Depth (bpp) | Screen 2 Pixel Panning Bits Used |
|---|---|
| 4 bpp | Bits [1:0] |
| 8 bpp | Bit 0 |
| 16 bpp | --- |

**Note**

Smooth horizontal panning can be achieved by a combination of this register and the LCD Display Start Address registers (REG[042h], REG[043h], REG[044h]).

| **LCD Display FIFO High Threshold Control Register** REG[04Ah] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | LCD Display FIFO High Threshold Bit 5 | LCD Display FIFO High Threshold Bit 4 | LCD Display FIFO High Threshold Bit 3 | LCD Display FIFO High Threshold Bit 2 | LCD Display FIFO High Threshold Bit 1 | LCD Display FIFO High Threshold Bit 0 |

bits 5-0 LCD Display FIFO High Threshold Bits [5:0]

These bits are used to optimize the display memory request arbitration. When this register is set to 00h, the threshold is automatically set in hardware. However, programming may be required if screen corruption is present (see Section 18.2, “Example Frame Rates” on page 192).

**Note**

This register does not need to be used in single display modes and may only be required in some display modes where two displays are active (see Section 16.3, “Bandwidth Limitation” on page 187).

| **LCD Display FIFO Low Threshold Control Register** REG[04Bh] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | LCD Display FIFO Low Threshold Bit 5 | LCD Display FIFO Low Threshold Bit 4 | LCD Display FIFO Low Threshold Bit 3 | LCD Display FIFO Low Threshold Bit 2 | LCD Display FIFO Low Threshold Bit 1 | LCD Display FIFO Low Threshold Bit 0 |

its 5-0 LCD Display FIFO Low Threshold Bits [5:0]
When this register is set to 00h, the threshold is automatically set in hardware. If it becomes necessary to adjust REG[04Ah] from its default value, then the following formula must be maintained:

REG[04Bh] ≥ REG[04Ah] and REG[04Bh] ≤ 3Ch

## 8.4.8 CRT/TV Configuration Registers

| **CRT/TV Horizontal Display Width Register** REG[050h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | CRT/TV Horizontal Display Width Bit 6 | CRT/TV Horizontal Display Width Bit 5 | CRT/TV Horizontal Display Width Bit 4 | CRT/TV Horizontal Display Width Bit 3 | CRT/TV Horizontal Display Width Bit 2 | CRT/TV Horizontal Display Width Bit 1 | CRT/TV Horizontal Display Width Bit 0 |

bits 6-0 CRT/TV Horizontal Display Width Bits [6:0]
These bits specify the CRT/TV horizontal display width, in 8 pixel resolution.

Horizontal display width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

| **CRT/TV Horizontal Non-Display Period Register** REG[052h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | CRT/TV Horizontal Non-Display Period Bit 5 | CRT/TV Horizontal Non-Display Period Bit 4 | CRT/TV Horizontal Non-Display Period Bit 3 | CRT/TV Horizontal Non-Display Period Bit 2 | CRT/TV Horizontal Non-Display Period Bit 1 | CRT/TV Horizontal Non-Display Period Bit 0 |

bits 5-0 CRT/TV Horizontal Non-Display Period Bits [5:0]
These bits specify the CRT/TV horizontal non-display period width in 8 pixel resolution.

Horizontal non-display period width in number of pixels =
((ContentsOfThisRegister) + 1) × 8 for CRT mode
(ContentsOfThisRegister) × 8 + 6 for TV mode with NTSC output
(ContentsOfThisRegister) × 8 + 7 for TV mode with PAL output

**Note**
For CRT, the recommended minimum value which should be programmed into this register is 3 (32 pixels).

**Note**
REG[052h] + 1 ≥ (REG[053h] + 1) + (REG[054h] bits 3-0 + 1)

**CRT/TV HRTC Start Position Register**
REG[053h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | CRT/TV HRTC Start Position Bit 5 | CRT/TV HRTC Start Position Bit 4 | CRT/TV HRTC Start Position Bit 3 | CRT/TV HRTC Start Position Bit 2 | CRT/TV HRTC Start Position Bit 1 | CRT/TV HRTC Start Position Bit 0 |

bits 5-0 CRT/TV HRTC Start Position Bits [5:0]
For CRT/TV, these bits specify the delay, in 8 pixel resolution, from the start of the horizontal non-display period to the leading edge of the HRTC pulse.

The following equations can be used to determine the HRTC start position in number of pixels for each display type:

HRTC start position in number of pixels=:
[(ContentsOfThisRegister) x 8 + 4] for CRT with 4/8 bpp color depth
[(ContentsOfThisRegister) x 8 + 5] for CRT in 16 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 7] for TV-NTSC in 4/8 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 5] for TV-NTSC in 16 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 7] for TV-PAL in 4/8 bpp color depth
[((ContentsOfThisRegister) + 1) x 8 - 5] for TV-PAL in 16 bpp color depth

**Note**
REG[052h] + 1 ≥ (REG[053h] + 1) + (REG[054h] bits 3-0 + 1)

**CRT/TV HRTC Pulse Width Register**
REG[054h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT HRTC Polarity Select | n/a | n/a | n/a | CRT HRTC Pulse Width Bit 3 | CRT HRTC Pulse Width Bit 2 | CRT HRTC Pulse Width Bit 1 | CRT HRTC Pulse Width Bit 0 |

bit 7 CRT HRTC Polarity Select
This bit selects the polarity of HRTC for CRTs.
When this bit = 1, the HRTC pulse is active high.
When this bit = 0, the HRTC pulse is active low.

**Note**
For TV, this bit must be set to 0.

bits 3-0 CRT HRTC Pulse Width Bits [3:0]
These bits specify the pulse width of the CRT HRTC output signal in 8 pixel resolution.

HRTC pulse width in number of pixels = ((ContentsOfThisRegister) + 1) × 8

**Note**
For TV, these bits must be set to 0.

**Note**
REG[052h] + 1 ≥ (REG[053h] + 1) + (REG[054h] bits 3-0 + 1)

**CRT/TV Vertical Display Height Register 0**
REG[056h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Vertical Display Height Bit 7 | CRT/TV Vertical Display Height Bit 6 | CRT/TV Vertical Display Height Bit 5 | CRT/TV Vertical Display Height Bit 4 | CRT/TV Vertical Display Height Bit 3 | CRT/TV Vertical Display Height Bit 2 | CRT/TV Vertical Display Height Bit 1 | CRT/TV Vertical Display Height Bit 0 |

**CRT/TV Vertical Display Height Register 1**
REG[057h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | CRT/TV Vertical Display Height Bit 9 | CRT/TV Vertical Display Height Bit 8 |

REG[056h] bits 7-0 CRT/TV Vertical Display Height Bits [9:0]
REG[057h] bits 1-0 These bits specify the CRT/TV vertical display height, in 1 line resolution.

Vertical display height in number of lines = (ContentsOfThisRegister) + 1

**CRT/TV Vertical Non-Display Period Register**
REG[058h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Vertical Non-Display Period Status (RO) | CRT/TV Vertical Non-Display Period Bit 6 | CRT/TV Vertical Non-Display Period Bit 5 | CRT/TV Vertical Non-Display Period Bit 4 | CRT/TV Vertical Non-Display Period Bit 3 | CRT/TV Vertical Non-Display Period Bit 2 | CRT/TV Vertical Non-Display Period Bit 1 | CRT/TV Vertical Non-Display Period Bit 0 |

bit 7 CRT/TV Vertical Non-Display Period Status
This is a read-only status bit.
When a read from this bit = 1, a CRT/TV vertical non-display period is occurring.
When a read from this bit = 0, the CRT/TV output is in a vertical display period.

bits 6-0 CRT/TV Vertical Non-Display Period Bits [6:0]
These bits specify the CRT/TV vertical non-display period height in 1 line resolution.

Vertical non-display period height in number of lines = (ContentsOfThisRegister) + 1

**Note**
(REG[058h] bits 6-0 + 1) ≥ (REG[059h] + 1) + (REG[05Ah] bits 2-0 + 1)

**CRT/TV VRTC Start Position Register**
REG[059h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | CRT/TV VRTC Start Position Bit 6 | CRT/TV VRTC Start Position Bit 5 | CRT/TV VRTC Start Position Bit 4 | CRT/TV VRTC Start Position Bit 3 | CRT/TV VRTC Start Position Bit 2 | CRT/TV VRTC Start Position Bit 1 | CRT/TV VRTC Start Position Bit 0 |

bits 6-0 CRT/TV VRTC Start Position Bits [6:0]
For CRT/TV, these bits specify the delay in lines from the start of the vertical non-display period to the leading edge of the VRTC pulse.

VRTC start position in number of lines = (ContentsOfThisRegister) + 1

**Note**
(REG[058h] bits 6-0 + 1) ≥ (REG[059h] + 1) + (REG[05Ah] bits 2-0 + 1)

**CRT VRTC Pulse Width Register**
REG[05Ah] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT VRTC Polarity Select | n/a | n/a | n/a | n/a | CRT VRTC Pulse Width Bit 2 | CRT VRTC Pulse Width Bit 1 | CRT VRTC Pulse Width Bit 0 |

bit 7 CRT VRTC Polarity Select
This bit selects the polarity of VRTC for CRT.
When this bit = 1, the VRTC pulse is active high.
When this bit = 0, the VRTC pulse is active low.

**Note**
For TV, this bit must be set to 0.

bits 2-0 CRT VRTC Pulse Width Bits [2:0]
These bits specify the pulse width of the CRT VRTC output signal in number of lines.

VRTC pulse width in number of lines = (ContentsOfThisRegister) + 1

**Note**
For TV, these bits must be set to 0.

**Note**
(REG[058h] bits 6-0 + 1) ≥ (REG[059h] + 1) + (REG[05Ah] bits 2-0 + 1)

| **TV Output Control Register** REG[05Bh] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | TV Chrominance Filter Enable | TV Luminance Filter Enable | DAC Output Level Select | n/a | TV S-Video/ Composite Output Select | TV PAL/NTSC Output Select |

bit 5 TV Chrominance Filter Enable
When this bit = 1, the TV chrominance filter is enabled.
When this bit = 0, the TV chrominance filter is disabled.
The chrominance filter adjusts the color of the TV by limiting the bandwidth of the chrominance signal (reducing cross-luminance distortion). This reduces the “ragged edges” seen at boundaries between sharp color transitions. This filter is most useful for composite video output.

bit 4 TV Luminance Filter Enable
When this bit = 1, the TV luminance filter is enabled.
When this bit = 0, the TV luminance filter is disabled.
The luminance filter adjusts the brightness of the TV by limiting the bandwidth of the luminance signal (reducing cross-chrominance distortion). This reduces the “rainbow-like” colors at boundaries between sharp luminance transitions. This filter is most useful for composite video output.

bit 3 DAC Output Level Select
When this bit is set to 1 it allows IREF to be reduced. This bit should be set as described in the following table.

*Table 8-21: DAC Output Level Selection*

| LCD | CRT | TV | REG[05Bh] bit 3 | IREF (mA) |
|---|---|---|---|---|
| Enabled | Disabled | Disabled | x | x |
| x | Enabled | Disabled | 1 | 4.6 |
| x | Enabled | Enabled | 0 | 9.2 |

x = don’t care

**Note**
Figure 4-3: “External Circuitry for CRT Interface” on page 36 shows an example implementation of the required external CRT/TV IREF circuitry.

bit 1 TV S-Video/Composite Output Select
When this bit = 1, S-Video TV signal output is selected.
When this bit = 0, Composite TV signal output is selected.

bit 0 TV PAL/NTSC Output Select
When this bit = 1, PAL format TV signal output is selected.
When this bit = 0, NTSC format TV signal output is selected.
**This bit must be set to 0 when CRT is enabled**.

### 8.4.9 CRT/TV Display Mode Registers

| **CRT/TV Display Mode Register**<br>REG[060h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| CRT/TV Display Blank | n/a | n/a | n/a | n/a | CRT/TV Bit-per-pixel Select Bit 2 | CRT/TV Bit-per-pixel Select Bit 1 | CRT/TV Bit-per-pixel Select Bit 0 |

bit 7 CRT/TV Display Blank
When this bit = 1 the CRT/TV display pipeline is disabled and all CRT/TV data outputs are forced to zero (the screen is blanked).
When this bit = 0 the CRT display pipeline is enabled.

bits 2-0 CRT/TV Bit-per-pixel Select Bits [2:0]
These bits select the bit-per-pixel for the displayed data.

**Note**
Color depth of 16 bpp bypasses the LUT and support up to 64K colors on the CRT/TV.

*Table 8-22 : CRT/TV Bit-per-pixel Selection*

| Bit-per-pixel Select Bits 1:0 | Color Depth (bpp) |
|---|---|
| 000 | Reserved |
| 001 | Reserved |
| 010 | 4 bpp |
| 011 | 8 bpp |
| 100 | Reserved |
| 101 | 16 bpp |
| 110-111 | Reserved |

| **CRT/TV Display Start Address Register 0** REG[062h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Display Start Address Bit 7 | CRT/TV Display Start Address Bit 6 | CRT/TV Display Start Address Bit 5 | CRT/TV Display Start Address Bit 4 | CRT/TV Display Start Address Bit 3 | CRT/TV Display Start Address Bit 2 | CRT/TV Display Start Address Bit 1 | CRT/TV Display Start Address Bit 0 |

| **CRT/TV Display Start Address Register 1** REG[063h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Display Start Address Bit 15 | CRT/TV Display Start Address Bit 14 | CRT/TV Display Start Address Bit 13 | CRT/TV Display Start Address Bit 12 | CRT/TV Display Start Address Bit 11 | CRT/TV Display Start Address Bit 10 | CRT/TV Display Start Address Bit 9 | CRT/TV Display Start Address Bit 8 |

| **CRT/TV Display Start Address Register 2** REG[064h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | CRT/TV Display Start Address Bit 19 | CRT/TV Display Start Address Bit 18 | CRT/TV Display Start Address Bit 17 | CRT/TV Display Start Address Bit 16 |

REG[062h] bits 7-0 CRT/TV Start Address Bits [19:0]
REG[063h] bits 7-0 This register forms the 20-bit address for the starting word of the CRT/TV image in the
REG[064h] bits 3-0 display buffer.

**This is a word address.** An entry of 00000h into these registers represents the first word of the display buffer, an entry of 00001h represents the second word of the display buffer, and so on.

| **CRT/TV Memory Address Offset Register 0** REG[066h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Memory Address Offset Bit 7 | CRT/TV Memory Address Offset Bit 6 | CRT/TV Memory Address Offset Bit 5 | CRT/TV Memory Address Offset Bit 4 | CRT/TV Memory Address Offset Bit 3 | CRT/TV Memory Address Offset Bit 2 | CRT/TV Memory Address Offset Bit 1 | CRT/TV Memory Address Offset Bit 0 |

| **CRT/TV Memory Address Offset Register 1** REG[067h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | CRT/TV Memory Address Offset Bit 10 | CRT/TV Memory Address Offset Bit 9 | CRT/TV Memory Address Offset Bit 8 |

REG[066h] bits 7-0 CRT/TV Memory Address Offset Bits [10:0]
REG[067h] bits 2-0 These bits are the CRT/TV display's 11-bit address offset from the starting word of line "n" to the starting word of line "n + 1". A virtual image can be formed by setting this register to a value greater than the width of the display. The displayed image is a window into the larger virtual image.

| **CRT/TV Pixel Panning Register** REG[068h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | CRT/TV Pixel Panning Bit 1 | CRT/TV Pixel Panning Bit 0 |

bits 1-0 CRT/TV Pixel Panning Bits [1:0]

This register is used to control the horizontal pixel panning of the CRT/TV display. The display can be panned to the left by programming its respective Pixel Panning Bits to a non-zero value. This value represents the number of pixels panned. The maximum pan value is dependent on the display mode as shown in the table below.

*Table 8-23 : CRT/TV Pixel Panning Selection*

| Color Depth (bpp) | Screen 2 Pixel Panning Bits Used |
|---|---|
| 4 bpp | Bits [1:0] |
| 8 bpp | Bit 0 |
| 16 bpp | --- |

**Note**

Smooth horizontal panning can be achieved by a combination of this register and the CRT/TV Display Start Address registers (REG[062h], REG[063h], REG[064h]).

| **CRT/TV Display FIFO High Threshold Control Register** REG[06Ah] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | CRT/TV Display FIFO High Threshold Bit 5 | CRT/TV Display FIFO High Threshold Bit 4 | CRT/TV Display FIFO High Threshold Bit 3 | CRT/TV Display FIFO High Threshold Bit 2 | CRT/TV Display FIFO High Threshold Bit 1 | CRT/TV Display FIFO High Threshold Bit 0 |

bits 5-0 CRT/TV Display FIFO High Threshold Bits [5:0]

These bits are used to optimize the display memory request arbitration. When this register is set to 00h, the threshold is automatically set in hardware. However, programming may be required if screen corruption is present (see Section 18.2, “Example Frame Rates” on page 192).

**Note**

This register does not need to be used in single display modes and may only be required in some display modes where two displays are active (see Section 16.3, “Bandwidth Limitation” on page 187).

| **CRT/TV Display FIFO Low Threshold Control Register** REG[06Bh] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | CRT/TV Display FIFO Low Threshold Bit 5 | CRT/TV Display FIFO Low Threshold Bit 4 | CRT/TV Display FIFO Low Threshold Bit 3 | CRT/TV Display FIFO Low Threshold Bit 2 | CRT/TV Display FIFO Low Threshold Bit 1 | CRT/TV Display FIFO Low Threshold Bit 0 |

bits 5-0 CRT/TV Display FIFO Low Threshold Bits [5:0]
When this register is set to 00h, the threshold is automatically set in hardware. If it becomes necessary to adjust REG[06Ah] from its default value, then the following formula must be maintained.

REG[06Bh] ≥ REG[06Ah] and REG[06Bh] ≤ 3Ch

## 8.4.10 LCD Ink/Cursor Registers

| **LCD Ink/Cursor Control Register** REG[070h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | LCD Ink/Cursor Mode Bit 1 | LCD Ink/Cursor Mode Bit 0 |

bits 1-0 LCD Ink/Cursor Control Bits [1:0]
These bits enable the LCD Ink/Cursor circuitry.

*Table 8-24 : LCD Ink/Cursor Selection*

| LCD Ink/Cursor Bits [1:0] | Mode |
|---|---|
| 00 | Inactive |
| 01 | Cursor |
| 10 | Ink |
| 11 | Reserved |

**Note**
While in Ink mode, the Cursor X and Y Position registers must be set to 00h.

| **LCD Ink/Cursor Start Address Register** | | | | | | | |
|---|---|---|---|---|---|---|---|
| REG[071h] | | | | | | | RW |
| LCD Ink/Cursor Start Address Bit 7 | LCD Ink/Cursor Start Address Bit 6 | LCD Ink/Cursor Start Address Bit 5 | LCD Ink/Cursor Start Address Bit 4 | LCD Ink/Cursor Start Address Bit 3 | LCD Ink/Cursor Start Address Bit 2 | LCD Ink/Cursor Start Address Bit 1 | LCD Ink/Cursor Start Address Bit 0 |

bits 7-0 LCD Ink/Cursor Start Address Bits [7:0]

Encoded bits defining the start address for the LCD Ink/Cursor. For Cursor modes, a start address of 0 should be valid for most applications. For Ink or special Cursor modes, the start address should be set at an address location that does not conflict with the display memory of dual panel buffer, which always takes the top M memory locations in bytes.

$M = (\text{Panel Height} \times \text{Panel Width} / 16) \times c$

where

c = 1 for monochrome panel
= 4 for color panel

*Table 8-25 : LCD Ink/Cursor Start Address Encoding*

| LCD Ink/Cursor Start Address Bits [7:0] | Start Address |
|---|---|
| 0 | Memory Size - 1024 |
| n = 160...1 | Memory Size - n × 8192 |
| n = 255...161 | invalid |

**Note**
The effect of this register takes place at the next LCD vertical non-display period.

**Note**
See Section 10, “Display Buffer” on page 157 for display buffer organization.

| **LCD Cursor X Position Register 0** | | | | | | | |
|---|---|---|---|---|---|---|---|
| REG[072h] | | | | | | | RW |
| LCD Cursor X Position Bit 7 | LCD Cursor X Position Bit 6 | LCD Cursor X Position Bit 5 | LCD Cursor X Position Bit 4 | LCD Cursor X Position Bit 3 | LCD Cursor X Position Bit 2 | LCD Cursor X Position Bit 1 | LCD Cursor X Position Bit 0 |

| **LCD Cursor X Position Register 1** | | | | | | | |
|---|---|---|---|---|---|---|---|
| REG[073h] | | | | | | | RW |
| LCD Cursor X Sign | n/a | n/a | n/a | n/a | n/a | LCD Cursor X Position Bit 9 | LCD Cursor X Position Bit 8 |

REG[073h] bit 7 LCD Cursor X Sign

When this bit = 1, it defines the LCD Cursor X Position register to be a negative number. The negative number shall not exceed 63 decimal.
When this bit = 0, it defines the LCD Cursor X Position register to be a positive number.

REG[072h] bits 7-0 LCD Cursor X Position Bits [9:0]
REG[073h] bits 1-0 A 10-bit register that defines the horizontal position of the LCD Cursor's top left hand corner in pixel units. This register is only valid when Cursor has been selected in the LCD Ink/Cursor select registers.

**Note**

The effect of REG[072h] through REG[074h] takes place only after REG[075h] is written and at the next LCD vertical non-display period.The effect of REG[075h] takes place at the next LCD vertical non-display period.

**LCD Cursor Y Position Register 0**
REG[074h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LCD Cursor Y Position Bit 7 | LCD Cursor Y Position Bit 6 | LCD Cursor Y Position Bit 5 | LCD Cursor Y Position Bit 4 | LCD Cursor Y Position Bit 3 | LCD Cursor Y Position Bit 2 | LCD Cursor Y Position Bit 1 | LCD Cursor Y Position Bit 0 |

**LCD Cursor Y Position Register 1**
REG[075h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LCD Cursor Y Sign | n/a | n/a | n/a | n/a | n/a | LCD Cursor Y Position Bit 9 | LCD Cursor Y Position Bit 8 |

REG[075h] bit 7 LCD Cursor Y Sign
When this bit = 1, it defines the LCD Cursor Y Position register to be a negative number. The negative number shall not exceed 63 decimal.
When this bit = 0, it defines the LCD Cursor Y Position register to be a positive number.

REG[074h] bits 7-0 LCD Cursor Y Position Bits [9:0]
REG[075h] bits 1-0 A 10-bit register that defines the vertical position of the LCD Cursor's top left hand corner in pixel units. This register is only valid when Cursor has been selected in the LCD Ink/Cursor select registers.

**Note**

The effect of REG[072h] through REG[074h] takes place only after REG[075h] is written and at the next LCD vertical non-display period.The effect of REG[075h] takes place at the next LCD vertical non-display period.

**LCD Ink/Cursor Blue Color 0 Register**
REG[076h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | LCD Ink/Cursor Blue Color 0 Bit 4 | LCD Ink/Cursor Blue Color 0 Bit 3 | LCD Ink/Cursor Blue Color 0 Bit 2 | LCD Ink/Cursor Blue Color 0 Bit 1 | LCD Ink/Cursor Blue Color 0 Bit 0 |

bits 4-0 LCD Ink/Cursor Blue Color 0 Bits[4:0]
These bits define the blue LCD Ink/Cursor color 0.

**LCD Ink/Cursor Green Color 0 Register**
REG[077h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | LCD Ink/Cursor Green Color 0 Bit 5 | LCD Ink/Cursor Green Color 0 Bit 4 | LCD Ink/Cursor Green Color 0 Bit 3 | LCD Ink/Cursor Green Color 0 Bit 2 | LCD Ink/Cursor Green Color 0 Bit 1 | LCD Ink/Cursor Green Color 0 Bit 0 |

bits 5-0 LCD Ink/Cursor Green Color 0 Bits[5:0]
These bits define the green LCD ink/Cursor color 0.

**LCD Ink/Cursor Red Color 0 Register**
REG[078h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | LCD Ink/Cursor Red Color 0 Bit 4 | LCD Ink/Cursor Red Color 0 Bit 3 | LCD Ink/Cursor Red Color 0 Bit 2 | LCD Ink/Cursor Red Color 0 Bit 1 | LCD Ink/Cursor Red Color 0 Bit 0 |

bits 4-0 LCD Ink/Cursor Red Color 0 Bits[4:0]
These bits define the red LCD Ink/Cursor color 0.

**LCD Ink/Cursor Blue Color 1 Register**
REG[07Ah] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | LCD Ink/Cursor Blue Color 1 Bit 4 | LCD Ink/Cursor Blue Color 1 Bit 3 | LCD Ink/Cursor Blue Color 1 Bit 2 | LCD Ink/Cursor Blue Color 1 Bit 1 | LCD Ink/Cursor Blue Color 1 Bit 0 |

bits 4-0 LCD Ink/Cursor Blue Color 1 Bits[4:0]
These bits define the blue LCD Ink/Cursor color 1.

**LCD Ink/Cursor Green Color 1 Register**
REG[07Bh] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | LCD Ink/Cursor Green Color 1 Bit 5 | LCD Ink/Cursor Green Color 1 Bit 4 | LCD Ink/Cursor Green Color 1 Bit 3 | LCD Ink/Cursor Green Color 1 Bit 2 | LCD Ink/Cursor Green Color 1 Bit 1 | LCD Ink/Cursor Green Color 1 Bit 0 |

bits 5-0 LCD Ink/Cursor Green Color 1 Bits[5:0]
These bits define the green LCD Ink/Cursor color 1.

**LCD Ink/Cursor Red Color 1 Register**
REG[07Ch] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | LCD Ink/Cursor Red Color 1 Bit 4 | LCD Ink/Cursor Red Color 1 Bit 3 | LCD Ink/Cursor Red Color 1 Bit 2 | LCD Ink/Cursor Red Color 1 Bit 1 | LCD Ink/Cursor Red Color 1 Bit 0 |

bits 4-0 LCD Ink/Cursor Red Color 1 Bits[4:0]
These bits define the red LCD Ink/Cursor color 1.

| **LCD Ink/Cursor FIFO High Threshold Register** REG[07Eh] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | LCD Ink/Cursor FIFO High Threshold Bit 3 | LCD Ink/Cursor FIFO High Threshold Bit 2 | LCD Ink/Cursor FIFO High Threshold Bit 1 | LCD Ink/Cursor FIFO High Threshold Bit 0 |

bits 3-0 LCD Ink/Cursor FIFO High Threshold Bits [3:0]
These bits are used to optimize the display memory request arbitration for the Hardware Cursor/Ink Layer. When this register is set to 00h, the threshold is automatically set in hardware.

## 8.4.11 CRT/TV Ink/Cursor Registers

| **CRT/TV Ink/Cursor Control Register** REG[080h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | CRT/TV Ink/Cursor Mode Bit 1 | CRT/TV Ink/Cursor Mode Bit 0 |

bits 1-0 CRT/TV Ink/Cursor Control Bits [1:0]
These bits enable the CRT/TV Ink/Cursor circuitry.

*Table 8-26 : CRT/TV Ink/Cursor Selection*

| CRT/TV Ink/Cursor Bits [1:0] | Mode |
|---|---|
| 00 | Inactive |
| 01 | Cursor |
| 10 | Ink |
| 11 | Reserved |

**Note**
While in Ink mode, the Cursor X and Y Position registers must be set to 00h.

| **CRT/TV Ink/Cursor Start Address Register** REG[081h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| CRT/TV Ink/Cursor Start Address Bit 7 | CRT/TV Ink/Cursor Start Address Bit 6 | CRT/TV Ink/Cursor Start Address Bit 5 | CRT/TV Ink/Cursor Start Address Bit 4 | CRT/TV Ink/Cursor Start Address Bit 3 | CRT/TV Ink/Cursor Start Address Bit 2 | CRT/TV Ink/Cursor Start Address Bit 1 | CRT/TV Ink/Cursor Start Address Bit 0 |

bits 7-0 CRT/TV Ink/Cursor Start Address Bits [7:0]

Encoded bits defining the start address for the CRT/TV Ink/Cursor. For Cursor modes, a start address of 0 should be valid for most applications. For Ink or special Cursor modes, the start address should be set at an address location that does not conflict with the display memory of dual panel buffer, which always takes the top memory locations (M) in bytes.

$M = (\text{Panel Height} \times \text{Panel Width} / 16) \times c$

where

c = 1 for monochrome panel
= 4 for color panel

*Table 8-27 : CRT/TV Ink/Cursor Start Address Encoding*

| CRT/TV Ink/Cursor Start Address Bits [7:0] | Start Address |
|---|---|
| 0 | Memory Size - 1024 |
| n = 160...1 | Memory Size - n × 8192 |
| n = 255...161 | Invalid |

**Note**
The effect of this register takes place at the next CRT/TV vertical non-display period.

**Note**
See Section 10, “Display Buffer” on page 157 for display buffer organization.

| **CRT/TV Cursor X Position Register 0** REG[082h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| CRT/TV Cursor X Position Bit 7 | CRT/TV Cursor X Position Bit 6 | CRT/TV Cursor X Position Bit 5 | CRT/TV Cursor X Position Bit 4 | CRT/TV Cursor X Position Bit 3 | CRT/TV Cursor X Position Bit 2 | CRT/TV Cursor X Position Bit 1 | CRT/TV Cursor X Position Bit 0 |

| **CRT/TV Cursor X Position Register 1** REG[083h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| CRT/TV Cursor X Sign | n/a | n/a | n/a | n/a | n/a | CRT/TV Cursor X Position Bit 9 | CRT/TV Cursor X Position Bit 8 |

REG[083h] bit 7 CRT/TV Cursor X Sign
When this bit = 1, it defines the CRT/TV Cursor X Position register to be a negative number. The negative number should not exceed 63 decimal.
When this bit = 0, it defines the CRT/TV Cursor X Position register to be a positive number.

REG[082h] bits 7-0 CRT/TV Cursor X Position Bits [9:0]
REG[083h] bits 1-0 A 10-bit register that defines the horizontal position of the CRT/TV Cursor's top left hand corner in pixel units. This register is only valid when Cursor has been selected in the CRT/TV Ink/Cursor select registers.

**Note**

The effect of REG[082h] through REG[084h] takes place only after REG[085h]is written to and at the next CRT/TV vertical non-display period.The effect of REG[085h] takes place at the next CRT/TV vertical non-display period.

**CRT/TV Cursor Y Position Register 0**
REG[084h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Cursor Y Position Bit 7 | CRT/TV Cursor Y Position Bit 6 | CRT/TV Cursor Y Position Bit 5 | CRT/TV Cursor Y Position Bit 4 | CRT/TV Cursor Y Position Bit 3 | CRT/TV Cursor Y Position Bit 2 | CRT/TV Cursor Y Position Bit 1 | CRT/TV Cursor Y Position Bit 0 |

**CRT/TV Cursor Y Position Register 1**
REG[085h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CRT/TV Cursor Y Sign | n/a | n/a | n/a | n/a | n/a | CRT/TV Cursor Y Position Bit 9 | CRT/TV Cursor Y Position Bit 8 |

REG[084h] bit 7 CRT/TV Cursor YSign
When this bit = 1, it defines the CRT/TV Cursor Y Position register to be a negative number. The negative number shall not exceed 63 decimal.
When this bit = 0, it defines the CRT/TV Cursor Y Position register to be a positive number.

REG[084h] bits 7-0 CRT/TV Cursor Y Position Bits [9:0]
REG[085h] bits 1-0 A 10-bit register that defines the vertical position of the CRT/TV Cursor's top left hand corner in pixel units. This register is only valid when Cursor has been selected in the CRT/TV Ink/Cursor select registers.

**Note**

The effect of REG[082h] through REG[084h] takes place only after REG[085h]is written to and at the next CRT/TV vertical non-display period.The effect of REG[085h] takes place at the next CRT/TV vertical non-display period.

**CRT/TV Ink/Cursor Blue Color 0 Register**
REG[086h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | CRT/TV Ink/Cursor Blue Color 0 Bit 4 | CRT/TV Ink/Cursor Blue Color 0 Bit 3 | CRT/TV Ink/Cursor Blue Color 0 Bit 2 | CRT/TV Ink/Cursor Blue Color 0 Bit 1 | CRT/TV Ink/Cursor Blue Color 0 Bit 0 |

bits 4-0 CRT/TV Ink/Cursor Blue Color 0 Bits[4:0]
These bits define the blue CRT/TV Ink/Cursor color 0.

**CRT/TV Ink/Cursor Green Color 0 Register**
REG[087h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | CRT/TV Ink/Cursor Green Color 0 Bit 5 | CRT/TV Ink/Cursor Green Color 0 Bit 4 | CRT/TV Ink/Cursor Green Color 0 Bit 3 | CRT/TV Ink/Cursor Green Color 0 Bit 2 | CRT/TV Ink/Cursor Green Color 0 Bit 1 | CRT/TV Ink/Cursor Green Color 0 Bit 0 |

bits 5-0 CRT/TV Ink/Cursor Green Color 0 Bits[5:0]
These bits define the green CRT/TV Ink/Cursor color 0.

**CRT/TV Ink/Cursor Red Color 0 Register**
REG[088h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | CRT/TV Ink/Cursor Red Color 0 Bit 4 | CRT/TV Ink/Cursor Red Color 0 Bit 3 | CRT/TV Ink/Cursor Red Color 0 Bit 2 | CRT/TV Ink/Cursor Red Color 0 Bit 1 | CRT/TV Ink/Cursor Red Color 0 Bit 0 |

bits 4-0 CRT/TV Ink/Cursor Red Color 0 Bits[4:0]
These bits define the red CRT/TV Ink/Cursor color 0.

**CRT/TV Ink/Cursor Blue Color 1 Register**
REG[08Ah] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | CRT/TV Ink/Cursor Blue Color 1 Bit 4 | CRT/TV Ink/Cursor Blue Color 1 Bit 3 | CRT/TV Ink/Cursor Blue Color 1 Bit 2 | CRT/TV Ink/Cursor Blue Color 1 Bit 1 | CRT/TV Ink/Cursor Blue Color 1 Bit 0 |

bits 4-0 CRT/TV Ink/Cursor Blue Color 1 Bits[4:0]
These bits define the blue CRT/TV Ink/Cursor color 1.

**CRT/TV Ink/Cursor Green Color 1 Register**
REG[08Bh] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | CRT/TV Ink/Cursor Green Color 1 Bit 5 | CRT/TV Ink/Cursor Green Color 1 Bit 4 | CRT/TV Ink/Cursor Green Color 1 Bit 3 | CRT/TV Ink/Cursor Green Color 1 Bit 2 | CRT/TV Ink/Cursor Green Color 1 Bit 1 | CRT/TV Ink/Cursor Green Color 1 Bit 0 |

bits 5-0 CRT/TV Ink/Cursor Green Color 1 Bits[5:0]
These bits define the green CRT/TV Ink/Cursor color 1.

**CRT/TV Ink/Cursor Red Color 1 Register**
REG[08Ch] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | CRT/TV Ink/Cursor Red Color 1 Bit 4 | CRT/TV Ink/Cursor Red Color 1 Bit 3 | CRT/TV Ink/Cursor Red Color 1 Bit 2 | CRT/TV Ink/Cursor Red Color 1 Bit 1 | CRT/TV Ink/Cursor Red Color 1 Bit 0 |

bits 4-0 CRT/TV Ink/Cursor Red Color 1 Bits[4:0]
These bits define the red CRT/TV Ink/Cursor color 1.

**CRT/TV Ink/Cursor FIFO High Threshold Register**
REG[08Eh] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | CRT/TV Ink/Cursor FIFO High Threshold Bit 3 | CRT/TV Ink/Cursor FIFO High Threshold Bit 2 | CRT/TV Ink/Cursor FIFO High Threshold Bit 1 | CRT/TV Ink/Cursor FIFO High Threshold Bit 0 |

bits 3-0 CRT/TV Ink/Cursor FIFO High Threshold Bits [5:0]
These bits are used to optimize the display memory request arbitration for the Hardware Cursor/Ink Layer. When this register is set to 00h, the threshold is automatically set in hardware.

## 8.4.12 BitBLT Configuration Registers

| **BitBLT Control Register 0**<br>REG[100h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| BitBLT Active Status | BitBLT FIFO Not Empty Status (RO) | BitBLT FIFO Half Full Status (RO) | BitBLT FIFO Full Status(RO) | n/a | n/a | BitBLT Destination Linear Select | BitBLT Source Linear Select |

bit 7 BitBLT Active Status

This register bit has two data paths, one for write, the other for read.

Write Data Path

When software writes a one to this bit, it initiates the 2D operation.

Read Data Path

The read back of this register indicates the status of the 2D engine.
When a read from this bit = 1, the 2D engine is busy.
When a read from this bit = 0, the 2D engine is idle and is ready for the next operation.

*Table 8-28 : BitBLT Active Status*

| **BitBLT Active Status** | | **State** |
|---|---|---|
| **Write** | **Read** | |
| 0 | 0 | Idle |
| 0 | 1 | Reserved |
| 1 | 0 | Initiating operation |
| 1 | 1 | Operation in progress |

bit 6 BitBLT FIFO Not-Empty Status

This is a read-only status bit.
When this bit = 0, the BitBLT FIFO is empty.
When this bit = 1, the BitBLT FiFO has at least one data.
To reduce system memory read latency, software can monitor this bit prior to a BitBLT read burst operation.

The following table shows the number of words available in BitBLT FIFO under different status conditions.

*Table 8-29: BitBLT FIFO Words Available*

| **BitBLT FIFO Full Status (REG[100h] Bit 4)** | **BitBLT FIFO Half Full Status (REG[100h] Bit 5)** | **BitBLT FIFO Not Empty Status (REG[100h] Bit 6)** | **Number of Words available in BitBLT FIFO** |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 to 6 |
| 0 | 1 | 1 | 7 to 14 |
| 1 | 1 | 1 | 15 to 16 |

bit 5 BitBLT FIFO Half Full Status
This is a read-only status bit.
When this bit = 1, the BitBLT FIFO is half full or greater than half full.
When this bit = 0, the BitBLT FIFO is less than half full.

bit 4 BitBLT FIFO Full Status
This is a read-only status bit.
When this bit = 1, the BitBLT FIFO is full.
When this bit = 0, the BitBLT FIFO is not full.

bit 1 BitBLT Destination Linear Select
When this bit = 1, the Destination BitBLT is stored as a contiguous linear block of memory.
When this bit = 0, the Destination BitBLT is stored as a rectangular region of memory.
The BitBLT Memory Address Offset (REG[10Ch], REG[10Dh]) determines the address offset from the start of one line to the next line.

bit 0 BitBLT Source Linear Select
When this bit = 1, the Source BitBLT is stored as a contiguous linear block of memory.
When this bit = 0, the Source BitBLT is stored as a rectangular region of memory.
The BitBLT Memory Address Offset (REG[10Ch], REG[10Dh]) determines the address offset from the start of one line to the next line.

**BitBLT Control Register 1**
REG[101h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | Reserved | n/a | n/a | n/a | BitBLT Color Format Select |

bit 4 Reserved.
This bit must be set to 0.

bit 0 BitBLT Color Format Select
This bit selects the color format that the 2D operation is applied to.
When this bit = 0, 8 bpp (256 color) format is selected.
When this bit = 1, 16 bpp (64K color) format is selected.

| **BitBLT ROP Code/Color Expansion Register** | | | | | | | |
|---|---|---|---|---|---|---|---|
| REG[102h] | | | | | | | RW |
| n/a | n/a | n/a | n/a | BitBLT ROP Code Bit 3 | BitBLT ROP Code Bit 2 | BitBLT ROP Code Bit 1 | BitBLT ROP Code Bit 0 |

bits 3-0 BitBLT Raster Operation Code/Color Expansion Bits [3:0]
ROP Code for Write BitBLT and Move BitBLT. Bits 2-0 also specify the start bit position for Color Expansion.

*Table 8-30 : BitBLT ROP Code/Color Expansion Function Selection*

| BitBLT ROP Code Bits [3:0] | Boolean Function for Write BitBLT and Move BitBLT | Boolean Function for Pattern Fill | Start Bit Position for Color Expansion |
|---|---|---|---|
| 0000 | 0 (Blackness) | 0 (Blackness) | bit 0 |
| 0001 | ~S . ~D or ~(S + D) | ~P . ~D or ~(P + D) | bit 1 |
| 0010 | ~S . D | ~P . D | bit 2 |
| 0011 | ~S | ~P | bit 3 |
| 0100 | S . ~D | P . ~D | bit 4 |
| 0101 | ~D | ~D | bit 5 |
| 0110 | S ^ D | P ^ D | bit 6 |
| 0111 | ~S + ~D or ~(S . D) | ~P + ~D or ~(P . D) | bit 7 |
| 1000 | S . D | P . D | bit 0 |
| 1001 | ~(S ^ D) | ~(P ^ D) | bit 1 |
| 1010 | D | D | bit 2 |
| 1011 | ~S + D | ~P + D | bit 3 |
| 1100 | S | P | bit 4 |
| 1101 | S + ~D | P + ~D | bit 5 |
| 1110 | S + D | P + D | bit 6 |
| 1111 | 1 (Whiteness) | 1 (Whiteness) | bit 7 |

**Note**
S = Source, D = Destination, P = Pattern.

| **BitBLT Operation Register**<br>REG[103h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | BitBLT Operation Bit 3 | BitBLT Operation Bit 2 | BitBLT Operation Bit 1 | BitBLT Operation Bit 0 |

bits 3-0 BitBLT Operation Bits [3:0]

Specifies the 2D Operation to be carried out based on the following table.

*Table 8-31 : BitBLT Operation Selection*

| BitBLT Operation Bits [3:0] | BitBLT Operation |
|---|---|
| 0000 | Write BitBLT with ROP. |
| 0001 | Read BitBLT. |
| 0010 | Move BitBLT in positive direction with ROP. |
| 0011 | Move BitBLT in negative direction with ROP. |
| 0100 | Transparent Write BitBLT. |
| 0101 | Transparent Move BitBLT in positive direction. |
| 0110 | Pattern Fill with ROP. |
| 0111 | Pattern Fill with transparency. |
| 1000 | Color Expansion. |
| 1001 | Color Expansion with transparency. |
| 1010 | Move BitBLT with Color Expansion. |
| 1011 | Move BitBLT with Color Expansion and transparency. |
| 1100 | Solid Fill. |
| Other combinations | Reserved |

**Note**

The BitBLT operations Pattern Fill with ROP and Pattern Fill with transparency require a BitBLT width > 2 for 8 bpp color depths and a BitBLT width > 1 for 16 bpp color depths. The BitBLT width is set in REG[110h], REG[111h].

| **BitBLT Source Start Address Register 0** REG[104h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Source Start Address Bit 7 | BitBLT Source Start Address Bit 6 | BitBLT Source Start Address Bit 5 | BitBLT Source Start Address Bit 4 | BitBLT Source Start Address Bit 3 | BitBLT Source Start Address Bit 2 | BitBLT Source Start Address Bit 1 | BitBLT Source Start Address Bit 0 |

| **BitBLT Source Start Address Register 1** REG[105h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Source Start Address Bit 15 | BitBLT Source Start Address Bit 14 | BitBLT Source Start Address Bit 13 | BitBLT Source Start Address Bit 12 | BitBLT Source Start Address Bit 11 | BitBLT Source Start Address Bit 10 | BitBLT Source Start Address Bit 9 | BitBLT Source Start Address Bit 8 |

| **BitBLT Source Start Address Register 2** REG[106h] RW | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | BitBLT Source Start Address Bit 20 | BitBLT Source Start Address Bit 19 | BitBLT Source Start Address Bit 18 | BitBLT Source Start Address Bit 17 | BitBLT Source Start Address Bit 16 |

REG[104h] bits 7-0 BitBLT Source Start Address Bits [20:0]
REG[105h] bits 7-0 A 21-bit register that specifies the source start address for the BitBLT operation.
REG[106h] bits 4-0 If data is sourced from the CPU, then bit 0 is used for byte alignment within a 16-bit word and the other address bits are ignored. In pattern fill operation, the BitBLT Source Start Address is defined by the following equation.

Value programmed to the Source Start Address Register =
Pattern Base Address + Pattern Line Offset + Pixel Offset.

The following table shows how Source Start Address Register is defined for 8 and 16 bpp color depths.

*Table 8-32 : BitBLT Source Start Address Selection*

| Color Format | Pattern Base Address[20:0] | Pattern Line Offset[2:0] | Pixel Offset[3:0] |
|---|---|---|---|
| 8 bpp | BitBLT Source Start Address[20:6] | BitBLT Source Start Address[5:3] | BitBLT Source Start Address[2:0] |
| 16 bpp | BitBLT Source Start Address[20:7] | BitBLT Source Start Address[6:4] | BitBLT Source Start Address[3:0] |

**Note**
For further information on the BitBLT Source Start Address register, see the *S1D13806 Programming Notes and Examples*, document number X28B-G-003-xx.

**BitBLT Destination Start Address Register 0**
REG[108h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Destination Start Address Bit 7 | BitBLT Destination Start Address Bit 6 | BitBLT Destination Start Address Bit 5 | BitBLT Destination Start Address Bit 4 | BitBLT Destination Start Address Bit 3 | BitBLT Destination Start Address Bit 2 | BitBLT Destination Start Address Bit 1 | BitBLT Destination Start Address Bit 0 |

**BitBLT Destination Start Address Register 1**
REG[109h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Destination Start Address Bit 15 | BitBLT Destination Start Address Bit 14 | BitBLT Destination Start Address Bit 13 | BitBLT Destination Start Address Bit 12 | BitBLT Destination Start Address Bit 11 | BitBLT Destination Start Address Bit 10 | BitBLT Destination Start Address Bit 9 | BitBLT Destination Start Address Bit 8 |

**BitBLT Destination Start Address Register 2**
REG[10Ah] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | BitBLT Destination Start Address Bit 20 | BitBLT Destination Start Address Bit 19 | BitBLT Destination Start Address Bit 18 | BitBLT Destination Start Address Bit 17 | BitBLT Destination Start Address Bit 16 |

REG[108h] bits 7-0 BitBLT Destination Start Address Bits [20:0]
REG[109h] bits 7-0 A 21-bit register that specifies the destination start address for the BitBLT operation.
REG[10Ah] bits 4-0

**BitBLT Memory Address Offset Register 0**
REG[10Ch] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Memory Address Offset Bit 7 | BitBLT Memory Address Offset Bit 6 | BitBLT Memory Address Offset Bit 5 | BitBLT Memory Address Offset Bit 4 | BitBLT Memory Address Offset Bit 3 | BitBLT Memory Address Offset Bit 2 | BitBLT Memory Address Offset Bit 1 | BitBLT Memory Address Offset Bit 0 |

**BitBLT Memory Address Offset Register 1**
REG[10Dh] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | BitBLT Memory Address Offset Bit 10 | BitBLT Memory Address Offset Bit 9 | BitBLT Memory Address Offset Bit 8 |

REG[10Ch] bits 7-0 BitBLT Memory Address Offset Bits [10:0]
REG[10Dh] bits 2-0 These bits are the display's 11-bit address offset from the starting word of line *n* to the starting word of line *n + 1*. They are used only for address calculation when the BitBLT is configured as a rectangular region of memory.

**BitBLT Width Register 0**
REG[110h] RW

| BitBLT Width Bit 7 | BitBLT Width Bit 6 | BitBLT Width Bit 5 | BitBLT Width Bit 4 | BitBLT Width Bit 3 | BitBLT Width Bit 2 | BitBLT Width Bit 1 | BitBLT Width Bit 0 |
|---|---|---|---|---|---|---|---|

**BitBLT Width Register 1**
REG[111h] RW

| n/a | n/a | n/a | n/a | n/a | n/a | BitBLT Width Bit 9 | BitBLT Width Bit 8 |
|---|---|---|---|---|---|---|---|

REG[110h] bits 7-0 BitBLT Width Bits [9:0]
REG[111h] bits 1-0 A 10-bit register that specifies the BitBLT width in pixels - 1.

BitBLT width in pixels = (ContentsOfThisRegister) + 1

**Note**
The BitBLT operations Pattern Fill with ROP and Pattern Fill with transparency require a BitBLT width > 2 for 8 bpp color depths and a BitBLT width > 1 for 16 bpp color depths.

**BitBLT Height Register 0**
REG[112h] RW

| BitBLT Height Bit 7 | BitBLT Height Bit 6 | BitBLT Height Bit 5 | BitBLT Height Bit 4 | BitBLT Height Bit 3 | BitBLT Height Bit 2 | BitBLT Height Bit 1 | BitBLT Height Bit 0 |
|---|---|---|---|---|---|---|---|

**BitBLT Height Register 1**
REG[113h] RW

| n/a | n/a | n/a | n/a | n/a | n/a | BitBLT Height Bit 9 | BitBLT Height Bit 8 |
|---|---|---|---|---|---|---|---|

REG[112h] bits 7-0 BitBLT Height Bits [9:0]
REG[113h] bits 1-0 A 10-bit register that specifies the BitBLT height in lines - 1.

BitBLT height in lines = (ContentsOfThisRegister) + 1

**BitBLT Background Color Register 0**
REG[114h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Background Color Bit 7 | BitBLT Background Color Bit 6 | BitBLT Background Color Bit 5 | BitBLT Background Color Bit 4 | BitBLT Background Color Bit 3 | BitBLT Background Color Bit 2 | BitBLT Background Color Bit 1 | BitBLT Background Color Bit 0 |

**BitBLT Background Color Register 1**
REG[115h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Background Color Bit 15 | BitBLT Background Color Bit 14 | BitBLT Background Color Bit 13 | BitBLT Background Color Bit 12 | BitBLT Background Color Bit 11 | BitBLT Background Color Bit 10 | BitBLT Background Color Bit 9 | BitBLT Background Color Bit 8 |

REG[114h] bits 7-0 BitBLT Background Color Bits [15:0]
REG[115h] bits 15-8 A 16-bit register that specifies the BitBLT background color for Color Expansion or key color for Transparent BitBLT. For 16 bpp color depths (REG[101h] bit 0 = 1), all 16 bits are used. For 8 bpp color depths (REG[101h] bit 0 = 0), only bits 7-0 are used.

**BitBLT Foreground Color Register 0**
REG[118h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Foreground Color Bit 7 | BitBLT Foreground Color Bit 6 | BitBLT Foreground Color Bit 5 | BitBLT Foreground Color Bit 4 | BitBLT Foreground Color Bit 3 | BitBLT Foreground Color Bit 2 | BitBLT Foreground Color Bit 1 | BitBLT Foreground Color Bit 0 |

**BitBLT Foreground Color Register 1**
REG[119h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BitBLT Foreground Color Bit 15 | BitBLT Foreground Color Bit 14 | BitBLT Foreground Color Bit 13 | BitBLT Foreground Color Bit 12 | BitBLT Foreground Color Bit 11 | BitBLT Foreground Color Bit 10 | BitBLT Foreground Color Bit 9 | BitBLT Foreground Color Bit 8 |

REG[118h] bits 7-0 BitBLT Foreground Color Bits [15:0]
REG[119h] bits 7-0 A 16-bit register that specifies the BitBLT foreground color for Color Expansion or Solid Fill. For 16 bpp color depths (REG[101h] bit 0 = 1), all 16 bits are used. For 8 bpp color depths (REG[101h] bit 0 = 0), only bits 7-0 are used.

### 8.4.13 Look-Up Table Registers

**Note**
Accessing the LCD Look-Up Table (LUT) requires an active LCD PCLK and accessing the CRT/TV LUT requires an active CRT/TV PCLK. For further information on the clocks, see Section 7, “Clocks” on page 92.

| **Look-Up Table Mode Register** REG[1E0h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | LUT Mode Bit 1 | LUT Mode Bit 0 |

bits 1-0 Look-Up Table Mode Bits [1:0]
These bits determine which of the on-chip Look-Up Tables (LUT) (LCD and CRT/TV) are accessible by REG[1E2h] and REG[1E4h].

*Table 8-33 : LUT Mode Selection*

| LUT Mode Bits [1:0] | Read | Write |
|---|---|---|
| 00 | LCD LUT | LCD and CRT/TV LUT’s |
| 01 | LCD LUT | LCD LUT |
| 10 | CRT/TV LUT | CRT/TV LUT |
| 11 | Reserved | Reserved |

| **Look-Up Table Address Register** REG[1E2h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LUT Address Bit 7 | LUT Address Bit 6 | LUT Address Bit 5 | LUT Address Bit 4 | LUT Address Bit 3 | LUT Address Bit 2 | LUT Address Bit 1 | LUT Address Bit 0 |

bits 7-0 LUT Address Bits [7:0]
These 8 bits control a pointer into the Look-Up Tables (LUT). The S1D13806 has three 256-position, 4-bit wide LUTs, one for each of red, green, and blue – refer to Section 12, “Look-Up Table Architecture” on page 161 for details.

This register selects which LUT entry is read/write accessible through the LUT Data Register (REG[1E4h]). Writing the LUT Address Register automatically sets the pointer to the Red LUT. Accesses to the LUT Data Register automatically increment the pointer.

For example, writing a value 03h into the LUT Address Register sets the pointer to R[3]. A subsequent access to the LUT Data Register accesses R[3] and moves the pointer onto G[3]. Subsequent accesses to the LUT Data Register move the pointer onto B[3], R[4], G[4], B[4], R[5], etc.

**Note**
The RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

| **Look-Up Table Data Register** REG[1E4h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LUT Data Bit 3 | LUT Data Bit 2 | LUT Data Bit 1 | LUT Data Bit 0 | n/a | n/a | n/a | n/a |

bits 7-4 LUT Data Bits [3:0]
This register is used to read/write the RGB Look-Up Tables. This register accesses the entry at the pointer controlled by the Look-Up Table Address register (REG[1E2h]). Accesses to the Look-Up Table Data register automatically increment the pointer.

**Note**
The RGB data is inserted into the LUT after the Blue data is written, i.e. all three colors must be written before the LUT is updated.

### 8.4.14 Power Save Configuration Registers

For further information on Power Save Mode, refer to Section 19, “Power Save Mode” on page 202.

| **Power Save Configuration Register** REG[1F0h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | Reserved | n/a | n/a | n/a | Power Save Mode Enable |

bit 4 Reserved.
This bit must be set to 1.

bit 0 Power Save Mode Enable
When this bit = 1, power save mode is enabled.
When this bit = 0, power save mode is disabled.

**Note**
For details on Power Save Mode, see Section 19, “Power Save Mode” on page 202.

| **Power Save Status Register** REG[1F1h] | | | | | | | RO |
|---|---|---|---|---|---|---|---|
| n/a | n/a | n/a | n/a | n/a | n/a | LCD Power Save Status | Memory Controller Power Save Status |

bit 1 LCD Power Save Status
This bit indicates the power save state of the LCD panel.
When this bit = 1, the panel is powered down.
When this bit = 0, the panel is powered up, or in transition of powering up or down.

**Note**
When this bit reads a 1, the system may safely shut down the LCD pixel clock source.

**Note**
When the LCD panel is not enabled (REG[1FCh] bit 0 = 0), this bit returns a 1.

bit 0 Memory Controller Power Save Status
This bit indicates the power save state of the memory controller.
When this bit = 1, the memory controller is powered down and the SDRAM is in self refresh mode.
When this bit = 0, the memory controller is powered up and is in normal mode.

**Note**
When this bit reads a 1, the system may safely shut down the memory clock source.

## 8.4.15 Miscellaneous Registers

| **CPU-to-Memory Access Watchdog Timer Register** REG[1F4h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | n/a | Mem. Access Watchdog Timer bit 5 | Mem. Access Watchdog Timer bit 4 | Mem. Access Watchdog Timer bit 3 | Mem. Access Watchdog Timer bit 2 | Mem. Access Watchdog Timer bit 1 | Mem. Access Watchdog Timer bit 0 |

bits 5-0 CPU-to-Memory Access Watchdog Timer Bits [5:0]

A non-zero value in this register enables the watchdog timer for CPU-to-memory access. When enabled, any CPU-to-memory access cycle is completed successfully within a time determined by the following equation.

Maximum CPU-to-memory access cycle time = $(8n + 7) \times T_{bclk} + 13 \times T_{mclk}$

where:

n = A non-zero value in this register

$T_{bclk}$ = Bus clock period, or Bus clock period x 2 (if CONF5 = 1, see Table 4-9 on page 33)

$T_{mclk}$ = Memory clock period

This function is required by some busses which time-out if the cycle duration exceeds a certain time period. This function is **not intended to arbitrarily shorten the CPU-to-memory access cycle time** in order gain higher CPU bandwidth. Doing so may significantly reduce the available display refresh bandwidth which may cause display corruption. This register does not affect CPU-to-register access or BitBLT access.

## 8.4.16 Common Display Mode Register

| **Display Mode Register** REG[1FCh] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| n/a | SwivelView Enable Bit 0 | n/a | n/a | n/a | Display Mode Select Bit 2 | Display Mode Select Bit 1 | Display Mode Select Bit 0 |

bit 6 SwivelView Enable Bit 0
When this bit = 1, the LCD and CRT display image is rotated 90° clockwise.
When this bit = 0, there is no hardware effect.
This bit in conjunction with SwivelView™ Enable Bit 1 achieves the following hardware rotations.

*Table 8-34: Setting SwivelView Modes*

| **SwivelView Enable Bits** | **SwivelView™ Modes** | | | |
|---|---|---|---|---|
| | **Normal** | **SwivelView 90°** | **SwivelView 180°** | **SwivelView 270°** |
| SwivelView Enable Bit 0 (REG[1FCh] bit 6) | 0 | 1 | 0 | 1 |
| SwivelView Enable Bit 1 (REG[040h] bit 4) | 0 | 0 | 1 | 1 |

**Note**
Please refer to Section 15, “SwivelView™” on page 177 for application and limitations.

bits 2-0 Display Mode Select Bits [2:0]
These bits select the display model according to the following table. The LCD display mode is enabled/disabled using bit 0.

*Table 8-35: Display Mode Selection*

| **Display Mode Select Bits [2:0]** | **Display Mode Enabled** |
|---|---|
| 000 | no display |
| 001 | LCD only |
| 010 | CRT only |
| 011 | EISD (CRT and LCD) |
| 100 | TV with flicker filter off |
| 101 | EISD (TV with flicker filter off and LCD) |
| 110 | TV with flicker filter on |
| 111 | EISD (TV with flicker filter on and LCD) |

**Note**
REG[018h] bit 7 must be set to 1 when the flicker filter is enabled.

**Note**

The **Flicker Filter** reduces the "flickering" effect seen on interlaced displays by averaging adjacent lines on the TV display. This "flickering" is caused by sharp vertical image transitions that occur over one line (1 vertical pixel). For example, one pixel high lines, edges of window boxes, etc. Flickering occurs because these high resolution lines are effectively displayed at half the refresh frequency due to interlacing.

## 8.5 MediaPlug Registers Descriptions

The S1D13806 has built-in support for Winnov's MediaPlug connection designed for video cameras. The following registers are used to control the connection and accept data from the camera. The MediaPlug registers decode A11-A0 and require A20 = 0 and A12 = 1. The MediaPlug registers are 16-bit wide. Byte access to the MediaPlug registers is not allowed. For further information, see Section 17, "MediaPlug Interface" on page 188.

**Note**

The MediaPlug control registers must not be accessed while Power Save Mode is enabled (REG[1F0h] bit 0 = 1).

### 8.5.1 MediaPlug Control Registers

| **MediaPlug LCMD Register**<br>REG[1000h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCMD Bit 7 | LCMD Bit 6 | LCMD Bit 5 | LCMD Bit 4 | LCMD Bit 3 | LCMD Bit 2 | LCMD Bit 1 | LCMD Bit 0 |
| LCMD Bit 15 | LCMD Bit 14 | LCMD Bit 13 | LCMD Bit 12 | LCMD Bit 11 | LCMD Bit 10 | LCMD Bit 9 | LCMD Bit 8 |

REG[1000h] bits 15-0 MediaPlug LCMD Bits [15:0]

A 16-bit register for setting and detecting various modes of operation of the MediaPlug Local Slave. This register is handled differently for reads and writes. The following table shows the MediaPlug description of the LCMD Register. See bit descriptions for details.

*Table 8-36: MediaPlug LCMD Read/Write Descriptions*

| **Data** | **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** |
|---|---|---|---|---|---|---|---|---|
| Write | TO[2:0] | | Xxxxxx | | | | | |
| Read | TO[2:0] | | 00b | | Rev[3:0] | | | |

| **Data** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
|---|---|---|---|---|---|---|---|---|
| Write | Xxxx | | | | IC | MC | P | W |
| Read | Rstat[2:0] | | | 0b | IC | MC | P | W |

bits 15-14 Timeout Option

These bits select the timeout delay in MediaPlug clock cycles.

*Table 8-37: Timeout Option Delay*

| Timeout Option Bits[15:14] | Timeout (MediaPlug clock cycles) |
|---|---|
| 00 | 1023 (default) |
| 01 | 64 |
| 10 | 128 |
| 11 | 64 |

bits 13-12 A read from these bits always returns 00b.
A write to these bits has no hardware effect.

bits 11-8 MediaPlug IC Revision
The revision for this MediaPlug IC is “0011b”.
A write to these bits has no hardware effect.

bit 7 Cable Detected Status
The cable detected status as determined by the MPD(1) pin.
When this bit = 0, a MediaPlug cable is connected.
When this bit = 1, a MediaPlug cable is not detected.
A write to this bit has no hardware effect.

bit 6 A read from this bit always returns 0b.
A write to this bit has no hardware effect.

bit 5 Remote Powered Status
The remote powered status as determined by the RCTRL pin.
When this bit = 0, the remote is not powered.
When this bit = 1, the remote is powered and connected.
A write to this bit has no hardware effect.

*Table 8-38: Cable Detect and Remote Powered Status*

| Cable Detected Status [bit 7] | Remote Powered Status [bit 5] | Status |
|---|---|---|
| 0 | 0 | cable connected but remote not powered |
| 0 | 1 | cable connected and remote powered |
| 1 | x | cable not connected |

bit 4 A read from this bit always returns 0b.
A write to this bit has no hardware effect.

bit 3 MediaPlug Clock Enable
When this bit = 0, the MediaPlug clock is disabled (default).
When this bit = 1, the MediaPlug clock is enabled.

bit 2 MediaPlug Clock
When this bit = 0, the MediaPlug cable clock (VMPCLK) is disabled (default).
When this bit = 1, the MediaPlug cable clock (VMPCLK) is enabled.

| | |
|---|---|
| bit 1 | Power Enable to Remote<br>When this bit = 0, power to remote is off (default).<br>When this bit =1, power to remote is on. |
| bit 0 | Watchdog Disable<br>When this bit = 0, the MediaPlug watchdog is enabled (default).<br>When this bit = 1, the MediaPlug watchdog is disabled. |

| **MediaPlug Reserved LCMD Register**<br>REG[1002h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| LCMD Bit 23 | LCMD Bit 22 | LCMD Bit 21 | LCMD Bit 20 | LCMD Bit 19 | LCMD Bit 18 | LCMD Bit 17 | LCMD Bit 16 |
| LCMD Bit 31 | LCMD Bit 30 | LCMD Bit 29 | LCMD Bit 28 | LCMD Bit 27 | LCMD Bit 26 | LCMD Bit 25 | LCMD Bit 24 |

REG[1002h] bits 15-0 MediaPlug Reserved LCMD Bits [15:0]
This register is not implemented and is reserved for future expansion of the LCMD register. A write to this register has no hardware effect. A read from this register always return 0000h.

| **MediaPlug CMD Register**<br>REG[1004h] | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| CMD Bit 7 | CMD Bit 6 | CMD Bit 5 | CMD Bit 4 | CMD Bit 3 | CMD Bit 2 | CMD Bit 1 | CMD Bit 0 |
| CMD Bit 15 | CMD Bit 14 | CMD Bit 13 | CMD Bit 12 | CMD Bit 11 | CMD Bit 10 | CMD Bit 9 | CMD Bit 8 |

REG[1002h] bits 15-0 MediaPlug CMD Bits [15:0]
A 16-bit register for setting the MediaPlug commands. This register is handled differently for reads and writes. The following table shows the MediaPlug description of the CMD Register. See bit descriptions for details.

*Table 8-39: MediaPlug CMD Read/Write Descriptions*

| **Data** | **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** |
|---|---|---|---|---|---|---|---|---|
| Write | I[12:5] | | | | | | | |
| Read | D | T | I[10:5] | | | | | |

| **Data** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
|---|---|---|---|---|---|---|---|---|
| Write | I[4:0] | | | | | C[2:0] | | |
| Read | I[4:0] | | | | | C[2:0] | | |

bit 15 Dirty Bit
This bit is set by the hardware when the command register is written.
It is cleared by hardware by the following conditions:
1. Remote-Reset (After this command has been acknowledged by remote.
2. End_Stream (After this command has been acknowledged by remote.
3. Write to DATA register if the CCC field is Write_Reg.
4. Read to DATA register if the CCC field is Read_Reg.
It is also set when the Remote Machine loses power or the cable is disconnected.

bit 14 Timeout Bit
It is set when Watchdog is enabled and MediaPlug read or write cycle takes longer than 64, 128, 1024 cycles of MediaPlug clock depending on LCMD register settings.
It is also set when the remote is not powered.
It is cleared at the beginning of every command write by the host.

bits 13-3 Index Field
This field is the address presented by the remote to the remote function. MediaPlug transmits the entire 16-bits of the first word of the command Register as written, but I12 (D15) and I11 (D14) are hidden from readback by the dirty bit and Watchdog error bit.

bit 2-0 Command Field
Selects the command as follows:

*Table 8-40: MediaPlug Commands*

| Command Field [bits 2:0] | Command |
|---|---|
| 000 | Remote-Reset: Hardware reset of remote. |
| 001 | Stream-End: Indicates end of data streaming operation. |
| 010 | Write-Register: Write remote register INDEX[5:0] with DATA. |
| 011 | Read-Register: Read remote register INDEX[5:0] to DATA. |
| 100 | Write_Stream: Begin streaming data to the remote. |
| 101 | NOP: The command is sent across the MediaPlug. There is no other effect. |
| 110 | NOP: The command is sent across the MediaPlug. There is no other effect. |
| 111 | Read-Stream: Begin streaming data from the remote. |

**MediaPlug Reserved CMD Register**
REG[1006h] RW

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CMD Bit 23 | CMD Bit 22 | CMD Bit 21 | CMD Bit 20 | CMD Bit 19 | CMD Bit 18 | CMD Bit 17 | CMD Bit 16 |
| CMD Bit 31 | CMD Bit 30 | CMD Bit 29 | CMD Bit 28 | CMD Bit 27 | CMD Bit 26 | CMD Bit 25 | CMD Bit 24 |

REG[1006h] bits 15-0 MediaPlug Reserved CMD Bits [15:0]
This register is not implemented and is reserved for future expansion of the CMD register. A write to this register has no hardware effect. A read from this register always return 0000h.

### 8.5.2 MediaPlug Data Registers

| **MediaPlug Data Register**<br>REG[1008h] to REG[1FFEh], even address | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| Data Bit 7 | Data Bit 6 | Data Bit 5 | Data Bit 4 | Data Bit 3 | Data Bit 2 | Data Bit 1 | Data Bit 0 |
| Data Bit 15 | Data Bit 14 | Data Bit 13 | Data Bit 12 | Data Bit 11 | Data Bit 10 | Data Bit 9 | Data Bit 8 |

Data Register bits 15-0 MediaPlug Data Bits [15:0]
A 16-bit register used for read/write and streaming read/write of MediaPlug data. This register is loosely decoded from 1008h to 1FFEh so that the port may be accessed using DWORD block transfer instructions.

## 8.6 BitBLT Data Registers Descriptions

The BitBLT data registers decode A19-A0 and require A20 = 1. The BitBLT data registers are 16-bit wide. Byte access to the BitBLT data registers is not allowed.

| **BitBLT Data Register 0**<br>A20-A0 = 100000h-1FFFFEh, even address | | | | | | | RW |
|---|---|---|---|---|---|---|---|
| Data Bit 7 | Data Bit 6 | Data Bit 5 | Data Bit 4 | Data Bit 3 | Data Bit 2 | Data Bit 1 | Data Bit 0 |
| Data Bit 15 | Data Bit 14 | Data Bit 13 | Data Bit 12 | Data Bit 11 | Data Bit 10 | Data Bit 9 | Data Bit 8 |

Data Register bits 15-0 BitBLT Data Bits [15:0]
A 16-bit register that specifies the BitBLT data. This register is loosely decoded from 100000h to 1FFFFEh.

# 9 2D BitBLT Engine

## 9.1 Overview

The S1D13806 is designed with a built-in 2D BitBLT engine which increases the performance of Bit Block Transfers (BitBLT). It supports 8 and 16 bit-per-pixel color depths.

The BitBLT engine supports rectangular and linear addressing modes for source and destination in a positive direction for all BitBLT operations except the move BitBLT which also supports in a negative direction.

The BitBLT operations support byte alignment of all types. The BitBLT engine has a dedicated BitBLT IO access space allowing it to support multi-tasking applications. This allows the BitBLT engine to support simultaneous BitBLT and CPU read/write operations.

## 9.2 BitBLT Operations

The S1D13806 2D BitBLT engine supports the following BitBLTs. For detailed information on using the individual BitBLT operations, refer to the S1D13806 Programming Notes and Examples, document number X28B-G-003-xx.

- Write BitBLT.
- Move BitBLT.
- Solid Fill BitBLT.
- Pattern Fill BitBLT.
- Transparent Write BitBLT.
- Transparent Move BitBLT.
- Read BitBLT.
- Color Expansion BitBLT.
- Move BitBLT with Color Expansion.

**Note**

For details on the BitBLT registers, see Section 8.4.12, “BitBLT Configuration Registers” on page 137.

# 10 Display Buffer

The system addresses the display buffer using CS#, M/R#, and the input pins AB[20:0]. When CS# = 0 and M/R# = 1, the display buffer is addressed by bits AB[20:0]. See the table below:

*Table 10-1 : S1D13806 Addressing*

| CS# | M/R# | Access |
|---|---|---|
| 0 | 0 | Register access - see Section 8.2, “Register Mapping” on page 97.<br>• REG[000h] is addressed when AB[12:0] = 0<br>• REG[001h] is addressed when AB[12:0] = 1<br>• REG[n] is addressed when AB[12:0] = n |
| 0 | 1 | Memory access: the 1.25M byte display buffer is addressed by AB[20:0] |
| 1 | X | S1D13806 not selected |

The display buffer address space is always 2M bytes. However, the physical display buffer is 1280k bytes. The space above the 1280k boundary is unavailable (see Figure 10-1: “Display Buffer Addressing”).

The display buffer can contain an image buffer, one or more Ink Layer/Hardware Cursor buffers, and a dual panel buffer.

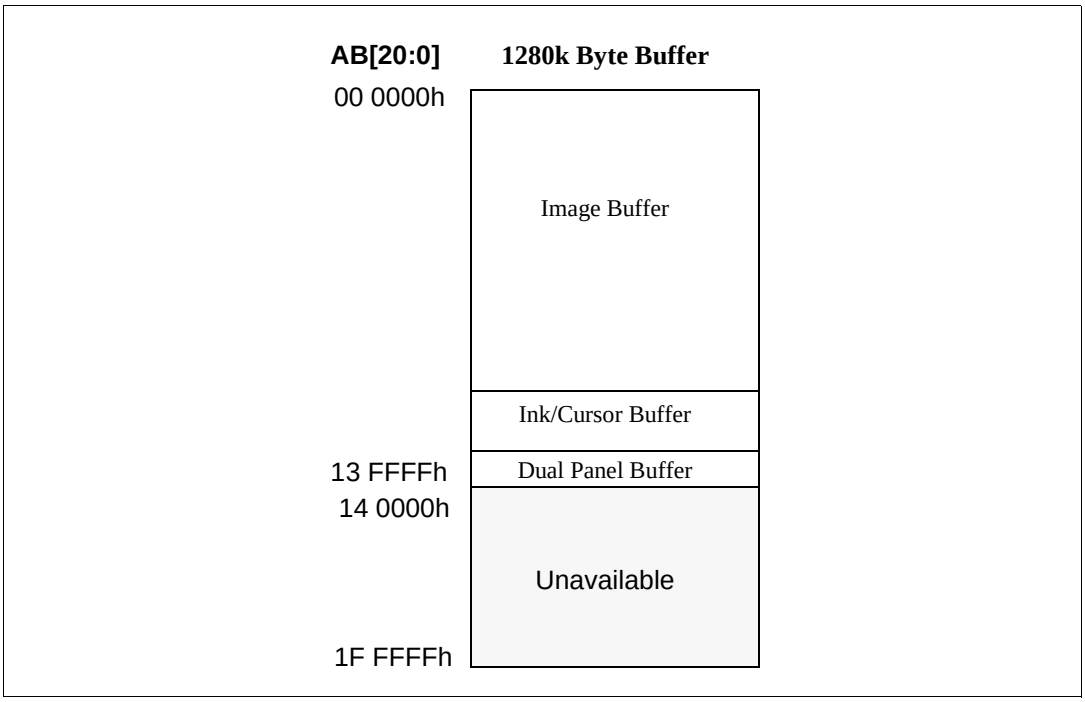



*Figure 10-1: Display Buffer Addressing*

## 10.1 Image Buffer

The image buffer contains the formatted display mode data – see Section 11.1, “Display Mode Data Format” on page 159.

The displayed image(s) may occupy only a portion of this space with the remaining area used for multiple images – possibly for animation or general storage. Section 11, “Display Configuration” on page 159 for the relationship between the image buffer and the displayed image.

## 10.2 Ink Layer/Hardware Cursor Buffers

The Ink Layer/Hardware Cursor buffers contain formatted image data for the Ink Layer and Hardware Cursor. There may be several Ink Layer/Hardware Cursor images stored in the display buffer but only one may be active at any given time.

For further information, see Section 14, “Ink Layer/Hardware Cursor Architecture” on page 173.

## 10.3 Dual Panel Buffer

In dual panel mode with the dual panel buffer enabled, the top of the display buffer is allocated to the dual panel buffer. The size of the dual panel buffer is a function of the panel resolution and the type of panel (color or monochrome).

Dual Panel Buffer Size (in bytes) = (panel width x panel height) × factor ÷ 16

where factor: = 4 for color panel
= 1 for monochrome panel

**Note**
Calculating the size of the dual panel buffer is required to avoid overwriting the Hardware Cursor/Ink Layer buffer.

***Example 1: For a 800x600 color panel the dual panel buffer size is 120,000 bytes. With a 1280k byte display buffer, the dual panel buffer resides from 12 2b40h to 13 FFFFh.***

# 11 Display Configuration

## 11.1 Display Mode Data Format

The following diagram show the display mode data formats for a little endian system.

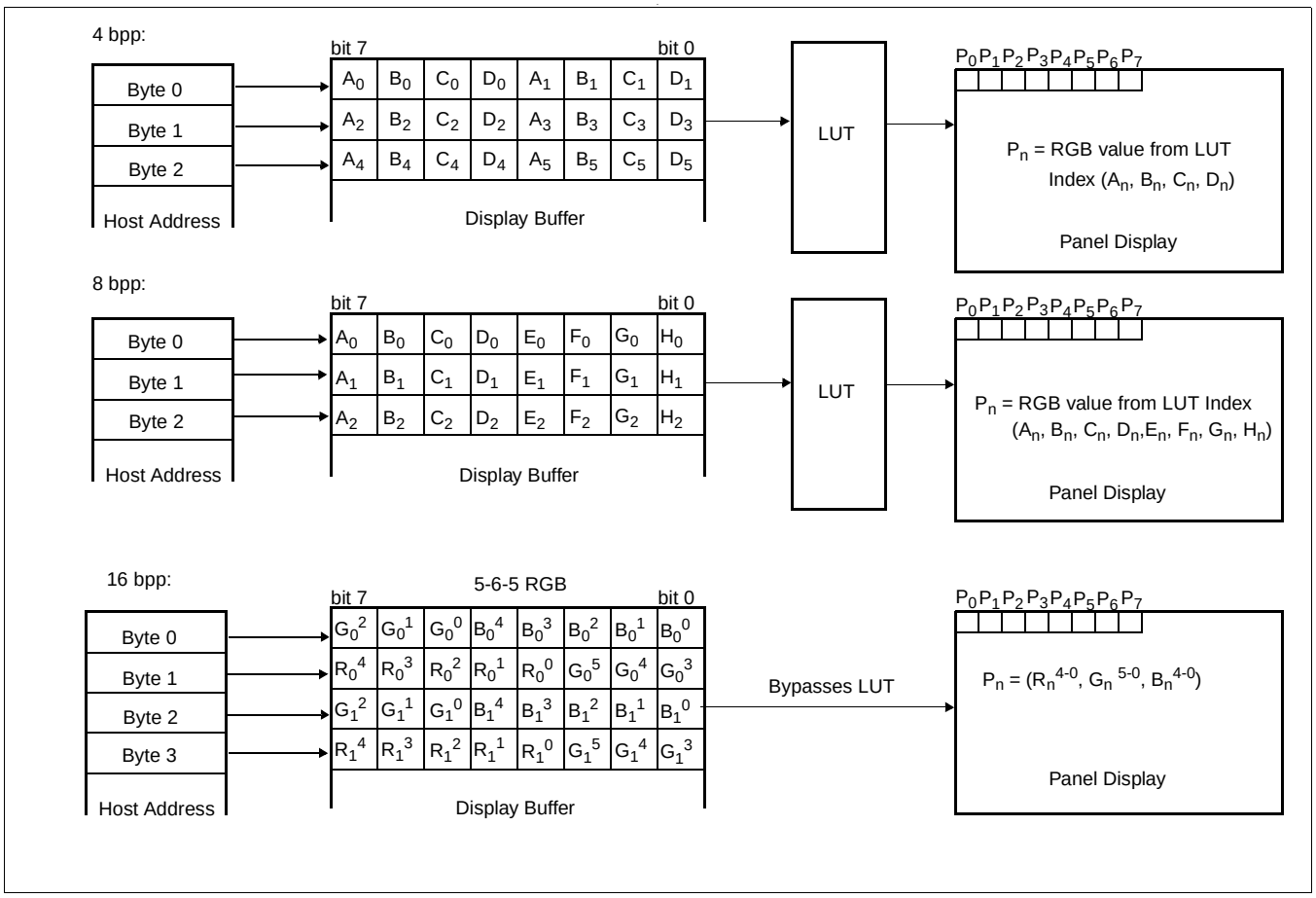



*Figure 11-1: 4/8/16 Bit-per-pixel Format Memory Organization*

**Note**

1. The Host-to-Display mapping shown here is for a little endian system.
2. For the 16 bit-per-pixel format, $R_n$, $G_n$, $B_n$ represent the red, green, and blue color components.

## 11.2 Image Manipulation

The figure below shows how the screen image is stored in the image buffer and positioned on the LCD display. The screen image on the CRT/TV is manipulated similarly. When EISD is enabled (see Section 16, “EPSON Independent Simultaneous Display (EISD)” on page 186), the images on the LCD and on the CRT/TV are independent of each other.

- For LCD: (REG[047h], REG[046h]) define the width of the virtual image.
  For CRT/TV: (REG[067h], REG[066h]) define the width of the virtual image.
- For LCD: (REG[044h], REG[043h], REG[042h]) define the starting word of the displayed image.
  For CRT/TV: (REG[064h], REG[063h], REG[062h]) define the starting word of the displayed image.
- For LCD: REG[048h] defines the starting pixel within the starting word.
  For CRT/TV: REG[068h] defines the starting pixel within the starting word.
- For LCD: REG[032h] defines the width of the LCD display.
  For CRT/TV: REG[050h] defines the width of the CRT/TV display.
- For LCD: (REG[039h], REG[038h]) define the height of the LCD display.
  For CRT/TV: (REG[057h], REG[056h]) define the height of the CRT/TV display.

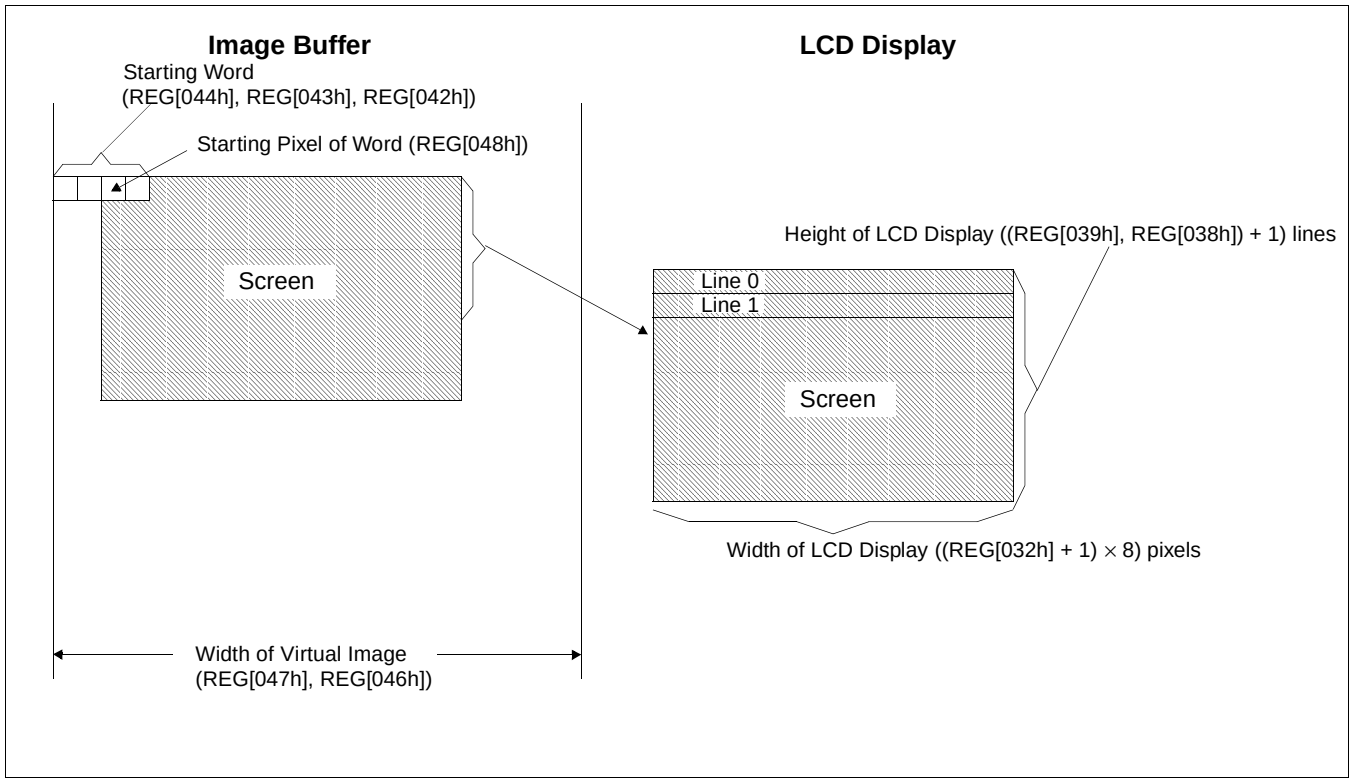



*Figure 11-2: Image Manipulation*

# 12 Look-Up Table Architecture

The following depictions are intended to show the display data output path only.

## 12.1 Monochrome Modes

The green LUT is used for all monochrome modes.

### 4 Bit-Per-Pixel Monochrome Mode

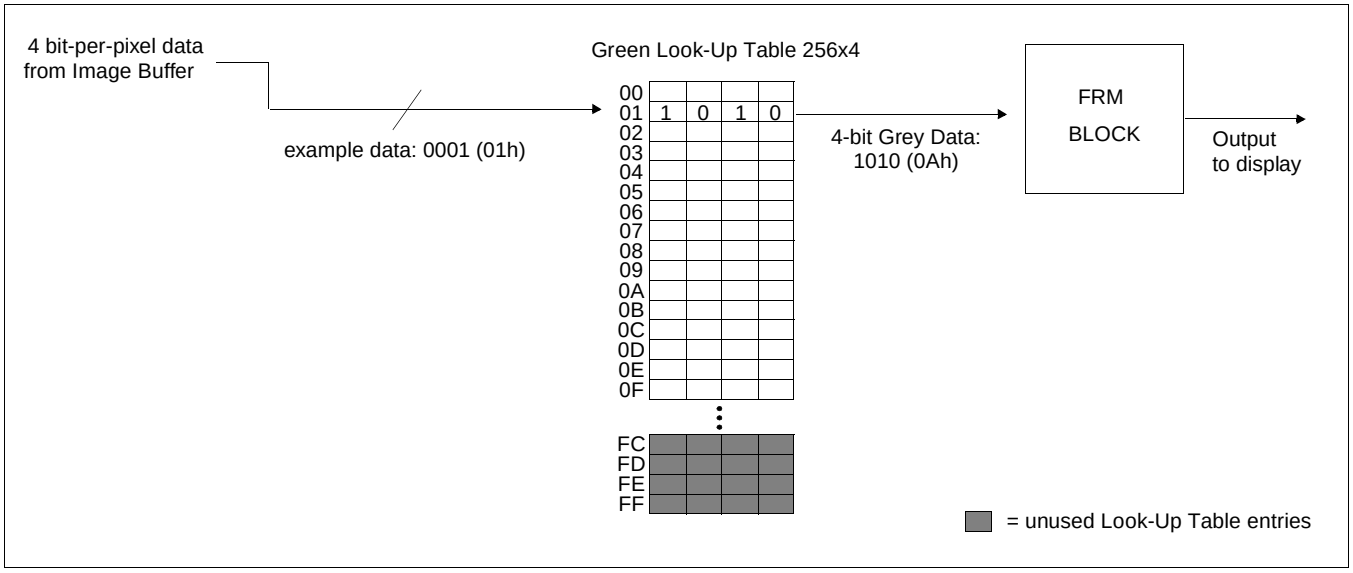



*Figure 12-1: 4 Bit-Per-Pixel Monochrome Mode Data Output Path*

## 8 Bit-Per-Pixel Monochrome Mode

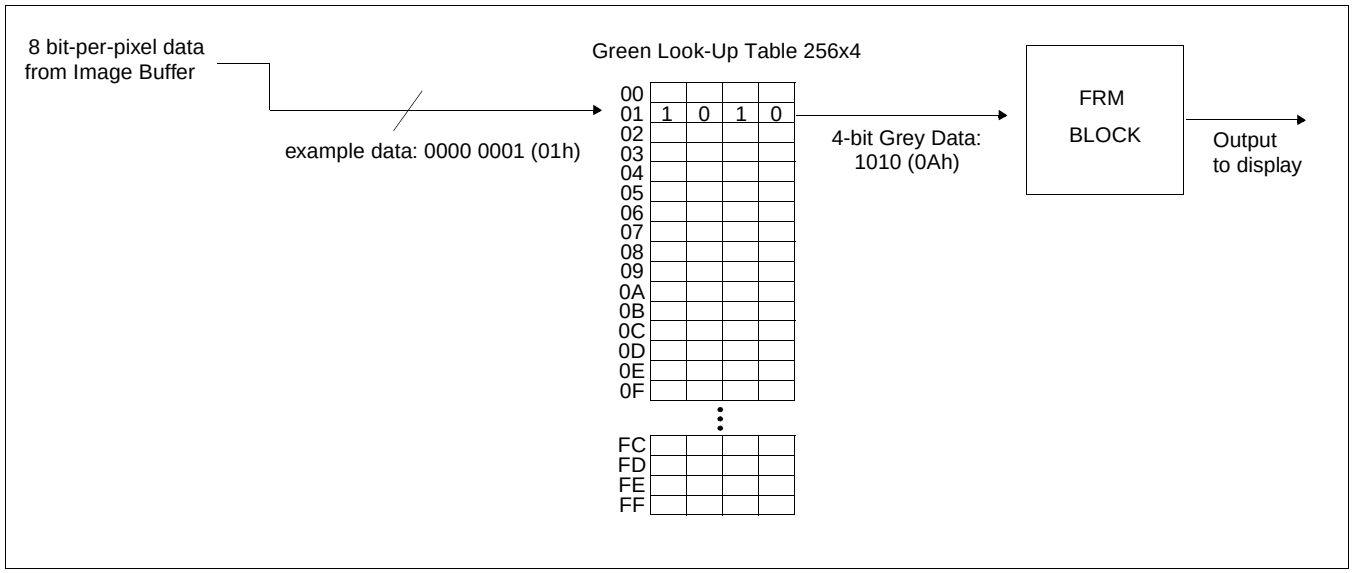



*Figure 12-2: 8 Bit-Per-Pixel Monochrome Mode Data Output Path*

## 16 Bit-Per-Pixel Monochrome Mode

A color depth of 16 bpp is required to achieve 64 gray shades in monochrome mode. In this mode the LUT is bypassed and the green component of the pixel is mapped to the FRM.

# 12.2 Color Modes

## 4 Bit-Per-Pixel Color Mode

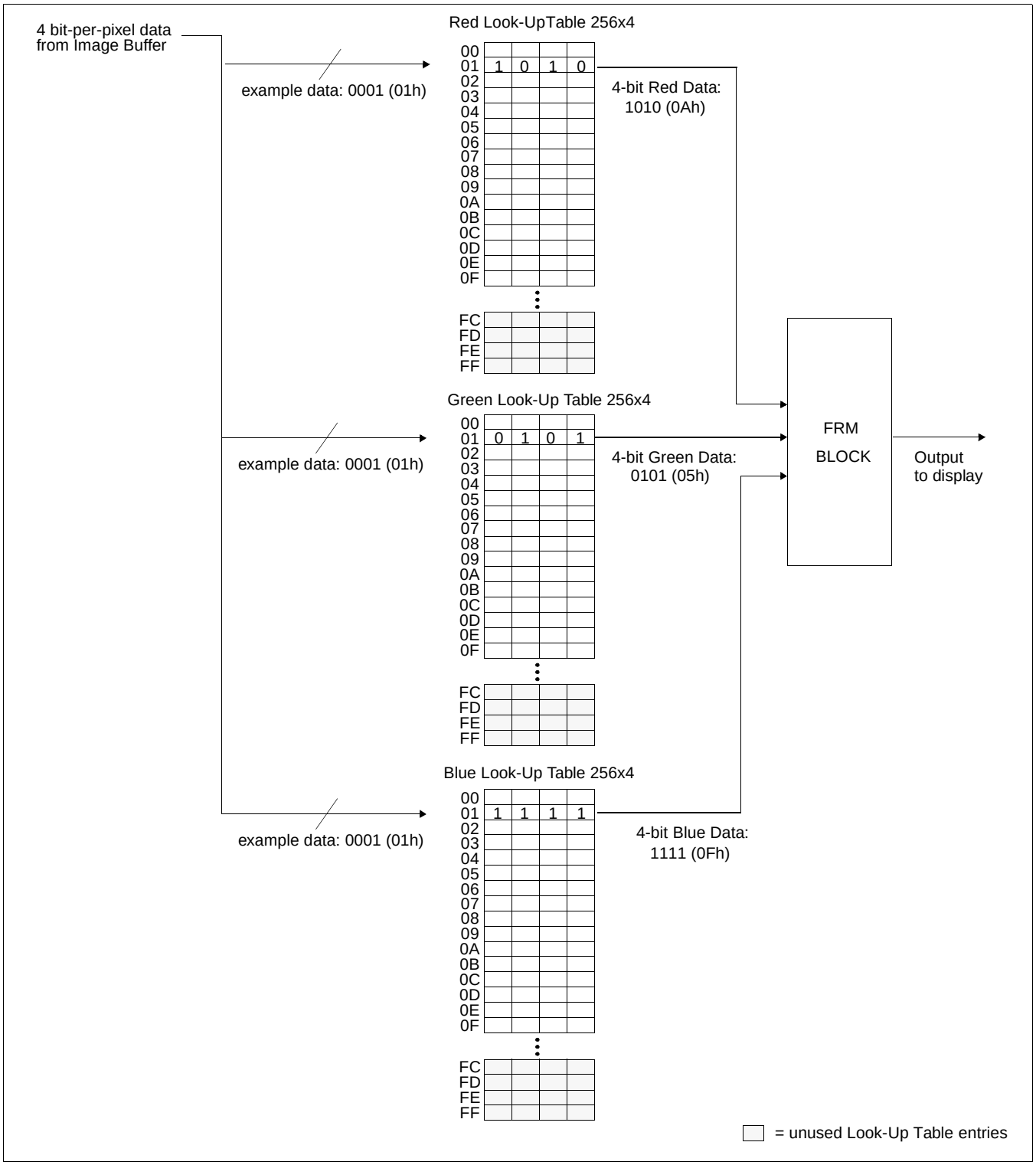



*Figure 12-3: 4 Bit-Per-Pixel Color Mode Data Output Path*

## 8 Bit-Per-Pixel Color Mode

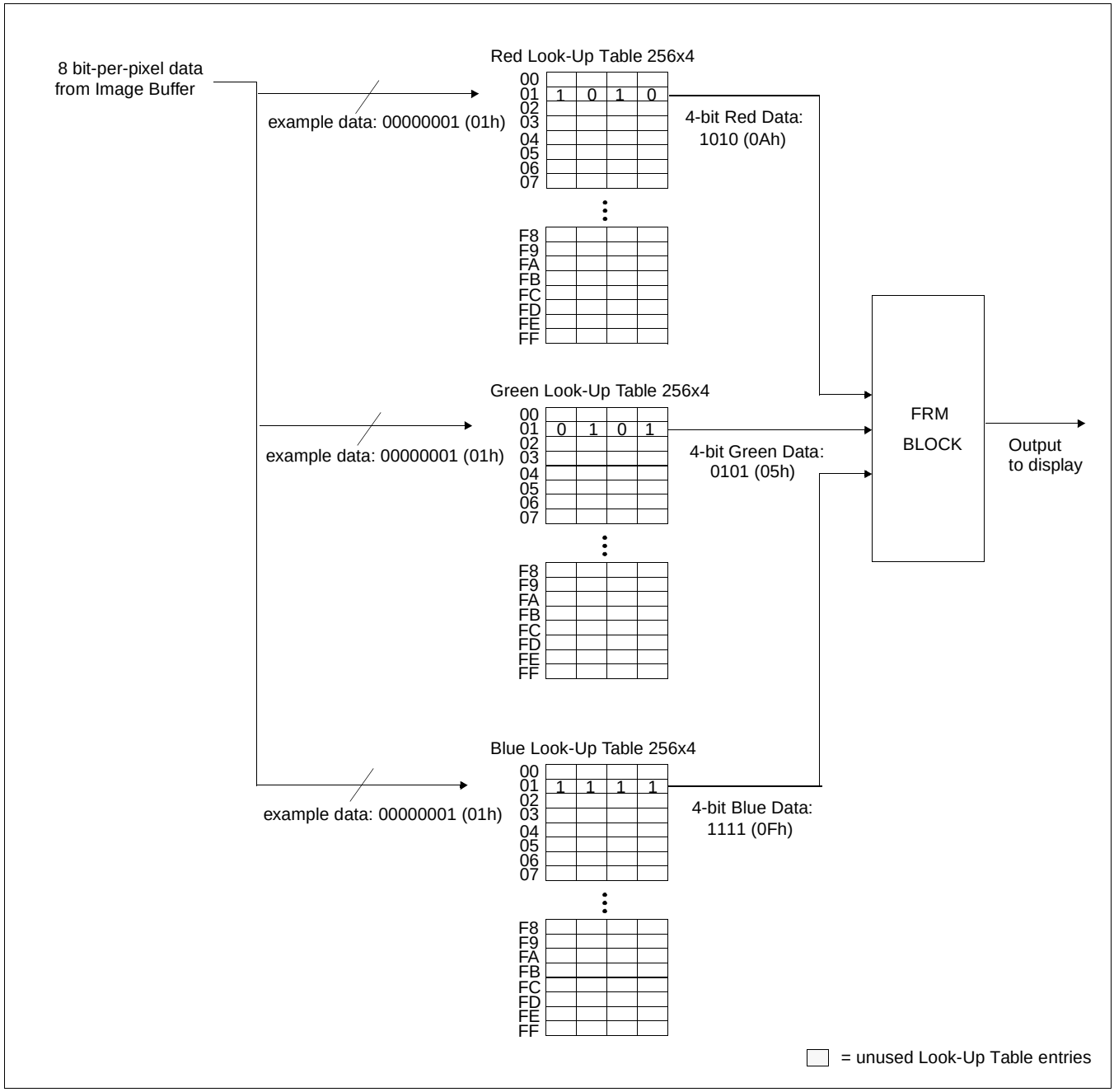



*Figure 12-4: 8 Bit-Per-Pixel Color Mode Data Output Path*

## 16 Bit-Per-Pixel Color Modes

The LUT is bypassed and the color data is directly mapped for this color mode – Section 11, “Display Configuration” on page 159.

# 13 TV Considerations

## 13.1 NTSC/PAL Operation

NTSC or PAL video is supported in either composite or S-video format. Filters may be enabled to reduce the distortion associated with displaying high resolution computer images on an interlaced TV display. The image can be vertically and horizontally positioned on the TV. Additionally, a dedicated Hardware Cursor (independent from the LCD display) is supported.

## 13.2 Clock Source

The required clock frequencies for NTSC/PAL are given in the following table.

*Table 13-1 : Required Clock Frequencies for NTSC/PAL*

| TV Format | Required Clock Frequency |
|---|---|
| NTSC | 14.318180 MHz (3.579545 MHz subcarrier) |
| PAL | 17.734475 MHz (4.43361875 MHz subcarrier) |

## 13.3 Filters

When displaying computer images on a TV, several image distortions are likely to arise:

- cross-luminance distortion.
- cross-chrominance distortion.
- flickering.

These distortions are caused by the high-resolution nature of computer images which typically contain sharp color transitions, and sharp luminance transitions (e.g., high contrast one pixel wide lines and fonts, window edges, etc.). Three filters are available to reduce these distortions.

### 13.3.1 Chrominance Filter (REG[05Bh] bit 5)

The chrominance filter adjusts the color of the TV by limiting the bandwidth of the chrominance signal (reducing cross-luminance distortion). This reduces the “ragged edges” seen at boundaries between sharp color transitions. This filter is controlled using REG[05Bh] bit 5 and is most useful for composite video output.

### 13.3.2 Luminance Filter (REG[05Bh] bit 4)

The luminance filter adjusts the brightness of the TV by limiting the bandwidth of the luminance signal (reducing cross-chrominance distortion). This reduces the “rainbow-like” colors at boundaries between sharp luminance transitions. This filter is controlled using REG[05Bh] bit 4 and is most useful for composite video output.

### 13.3.3 Anti-flicker Filter (REG[1FCh] bits [2:1])

The “flickering” effect seen on interlaced displays is caused by sharp vertical image transitions that occur over one line (1 vertical pixel). For example, one pixel high lines, edges of window boxes, etc. Flickering occurs because these high resolution lines are effectively displayed at half the refresh frequency due to interlacing. The anti-flicker filter averages adjacent lines on the TV display to reduce flickering. This filter is controlled using the Display Mode register (REG[1FCh] bits [2:1]).

**Note**

When TV with anti-flicker filter is enabled, the Flicker Filter Clock Enable bit (REG[18h] bit 7) must be set to 1.

## 13.4 TV Output Levels

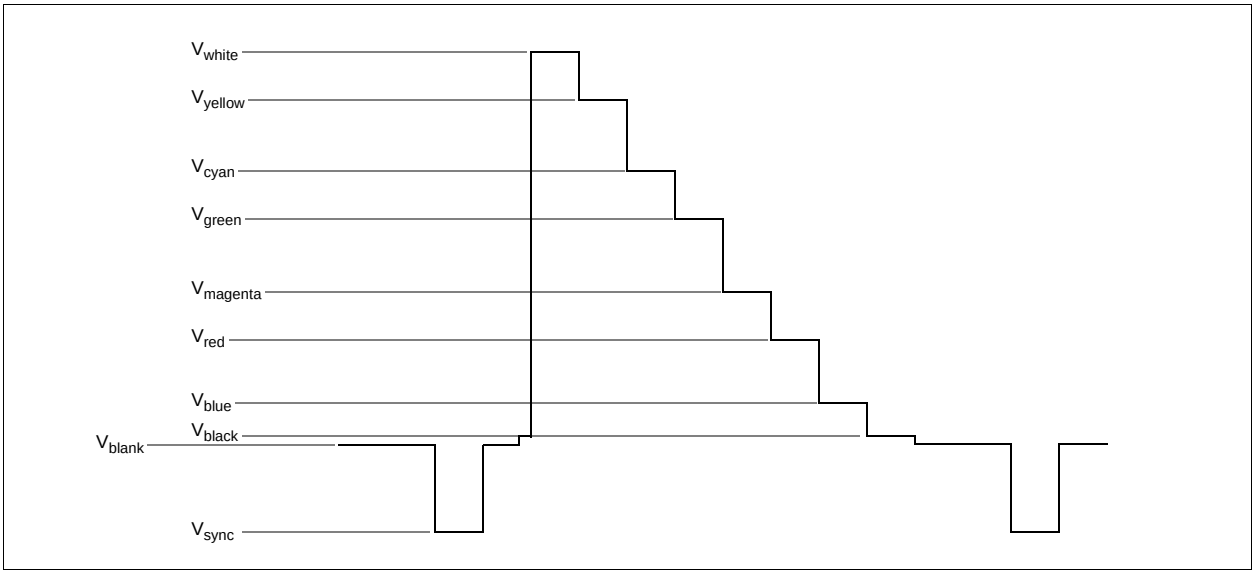



*Figure 13-1: NTSC/PAL SVideo-Y (Luminance) Output Levels*

*Table 13-2 : NTSC/PAL SVideo-Y (Luminance) Output Levels*

| Symbol | Parameter | RGB | NTSC / PAL (mv) | NTSC / PAL (IRE) |
|---|---|---|---|---|
| $V_{white}$ | White | 1F 3F 1F | 996 | 99.5 |
| $V_{yellow}$ | Yellow | 1F 3F 00 | 923 | 89 |
| $V_{cyan}$ | Cyan | 00 3F 1F | 798 | 72 |
| $V_{green}$ | Green | 00 3F 00 | 725 | 62 |
| $V_{magenta}$ | Magenta | 1F 00 1F | 608 | 45 |
| $V_{red}$ | Red | 1F 00 00 | 536 | 35 |
| $V_{blue}$ | Blue | 00 00 1F | 410 | 17 |
| $V_{black}$ | Black | 00 00 00 | 338 | 7.3 |
| $V_{blanking}$ | Blanking | N.A. | 284 | 0 |
| $V_{sync}$ | Sync Tip | N.A. | 0 | -40 |

**Note**

RGB values assume a 16 bpp color depth with 5-6-5 pixel packing.

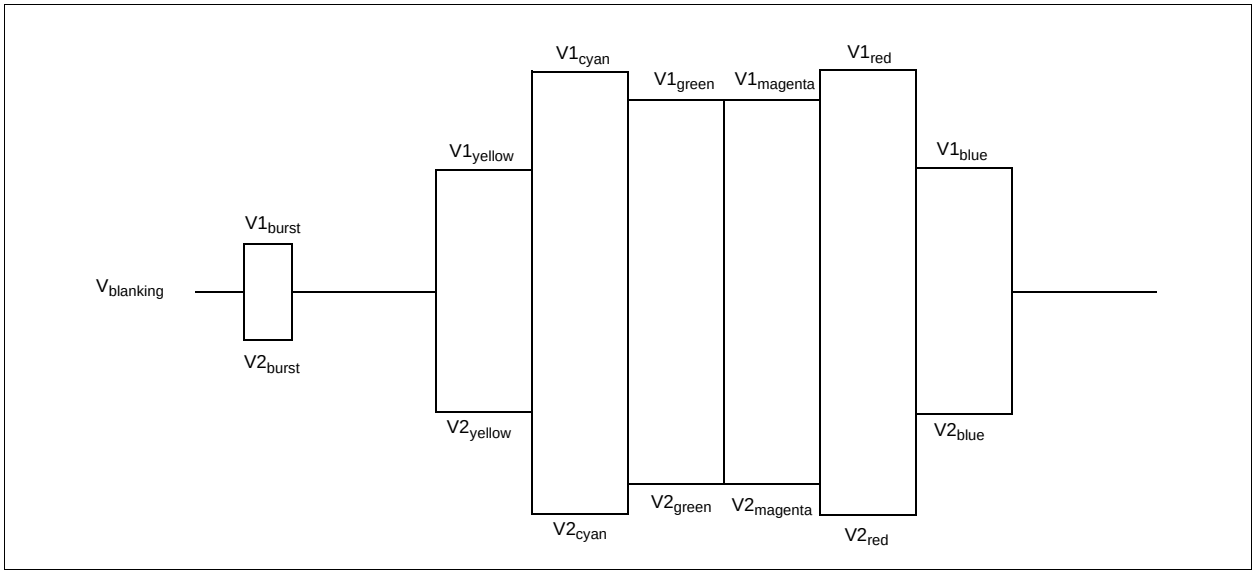



*Figure 13-2: NTSC/PAL SVideo-C (Chrominance) Output Levels*

*Table 13-3 : NTSC/PAL SVideo-C (Chrominance) Output Levels*

| Symbol | Parameter | RGB | NTSC / PAL (mv) | NTSC / PAL (IRE) |
|---|---|---|---|---|
| $V1_{burst}$ | Burst positive peak | N.A. | 552 / 541 | 20 / 18.5 |
| $V1_{yellow}$ | Yellow positive peak | 1F 3F 00 | 700 | 40.8 |
| $V1_{cyan}$ | Cyan positive peak | 00 3F 1F | 815 | 57 |
| $V1_{green}$ | Green positive peak | 00 3F 00 | 751 | 48 |
| $V1_{magenta}$ | Magenta positive peak | 1F 00 1F | 751 | 48 |
| $V1_{red}$ | Red positive peak | 1F 00 00 | 815 | 57 |
| $V1_{blue}$ | Blue positive peak | 00 00 1F | 700 | 40.8 |
| $V_{blanking}$ | Blanking | N.A. | 410 | 0 |
| $V2_{burst}$ | Burst negative peak | N.A. | 268 / 279 | -20 / -18.5 |
| $V2_{yellow}$ | Yellow negative peak | 1F 3F 00 | 121 | -40.8 |
| $V2_{cyan}$ | Cyan negative peak | 00 3F 1F | 5 | -57 |
| $V2_{green}$ | Green negative peak | 00 3F 00 | 70 | -48 |
| $V2_{magenta}$ | Magenta negative peak | 1F 00 1F | 70 | -48 |
| $V2_{red}$ | Red negative peak | 1F 00 00 | 5 | -57 |
| $V2_{blue}$ | Blue negative peak | 00 00 1F | 121 | -40.8 |

**Note**

RGB values assume a 16 bpp color depth with 5-6-5 pixel packing.

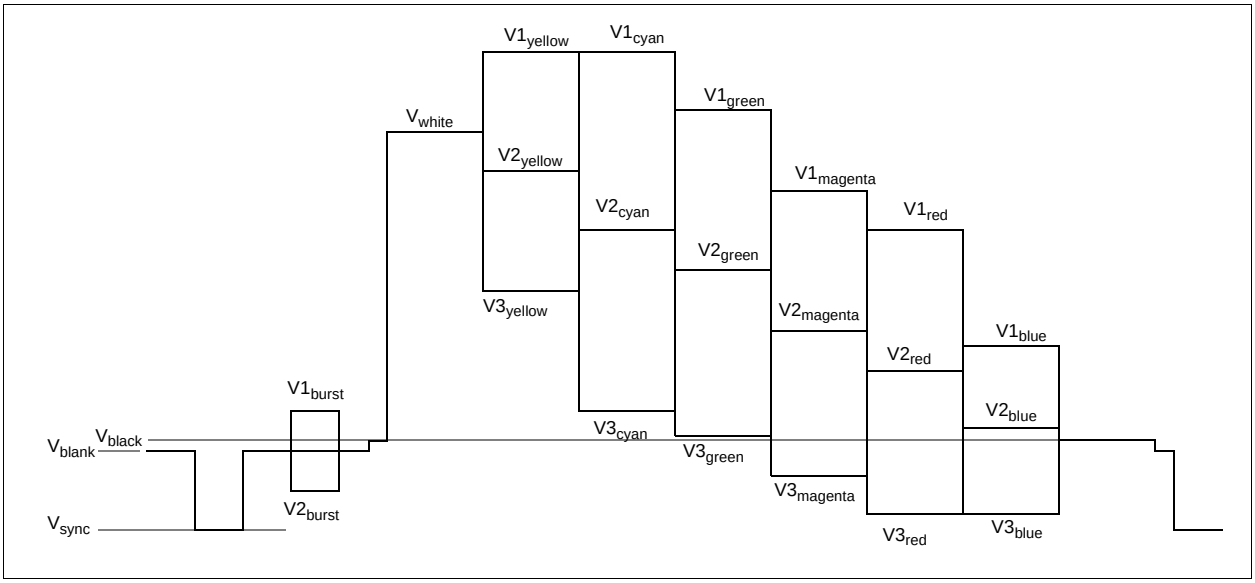



*Figure 13-3: NTSC/PAL Composite Output Levels*

*Table 13-4 : NTSC/PAL Composite Output Levels*

| Symbol | Parameter | RGB | NTSC / PAL (mv) | NTSC / PAL (IRE) |
|---|---|---|---|---|
| $V1_{yellow}$ | Yellow chrominance positive peak | 1F 3F 00 | 1211 | 130 |
| $V1_{cyan}$ | Cyan chrominance positive peak | 00 3F 1F | 1202 | 128 |
| $V1_{green}$ | Green chrominance positive peak | 00 3F 00 | 1065 | 109 |
| $V1_{magenta}$ | Magenta chrominance positive peak | 1F 00 1F | 948 | 93 |
| $V1_{red}$ | Red chrominance positive peak | 1F 00 00 | 939 | 92 |
| $V1_{blue}$ | Blue chrominance positive peak | 00 00 1F | 699 | 58 |
| $V_{white}$ | White luminance level | 1F 3F 1F | 995 | 99 |
| $V2_{yellow}$ | Yellow luminance level | 1F 3F 00 | 923 | 89 |
| $V2_{cyan}$ | Cyan luminance level | 00 3F 1F | 797 | 72 |
| $V2_{green}$ | Green luminance level | 00 3F 00 | 725 | 62 |
| $V2_{magenta}$ | Magenta luminance level | 1F 00 1F | 608 | 45 |
| $V2_{red}$ | Red luminance level | 1F 00 00 | 535 | 35 |
| $V2_{blue}$ | Blue luminance level | 00 00 1F | 411 | 18 |
| $V_{black}$ | Black luminance level | 00 00 00 | 338 | 7.3 |
| $V3_{yellow}$ | Yellow chrominance negative peak | 1F 3F 00 | 634 | 49 |
| $V3_{cyan}$ | Cyan chrominance negative peak | 00 3F 1F | 392 | 15 |
| $V3_{green}$ | Green chrominance negative peak | 00 3F 00 | 384 | 14 |
| $V3_{magenta}$ | Magenta chrominance negative peak | 1F 00 1F | 267 | -2.6 |
| $V3_{red}$ | Red chrominance negative peak | 1F 00 00 | 130 | -22 |
| $V3_{blue}$ | Blue chrominance negative peak | 00 00 1F | 122 | -23 |
| $V_{blank}$ | Blank Level | N.A. | 284 | 0 |
| $V1_{burst}$ | Burst positive peak | N.A. | 426 / 415 | 20 / 18 |
| $V2_{burst}$ | Burst negative peak | N.A. | 142 / 153 | -20 / -19 |
| $V_{sync}$ | Sync Tip | N.A. | 0 | -40 |

**Note**

RGB values assume a 16 bpp color depth with 5-6-5 pixel packing.

### 13.4.1 TV Image Display and Positioning

This section describes how to setup and position an image to be displayed on a TV. Figure 13-4: “NTSC/PAL Image Positioning” shows an image positioned in the TV display with the related programmable parameters. The TV display area is shaded.

The size of the display image determines the register values for the Horizontal Display Period, Horizontal Non-Display Period, Vertical Display Period, and Vertical Non-Display Period. The maximum and minimum values for these registers are given in Table 13-5, “Minimum and Maximum Values for NTSC/PAL TV,” on page 171. The line period and frame period determined by these registers must also satisfy the following equations.

NTSC:

$$(((REG[050]\ bits[6:0]) + 1) \times 8) + (((REG[052]\ bits[5:0]) \times 8) + 6) = 910$$

$$(\{(REG[057]\ bits[1:0]), (REG[056]\ bits[7:0])\} + 1) + ((REG[058]\ bits[6:0]) + 1) \times 2 + 1) = 525$$

PAL:

$$(((REG[050]\ bits[6:0]) + 1) \times 8) + (((REG[052]\ bits[5:0]) \times 8) + 7) = 1135$$

$$(\{(REG[057]\ bits[1:0]), (REG[056]\ bits[7:0])\} + 1) + ((REG[058]\ bits[6:0]) + 1) \times 2 + 1) = 625$$

The HRTC Start Position and VRTC Start Position registers position the image horizontally and vertically. The maximum and minimum register values for these registers are given in Table 13-5, “Minimum and Maximum Values for NTSC/PAL TV”. Increasing the HRTC Start Position moves the image left, while increasing the VRTC Start Position moves the image up.

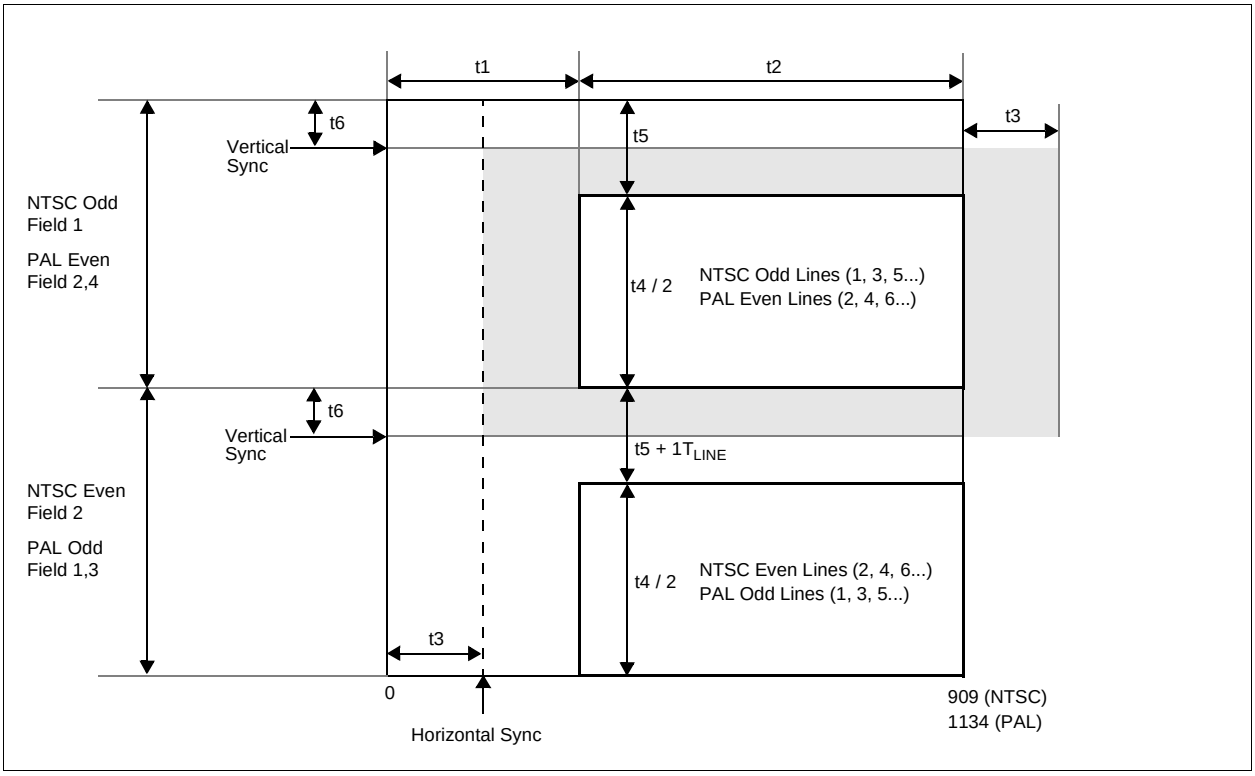



*Figure 13-4: NTSC/PAL Image Positioning*

The maximum Horizontal and Vertical Display Widths shown in Table 13-5, "Minimum and Maximum Values for NTSC/PAL TV" include display areas that are normally hidden by the edges of the TV. The visible display dimensions are shown in Figure 13-5: "Typical Display Dimensions and Visible Display Dimensions for NTSC and PAL" as a guideline. The actual visible display area for a particular television may differ slightly from those dimensions given. Table 13-6, "Register Values for Example NTSC/PAL Images" lists some register values for some example images.

*Table 13-5 : Minimum and Maximum Values for NTSC/PAL TV*

| Symbol | Parameter | Register(s) | NTSC | | PAL | | Units |
|---|---|---|---|---|---|---|---|
| | | | min | max | min | max | |
| t1 | TV Horizontal Non-Display Period | 52 | 158 | 510 | 215 | 511 | $T_{4SC}$ |
| t2 | TV Horizontal Display Width | 50 | 400 | 752 | 624 | 920 | $T_{4SC}$ |
| t3 | TV HRTC Start Position | 53 | 25 | t2 - 158 | 25 | t2 - 215 | $T_{4SC}$ |
| t4 | TV Vertical Display Height | 57, 56 | 270 | 484 | 370 | 572 | $T_{LINE}$ |
| t5 | TV Vertical Non-Display Period | 58 | 20 (21) | 127 (128) | 26 (27) | 127 (128) | $T_{LINE}$ |
| t6 | TV Vertical Start Position | 59 | 0 | t5 - 20 | 0 | t5 - 26 | $T_{LINE}$ |

**Note**

The TV Vertical Non-Display Period (t5) varies by 1 line depending on the field that it follows.

**Note**

For NTSC panels the minimum and maximum values will vary for each application.

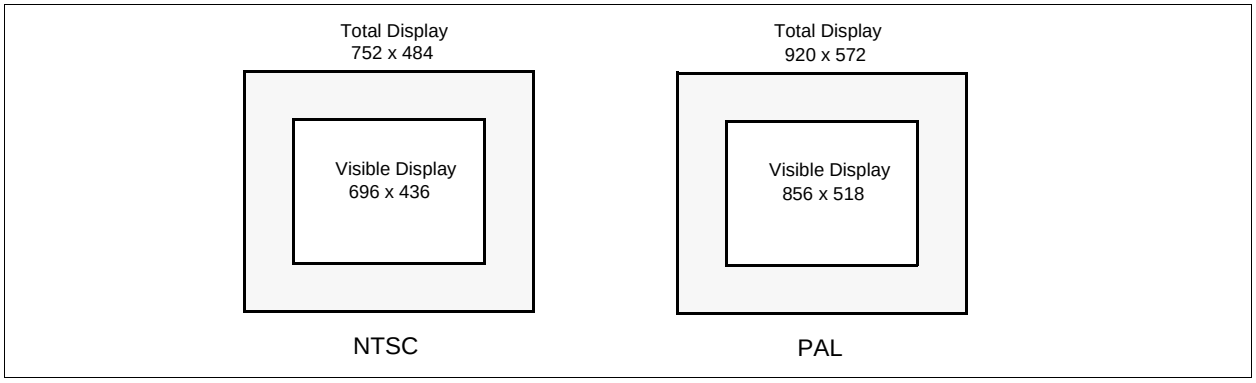



*Figure 13-5: Typical Display Dimensions and Visible Display Dimensions for NTSC and PAL*

**Note**

For most implementations, the visible display does not equal the total display. The total display dimensions and the visible display dimensions must be determined for each specific implementation.

*Table 13-6 : Register Values for Example NTSC/PAL Images*

| Parameter | Register | NTSC | | | PAL | | | |
|---|---|---|---|---|---|---|---|---|
| | | 752x484 | 696x436 | 640x480 | 920x572 | 856x518 | 800x572 | 640x480 |
| TV Horizontal Display Width | 50 | 5Dh | 56h | 4Fh | 72h | 6Ah | 63h | 4Fh |
| TV Horizontal Non-Display Period | 52 | 13h | 1Ah | 21h | 1Ah | 22h | 29h | 3Dh |
| TV HRTC Start Position | 53 | 02h | 04h | 09h | 02h | 05h | 09h | 15h |
| TV Vertical Display Height | 57 | 01h | 01h | 01h | 02h | 02h | 02h | 01h |
| | 56 | E3h | B3h | DFh | 3Bh | 05h | 3Bh | DFh |
| TV Vertical Non-Display Period | 58 | 13h | 2Bh | 15h | 19h | 34h | 19h | 47h |
| TV Vertical Start Position | 59 | 00h | 0Ch | 00h | 00h | 0Dh | 00h | 17h |

## 13.4.2 TV Cursor Operation

See Section 14, “Ink Layer/Hardware Cursor Architecture” on page 173.

# 14 Ink Layer/Hardware Cursor Architecture

## 14.1 Ink Layer/Hardware Cursor Buffers

The Ink Layer/Hardware Cursor buffers contain formatted image data for the Ink Layer or Hardware Cursor. There may be several Ink Layer/Hardware Cursor images stored in the display buffer but only one may be active at any given time. The active Ink Layer/Hardware Cursor buffer is selected by the Ink/Cursor Start Address register (REG[071h] for LCD, REG[081h] for CRT/TV). This register defines the start address for the active Ink/Cursor buffer. The Ink/Cursor buffer must be positioned where it does not conflict with the image buffer and dual panel buffer. The start address for the Ink/Cursor buffer is programmed as shown in the following table.

*Table 14-1 : Ink/Cursor Start Address Encoding*

| Ink/Cursor Start Address Bits [7:0] | Start Address (Bytes) | Comments |
|---|---|---|
| 0 | 1280K - 1024 | This default value is suitable for a Hardware Cursor when there is no dual panel buffer. |
| n = 160...1 | 1280K - (n × 8192) | These positions can be used to:<br>• position an Ink Layer buffer at the top of the display buffer;<br>• position an Ink Layer buffer between the image and dual panel buffers;<br>• position a Hardware Cursor buffer between the image and dual panel buffers;<br>• select from a multiple of Hardware Cursor buffers. |
| n = 255...161 | Invalid | |

The Ink/Cursor image is stored contiguously. The address offset from the starting word of line *n* to the starting word of line *n+1* is calculated as follows:

LCD Ink Address Offset (words) = REG[032h] + 1
CRT/TV Ink Address Offset (words) = REG[050h] + 1
LCD or CRT/TV Cursor Address Offset (words) = 8

## 14.2 Ink/Cursor Data Format

The Ink/Cursor image is always 2 bit-per-pixel. The following diagram shows the Ink/Cursor data format for a little endian system.

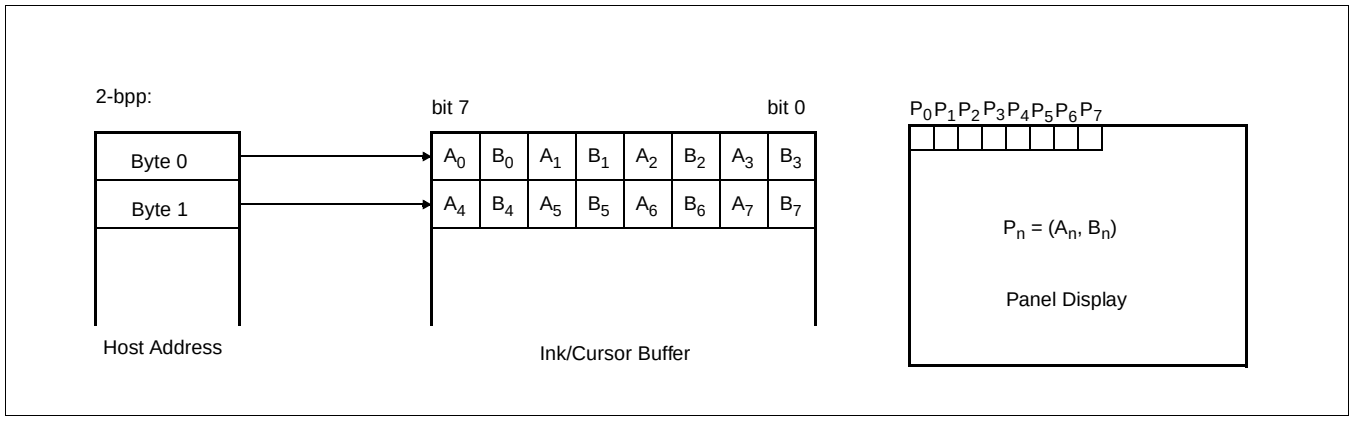



*Figure 14-1: Ink/Cursor Data Format*

The image data for pixel n, ($A_n$,$B_n$), selects the color for pixel n as follows.

*Table 14-2 : Ink/Cursor Color Select*

| ($A_n$,$B_n$) | Color | Comments |
|---|---|---|
| 00 | Color 0 | Ink/Cursor Color 0 Register, (REG[078h], REG[077h], REG[076h] for LCD, REG[088h], REG[087h], REG[086h] for CRT/TV) |
| 01 | Color 1 | Ink/Cursor Color 1 Register, (REG[07Ah], REG[07Bh],REG[07Ah] for LCD, REG[08Ah], REG[08Bh], REG[08Ah] for CRT/TV) |
| 10 | Background | Ink/Cursor is transparent – show background |
| 11 | Inverted Background | Ink/Cursor is transparent – show inverted background |

# 14.3 Ink/Cursor Image Manipulation

## 14.3.1 Ink Image

The Ink image should always start at the top left pixel (i.e. Cursor X Position and Cursor Y Position registers should always be set to zero). The width and height of the ink image are automatically calculated to completely cover the display.

## 14.3.2 Cursor Image

The Cursor image size is always 64 x 64 pixels. The Cursor X Position and Cursor Y Position registers specify the position of the top left pixel. The following diagram shows how to position an unclipped cursor.

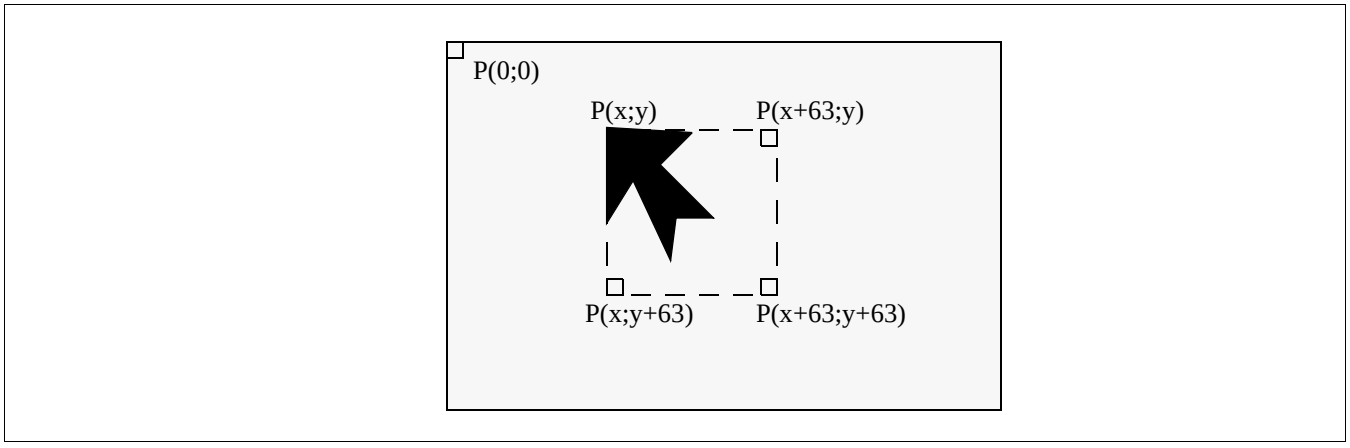



*Figure 14-2: Unclipped Cursor Positioning*

where

For LCD:
x = (REG[073h] bits [1:0], REG[072h]) **and** REG[073h] bit 7 = 0
y = (REG[075h] bits [1:0], REG[074h]) **and** REG[075h] bit 7 = 0

For CRT/TV:
x = (REG[083h] bits [1:0], REG[082h]) **and** REG[083h] bit 7 = 0
y = (REG[085h] bits [1:0], REG[084h]) **and** REG[085h] bit 7 = 0

The following diagram shows how to position a cursor that is clipped at the top and left sides of the display.

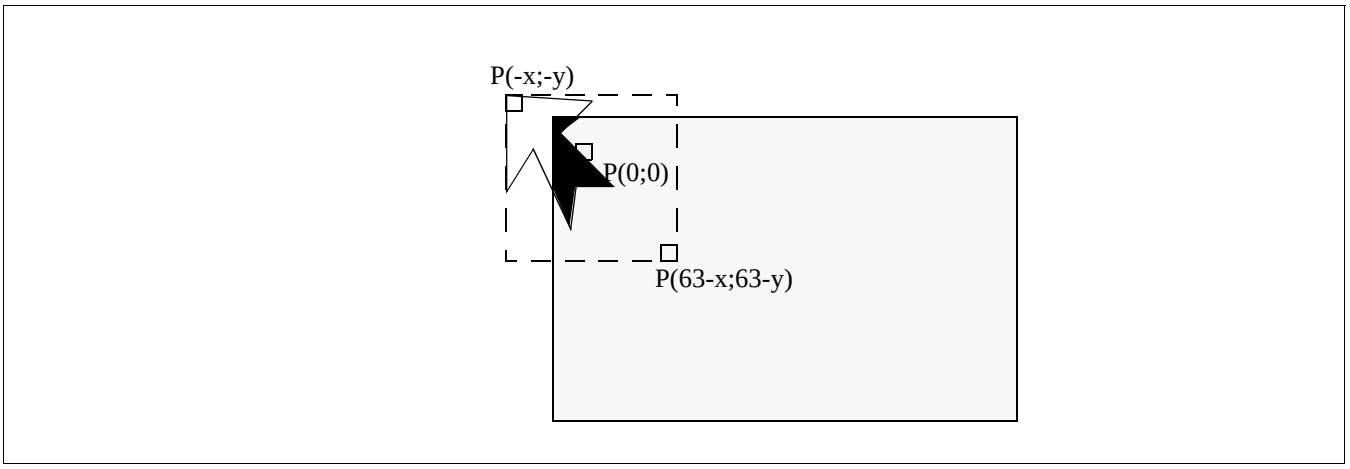



*Figure 14-3: Clipped Cursor Positioning*

where

For LCD:
x = (REG[073h] bits [1:0], REG[072h]) <= 63 **and** REG[073h] bit 7 = 1
y = (REG[075h] bits [1:0], REG[074h]) <= 63 **and** REG[075h] bit 7 = 1

For CRT/TV:
x = (REG[083h] bits [1:0], REG[082h]) <= 63 **and** REG[083h] bit 7 = 1
y = (REG[085h] bits [1:0], REG[084h]) <= 63 **and** REG[085h] bit 7 = 1

# 15 SwivelView™

## 15.1 Concept

Most computer displays are refreshed in landscape – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView is designed to rotate the displayed image on an LCD by 90°, 180°, or 270° in a clockwise direction. 90° rotation is also available on CRT.

The rotation is done in hardware and is transparent to the user for all display buffer reads and writes. By processing the rotation in hardware, SwivelView offers a performance advantage over software rotation of the displayed image.

## 15.2 90° SwivelView

90° SwivelView uses a $1024 \times 1024$ pixel virtual window. The following figures show how the display buffer memory map changes in 90° SwivelView. The display is refreshed in the following sense: C–A–D–B. The application image is written to the S1D13806 in the following sense: A–B–C–D. The S1D13806 rotates and stores the application image in the following sense: C–A–D–B, the same sense as display refresh.

The user can read/write to the display buffer naturally, without the need to rotate the image first in software. The registers that control the panning and scrolling of the panel window are designed for a landscape window. However, it is still possible to pan and scroll the portrait window in 90° SwivelView, but the user must program these registers somewhat differently (See Section 15.2.1, “Register Programming” on page 178).

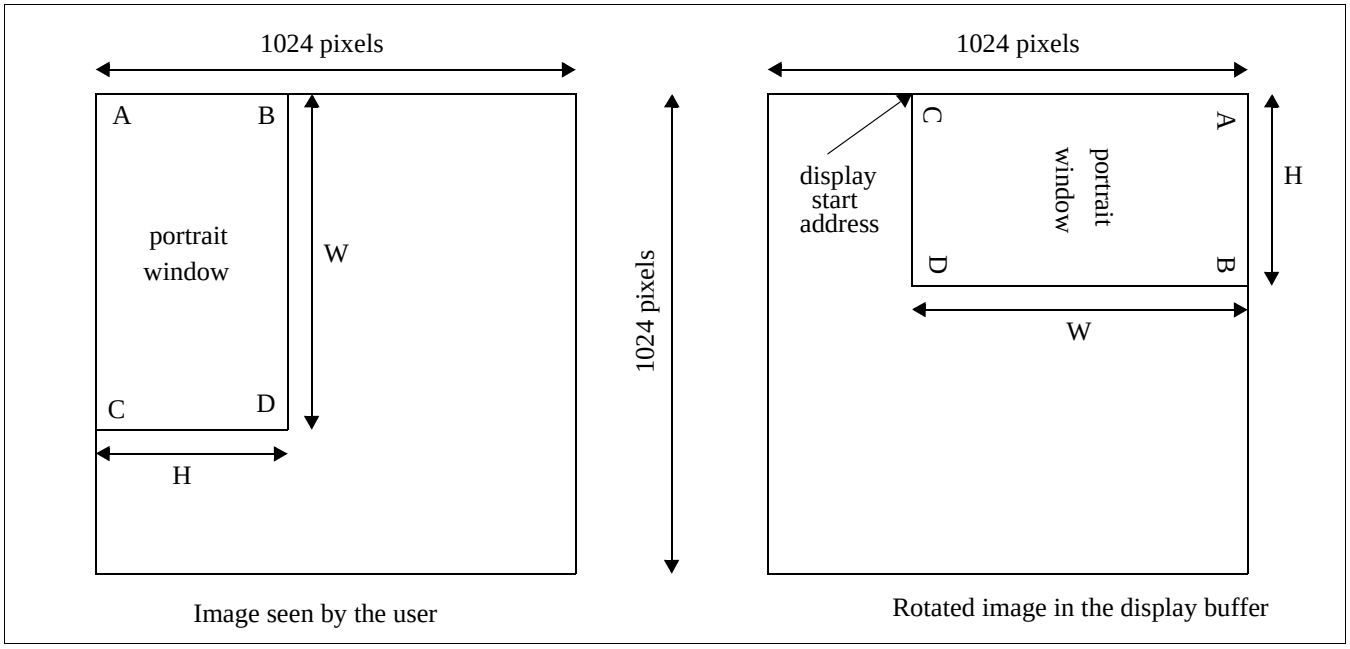



*Figure 15-1: Relationship Between Screen Image and 90° Rotated Image in the Display Buffer*

**Note**

W is the width of the LCD panel/CRT in number of pixels, (or the height of the portrait window in number of lines).
H is the height of the LCD panel/CRT in number of lines, (or the width of the portrait window in number of pixels).

**Note**

The image must be written with a 1024 pixel offset between adjacent lines (1024 bytes for 8 bpp color depth or 2048 bytes for 16 bpp color depth) and the display start address must be calculated (see below).

## 15.2.1 Register Programming

#### Enabling 90° Rotation on CPU Read/Write to Display Buffer

Set SwivelView Enable bits 1:0 to 01b. All CPU accesses to the display buffer are translated to provide 90° clockwise rotation of the display image.

#### Memory Address Offset

The LCD/CRT Memory Address Offset register (REG[046h], REG[047h] for LCD, or REG[066h], REG[067h] for CRT) must be set for a 1024 pixel offset:

LCD/CRT Memory Address Offset (words)

| | |
|---|---|
| = 1024 | for 16 bpp color depth |
| = 512 | for 8 bpp color depth |

#### Display Start Address

As seen in Figure 15-1: “Relationship Between Screen Image and 90° Rotated Image in the Display Buffer” on page 178, the Display Start Address is determined by the location of the image corner “C”, and it is generally non-zero. The LCD/CRT Display Start Address register (REG[042h], REG[043h], REG[044h] for LCD, or REG[062h], REG[063h], REG[064h] for CRT) must be set accordingly.

LCD/CRT Display Start Address (words)
= (1024 - W) for 16 bpp color depth
= (1024 - W) / 2 for 8 bpp color depth

where W is the width of the panel in number of pixels.

#### Horizontal Panning

Horizontal panning is achieved by changing the LCD/CRT Display Start Address register:

- Increase/decrease LCD/CRT Display Start Address register by 1024 (16 bpp color depth) or 512 (8 bpp color depth) pans the display window to the right/left by 1 pixel.

The amount the display window can be panned to the right is limited to 1024 pixels and limited by the amount of physical memory installed.

#### Vertical Scrolling

Vertical scrolling is achieved by changing the LCD/CRT Display Start Address register and/or the LCD/CRT Pixel Panning register:

- Increment/decrement LCD/CRT Display Start Address register in 8 bpp color depth scrolls the display window up/down by 2 lines.
- Increment/decrement LCD/CRT Display Start Address register in 16 bpp color depth scrolls the display window up/down by 1 line.
- Increment/decrement LCD/CRT Pixel Panning register in 8 bpp color depth scrolls the display window up/down by 1 line.

### 15.2.2 Physical Memory Requirement

Because the user must now deal with a virtual image of 1024×1024, the amount of image buffer required for a particular display mode has increased. The minimum amount of image buffer required is:

Minimum Required Image Buffer (bytes)
= $(1024 \times H) \times 2$ for 16 bpp color depth
= $(1024 \times H)$ for 8 bpp color depth

where H is the height of the panel in number of lines.

This minimum amount is required to display a 90° SwivelView image without panning; scrolling, however, is permissible. The degree an image can be panned depends on the amount of physical memory installed and how much of that is used by the dual panel buffer, Ink Layer, or Hardware Cursor. An image cannot be panned outside the 1024×1024 virtual display. Often it cannot be panned within the entire virtual display because part of the virtual display memory may be taken up by the dual panel buffer, Ink Layer, Hardware Cursor, or even the CRT/TV display buffer.

The dual panel buffer is used for dual panel mode and has the following memory requirements.

Dual Panel Buffer (bytes)

| | |
|---|---|
| $=(W \times H) / 4$ | for color mode |
| $=(W \times H) / 16$ | for monochrome mode |

where W is the width of the panel in number of pixels, and H is the height of the panel in number of lines.

The dual panel buffer is always located at the end of the physical memory.

The Hardware Cursor or Ink Layer also takes up memory. If this memory is > 1KB, it must be located at an 8KB boundary, otherwise it may be located at the last 1KB area. The Hardware Cursor or Ink Layer must not overlap the image buffer or the dual panel buffer.

Even though the virtual display is 1024×1024 pixels, the actual panel window is always smaller. Thus it is possible for the display buffer to be smaller than the virtual display but large enough to fit both the required image buffer and the dual panel buffer. This situation limits the maximum “accessible” horizontal virtual size as follows.

Maximum Accessible Horizontal Virtual Size (pixels)

= (Physical Memory - Dual Panel Buffer - Ink Layer) / 2048 for 16 bpp color depth
= (Physical Memory - Dual Panel Buffer - Ink Layer) / 1024 for 8 bpp color depth

For example, a 800×600 TFT panel running a color depth of 16 bpp requires 1200K byte of image buffer, 0K byte of dual panel buffer memory and 0K byte of ink layer memory (ink layer is not supported in this configuration, see Table 15-1, “Memory Size Required for SwivelView 90° and 270°,” on page181) . The virtual display size is 2048×2048 = 2M byte. This display can still be supported by the 1280K embedded DRAM even though it is smaller than the 2M byte virtual display because the size of the embedded DRAM is larger than the 1200K byte minimum required image buffer. The maximum accessible horizontal virtual size is = (1280K byte - 0K byte - 0K byte) / 2048 = 640. The programmer therefore has room to pan the portrait window to the right by 640 - 600 = 40 pixels. The programmer also should not read/write to the memory beyond the maximum accessible horizontal virtual size because that memory is either reserved for the dual panel buffer or not associated with any real memory at all.

The following table summarizes the SwivelView 90° and 270° memory requirements for different panel sizes and display modes. Note that the S1D13806 memory size is 1280K byte. The calculation of the minimum required image buffer size is based on the image buffer and the dual panel buffer only. As noted in the table, the memory requirements of the Hardware Cursor/Ink Layer are not taken into account. The Hardware Cursor requires 1K byte of memory and the 2-bit Ink Layer requires (W × H) / 4 bytes of memory. Both the Hardware cursor and Ink Layer must reside at 8K byte boundaries, but only one is supported at a time. The following table shows only one possible Hardware Cursor/Ink Layer location – at the highest possible 8K byte boundary below the dual panel buffer which is always at the top.

*Table 15-1 : Memory Size Required for SwivelView 90° and 270°*

| Panel Size | Panel Type | | Color Depth | Image Buffer Size | Dual Panel Buffer Size | Ink/Cursor Buffer Size | Ink/Cursor Location |
|---|---|---|---|---|---|---|---|
| 320 × 240 | Single | Color | 8 bpp | 240KB | 0KB | 18.75KB/1KB | 1256KB/1279KB |
| | | | 16 bpp | 480KB | | | |
| | | Mono | 8 bpp | 240KB | | | |
| | | | 16 bpp | 480KB | | | |
| 640 × 480 | Single | Color | 8 bpp | 480KB | 0KB | 75KB/1KB | 1200KB/1279KB |
| | | | 16 bpp | 960KB | | | |
| | | Mono | 8 bpp | 480KB | | | |
| | | | 16 bpp | 960KB | | | |
| | Dual | Color | 8 bpp | 480KB | 75KB | | 1128KB/1200KB |
| | | | 16 bpp | 960KB | | | |
| | | Mono | 8 bpp | 480KB | 18.75KB | | 1184KB/1256KB |
| | | | 16 bpp | 960KB | | | |
| 800 × 600 | Single | Color | 8 bpp | 600KB | 0KB | 117.19KB/1KB | 1160KB/1279KB |
| | | | 16 bpp | 1200KB | | | --/1279KB |
| | | Mono | 8 bpp | 600KB | | | 1160KB/1279KB |
| | | | 16 bpp | 1200KB | | | --/1279KB |
| | Dual | Color | 8 bpp | 600KB | 117.19KB | | 1040KB/1160KB |
| | | | 16 bpp[1] | Not Supported | | | |
| | | Mono | 8 bpp | 600KB | 29.30KB | | --/1248KB |
| | | | 16 bpp | 1200KB | | | |

**Note**

1. 800x600 color 16bpp dual panel is not supported as there is not enough memory to support the Dual Panel Buffer.

**Note**

Where KB = 1024 bytes, and MB = 1024K bytes.

### 15.2.3 Limitations

The following limitations apply to 90° SwivelView:

- Only 8/16 bpp color depths are supported – 4 bpp color depth is not supported.
- Hardware cursor and ink images are not rotated – software rotation must be used. SwivelView Enable bit 0 must be set to 0 when the user is accessing the Hardware Cursor or the Ink Layer buffer.
- For 90° SwivelView modes, BitBLT (Bit Block Transfer) operations are still supported. However, the BitBLT data must first be rotated by software. For further information, refer to the *S1D13806 Programmers Notes And Examples*, document number X28B-G-003-xx.

## 15.3 180° SwivelView

180° SwivelView is where the image is simply **displayed** 180° clockwise rotated. For 180° SwivelView a virtual window is not required and all color depths (4/8/16 bpp) are supported.

### 15.3.1 Register Programming

#### Reverse Display Buffer Fetching Address Direction

Set SwivelView Enable bits 1:0 to 10b. During screen refresh, the direction of the address for display buffer fetching is reversed. This setting does not affect CPU to display buffer access in any way.

#### Display Start Address

The Display Start Address must be programmed to be at the bottom-right corner of the image, since the display is now refreshed in the reverse direction. The LCD Display Start Address register (REG[042h], REG[043h], REG[044h]) must be set accordingly.

LCD Display Start Address (words)

$= (MA\_Offset \times H) - (MA\_Offset - W) - 1$ for 16 bpp color depth
$= (MA\_Offset \times H) - (MA\_Offset - W/2) - 1$ for 8 bpp color depth
$= (MA\_Offset \times H) - (MA\_Offset - W/4) - 1$ for 4 bpp color depth

where H is the height of the panel in number of lines, W is the width of the panel in number of pixels, and MA_Offset is the LCD Memory Address Offset.

#### Horizontal Panning

Horizontal panning works in the same way as when SwivelView is not enabled, except that the effect of the LCD Pixel Panning register is reversed:

- Increment/decrement LCD Display Start Address register pans the display window to the right/left.
- Increment/decrement LCD Pixel Panning register pans the display window to the left/right.

#### Vertical Panning

Vertical panning works in the same way as when SwivelView is not enabled:

- Increase/decrease LCD Display Start Address register by one memory address offset scrolls the display window down/up by 1 line.

### 15.3.2 Physical Memory Requirement

180° SwivelView mode requires the same physical memory as 0° SwivelView (un-rotated display).

### 15.3.3 Limitations

The following limitations apply to 180° SwivelView:

- Hardware Cursor and Ink Layer images are not rotated – software rotation must be used.
- CRT/TV mode is not supported.
- For 180° SwivelView modes, BitBLT (Bit Block Transfer) operations are supported normally. For further information, refer to the *S1D13806 Programmers Notes And Examples*, document number X28B-G-003-xx.

## 15.4 270° SwivelView

270° SwivelView is where the image is displayed 270° clockwise rotated. A $1024 \times 1024$ pixel virtual window is required as in 90° SwivelView. See Figure 15-1: “Relationship Between Screen Image and 90° Rotated Image in the Display Buffer” on page 178.

## 15.4.1 Register Programming

#### Enabling 270° Rotation on CPU Read/Write to Display Buffer

Set SwivelView Enable bits 1:0 to 11b.

The LCD Memory Address Offset register (REG[046h], REG[047h]) must be set for a 1024 pixel offset.

LCD Memory Address Offset (words)

| | |
|---|---|
| = 1024 | for 16 bpp color depth |
| = 512 | for 8 bpp color depth |

#### Display Start Address

The Display Start Address must be programmed to be at the bottom-right corner of the image, since the display is now refreshed in the reverse direction. The LCD Display Start Address register (REG[042h], REG[043h], REG[044h]) must be set accordingly.

LCD Display Start Address (words)

$$= ((\text{LCD Memory Address Offset}) \times H) - 1$$

where H is the height of the panel in number of lines.

#### Horizontal Panning

Horizontal panning is achieved by changing the LCD Display Start Address register. It works in the same way as in 90° SwivelView mode:

- Increase/decrease LCD Display Start Address register by 1024 (16 bpp color depth) or 512 (8 bpp color depth) pans the display window to the right/left by 1 pixel.

The amount the display window can be panned to the right is limited to 1024 pixels and limited by the amount of physical memory installed.

#### Vertical Scrolling

Vertical scrolling is achieved by changing the LCD Display Start Address register and/or the LCD Pixel Panning register. It works in the same way as in 90° SwivelView mode, except that the effect of the LCD Pixel Panning register is reversed:

- Increment/decrement LCD Display Start Address register in 8 bpp color depth scrolls the display window up/down by 2 lines.
- Increment/decrement LCD Display Start Address register in 16 bpp color depth scrolls the display window up/down by 1 line.
- Increment/decrement LCD Pixel Panning register in 8 bpp color depth scrolls the display window down/up by 1 line.

### 15.4.2 Physical Memory Requirement

270° SwivelView mode has the same physical memory requirement as in 90° SwivelView mode. See Section 15.2.2, “Physical Memory Requirement” on page 179.

### 15.4.3 Limitations

The following limitations apply to 270° SwivelView:

- Only 8/16 bpp color depths are supported – 4 bpp color depth is not supported.
- Hardware Cursor and Ink Layer images are not rotated – software rotation must be used. SwivelView Enable bit 0 must be set to 0 when the user is accessing the Hardware Cursor or the Ink Layer memory.
- CRT/TV mode is not supported. SwivelView Enable bit 0 must be set to 0 when the user is accessing the CRT/TV display buffer.
- For 270° SwivelView modes, BitBLT (Bit Block Transfer) operations are still supported. However, the BitBLT data must first be rotated by software. For further information, refer to the *S1D13806 Programmers Notes And Examples*, document number X28B-G-003-xx.

# 16 EPSON Independent Simultaneous Display (EISD)

EPSON Independent Simultaneous Display (EISD) allows the S1D13806 to display independent images on two different displays (LCD panel and CRT or TV).

## 16.1 Registers

The LCD panel timings and mode setup are programmed through the Panel Configuration Registers (REG[03Xh]) and the LCD Display Mode Registers (REG[04Xh]). The CRT/TV timings and mode setup are programmed through the CRT/TV Configuration Registers (REG[05Xh]) and the CRT/TV Display Mode Registers (REG[06Xh]). The Ink Layer or Hardware Cursor can also be independently controlled on the two displays. The LCD Ink/Cursor Registers (REG[07Xh]) control the Ink/Cursor on the LCD display; the CRT/TV Ink/Cursor Registers (REG[08Xh]) control the Ink/Cursor on the CRT or TV. Each display uses its own Look-Up Table (LUT), although there is only one set of LUT Registers (REG[1E0h], REG[1E2h], REG[1E4h]). Use the LUT Mode Register (REG[1E0h]) to select access to the LCD and/or CRT/TV LUTs.

The pixel clock source for the two displays may be independent. Use the Clock Configuration Registers (REG[014h], REG[018h]) to select the LCD pixel clock source and the CRT/TV pixel clock source, respectively. Typically, CLKI2 is used for the CRT/TV display, while CLKI is used for the LCD display. Memory clock may come from CLKI or BUSCLK.

## 16.2 Display Mapping

To display different images on the LCD and CRT/TV, the two images should reside in non-overlapping areas of the display buffer, and the display start addresses point to the corresponding areas. The display buffer is mapped to the CPU address AB[20:0] linearly.

The LCD and CRT/TV may display identical images by setting the display start addresses for the LCD and the CRT/TV to the same address. In this case only one image is needed in the display buffer.

## 16.3 Bandwidth Limitation

When EISD is enabled, the LCD and CRT/TV displays must share the total bandwidth available to the S1D13806. The result is that display modes with a high resolution or color depth may not be supported. In some cases, Ink Layers may not be possible on one or both of the displays. EISD increases the total demand for display refresh bandwidth and reduces CPU bandwidth, resulting in lower CPU performance.

In a few cases when EISD is enabled, the default LCD and CRT/TV Display FIFO High Threshold Control register values are not optimally set, causing display problems with one or both of the displays. This condition may be corrected by adjusting the values of the LCD and CRT/TV Display FIFO High Threshold Control registers (REG[04Ah] for LCD and REG[06Ah] for CRT/TV). See Section 18.2, “Example Frame Rates” on page 192 for required FIFO settings.

Changing this register to a non-zero value sets the high threshold FIFO level to this value. This register may not exceed 59 decimal. The high threshold FIFO level controls how often display fetch requests are issued by the FIFO. In general, a higher high threshold FIFO level increases the bandwidth to that display pipe, and a lower level reduces it.

When the FIFO High Threshold Control register is set to 00h (default), the following settings are used:

- 11h for 4 bpp color depth
- 21h for 8 bpp color depth
- 23h for 16 bpp color depth

Most display problems may be corrected by increasing the associated high threshold FIFO level for that display. However, because the total available bandwidth is fixed, this change may create display problem for the other display. In this case, reducing the high threshold FIFO level for the other display instead may work. Sometimes, a combination of these two methods is required. Correcting EISD display problems by adjusting the FIFO High Threshold Control registers is mostly a trial-and-error process.

**Note**

While the user is free to experiment with these registers, recommended FIFO level settings for some of the more common EISD modes requiring non-default FIFO level settings are listed in Section 18.2, “Example Frame Rates” on page 192.

# 17 MediaPlug Interface

Winnov's MediaPlug Slave interface has been incorporated into the S1D13806. The MediaPlug Slave follows the *Specification For Winnov MediaPlug Slave, Local module*, Document Rev 0.3 with the following exceptions.

## 17.1 Revision Code

The MediaPlug Slave Revision Code can be determined by reading bits 11:8 of the LCMD register. The revision code for this implementation is 0011b.

## 17.2 How to enable the MediaPlug Slave

The MediaPlug Slave interface is enabled/disabled at the rising edge of RESET# by the state of CONF7. When CONF7 is set to 1, the MediaPlug functionality is enabled and GPIO12 is configured as the MediaPlug power control output pin (VMPEPWR) - see Table 4-9, “Summary of Power-On/Reset Options,” on page 33.

## 17.3 MediaPlug Interface Pin Mapping

The S1D13806 provides 8 pins for use by the MediaPlug interface (VMP[7:0]). GPIO12 is also used as the MediaPlug power control output pin (VMPEPWR) when the MediaPlug interface is enabled. The following table lists the MediaPlug pin mapping when the interface is enabled.

*Table 17-1: MediaPlug Interface Pin Mapping*

| S1D13806 Pin Names | IO Type | MediaPlug I/F |
|---|---|---|
| VMP0 | O | VMPCLKN |
| VMP1 | O | VMPCLK |
| VMP2 | IO | VMPD3 |
| VMP3 | IO | VMPD2 |
| VMP4 | IO | VMPD1 |
| VMP5 | IO | VMPD0 |
| VMP6 | I | VMPRCTL |
| VMP7 | O | VMPLCRL |
| GPIO12 | O | VMPEPWR |

**Note**
VMPEPWR is controlled by bit 1 of the MediaPlug LCMD register.

# 18 Clocking

## 18.1 Frame Rate Calculation

### 18.1.1 LCD Frame Rate Calculation

The maximum LCD frame rate is calculated using the following formula.

$$\text{max. LCD Frame Rate} = \frac{\text{LPCLK}_{max}}{(\text{LHDP} + \text{LHNDP}) \times \left(\frac{\text{LVDP}}{n} + \text{LVNDP}\right)}$$

Where:

LPCLKmax = maximum LCD pixel clock frequency

LVDP = LCD Vertical Display Height
= REG[039h] bits [1:0], REG[038h] bits [7:0] + 1

LVNDP = LCD Vertical Non-Display Period
= REG[03Ah] bits [5:0] + 1

LHDP = LCD Horizontal Display Width
= ((REG[032h] bits [6:0]) + 1) × 8Ts

LHNDP = LCD Horizontal Non-Display Period
= ((REG[034h] bits [4:0]) + 1) × 8Ts

Ts = minimum LCD pixel clock (LPCLK) period

n = 1 for single panel
= 2 for dual panel

### 18.1.2 CRT Frame Rate Calculation

The maximum CRT frame rate is calculated using the following formula.

$$\text{max. CRT Frame Rate} = \frac{\text{CPCLK}_{max}}{(\text{CHDP} + \text{CHNDP}) \times (\text{CVDP} + \text{CVNDP})}$$

Where:

CPCLKmax = maximum CRT pixel clock frequency

CVDP = CRT Vertical Display Height
= REG[057h] bits [1:0], REG[056h] bits [7:0] + 1

CVNDP = CRT Vertical Non-Display Period
= REG[058h] bits [6:0] + 1

CHDP = CRT Horizontal Display Width
= ((REG[050h] bits [6:0]) + 1) × 8Ts

CHNDP = CRT Horizontal Non-Display Period
= ((REG[052h] bits [5:0]) + 1) × 8Ts

Ts = minimum CRT pixel clock (CPCLK) period

### 18.1.3 TV Frame Rate Calculation

The maximum TV frame rate is calculated using the following formula.

$$\text{max. TV Frame Rate} = \frac{\text{TPCLK}_{max}}{(\text{THDP} + \text{THNDP}) \times \left(\frac{\text{TVDP}}{2} + \text{TVNDP} + 0.5\right)}$$

Where:

TPCLKmax = maximum TV pixel clock frequency

TVDP = TV Vertical Display Height
= REG[057h] bits [1:0], REG[056h] bits [7:0] + 1

TVNDP = TV Vertical Non-Display Period
= REG[058h] bits [6:0] + 1

THDP = TV Horizontal Display Width
= ((REG[050h] bits [6:0]) + 1) × 8Ts

THNDP = TV Horizontal Non-Display Period
= for NTSC output use ((REG[052h] bits [5:0]) × 8Ts) + 6
= for PAL output use ((REG[052h] bits [5:0]) × 8Ts) + 7

Ts = minimum TV pixel clock (TPCLK) period

## 18.2 Example Frame Rates

For all example frame rates the following conditions apply:

- Dual panel buffer is enabled for dual panel.
- TV Flicker Filter is enabled for TV.
- MCLK is 50MHz.

### 18.2.1 Frame Rates for 640x480 with EISD Disabled

*Table 18-1: Frame Rates for 640x480 with EISD Disabled*

| LCD Type | | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Passive Single / TFT | | No | 640 | 480 | 4 | 40 | 56 | 1 | 119.5 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 640 | 480 | 8 | 40 | 64 | 1 | 118.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 640 | 480 | 16 | 40 | 64 | 1 | 118.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| Mono Passive Dual | | No | 640 | 480 | 4 | 40 | 64 | 1 | 235.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 640 | 480 | 8 | 40 | 72 | 1 | 233.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 640 | 480 | 16 | 31 | 72 | 1 | 181.0 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| Color Passive Dual | | No | 640 | 480 | 4 | 40 | 64 | 1 | 235.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 640 | 480 | 8 | 40 | 72 | 1 | 233.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 640 | 480 | 16 | 30 | 64 | 1 | 176.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| Passive Single / TFT | | Yes | 640 | 480 | 4 | 40 | 56 | 1 | 119.5 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 640 | 480 | 8 | 40 | 64 | 1 | 118.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 640 | 480 | 16 | 40 | 64 | 1 | 118.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| Mono Passive Dual | | Yes | 640 | 480 | 4 | 40 | 64 | 1 | 235.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 640 | 480 | 8 | 40 | 72 | 1 | 233.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 640 | 480 | 16 | 30 | 64 | 1 | 176.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| Color Passive Dual | | Yes | 640 | 480 | 4 | 40 | 64 | 1 | 235.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 640 | 480 | 8 | 36 | 72 | 1 | 209.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 640 | 480 | 16 | 26 | 56 | 1 | 155.0 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 640 | 480 | 4 | 36 | 192 | 29 | 85.0 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 640 | 480 | 8 | 36 | 192 | 29 | 85.0 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 640 | 480 | 16 | 36 | 192 | 29 | 85.0 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | NTSC TV | No | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | NTSC TV | No | 640 | 480 | 16 | 14.32 | 270 | 22 | 60 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | PAL TV | No | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | PAL TV | No | 640 | 480 | 16 | 17.73 | 495 | 72 | 50 |

Example Frame Rates with Ink Layer Enabled

*Table 18-1: Frame Rates for 640x480 with EISD Disabled*

| LCD Type | | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 640 | 480 | 4 | 36 | 192 | 29 | 85.0 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 640 | 480 | 8 | 36 | 192 | 29 | 85.0 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 640 | 480 | 16 | 36 | 200 | 20 | 85.7 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | NTSC TV | Yes | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | NTSC TV | Yes | 640 | 480 | 16 | 14.32 | 270 | 22 | 60 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | PAL TV | Yes | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | PAL TV | Yes | 640 | 480 | 16 | 17.73 | 495 | 72 | 50 |

Example Frame Rates with Ink Layer Enabled

## 18.2.2 Frame Rates for 800x600 with EISD Disabled

*Table 18-2: Frame Rates for 800x600 with EISD Disabled*

| LCD Type | | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TFT | | No | 800 | 600 | 8 | 65 | 232 | 35 | 99.2 | | | | | | | | | |
| | | No | 800 | 600 | 16 | 44.4 | 160 | 35 | 72.8 | | | | | | | | | |
| Color Passive Dual | | No | 800 | 600 | 4 | 40 | 64 | 1 | 153.8 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 800 | 600 | 8 | 40 | 72 | 1 | 152.4 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | No | 800 | 600 | 16 | 30 | 64 | 1 | 115.3 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| TFT | | Yes | 800 | 600 | 8 | 65 | 232 | 35 | 99.2 | | | | | | | | | |
| TFT[1] | | Yes | 800 | 600 | 16 | 40 | 144 | 35 | 66.7 | | | | | | | | | |
| Color Passive Dual | | Yes | 800 | 600 | 4 | 38 | 64 | 1 | 146.1 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 800 | 600 | 8 | 36 | 72 | 1 | 137.2 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| | | Yes | 800 | 600 | 16 | 26 | 56 | 1 | 100.9 | -- | -- | -- | -- | -- | -- | -- | -- | -- |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 800 | 600 | 4 | 40 | 256 | 28 | 60.3 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 800 | 600 | 16 | 40 | 224 | 25 | 62.5 |
| | | | | | | | | | | | CRT | No | 800 | 600 | 4 | 49.5 | 256 | 28 | 74.6 |
| | | | | | | | | | | | CRT | No | 800 | 600 | 8 | 49.5 | 256 | 28 | 74.6 |
| | | | | | | | | | | | CRT | No | 800 | 600 | 4 | 56.25 | 256 | 28 | 84.8 |
| | | | | | | | | | | | CRT | No | 800 | 600 | 8 | 56.25 | 256 | 28 | 84.8 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 800 | 600 | 4 | 40 | 256 | 28 | 60.3 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT[2] | Yes | 800 | 600 | 16 | 40 | 224 | 25 | 62.5 |
| | | | | | | | | | | | CRT | Yes | 800 | 600 | 4 | 49.5 | 256 | 28 | 74.6 |
| | | | | | | | | | | | CRT | Yes | 800 | 600 | 8 | 49.5 | 256 | 28 | 74.6 |
| | | | | | | | | | | | CRT | Yes | 800 | 600 | 4 | 56.25 | 256 | 28 | 84.8 |
| | | | | | | | | | | | CRT | Yes | 800 | 600 | 8 | 56.25 | 256 | 28 | 84.8 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[07Eh] = 0Ch.
2. REG[08Eh] = 0Ah.

### 18.2.3 Frame Rates for 1024x768 with EISD Disabled

*Table 18-3: Frame Rates for 1024x768 with EISD Disabled*

| LCD Type | | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TFT | | No | 1024 | 768 | 8 | 65 | 160 | 37 | 68.2 | | | | | | | | | |
| TFT[1] | | Yes | 1024 | 768 | 8 | 65 | 160 | 37 | 68.2 | | | | | | | | | |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 1024 | 768 | 4 | 65 | 320 | 41 | 59.8 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 1024 | 768 | 4 | 65 | 320 | 41 | 59.8 |
| -- | -- | -- | -- | -- | -- | -- | -- | -- | -- | CRT | Yes | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[07Eh] = 0Ch.

## 18.2.4 Frame Rates for LCD and CRT (640x480) with EISD Enabled

*Table 18-4: Frame Rates for LCD and CRT (640x480) with EISD Enabled*

| LCD Type | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK( MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Passive Single | No | 320 | 240 | 16 | 17 | 64 | 1 | 183.7 | CRT | No | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| | No | 640 | 240 | 16 | 17 | 64 | 1 | 100.2 | CRT | No | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| | No | 640 | 480 | 4 | 40 | 112 | 1 | 110.6 | CRT | No | 640 | 480 | 4 | 25.18 | 160 | 44 | 60.1 |
| | No | 640 | 480 | 8 | 40 | 144 | 1 | 106.1 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | No | 640 | 480 | 16 | 12 | 56 | 1 | 71.5 | CRT | No | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| TFT | No | 800 | 600 | 8 | 41 | 144 | 26 | 69.4 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| TFT | No | 1024 | 768 | 8 | 41 | 112 | 37 | 44.8 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | No | 800 | 600 | 4 | 38 | 120 | 1 | 137.2 | CRT | No | 640 | 480 | 4 | 25.18 | 160 | 44 | 60.1 |
| | No | 800 | 600 | 8 | 27.6 | 104 | 1 | 101.4 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Passive Single | Yes | 640 | 480 | 4 | 40 | 112 | 1 | 110.6 | CRT | No | 640 | 480 | 4 | 25.18 | 160 | 44 | 60.1 |
| | Yes | 640 | 480 | 8 | 31.6 | 112 | 1 | 87.4 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| TFT | Yes | 800 | 600 | 8 | 31.6 | 112 | 26 | 55.4 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Mono Passive Dual | Yes | 640 | 480 | 8 | 27.6 | 104 | 1 | 153.9 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | Yes | 640 | 480 | 8 | 23.2 | 88 | 1 | 132.2 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual[1] | Yes | 640 | 480 | 16 | 11.6 | 48 | 1 | 70.0 | CRT | No | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | Yes | 800 | 600 | 8 | 23.2 | 88 | 1 | 86.8 | CRT | No | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Passive Single[2] | No | 640 | 240 | 16 | 13.7 | 56 | 1 | 81.7 | CRT | Yes | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| Passive Single | No | 640 | 480 | 8 | 31.7 | 112 | 1 | 87.6 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Mono Passive Dual[2] | No | 640 | 480 | 8 | 27.1 | 104 | 1 | 151.1 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| | No | 640 | 480 | 16 | 11 | 48 | 1 | 66.4 | CRT | Yes | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | No | 640 | 480 | 8 | 19 | 88 | 1 | 108.3 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | No | 800 | 600 | 4 | 33.2 | 104 | 1 | 122.0 | CRT | Yes | 640 | 480 | 4 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual[2] | No | 800 | 600 | 8 | 22.6 | 88 | 1 | 84.6 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Passive Single[3] | Yes | 640 | 240 | 16 | 11.8 | 48 | 1 | 71.2 | CRT | Yes | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| Passive Single | Yes | 640 | 480 | 8 | 25.7 | 96 | 1 | 72.6 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Mono Passive Dual[2] | Yes | 640 | 480 | 8 | 22.6 | 88 | 1 | 128.8 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual | Yes | 640 | 480 | 8 | 15 | 72 | 1 | 87.4 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |

Example Frame Rates with Ink Layer Enabled

*Table 18-4: Frame Rates for LCD and CRT (640x480) with EISD Enabled*

| LCD Type | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK( MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Color Passive Dual[3] | Yes | 640 | 480 | 16 | 9.57 | 40 | 1 | 58.4 | CRT | Yes | 640 | 480 | 16 | 25.18 | 160 | 44 | 60.1 |
| Color Passive Dual[2] | Yes | 800 | 600 | 8 | 19.4 | 72 | 1 | 73.9 | CRT | Yes | 640 | 480 | 8 | 25.18 | 160 | 44 | 60.1 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[06Ah] = 3Ch. REG[06Bh] = 3Ch.
2. REG[08Eh] = 0Ch.
3. REG[06Ah] = 3Ch. REG[06Bh] = 3Ch. REG[07Eh] = 0Ch. REG[08Eh] = 0Ch.

## 18.2.5 Frame Rates for LCD and CRT (800x600) with EISD Enabled

*Table 18-5: Frame Rates for LCD and CRT (800x600) with EISD Enabled*

| LCD Type | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Passive Single | No | 640 | 240 | 8 | 34 | 120 | 1 | 185.6 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| | No | 640 | 480 | 8 | 34 | 120 | 1 | 93.0 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Color Passive Dual | No | 640 | 480 | 8 | 22.5 | 88 | 1 | 128.2 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| TFT[1] | No | 800 | 600 | 8 | 34 | 120 | 28 | 58.8 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Color Passive Dual | No | 800 | 600 | 4 | 38.6 | 112 | 1 | 140.6 | CRT | No | 800 | 600 | 4 | 40 | 256 | 28 | 60.3 |
| | No | 800 | 600 | 8 | 22.5 | 88 | 1 | 84.2 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Passive Single | Yes | 640 | 240 | 8 | 26.2 | 96 | 1 | 147.7 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| | Yes | 640 | 480 | 8 | 26.2 | 96 | 1 | 74.0 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Mono Passive Dual | Yes | 640 | 480 | 8 | 22.5 | 88 | 1 | 128.2 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Color Passive Dual[2] | Yes | 640 | 480 | 8 | 19 | 72 | 1 | 110.7 | CRT | No | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Passive Single[3] | No | 640 | 240 | 8 | 24.4 | 88 | 1 | 139.1 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Passive Single | No | 640 | 480 | 8 | 24.4 | 88 | 1 | 69.7 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Mono Passive Dual[4] | No | 640 | 480 | 8 | 20.6 | 80 | 1 | 118.7 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Color Passive Dual[5] | No | 640 | 480 | 8 | 17.2 | 64 | 1 | 101.4 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| | No | 800 | 600 | 8 | 17.2 | 64 | 1 | 66.1 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Passive Single[3] | Yes | 640 | 240 | 8 | 19.8 | 72 | 1 | 115.4 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Passive Single | Yes | 640 | 480 | 8 | 19.8 | 72 | 1 | 57.8 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Mono Passive Dual[6] | Yes | 640 | 480 | 8 | 17.2 | 64 | 1 | 101.4 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |
| Color Passive Dual[6] | Yes | 640 | 480 | 8 | 14.7 | 56 | 1 | 87.6 | CRT | Yes | 800 | 600 | 8 | 40 | 256 | 28 | 60.3 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[04Ah] = 30h. REG[06Ah] = 30h. REG[04Bh] = 3Ch. REG[06Bh] = 3Ch.
2. REG[04Ah] = 1Ah. REG[06Bh] = 25h.
3. REG[06Ah] = 23h. REG[08Eh] = 0Ch.
4. REG[08Eh] = 0Ch.

## 18.2.6 Frame Rates for LCD and CRT (1024x768) with EISD Enabled

*Table 18-6: Frame Rates for LCD and CRT (1024x768) with EISD Enabled*

| LCD Type | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Passive Single[1] | No | 320 | 240 | 8 | 31 | 144 | 1 | 277.2 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| Passive Single[2] | No | 640 | 240 | 8 | 21.1 | 80 | 1 | 121.6 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| Passive Single | No | 640 | 480 | 8 | 21.1 | 80 | 1 | 60.9 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| Color Passive Dual[2] | No | 640 | 480 | 8 | 13.8 | 56 | 1 | 82.3 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| Passive Single[3] | Yes | 320 | 240 | 8 | 16.2 | 56 | 1 | 178.8 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| | Yes | 640 | 240 | 8 | 16.2 | 56 | 1 | 96.6 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |
| Passive Single | Yes | 640 | 480 | 8 | 20 | 72 | 1 | 58.4 | CRT | No | 1024 | 768 | 8 | 65 | 320 | 41 | 59.8 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[04Ah] = 25h. REG[04Bh] = 3Ch. REG[06Ah] = 30h. REG[06Bh] = 3Ch.
2. REG[04Ah] = 1Ah. REG[06Ah] = 30h. REG[06Bh] = 3Ch.
3. REG[07Eh] = 0Ch.

## 18.2.7 Frame Rates for LCD and NTSC TV with EISD Enabled

*Table 18-7: Frame Rates for LCD and NTSC TV with EISD Enabled*

| LCD Type | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Passive Single / TFT | No | 320 | 240 | 16 | 10.7 | 56 | 1 | 118.1 | NTSC TV | No | 640 | 480 | 16 | 14.32 | 270 | 22 | 60 |
| | No | 640 | 240 | 16 | 10.7 | 56 | 1 | 63.8 | NTSC TV | No | 640 | 480 | 16 | 14.32 | 270 | 22 | 60 |
| | No | 640 | 480 | 4 | 40 | 152 | 1 | 105.0 | NTSC TV | No | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| | No | 640 | 480 | 8 | 27.6 | 136 | 1 | 73.9 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Mono Passive Dual | No | 640 | 480 | 8 | 24 | 128 | 1 | 129.6 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Color Passive Dual | No | 640 | 480 | 8 | 21.1 | 112 | 1 | 116.4 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| TFT | No | 800 | 600 | 8 | 27.6 | 136 | 35 | 46.4 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Color Passive Dual | No | 800 | 600 | 8 | 21.1 | 112 | 1 | 76.9 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Passive Single | Yes | 640 | 480 | 4 | 39 | 144 | 1 | 103.4 | NTSC TV | No | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| Mono Passive Dual | Yes | 640 | 480 | 8 | 20.5 | 112 | 1 | 113.1 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Color Passive Dual | Yes | 640 | 480 | 4 | 28.1 | 112 | 1 | 155.0 | NTSC TV | No | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| | Yes | 640 | 480 | 8 | 18.2 | 96 | 1 | 102.6 | NTSC TV | No | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Passive Single | No | 640 | 240 | 8 | 20.4 | 104 | 1 | 113.8 | NTSC TV | Yes | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| | No | 640 | 480 | 4 | 33.7 | 128 | 1 | 91.2 | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| Mono Passive Dual | No | 640 | 480 | 8 | 18.4 | 96 | 1 | 103.7 | NTSC TV | Yes | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Color Passive Dual | No | 640 | 480 | 4 | 23.7 | 96 | 1 | 133.6 | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| | No | 640 | 480 | 8 | 16 | 88 | 1 | 91.2 | NTSC TV | Yes | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Passive Single | Yes | 640 | 240 | 4 | 27.4 | 104 | 1 | 152.8 | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| Passive Single[1] | Yes | 640 | 240 | 8 | 17.5 | 88 | 1 | 99.7 | NTSC TV | Yes | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Mono Passive Dual | Yes | 640 | 480 | 4 | 23.7 | 96 | 1 | 133.6 | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| Mono Passive Dual[1] | Yes | 640 | 480 | 8 | 15.6 | 80 | 1 | 89.9 | NTSC TV | Yes | 640 | 480 | 8 | 14.32 | 270 | 22 | 60 |
| Color Passive Dual | Yes | 640 | 480 | 4 | 20.4 | 88 | 1 | 116.3 | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |
| | Yes | 640 | 480 | 8 | 14.2 | 80 | 1 | 81.8 | NTSC TV | Yes | 640 | 480 | 4 | 14.32 | 270 | 22 | 60 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[07Eh] = 0Ch.

## 18.2.8 Frame Rates for LCD and PAL TV with EISD Enabled

*Table 18-8: Frame Rates for LCD and PAL TV with EISD Enabled*

| LCD Type | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | max PCLK (MHz) | min HNDP (pixels) | min VNDP (lines) | max Frame Rate (Hz) | CRT/ TV | Ink | Horiz Res (pixels) | Vert Res (lines) | bpp | PCLK (MHz) | HNDP (pixels) | VNDP (lines) | Frame Rate (Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Passive Single | No | 320 | 240 | 16 | 7.5 | 40 | 1 | 86.4 | PAL TV | No | 640 | 480 | 16 | 17.73 | 495 | 72 | 50 |
| | No | 640 | 240 | 16 | 9 | 40 | 1 | 55.0 | PAL TV | No | 640 | 480 | 16 | 17.73 | 495 | 72 | 50 |
| | No | 640 | 480 | 4 | 40 | 152 | 1 | 105.0 | PAL TV | No | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| | No | 640 | 480 | 8 | 25.8 | 128 | 1 | 69.8 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Mono Passive Dual | No | 640 | 480 | 8 | 22.2 | 120 | 1 | 121.2 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Color Passive Dual | No | 640 | 480 | 8 | 19 | 104 | 1 | 106.0 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| TFT[1] | No | 800 | 600 | 8 | 43 | 136 | 35 | 72.3 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Color Passive Dual | No | 800 | 600 | 8 | 19 | 104 | 1 | 69.8 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Passive Single | Yes | 640 | 480 | 4 | 37.2 | 144 | 1 | 98.6 | PAL TV | No | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| Mono Passive Dual[2] | Yes | 640 | 480 | 8 | 19 | 104 | 1 | 106.0 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Color Passive Dual | Yes | 640 | 480 | 4 | 26.2 | 104 | 1 | 146.1 | PAL TV | No | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| | Yes | 640 | 480 | 8 | 16.3 | 88 | 1 | 92.9 | PAL TV | No | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Passive Single | No | 640 | 240 | 8 | 18.1 | 96 | 1 | 102.0 | PAL TV | Yes | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| | No | 640 | 480 | 4 | 31.7 | 120 | 1 | 86.7 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| Mono Passive Dual | No | 640 | 480 | 4 | 26 | 112 | 1 | 143.4 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| | No | 640 | 480 | 8 | 16.1 | 88 | 1 | 91.8 | PAL TV | Yes | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Color Passive Dual | No | 640 | 480 | 4 | 22.7 | 96 | 1 | 128.0 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| | No | 640 | 480 | 8 | 13.9 | 72 | 1 | 81.0 | PAL TV | Yes | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Passive Single | Yes | 640 | 240 | 4 | 21 | 96 | 1 | 118.4 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| Passive Single[2] | Yes | 640 | 240 | 8 | 15.4 | 80 | 1 | 88.8 | PAL TV | Yes | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Mono Passive Dual | Yes | 640 | 480 | 4 | 22.7 | 96 | 1 | 128.0 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| Mono Passive Dual[2] | Yes | 640 | 480 | 8 | 13.9 | 72 | 1 | 81.0 | PAL TV | Yes | 640 | 480 | 8 | 17.73 | 495 | 72 | 50 |
| Color Passive Dual | Yes | 640 | 480 | 4 | 19.6 | 80 | 1 | 113.0 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |
| | Yes | 640 | 480 | 8 | 12.3 | 64 | 1 | 72.5 | PAL TV | Yes | 640 | 480 | 4 | 17.73 | 495 | 72 | 50 |

Example Frame Rates with Ink Layer Enabled

**The FIFO values for these display modes must be set as follows:**

1. REG[04Ah] = 3Ch. REG[04Bh] = 3Ch.
2. REG[07Eh] = 7Ch.

# 19 Power Save Mode

The S1D13806 includes a software initiated power save mode designed for very low-power applications. In addition, the S1D13806 dynamically disables internal clock networks when not required. Similarly, the LCD and/or CRT/TV pipelines are shut down when not required for the selected display mode.

For power save mode AC Timing, see Section 6.4.2, “Power Save Status” on page 63.

## 19.1 Overview

Power save mode is initiated by setting REG[1F0h] bit 0 to 1. When power save mode is enabled the following conditions apply.

- LCD display is disabled.
- CRT/TV display is disabled.
- Memory access is not allowed.
- Memory is in self-refresh mode.
- Register access is allowed.

## 19.2 Power Save Status Bits

#### LCD Power Save Status bit

The LCD Power Save Status bit (REG[1F1h] bit 0) indicates the state of the LCD panel. When this bit returns a 1, the panel is powered down. When this bit returns a 0, the panel is powered up, or in transition of powering up or down.

The system may disable the LCD pixel clock source when this bit returns a 1. The LCD Power Save Status bit is set to 1 after chip reset.

#### Memory Controller Power Save Status bit

The Memory Controller Power Save Status bit (REG[1F1h] bit 1) indicates the state of the SDRAM interface. When this bit returns a 1, the SDRAM interface is powered down and the SDRAM is in self-refresh mode. This condition occurs shortly after power save mode is invoked. When this bit returns a 0, the SDRAM interface is active.

The system may disable the memory clock source when this bit returns a 1. The Memory Controller Power Save Status bit is set to 0 after chip reset.

## 19.3 Power Save Mode Summary

*Table 19-1: Power Save Mode Summary*

| Function | LCD Disabled | CRT/TV Disabled | Power Save Mode Enabled |
|---|---|---|---|
| LCD Display Active? | no | -- | No |
| CRT/TV Display Active? | -- | no | No |
| Register Access Possible? | Yes | Yes | Yes |
| Memory Access Possible? | Yes | Yes | No |
| LCD LUT Access Possible? | Yes[1] | -- | Yes |
| CRT/TV LUT Access Possible? | -- | Yes[2] | Yes |
| LCD interface | Forced Low | -- | Forced Low |
| CRT/TV interface | -- | Disabled | Disabled |
| SDRAM interface | Active | Active | Self-Refresh |
| Host Interface | Active | Active | Active |

**Note**
1. LCD pixel clock required.

**Note**
2. CRT/TV pixel clock required.

# 20 Mechanical Data

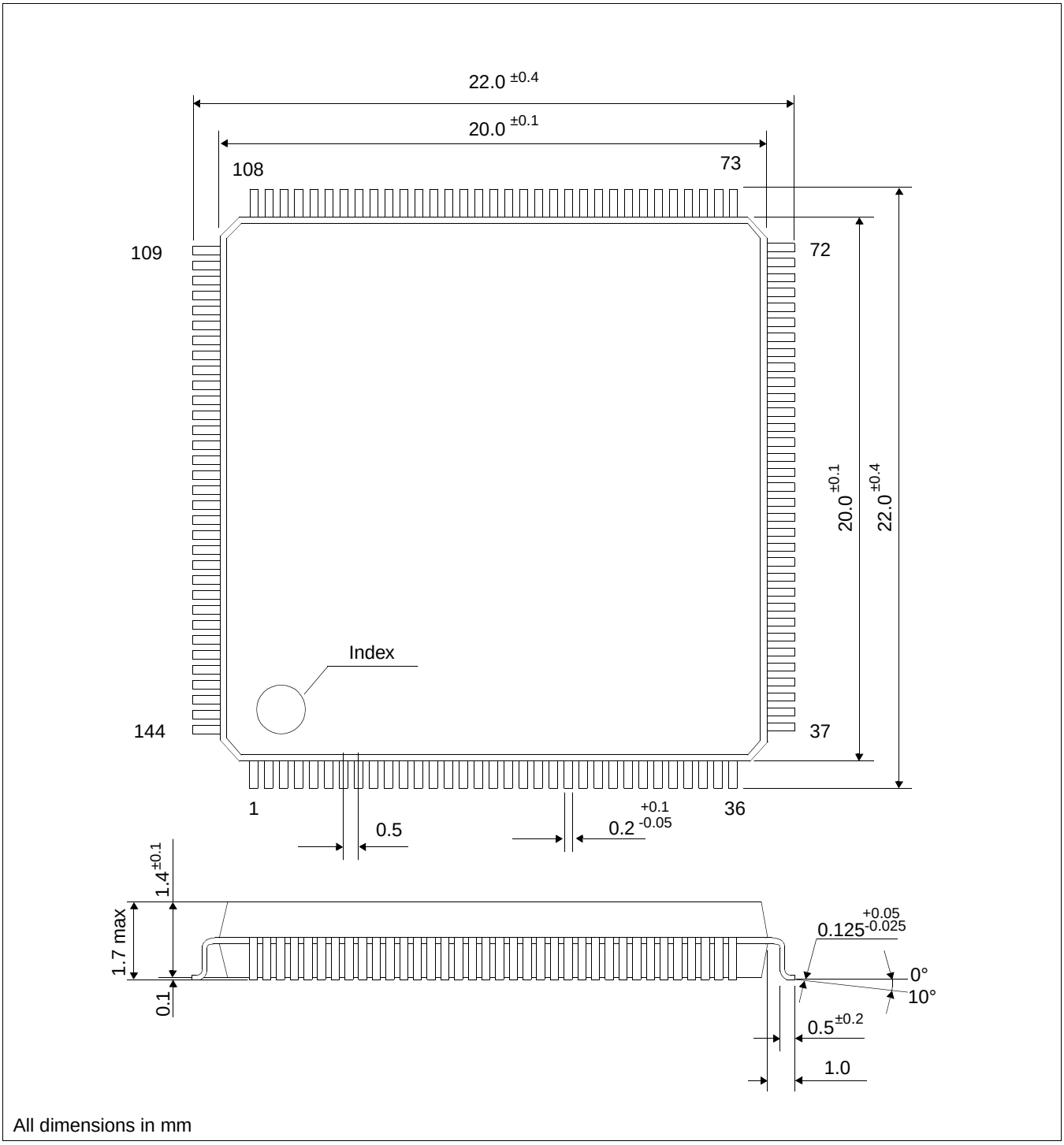



*Figure 20-1: Mechanical Drawing 144-pin QFP20*

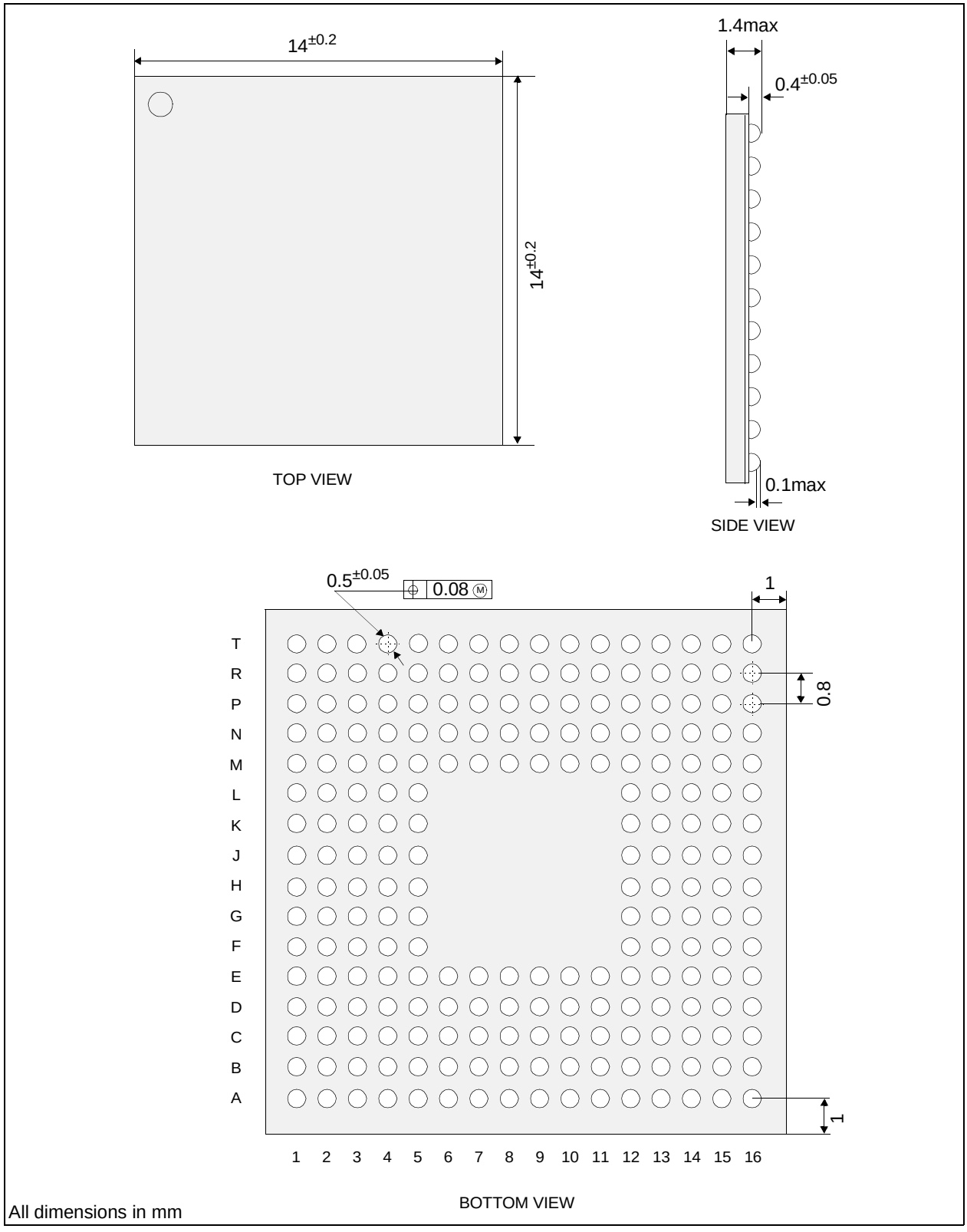



*Figure 20-2: Mechanical Drawing 220-pin PFBGA*

# 21 References

The following documents contain additional information related to the S1D13806. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Electronics America website at **www.eea.epson.com** or the Epson Research and Development Website at **www.erd.epson.com**.

- 13806CFG Configuration Utility Users Manual (X28B-B-001-xx)
- 13806SHOW Demonstration Program Users Manual (X28B-B-002-xx)
- 13806PLAY Diagnostic Utility Users Manual (X28B-B-003-xx)
- 13806BMP Demonstration Program Users Manual (X28B-B-004-xx)
- 13806FILT Test Utility Users Manual (X28B-B-005-xx)
- 13806SWIVEL Demonstration Utility Users Manual (X28B-B-006-xx)
- S1D13806 Product Brief (X28B-C-001-xx)
- S1D13806 Windows CE v2.x Display Driver (X28B-E-001-xx)
- S1D13806 Wind River WindML v2.0 Display Driver (X28B-E-002-xx)
- S1D13806 Wind River UGL v1.2 Display Driver (X28B-E-003-xx)
- S1D13806 Linux Console Driver (X28B-E-004-xx)
- S1D13806 QNX Photon v2.0 Display Driver (X28B-E-005-xx)
- S1D13806 Windows CE v3.x Display Driver (X28B-E-006-xx)
- S1D13806 Programming Notes And Examples (X28B-G-003-xx)
- S5U13806B00C Rev. 1.0 Evaluation Board User Manual (X28B-G-004-xx)
- Interfacing to the PC Card Bus (X28B-G-005-xx)
- S1D13806 Power Consumption (X28B-G-006-xx)
- Interfacing to the NEC VR4102/VR4111 Microprocessors (X28B-G-007-xx)
- Interfacing to the Motorola MPC821 Microprocessor (X28B-G-008-xx)
- Interfacing to the Philips MIPS PR31500/PR31700 Microprocessors (X28B-G-009-xx)
- Interfacing to the Toshiba MIPS TX3912 Microprocessor (X28B-G-010-xx)
- Interfacing to the NEC VR4121 Microprocessor (X28B-G-011-xx)
- Interfacing to the StrongArm SA-1110 Microprocessor (X28B-G-012-xx)
- S1D13806 Register Summary (X28B-R-001-xx)

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