

# System Reset Monolithic IC PST573

## Outline

This IC functions in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted. This ultra-low current consumption high reset type system reset IC was developed using high resistance process and low current circuit design technology.

## Features

- |   |   |   |
|---|---|---|
| 1. Ultra-low current consumption                    | $I_{CCH}=450\mu A$ typ. $I_{CCL}=1\mu A$ typ. |   |
| 2. Low operating limit voltage                      | 0.65V typ.                                    |   |
| 3. Output current high for ON                       | -6mA typ.                                     |   |
| 4. Hysteresis voltage provided in detection voltage | 50mV typ.                                     |   |
| 5. 10 ranks of detection voltage                    | PST573  | C : 4.5V typ. H : 3.1V typ.<br>D : 4.2V typ. I : 2.9V typ.<br>E : 3.9V typ. J : 2.7V typ.<br>F : 3.6V typ. K : 2.5V typ.<br>G : 3.3V typ. L : 2.3V typ. |

## Package

MMP-3A (PST573□M)

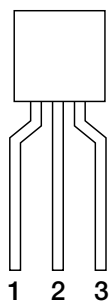
TO-92A (PST573□)

\*□ contains detection voltage rank .

## Applications

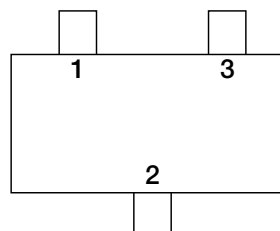
1. Reset circuits in microcomputers, CPUs and MPUs.
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.

## Pin Assignment



TO-92A

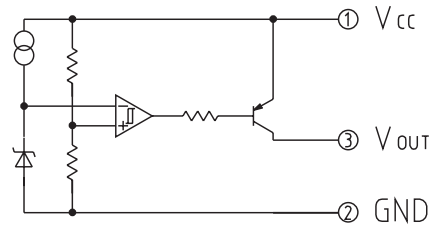
1	V <sub>CC</sub>
2	GND
3	V <sub>OUT</sub>



MMP-3A

1	V <sub>CC</sub>
2	GND
3	V <sub>OUT</sub>

**Equivalent Circuit Diagram**



**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CC</sub> max.	-0.3~10	V
Allowable loss	P <sub>d</sub>	200(MMP-3A) 300(TO-92A)	mW

**Electrical Characteristics** (Ta=25°C) (Except where noted otherwise, resistance unit is Ω)

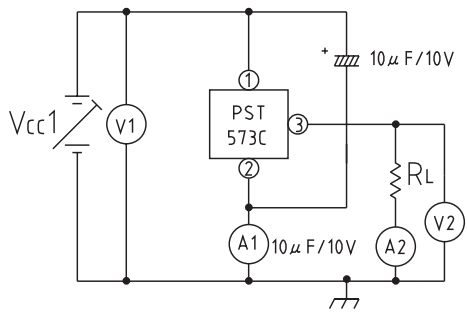
Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units	
Detection voltage	V <sub>s</sub>	1	R <sub>L</sub> =4.7k V <sub>OL</sub> ≤ V <sub>CC</sub> -0.4V V <sub>CC</sub> =H→L	PST573C	4.3	4.5	4.7	V
				PST573D	4.0	4.2	4.4	
				PST573E	3.7	3.9	4.1	
				PST573F	3.4	3.6	3.8	
				PST573G	3.1	3.3	3.5	
				PST573H	2.9	3.1	3.3	
				PST573I	2.75	2.90	3.05	
				PST573J	2.55	2.70	2.85	
				PST573K	2.35	2.50	2.65	
PST573L	2.15	2.30	2.45					
Hysteresis voltage	ΔV <sub>s</sub>	1	R <sub>L</sub> =4.7kΩ V <sub>CC</sub> =L→H→L	25	50	100	mV	
Detection voltage temperature coefficient	V <sub>s</sub> /ΔT	1	R <sub>L</sub> =4.7kΩ Ta=-20°C~+75°C		±0.01		%/°C	
High level output voltage	V <sub>OH</sub>	1	V <sub>CC</sub> =V <sub>s</sub> min. -0.05V R <sub>L</sub> =4.7kΩ	V <sub>CC</sub> -0.4			V	
Output leakage current	I <sub>OH</sub>	1	V <sub>CC</sub> =7.5V			±0.1	μA	
Circuit current while on	I <sub>CC</sub> L	1	V <sub>CC</sub> =V <sub>s</sub> min. -0.05V R <sub>L</sub> =∞		450	700	μA	
Circuit current while off	I <sub>CC</sub> H	1	V <sub>CC</sub> =V <sub>s</sub> typ. /0.85V R <sub>L</sub> =∞		1.0	1.8	μA	
"H"transport delay time	tpLH	2	R <sub>L</sub> =4.7kΩ *1 C <sub>L</sub> =100pF		25	60	μS	
"L"transport delay time	tpHL	2	R <sub>L</sub> =4.7kΩ *1 C <sub>L</sub> =100pF		8	20	μS	
Operation limit voltage	V <sub>op</sub> L	1	R <sub>L</sub> =4.7kΩ V <sub>OL</sub> ≥ V <sub>CC</sub> -0.4V		0.65	0.85	V	
Output current while on I	I <sub>OL</sub> I	1	V <sub>CC</sub> =V <sub>s</sub> min. -0.05V R <sub>L</sub> =0	-2.0	-6.0		mA	
Output current while on II	I <sub>OL</sub> II	1	Ta=-20°C~+75°C *2 R <sub>L</sub> =0	-1.5			mA	

\*1 : tpLH : V<sub>CC</sub>=(V<sub>s</sub> typ.-0.4V)→(V<sub>s</sub> typ.+0.4V), tpHL : V<sub>CC</sub>=(V<sub>s</sub> typ.+0.4V)→(V<sub>s</sub> typ.-0.4V)

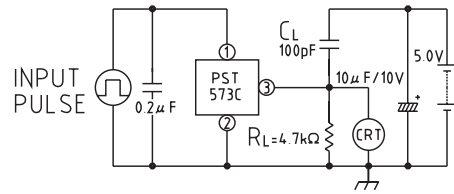
\*2 : V<sub>CC</sub>=V<sub>s</sub> min.-0.15V

Measuring Circuit

[1]

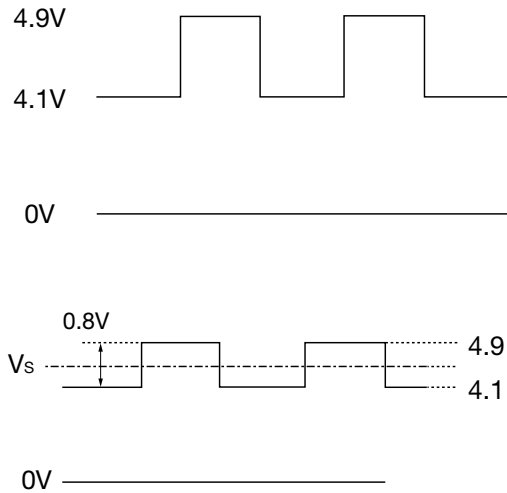


[2]



A : DC ammeter  
V : DC voltmeter  
CRT: Oscilloscope

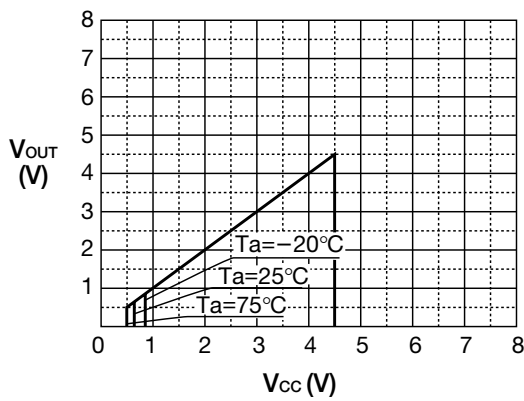
INPUT PULSE



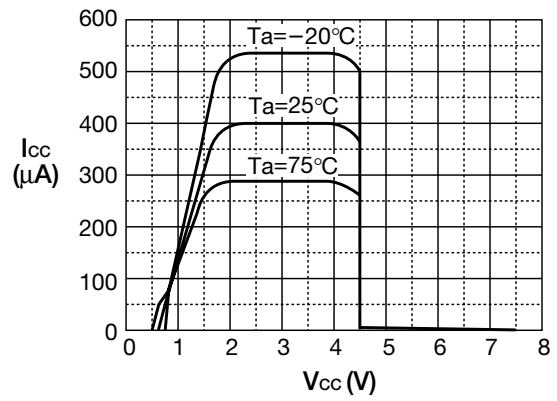
Note: Input model is an example for PST573C.

Characteristics (Example: PST573C)

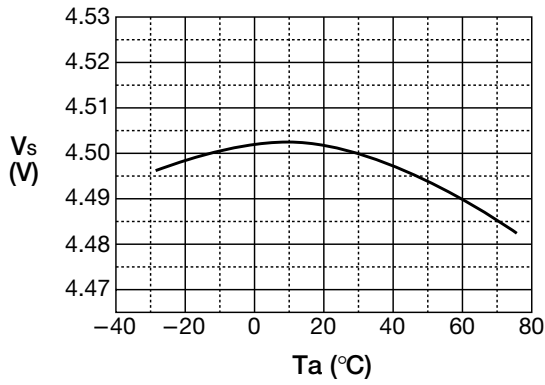
■ Vcc vs. Vout



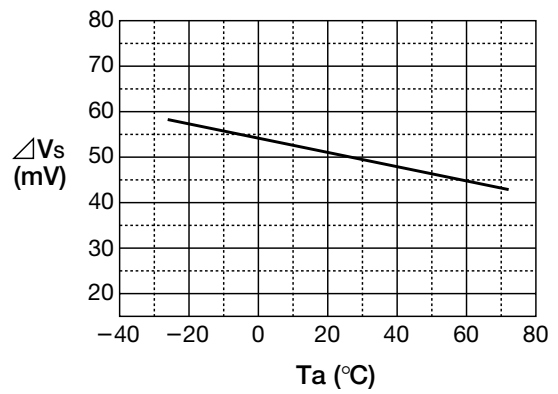
■ Vcc vs. Icc



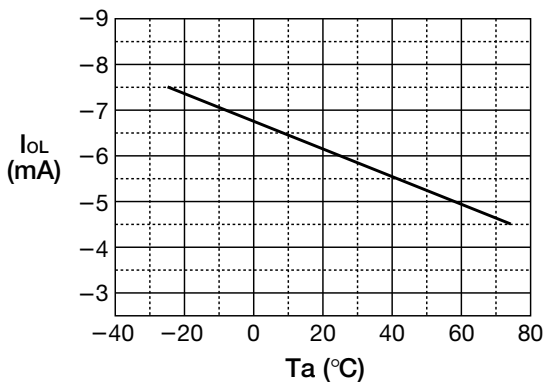
■  $V_s$  vs.  $T_a$



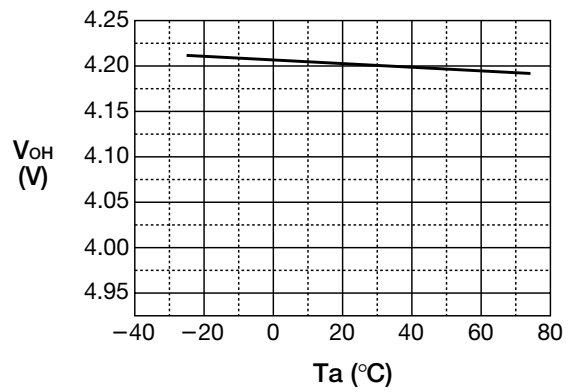
■  $\Delta V_s$  vs.  $T_a$



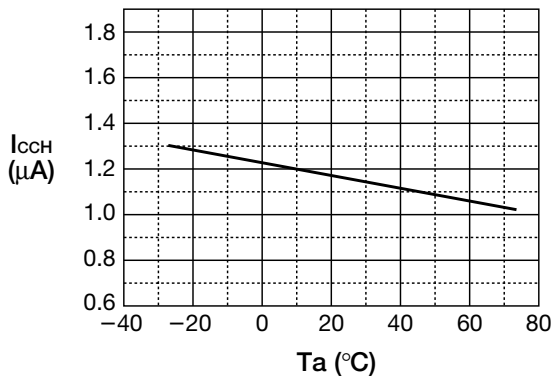
■  $I_{OL}$  vs.  $T_a$



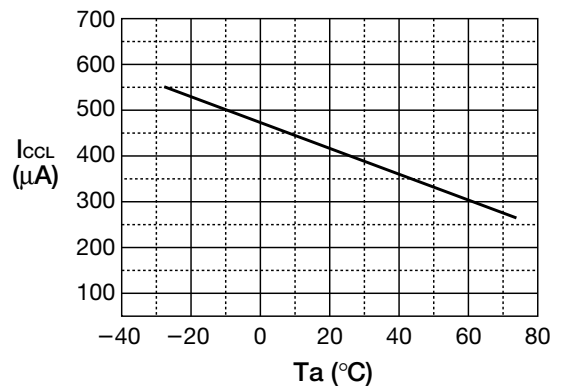
■  $V_{OH}$  vs.  $T_a$



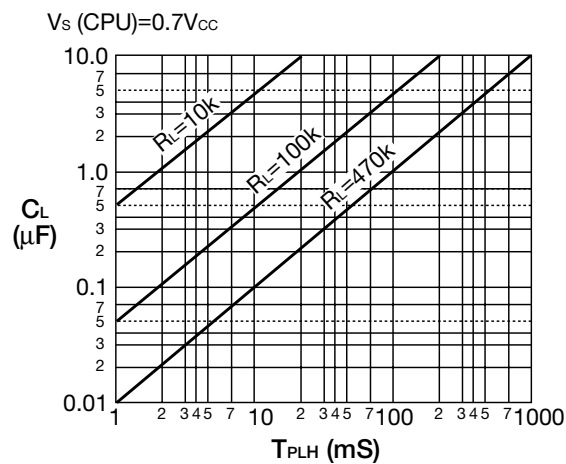
■  $I_{CCH}$  vs.  $T_a$



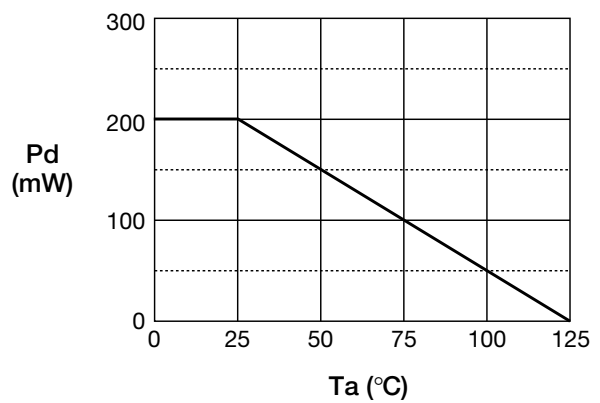
■  $I_{CCL}$  vs.  $T_a$



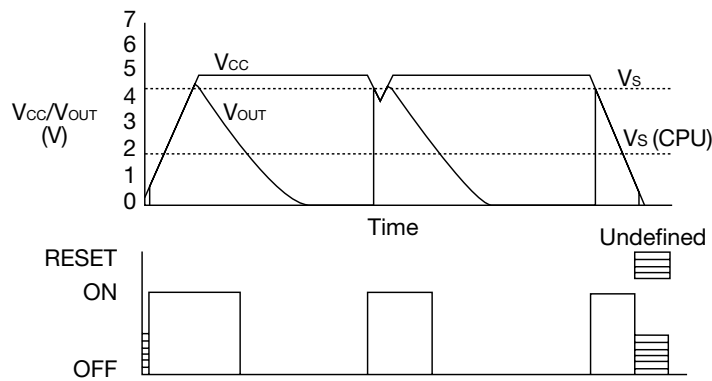
■  $C_L$  (RL) vs.  $t_{PLH}$



■  $P_d$  vs.  $T_a$

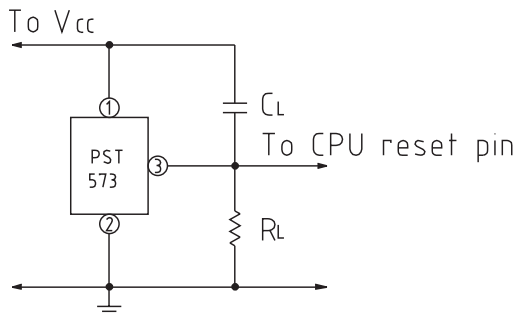


Timing Chart



Application circuits

1. Normal hard reset



Delay time (tpLH)

$$\approx C_L \times R_L \times \left[ \ln \frac{V_{CC}-0.2}{V_{s\text{cpu}}} \right] + 0.025 \text{ (mS)}$$

CL : μF

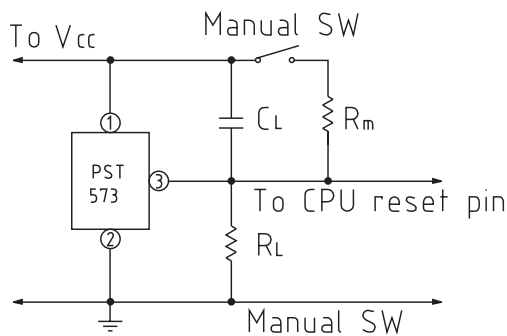
RL : kΩ

Vs cpu : Reset threshold voltage of CPU, MPU, etc.

Voltage: V

Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

2. Manual reset added



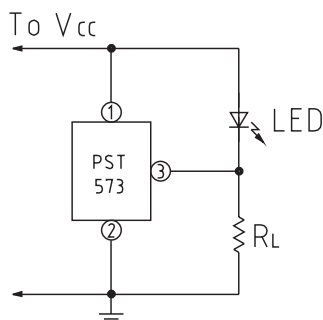
Note 1: Use RL, CL and Rm to prevent manual switch chattering.

Note that Rm should be set to the following conditions.

$$R_m \leq 1/20R_L$$

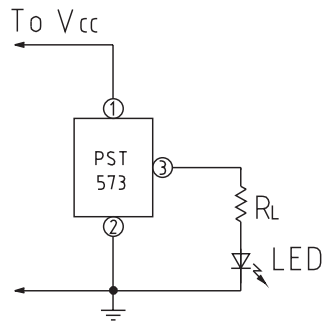
Note 2: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

3. Battery checker (LED ON for high voltage)



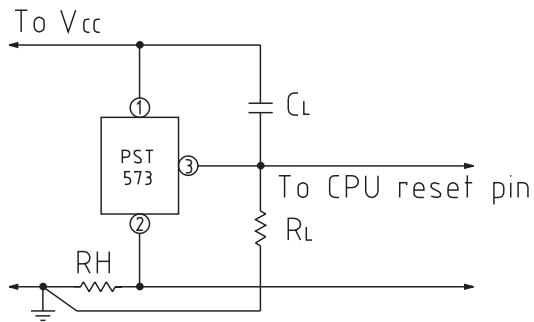
Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

4 Battery checker (LED ON for low voltage)



Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

5. Hysteresis voltage UP method



When increasing hysteresis voltage for stable system operation, determine RH as follows and connect externally.

However,  $I_{CCH}$  is  $-5000\text{PPM}/^\circ\text{C}$ , so perform temperature compensation at RH when using over a wide temperature range.

Hysteresis voltage UP amount ( $\Delta V_{sup}$ ) is

$$\Delta V_{sup} \cong RH \times I_{CCL}$$

Total hysteresis voltage ( $\Delta V_{stotal}$ ) is

$$\Delta V_{stotal} \cong V_s + \Delta V_{sup}$$

Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.